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| **Project Plan** | | | |
| Task | Description | Deliverables | Time Frame |
| Read papers about DCSK and the underlying systems. | Read as much as necessary. | --- | 10 and 11 Nov. |
| **System Architecture Phase.** | 1. Designing the architecture of the whole system.    1. Main modules.    2. High-level connectivity.    3. Different clock domains (if any). 2. A number of (basic) test scenarios. | 1. Add to report: system architecture. 2. Add to report: system modelling. 3. Add to presentation: system architecture. 4. Add to presentation: system modelling. | 12th, 13th, 14th, and 15th of Nov. |
| **System Implementation Phase.** | Describing each module on its own:   1. Ports. 2. Main functionality. 3. Block diagram. 4. Timing diagrams. | Add to report: module architecture. | 16th and 17th of Nov. |
| Module level RTL implementation and testing. | 1. Implement all the modules as described in the previous steps. 2. Unit testing of each module. | RTL code of each module | 18th, 19th, and 20th of Nov. |
| System integration and testing. | 1. Integrating all the modules with the rest of the system. 2. System tests. | 1. Add to report: system testing. 2. Add to presentation: system testing. | 21st, 22nd, and 23rd of Nov. |
| Synthesis. | Solve all problems (if any). | 1. Add to report: synthesis results. 2. Add to presentation: synthesis results. | 24th, and 25th of Nov. |
| Photo-Session Day | Video day! | The 15 min video. | 26th of Nov. |

# Deliverables

1. SystemVerilog RTL microarchitecture code.
2. Unit and integration tests.
3. FPGA end-to-end tests.
4. A report discussing everything from start to finish.
   1. Proposed architecture.
   2. Implementation details.
   3. Synthesis results.
   4. Whatever we see fit.
5. A presentation that summarizes the report.
6. A 15 min video where all team members talk about the project.