Schematic To GDS Implementation of Successive Approximation Register Control Logic

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Abstract

Successive approximation register analog to digital converter (SAR ADC) is a type of ADC that uses binary search to search the entire range of values for the proper value that best represents the analog quantity of interest. This document presents an implementation of the SAR ADC digital control logic described in (Scott, Boser, & Pister, 2003) as the final project for **CND211**. The project started with writing the RTL of the above-mentioned SAR implementation in SystemVerilog, then a class-based environment was built along with a model of the analog part of the SAR ADC to perform end-to-end tests on the design. Linting was performed using *Synopsys SpyGlass*. The requirements for the final project of **CND211** was a 100MSps 10-bit SAR ADC. Synthesis was performed on *Synopsys Design Compiler* using Synopsys educational PDK (*SAED90nm*) with a clock frequency of 1.1 GHz (with MCMM) to meet the required sampling frequency of 100MSps. Formal verification was performed using *Synopsys Formality.* After obtaining the netlist, floor and power planning, placement, CTS, and routing were performed on *Synopsys IC Compiler II* to finally obtain the GDS file. Timing closure was performed using *Synopsys PrimeTime.*

Keywords

SAR, ADC, Synopsys, CND, STA, Synthesis, GDS, Hardware implementation, SystemVerilog, Design Compiler, Formality, ICC2, SpyGlass, PrimeTime.

Preface

This section discusses the following:

- About This Document.
- Typographic Conventions.
- Terminology and Acronyms.

About This Document

This document describes the thought process of, and challenges encountered when implementing the SAR ADC as described in the paper. This document briefly explains the working of the SAR ADC, then describes the test environment used, the goes through the synthesis flow all the way until obtaining a GDS file.

Typographic Conventions

Convention	Meaning
italic	Introduces special terminology.
bold	Highlights module names and interfaces.
`MONOSPACE_UPPERCASE`	Highlights module parameters.
`monospace_italic`	Highlights signal names.

Terminology and Acronyms

Term/Acronym	Definition
ADC	Analog to Digital Converter
CTS	Clock Tree Synthesis
E2E	End-to-End
FF	Flipflop
GDS	Graphic Data Stream
IP	Intellectual Property
LEF	Library Exchange Format
LVT	Low voltage threshold
MCMM	Multi-Corner Multi-Mode
PDK	Process Design Kit
RTL	Register Transfer Level
SAR	Successive Approximation Register
STA	Static Timing Analysis
SV	SystemVerilog

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Chapter 1 Introduction

This chapter describes the following:

- Brief introduction to SAR ADC.
- Our work.

Introduction to SAR ADC

The SAR ADC is a type of ADC that uses binary search to find the correct digital value for a given analog quantity It consists of an analog part and a digital part. It starts by assuming that the measured quantity is exactly equal to $\frac{1}{2} \times 2^{\text{ADC\_RESOLUTION}}$ and then successively approximates the value bit by bit based on a comparison between the actual measured quantity and the SAR output converted to an analog voltage. If the SAR output is larger than the quantity measured, then a comparator in the analog part signals the SAR to search for lower numbers (by putting a zero in the current bit). If the contrary is proven, then the SAR searches higher numbers, by setting the corresponding bit.

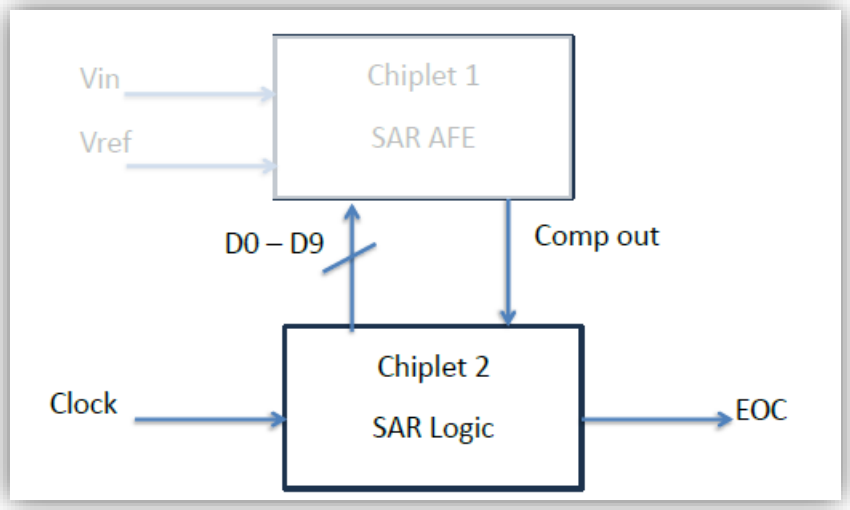


Figure 1-1 CND211 Final Project Givens

Our Work

The implemented SAR ADC digital backend is a 10-bit 100MSps IP that has a system frequency of 1.1 GHZ. Deliverables are the synthesizable SystemVerilog RTL, a class based, easily expandable testing environment, various timing reports at each stage of the design, a Verilog netlist, and the fully placed and routed IP as a GDS file.

Synopsys is a main sponsor of our training at the Centre of Nanoelectronics and devices, as a result, the team had access to the following:

1. VCS
2. SAED90nm PDK
3. SpyGlass
4. Design Compiler
5. Formality
6. IC Compiler II
7. PrimeTime

Chapter 2 Architecture

This chapter discusses the architecture of the implemented IP as shown in the referenced paper.

SAR Architecture

The SAR ADC generally requires `ADC_RESOLUTION`+1 clock cycles to finish a conversion. This means that we need 11 stages of the generic implementation shown in Figure 2-1.

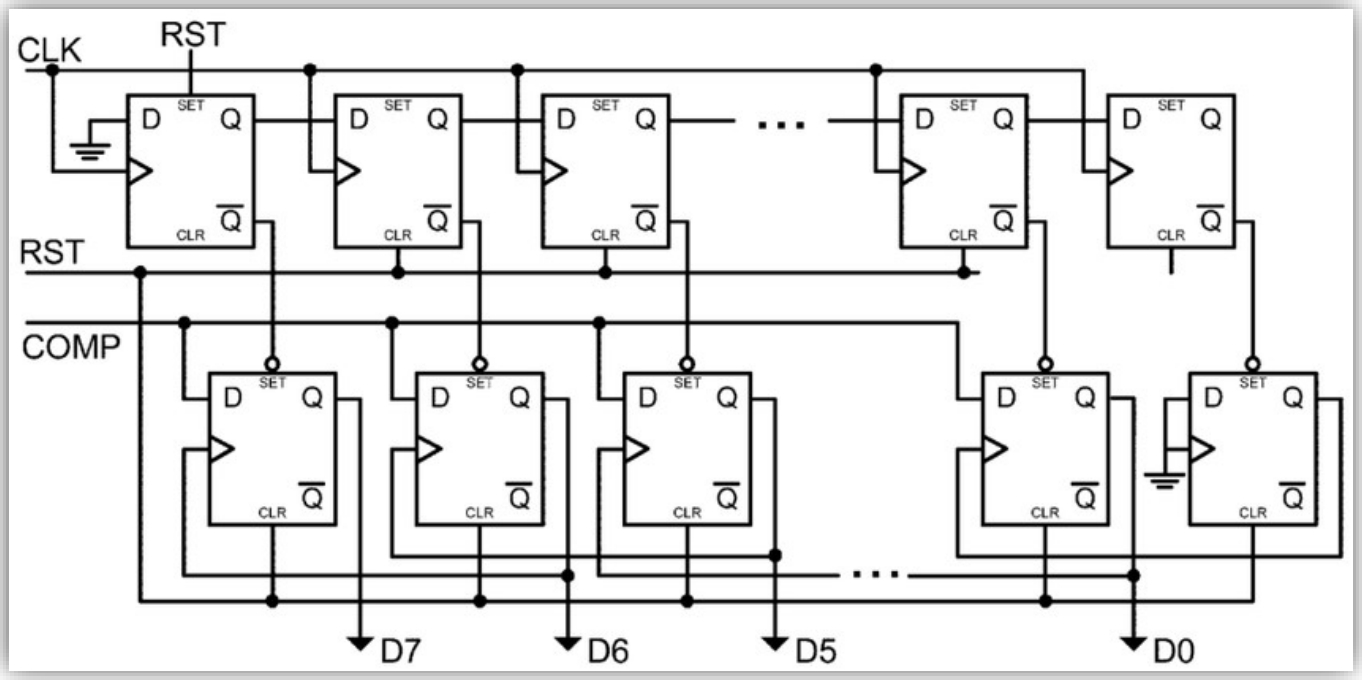


Figure 2-1 SAR ADC Schematic

The implementation is divided into two sections: the **set propagator** (top half) and the **custom sar reg** (bottom half). The **set propagator** shifts a pulse through the *`set`* pins of the **custom sar reg**. This starts the conversion process. Each register in the bottom half when set enables the clock of the register that precedes it, which loads the value of the comparison: $V_{analog} > V_{ADC}$ into the register.

Table 2-1 Pinout of the implemented IP

Port	Direction	Width	Description
`i_clk`	Input	1	1.1 GHz Clock
`i_start`	Input	1	Start Conversion
`i_comp`	Input	1	Asserted if $V_{analog} > V_{ADC}$
`o_eoc`	Output	1	End of Conversion
`o_a2d`	Output	`ADC_RESOLUTION`	Converted Value

Registers 10 through 1 of the **set propagator** is an active-low asynchronous reset positive edge-triggered D flipflop, which are reset using the `i_start` signal. Register zero is the same except that is asynchronously set. Each register in the **custom sar reg** is an active low asynchronous set-reset positive edge-triggered D flipflop.

Chapter 3 Verification Environment

This chapter introduces the following:

- Architecture of The Test Environment.
- Coverage Statistics.

Test Environment Architecture

The test environment built is a class based SystemVerilog E2E testbench. A model of the analog part shown in Figure 1-1 was implemented to test the digital part.

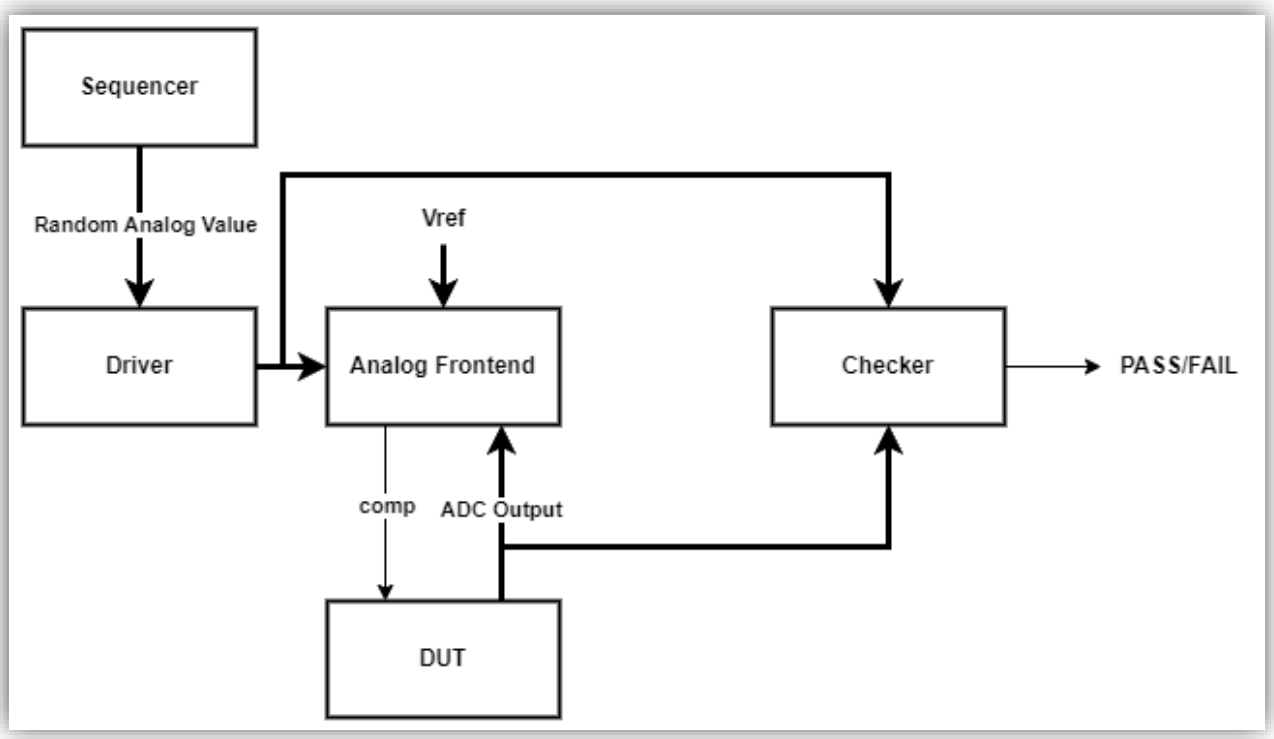


Figure 3-1 Test environment block diagram.

Sequencer

This block sends random analog values (in the form of transactions) as the measured quantities to the analog front end to be compared with the ADC output from the DUT.

Driver

The driver converts the transaction received from the sequencer to “pin wiggles” at the analog frontend. This provides random stimulation to the design.

Analog Frontend

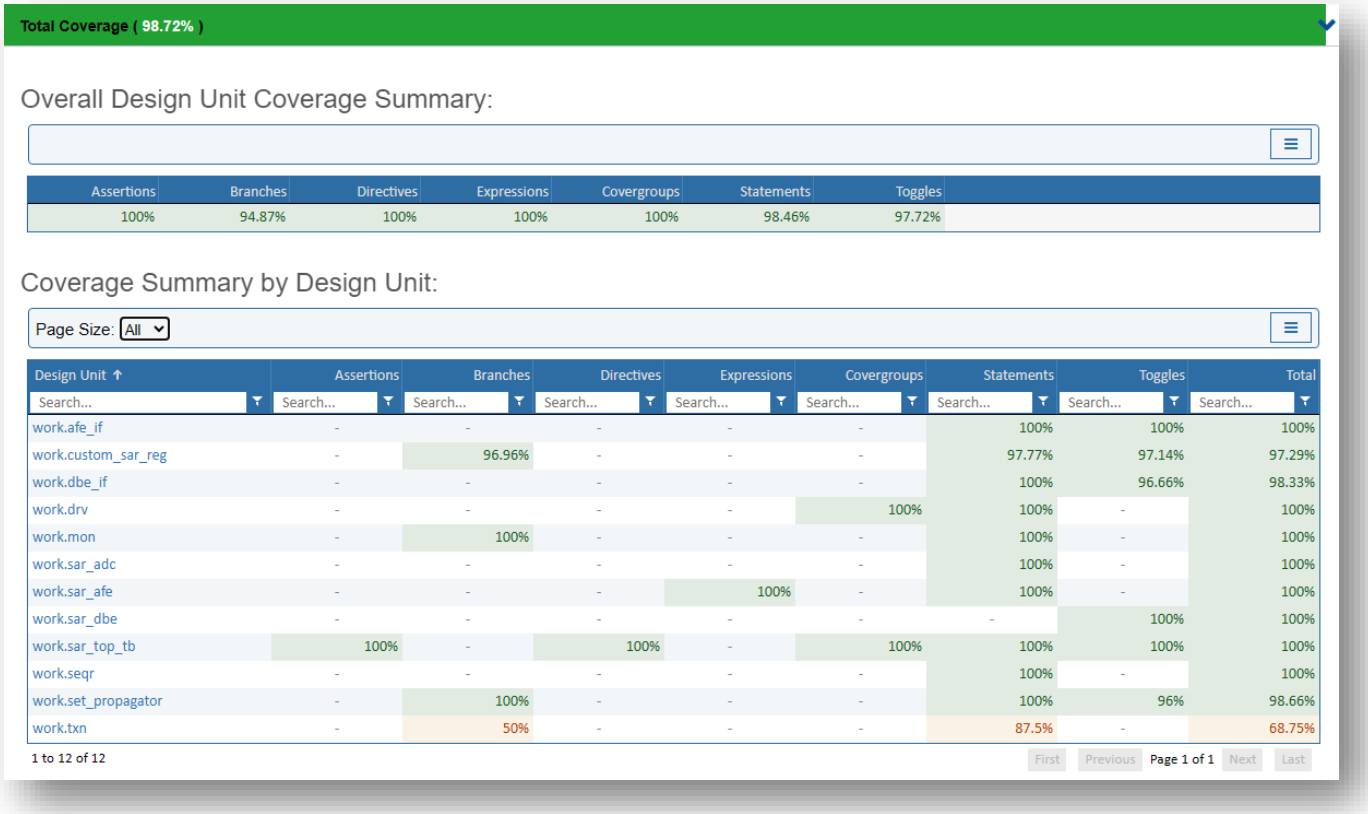
The SystemVerilog model of the analog frontend acts as an operational amplifier used as a comparator. It compares the output of the ADC with the analog value measured (which is randomly generated in the sequencer in our setup) and outputs the comparison signal.

Checker

The checker has a DAC built in that converts the ADC output to an analog value which is then compared with the random value generated at the sequencer. Due to the quantization error, the checker allows for a mismatch of up to $\pm 1\ LSB$.

Coverage Statistics

The following cover groups were collected: 64 bins for the whole range of possible values (0-1024) and another cover group to cover the delay between each analog value driven, whether it is zero, or non-zero. The *work.txn* design unit is the transaction class. This class has a print function that returns without printing if the simulation verbosity mode is set to 0. This means that the function gets called but skips the printing part. The skipped part is what is causing the low coverage percentage. Other than that, the percentage of coverage collected is satisfactory.



Total Coverage (98.72%)

Overall Design Unit Coverage Summary:

Assertions	Branches	Directives	Expressions	Covergroups	Statements	Toggles
100%	94.87%	100%	100%	100%	98.46%	97.72%

Coverage Summary by Design Unit:

Page Size: All

Design Unit	Assertions	Branches	Directives	Expressions	Covergroups	Statements	Toggles	Total
work.afe_if	-	-	-	-	-	100%	100%	100%
work.custom_sar_reg	-	96.96%	-	-	-	97.77%	97.14%	97.29%
work.dbe_if	-	-	-	-	-	100%	96.66%	98.33%
work.drv	-	-	-	-	100%	100%	-	100%
work.mon	-	100%	-	-	-	100%	-	100%
work.sar_adc	-	-	-	-	-	100%	-	100%
work.sar_afe	-	-	-	100%	-	100%	-	100%
work.sar_dbe	-	-	-	-	-	-	100%	100%
work.sar_top_tb	100%	-	100%	-	100%	100%	100%	100%
work.seqr	-	-	-	-	-	100%	-	100%
work.set_propagator	-	100%	-	-	-	100%	96%	98.66%
work.txn	-	50%	-	-	-	87.5%	-	68.75%

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Figure 3-2 Coverage Summary.

Chapter 4 Linting

This chapter discusses the following:

- Linting Goals Covered.
- Linting Results.

Goals Covered

The following goals were covered in SpyGlass:

1. Lint RTL.
2. Lint RTL Enhanced.
3. Lint RTL Turbo.

Linting Results

All these goals check for connectivity issues, simulation issues, recommended design practices, and synthesis issues. Of course, the design from the paper has some unorthodox design techniques, so the linting tool is expected to complain. The following design techniques do work for our use case but are considered unconventional by both the authors and SpyGlass. As a result, various errors/warnings were reported:

1. Flip-Flop clock pin is driven by a constant clock value.
    a. SpyGlass is referring to FF number 0 in the **custom sar reg.**
    b. The behavior modeled is like an SR latch, but thanks to SystemVerilog, the use of the keyword `always_ff` prevents latch inference. Thus, this linting error can be waived.
2. Flip-Flop outputs must not be used as clocks of other flip-flops.
    a. SpyGlass is referring to the **custom sar reg**.
    b. The clock connections of the **custom sar reg** put the "successive" in successive approximation register. They are required by design and thus this error too can be waived.
    c. This also caused another error because the clock signals are not module inputs. This too can be waived for the reasons stated in point b.
3. Flip-Flop asynchronous set pins are being driven by Flip-Flop pins.
    a. SpyGlass is referring to the outputs of the **set propagator** driving the set pins of the **custom sar reg**.
    b. This is required by design and can be waived.

While the techniques employed in this implementation are considered by the tool to be bad practice, they are required for the design to work. Another great advantage is that the critical path is virtually empty. The required 1.1GHz on a 90nm technology node is a very tough challenge. Indeed, some sacrifices must be made to meet the requirements with the given restrictions. The authors claim that better designs can be made to meet the same requirements with a smaller technology node, or even a technology node with more choices of FFs.

Chapter 5 Synthesis

This section discusses the following:

- PDK Summary.
- Synthesis Corners.
- Static Timing Analysis.

PDK Summary

For our implementation, we are using the SAED90nm educational PDK which offers a limited but suitable range of standard cells with various drive strengths.

To achieve the required frequency with the given PDK, a design with a virtually empty critical path was needed, because simply at this frequency, the 90nm technology node is not suitable for anything more complex than an empty critical path. A simple NAND gate in the path would cause a violation. The low voltage threshold variants of the cells were used to give the circuit the best chance to meet the required system frequency of 1.1GHz.

Synthesis Corners

MCMM simulation was performed to give the design the worst cast in both setup and hold checking, which ensures the robustness of the system.

Table 5-1 Synthesis Corners

	Temperature	Voltage
Max Corner	125	0.65
Min Corner	-40	0.9

Static Timing Analysis

STA was performed using the above corners. Our design has a critical path slack of 90 picoseconds.

```
Timing Path Group 'i_clk'
----------------------------------
Levels of Logic:                0.00
Critical Path Length:           0.49
Critical Path Slack:            0.09
Critical Path Clk Period:       0.91
Total Negative Slack:           0.00
No. of Violating Paths:         0.00
Worst Hold Violation:           0.00
Total Hold Violation:           0.00
No. of Hold Violations:         0.00
----------------------------------
```

Figure 5-1 Synthesis QoR - Timing.

```
--------------------------------------------------------------------

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

--------------------------------------------------------------------
```

Figure 5-2 Zero timing violations.

```
Operating Conditions: WORST   Library: saed90nm_max_htm_lvt
Wire Load Model Mode: enclosed

  Startpoint: u_SET_PROP_q_reg_10_/CLK
              (internal path startpoint clocked by i_clk)
  Endpoint: u_SET_PROP_q_reg_9_
            (rising edge-triggered flip-flop clocked by i_clk)
  Path Group: i_clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  sar_dbe_ADC_RESOLUTION10
                     8000                  saed90nm_max_htm_lvt

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  clock i_clk (rise edge)                                 0.00       0.00
  clock network delay (ideal)                             0.18       0.18
  input external delay                                    0.00       0.18 r
  u_SET_PROP_q_reg_10_/CLK (DFFASX1_LVT)                  0.00       0.18 r
  u_SET_PROP_q_reg_10_/Q (DFFASX1_LVT)                    0.45       0.63 r
  u_SET_PROP_q_reg_9_/D (DFFARX1_LVT)                     0.04       0.67 r
  data arrival time                                                  0.67

  clock i_clk (rise edge)                                 0.91       0.91
  clock network delay (ideal)                             0.18       1.09
  clock uncertainty                                      -0.09       1.00
  u_SET_PROP_q_reg_9_/CLK (DFFARX1_LVT)                   0.00       1.00 r
  library setup time                                     -0.24       0.76
  data required time                                                 0.76
  ---------------------------------------------------------------------------
  data required time                                                 0.76
  data arrival time                                                 -0.67
  ---------------------------------------------------------------------------
  slack (MET)                                                        0.09
```

Figure 5-3 Critical path timing report.

```
Operating Conditions: BEST   Library: saed90nm_min_ltl_lvt
Wire Load Model Mode: enclosed

  Startpoint: u_SET_PROP_q_reg_9_
              (rising edge-triggered flip-flop clocked by i_clk)
  Endpoint: u_SET_PROP_q_reg_8_
            (rising edge-triggered flip-flop clocked by i_clk)
  Path Group: i_clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  sar_dbe_ADC_RESOLUTION10
                     8000                  saed90nm_max_htm_lvt

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  clock i_clk (rise edge)                                 0.00       0.00
  clock network delay (ideal)                             0.18       0.18
  u_SET_PROP_q_reg_9_/CLK (DFFARX1_LVT)                   0.00       0.18 r
  u_SET_PROP_q_reg_9_/Q (DFFARX1_LVT)                     0.13       0.31 f
  u_SET_PROP_q_reg_8_/D (DFFARX1_LVT)                     0.00       0.31 f
  data arrival time                                                  0.31

  clock i_clk (rise edge)                                 0.00       0.00
  clock network delay (ideal)                             0.18       0.18
  clock uncertainty                                       0.09       0.27
  u_SET_PROP_q_reg_8_/CLK (DFFARX1_LVT)                   0.00       0.27 r
  library hold time                                      -0.01       0.27
  data required time                                                 0.27
  ---------------------------------------------------------------------------
  data required time                                                 0.27
  data arrival time                                                 -0.31
  ---------------------------------------------------------------------------
  slack (MET)                                                        0.05
```

Figure 5-4 Worst hold timing report.

```
****************************************
Report : constraint
         -all_violators
         -verbose
Design : sar_dbe_ADC_RESOLUTION10
Version: V-2023.12
Date   : Fri May 10 17:39:29 2024
****************************************

This design has no violated constraints.
```

Figure 5-5 Constraint violation report.

```
Number of ports:                         14
Number of nets:                          48
Number of cells:                         35
Number of combinational cells:           12
Number of sequential cells:              22
Number of macros/black boxes:             0
Number of buf/inv:                       12
Number of references:                     4

Combinational area:                66.355202
Buf/Inv area:                      66.355202
Noncombinational area:            739.123222
Macro/Black Box area:               0.000000
Net Interconnect area:             25.054050

Total cell area:                  805.478424
Total area:                       830.532474
```

Figure 5-6 Area report - Synthesis

Chapter 6 Formal Verification

This chapter discusses the formal verification process and the peculiarities encountered.

The formal verification process was performed using *Synopsys Formality*. The netlist and the RTL files were compared for formal equivalence and other than a single point, verification succeeded.

This single point was due to the FF which clock pin is tied low (in the **custom sar reg**). Since we are using only the set and reset pins of the FF, this compare point showed up as a latch instead of a flip-flop. But since the RTL was written in SystemVerilog, Design compiler inferred a D flip-flop as intended. Formality did not see through this and inferred a latch and as a result the verification failed due to this single discrepancy. After performing *set_dont_verify* on the violating point, and rerunning verification, the verification succeeds.

```
----------------------------------------------------------------------------------------
Matched Compare Points     BBPin    Loop   BBNet     Cut     Port     DFF     LAT   TOTAL
----------------------------------------------------------------------------------------
Passing (equivalent)           0       0       0       0       11       21       0      32
Failing (not equivalent)       0       0       0       0        0        0       1       1
****************************************************************************************
```

Figure 6-1 One failed compare point. (LAT)ch

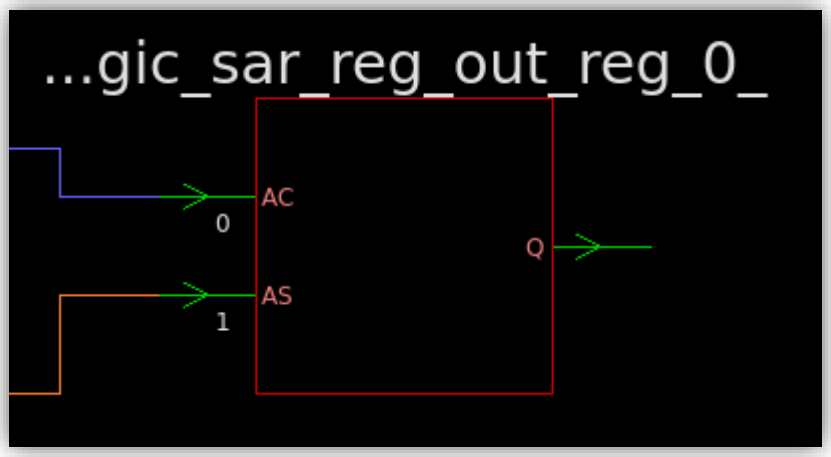

Figure 6-2 Compare point - Reference. Missing clock pin.

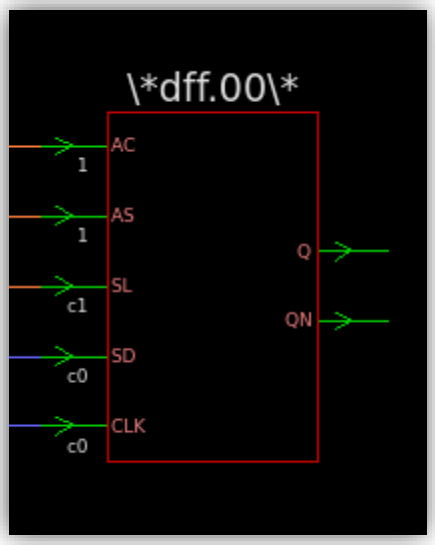

Figure 6-3 Compare point – implementation.

Matched Compare Points	BBPin	Loop	BBNet	Cut	Port	DFF	LAT	TOTAL
Passing (equivalent)	0	0	0	0	11	21	0	32
Failing (not equivalent)	0	0	0	0	0	0	0	0
Not Compared								
Don't verify	0	0	0	0	0	0	1	1

Figure 6-4 After applying set_dont_verify.

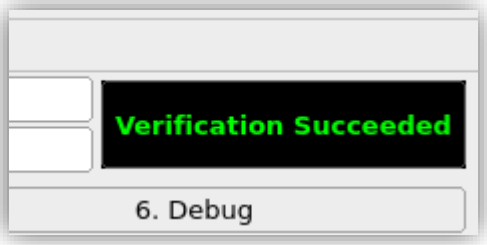

Figure 6-5 Verification Succeeded.

Chapter 7 ASIC Flow

This chapter discusses the following:

- NDM Library Creation
- Floor Planning.
- Power Planning.
- Placement.
- Clock Tree Synthesis.
- Routing

NDM Library Creation

Since we were using LVT cells instead of the normal cells, we had to include a different *.lef* file that what was given to us in the labs. Two errors of the same type prevent the importing of the LVT .lef file that is included with the given PDK.

The following cells give the same error:

> The height or width of MACRO LSDNENCLX4_LVT is not a multiple of any site definition in the technology data.

The same error is reported for LSDNENCLX8_LVT. Upon checking the .lef file, the authors found that it is not the height that is non-compliant, but the width. The site definition is 0.32 by 2.88, and the height of both cells is not an integer multiple of the site definition. (LSDNENCLX4_LVT and LSDNENCLX8_LVT have heights of 13.065 and 15.225). Upon reading the data-book of the PDK, the violating cells were confirmed to be high to low level shifters with high active enables /clamp low. Perhaps creating a new site definition is a cleaner solution, but our design does not use any level shifters and thus these cells were removed from the file. The .lef file is now imported successfully.

Floor And Power Planning

Floor Planning

The floor plan has an aspect ratio of 1 (square) and a side length of 28 µm. The pins on each side are placed such that the spacing between each pin and its neighboring pin is equal.

Power Planning

Since this IP will be part of a chip, it makes no sense to have a power ring. A mesh is enough. When adding the analog part of the SAR the power ring can be added according to specification. A power mesh was added to the design and a pin was added to each strip of the mesh then the standard cell power rails were added.

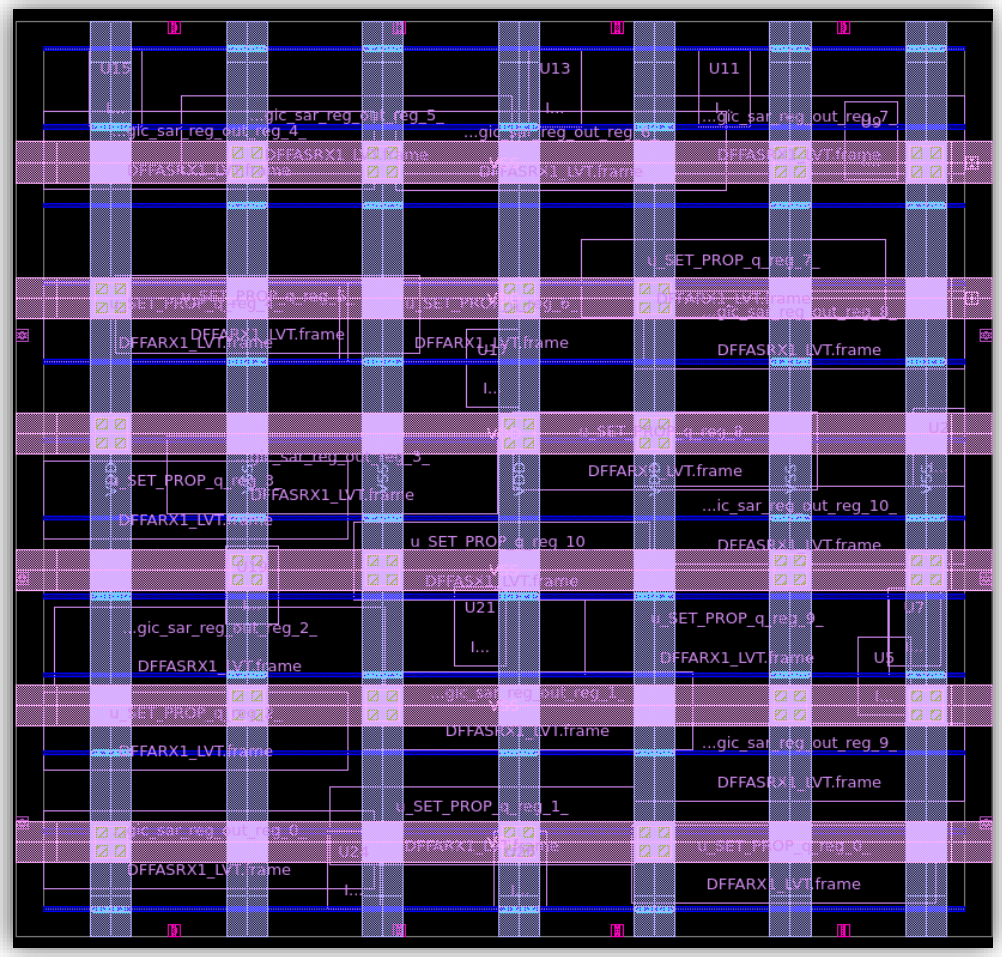

Figure 7-1 After Floor and Power Planning

Placement

After performing placement, the following QoR were obtained:

```
Area
----------------------------------------
Combinational Area:               66.36
Noncombinational Area:           739.12
Buf/Inv Area:                     66.36
Total Buffer Area:                 0.00
Total Inverter Area:              66.36
Macro/Black Box Area:              0.00
Net Area:                             0
Net XLength:                     443.15
Net YLength:                     439.97
----------------------------------------
Cell Area (netlist):                             805.48
Cell Area (netlist and physical only):           805.48
Net Length:                      883.12
```

Figure 7-2 Area Report - After placement.

```
----------------------------------------
Levels of Logic:                      0
Critical Path Length:              0.45
Critical Path Slack:               0.12
Critical Path Clk Period:          0.91
Total Negative Slack:              0.00
No. of Violating Paths:               0
Worst Hold Violation:              0.00
Total Hold Violation:              0.00
No. of Hold Violations:               0
----------------------------------------
```

Figure 7-3 Timing Summary - After placement.

CTS

After synthesizing the clock tree, we obtained the following results.

```
Area
---------------------------------------
Combinational Area:               66.36
Noncombinational Area:           739.12
Buf/Inv Area:                     66.36
Total Buffer Area:                 0.00
Total Inverter Area:              66.36
Macro/Black Box Area:              0.00
Net Area:                             0
Net XLength:                     457.32
Net YLength:                     473.89
---------------------------------------
Cell Area (netlist):                             805.48
Cell Area (netlist and physical only):           805.48
Net Length:                      931.21
```

Figure 7-4 Area - After CTS.

```
Scenario           'default'
Timing Path Group  'i_clk'
---------------------------------------
Levels of Logic:                     0
Critical Path Length:             0.49
Critical Path Slack:              0.13
Critical Path Clk Period:         0.91
Total Negative Slack:             0.00
No. of Violating Paths:              0
Worst Hold Violation:             0.00
Total Hold Violation:             0.00
No. of Hold Violations:              0
---------------------------------------
```

Figure 7-5 Timing - After CTS.

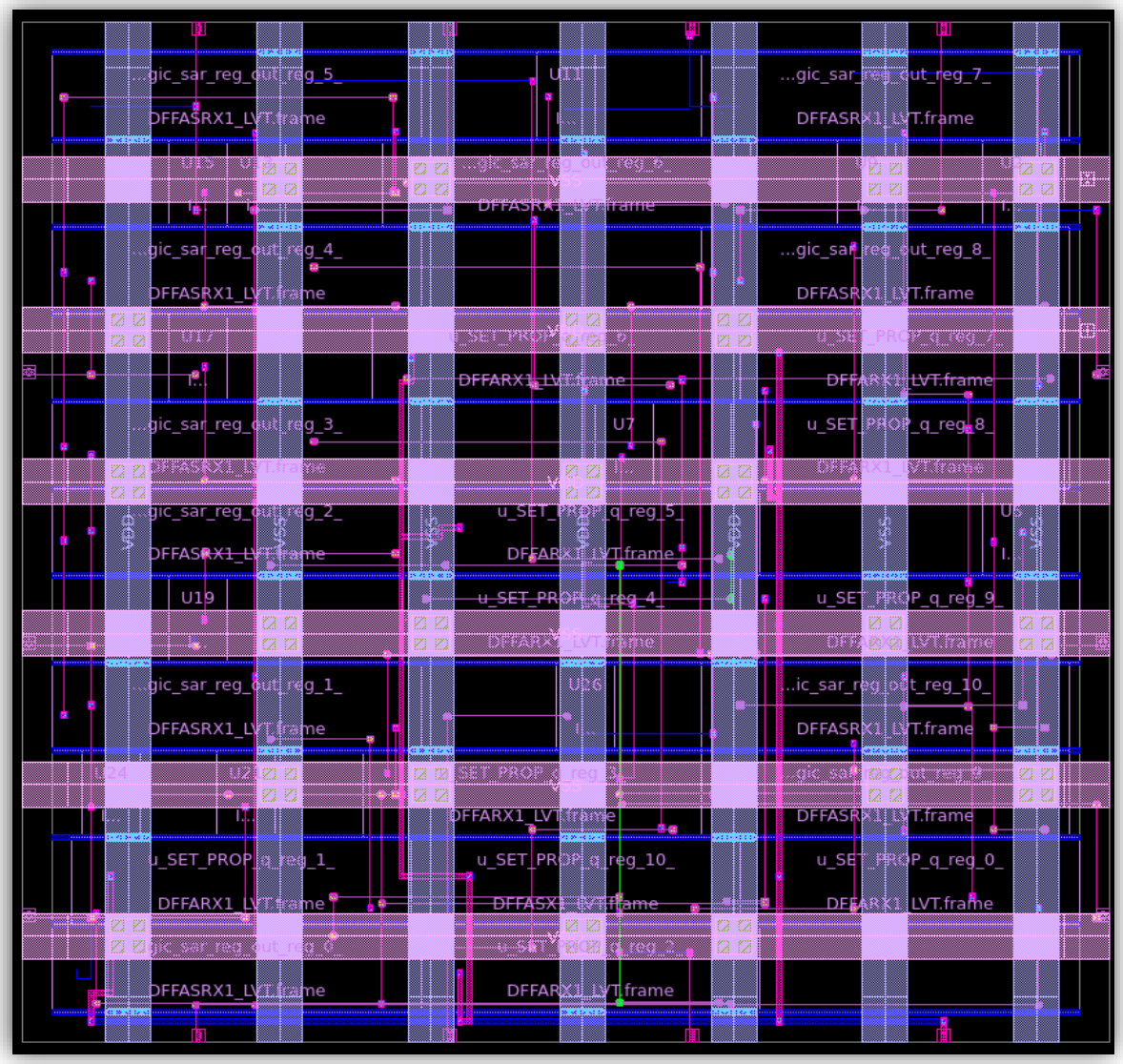

Figure 7-6 After CTS.

Routing

After routing and placing filler cells, we obtained the following results.

```
Area
---------------------------------------
Combinational Area:                66.36
Noncombinational Area:            739.12
Buf/Inv Area:                      66.36
Total Buffer Area:                  0.00
Total Inverter Area:               66.36
Macro/Black Box Area:               0.00
Net Area:                              0
Net XLength:                      472.48
Net YLength:                      490.87
---------------------------------------
Cell Area (netlist):                             805.48
Cell Area (netlist and physical only):          1074.59
Net Length:                       963.35
```

Figure 7-7 Final Area.

```
Scenario           'default'
Timing Path Group  'i_clk'
---------------------------------------
Levels of Logic:                       0
Critical Path Length:               0.49
Critical Path Slack:                0.12
Critical Path Clk Period:           0.91
Total Negative Slack:               0.00
No. of Violating Paths:                0
Worst Hold Violation:               0.00
Total Hold Violation:               0.00
No. of Hold Violations:                0
---------------------------------------
```

Figure 7-8 Final Timing.

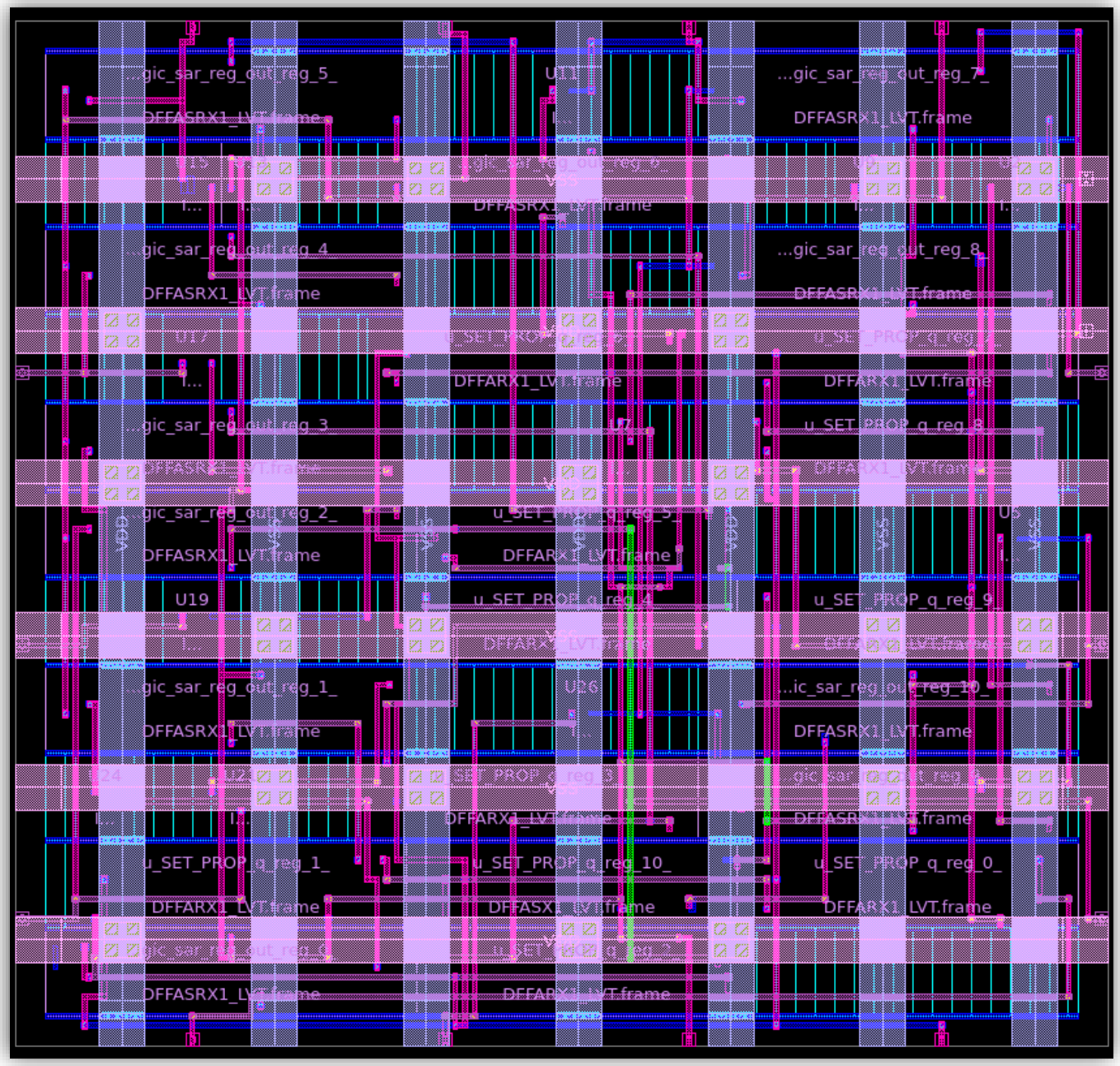

Figure 7-9 Final IC

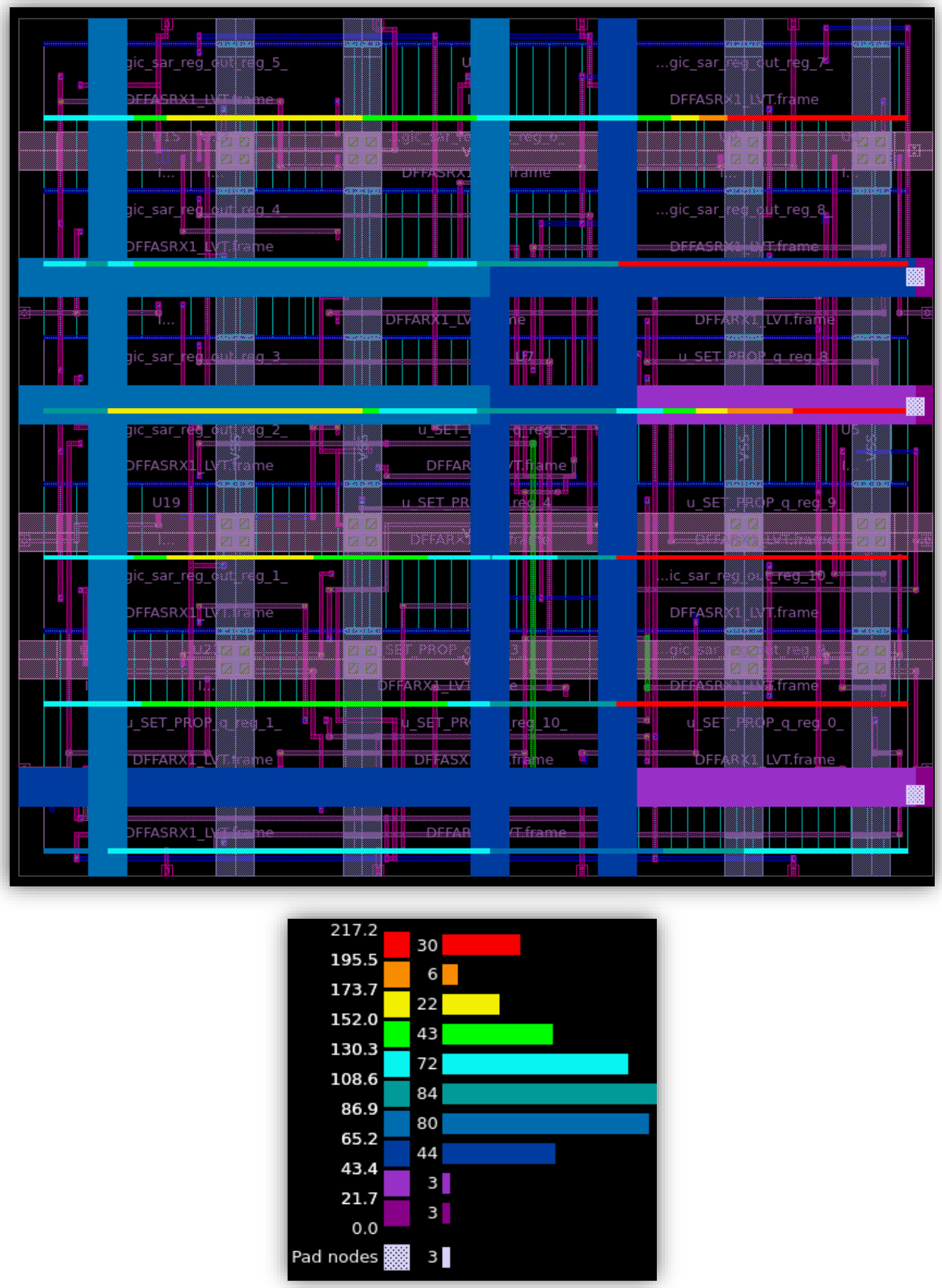

Figure 7-10 IR Drop.

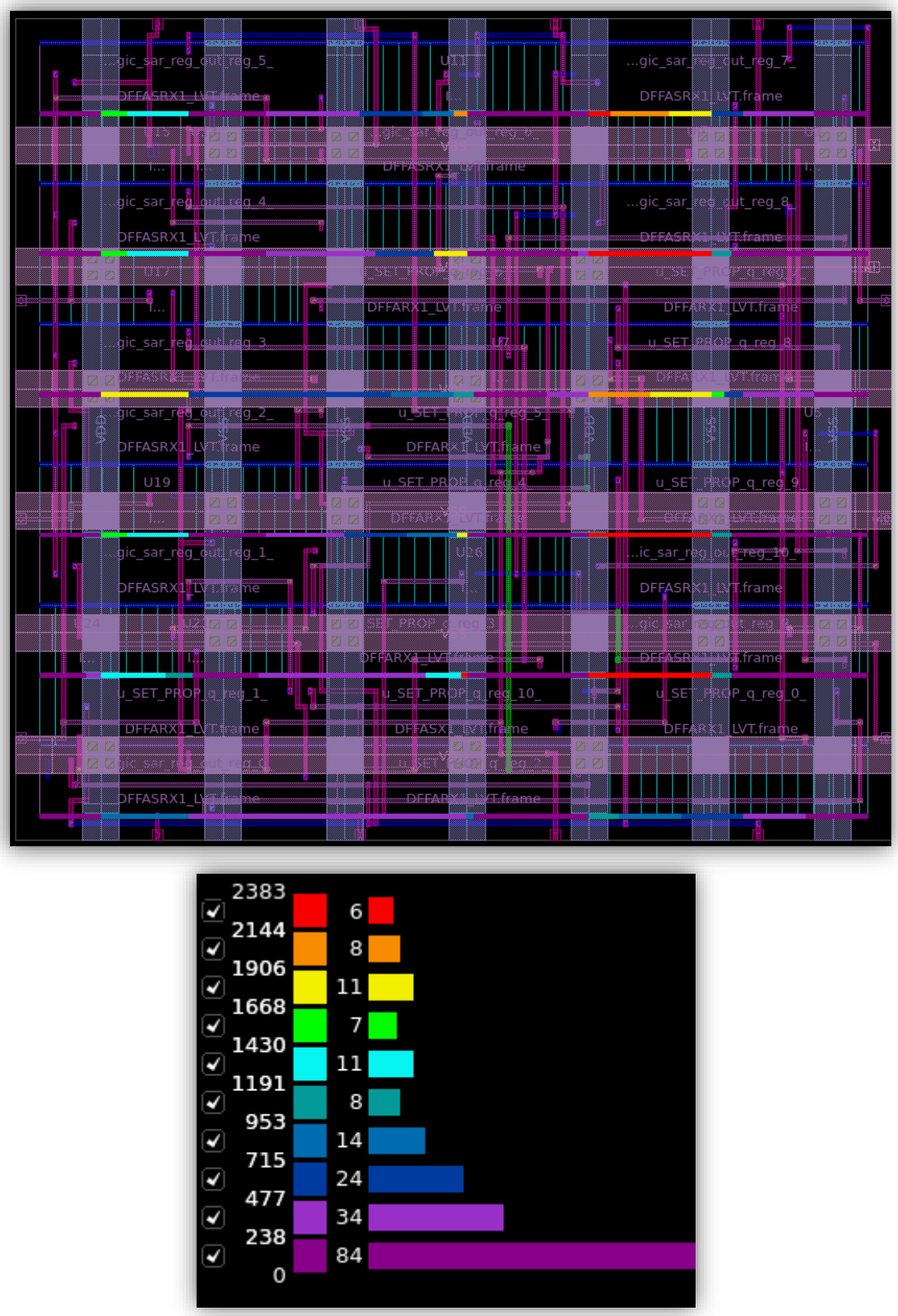

Figure 7-11 Electromigration.

Final Timing

Synopsys PrimeTime was used to obtain the following results.

```
****************************************
Report : global_timing
         -format { narrow }
Design : sar_dbe_ADC_RESOLUTION10
Version: V-2023.12
Date   : Tue May 14 15:39:01 2024
****************************************

No setup violations found.

No hold violations found.
```

Figure 7-12 Final Timing Report

Endpoints Summary | Path Collections

Timing is up to date. Update

Endpoint slack data: Scenarios Path Groups Failing

Enter filter expression

Scenario	Mode	Corner	Path Group	Analysis	Endpoints	NVE	WNS	TNS
default	default	default	**async_default**	setup	***	0	0.000	0.000
default	default	default	**async_default**	hold	***	0	0.000	0.000
default	default	default	**clock_gating_default**	setup	***	0	0.000	0.000
default	default	default	**clock_gating_default**	hold	***	0	0.000	0.000
default	default	default	**default**	setup	***	0	0.000	0.000
default	default	default	**default**	hold	***	0	0.000	0.000
default	default	default	i_clk	setup	***	0	0.000	0.000
default	default	default	i_clk	hold	***	0	0.000	0.000

Figure 7-13 PrimeTime - No Violations.

Chapter 8 Conclusion

In conclusion, pushing the limits of the PDK requires unconventional design techniques that even the tools consider outright wrong. The reason for selecting this PDK is that none of the authors have access to a solvent account and no one can download or acquire the relatively newer PDK, SAED32nm.

Chapter 9 References

Scott, M. D., Boser, B. E., & Pister, K. (2003). An ultralow-energy ADC for Smart Dust. *IEEE Journal of Solid-State Circuits*, 1123-1129.