vonNeumann RISC Processor CMPN301

GitHub

Phase1 Requirement: Report Containing:

- Instruction format of your design
  - Opcode of each instruction
  - Instruction bits details
- Schematic diagram of the processor with data flow details.
  - ALU / Registers / Memory Blocks
  - Dataflow Interconnections between Blocks & its sizes
  - Control Unit detailed design
- Pipeline stages design
  - Pipeline registers details (Size, Input, Connection, …)
  - Pipeline hazards and your solution including
    - Data Forwarding
    - Static Branch Prediction

Phase 1 Due Date

- Deliver a softcopy on blackboard.
- **Week 9, Sunday 16th of May 2021 at 9 am.** The discussion time will be announced prior to the delivery.

• Opcode of 7 instructions: (From NOP to OUT rdst) • Schematic of control unit • Solution of structural hazards	ياسر
• Opcode of 7 instructions: (From IN Rdst to Or Rsrc, Rdst) • Schematics of registers and memory blocks • Solution of control hazards • Instruction bit details	سيف
• Opcode of 7 instructions: (From SHL Rsrc, Imm to Or Rsrc, Rdst) • Schematic of ALU • Solution of data hazards	أندرو
• Opcode of 7 instructions: (From JZ rdst to last instruction) • Schematic of dataflow interconnections between blocks and it's sizes • Pipeline registers details (Size, Input, Connection, …)	عامر