# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Regular Write** with **odd** number of data bytes & there are **no coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 1;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>i_regf_cmd_attr_tb = 0;<br>i_regf_dtt_tb = xxx;<br>i_regf_DATA_LEN_tb = odd number | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| | | A dummy data is sent to complete the data word bits | High |
| | | The slave doesn't abort the write operation | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Regular Write** with **odd** number of data bytes & there are **coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 0;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>i_regf_cmd_attr_tb = 0;<br>i_regf_dtt_tb = xxx;<br>i_regf_DATA_LEN_tb = odd number | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Sending** crc word -> **RETART** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| | | A dummy data is sent to complete the data word bits | High |
| | | The slave doesn't abort the write operation | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Regular Write** with **even** number of data bytes & there are **no coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 1;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>i_regf_cmd_attr_tb = 0;<br>i_regf_dtt_tb = xxx;<br>i_regf_DATA_LEN_tb = even number | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| | | The slave doesn't abort the write operation | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Regular Write** with **even** number of data bytes & there are **coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 0;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>i_regf_cmd_attr_tb = 0;<br>i_regf_dtt_tb = xxx;<br>i_regf_DATA_LEN_tb = even number | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| | | The slave doesn't abort the write operation | High |
| | | | |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Regular read** with **odd** number of data bytes & there are **no coming** configurations to be executed & allowing short read | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 1;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = 1 ;<br>i_regf_wr_rd_bit_tb = 1;<br>i_regf_cmd_attr_tb = 0;<br>i_regf_dtt_tb = xxx;<br>i_regf_DATA_LEN_tb = odd number<br>i_rx_sda_tb = 0 after the last frame indicating to **crc** | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **receiving** crc word -> **EXIT** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| | | The slave sends all the required data | High |
| | | A dummy data is sent to complete the data word bits | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Regular read** with **odd** number of data bytes & there are **coming** configurations to be executed & allowing short read | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 0;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = 1 ;<br>i_regf_wr_rd_bit_tb = 1;<br>i_regf_cmd_attr_tb = 0;<br>i_regf_dtt_tb = xxx;<br>i_regf_DATA_LEN_tb = odd number<br>i_rx_sda_tb = 0 after the last frame indicating to **crc** | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **receiving** crc word -> **RESTART** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| | | The slave sends all the required data | High |
| | | A dummy data is sent to complete the data word bits | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Regular read** with **even** number of data bytes & there are **coming** configurations to be executed & allowing short read | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 0;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = 1 ;<br>i_regf_wr_rd_bit_tb = 1;<br>i_regf_cmd_attr_tb = 0;<br>i_regf_dtt_tb = xxx;<br>i_regf_DATA_LEN_tb = even number<br>i_rx_sda_tb = 0 after the last frame indicating to **crc** | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **receiving** crc word -> **RESTART** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave sends all the required data | High |
| | | The slave sends all the required data | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Regular read** with **even** number of data bytes & there are **no coming** configurations to be executed & allowing short read | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 1 ;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = 1 ;<br>i_regf_wr_rd_bit_tb = 1;<br>i_regf_cmd_attr_tb = 0;<br>i_regf_dtt_tb = xxx;<br>i_regf_DATA_LEN_tb = even number<br>i_rx_sda_tb = 0 after the last frame indicating to **crc** | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **receiving** crc word -> **EXIT** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave sends all the required data | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Immidiate Write** with **one** data byte & there are **coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 0;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>**i_regf_cmd_attr_tb = 1;**<br>i_regf_dtt_tb = xxx;<br>i_regf_DATA_LEN_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **RESTART** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Immidiate Write** with **one** data byte & there are **no coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 1;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>**i_regf_cmd_attr_tb = 1;**<br>**i_regf_dtt_tb = 1;**<br>i_regf_DATA_LEN_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Immidiate Write** with **two** data bytes & there are **coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 0;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>**i_regf_cmd_attr_tb = 1;**<br>**i_regf_dtt_tb = 2;**<br>i_regf_DATA_LEN_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **RESTART** pattern<br><br>Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Immidiate Write** with **two** data bytes & there are **no coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 1;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>**i_regf_cmd_attr_tb = 1;**<br>**i_regf_dtt_tb = 2;**<br>i_regf_DATA_LEN_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Immidiate Write** with **three** data bytes & there are **coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 0;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>**i_regf_cmd_attr_tb = 1;**<br>**i_regf_dtt_tb = 3;**<br>i_regf_DATA_LEN_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **RESTART** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Immidiate Write** with **three** data bytes & there are **no coming** configurations to be executed | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>**i_regf_toc_tb = 1;**<br>i_regf_dev_index_tb equals any value except 0;<br>i_regf_short_read_tb = x ;<br>i_regf_wr_rd_bit_tb = 0;<br>**i_regf_cmd_attr_tb = 1;**<br>**i_regf_dtt_tb = 3;**<br>i_regf_DATA_LEN_tb = even number | The sequence of sending command word -> first data byte dummy byte -> … -> **Sending** crc word -> **EXIT** pattern | High |
| | | Flag o_engine_done set to 1 after exit pattern | High |
| | | The slave recognizes its address and pulls down the line to 0 means as an ack | High |
| | | | |
| | | | |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| The Master in The Reset Mode | i_sys_rst_tb = 1 ;<br>i_sys_rst_tb = 1->0 ;<br>i_sys_rst_tb = 0 ;<br>i_sys_rst_tb = 0->1 ; | @ negedge of i_sys_rst_tb the master enters the rst mode | High |
| | | o_scl_tb line is set to 1 & o_sdahnd_serial_data_tb is set to 1 (open drain) within time i_sys_rst_tb is being 0 | High |
| | | @ posedge of i_sys_rst_tb the master operates normally | High |
| | | | |
| | | | |

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| Enabling N.T Block | i_sys_rst_tb = 1 ;<br>i_engine_en_tb =1;<br><br>i_engine_en_tb =0; | The NT Block doesn't respond until being enabled | High |
| | | If the enable is high the block excute the required configuration and respond with done | High |

# MIPI I3C N.T Test Plan

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **No Acknowledgment** for Write or Read operations | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>i_regf_wr_rd_bit_tb = 0 or 1;<br><br>i_sda_rx_tb = 1 @ the beginning of the first data word | The sequence of sending command word -> Error (no ack) -> RESTART or EXIT depending on the value of (i_regf_toc) | High |
| | | The type of error flag is NACK_Error | High |

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Aborting** Write operation | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>i_regf_wr_rd_bit_tb = 0;<br><br>i_sda_rx_tb = 0 @ the beginning of the second or third or fourth or….. data word | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Error(aborting)** -> RESTART or EXIT depending on the value of (i_regf_toc) | High |
| | | The slave aborts the write operation and the type of error flag is BUS_ABORTED_Error | High |

| Feature | Stimulus | Checker List | Priority |
|---|---|---|---|
| **Framing Error** | i_sys_rst_tb = 1;<br>i_engine_en_tb =1;<br>i_regf_wr_rd_bit_tb = 1; | The sequence of sending command word -> first data byte -> second data byte -> third data byte -> … -> **Error(unexpected bits)** -> RESTART or EXIT depending on the value of (i_regf_toc) | High |
| | | the preamble bits of any word ,crc token values , parity and crc value are not correct | High |
| | | type of error flag is (CRC_Error , Parity_Error | |

# MIPI I3C N.T Test Plan