Project verfication

FIFO

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Test plan :

* test the read and write operations of the fifo

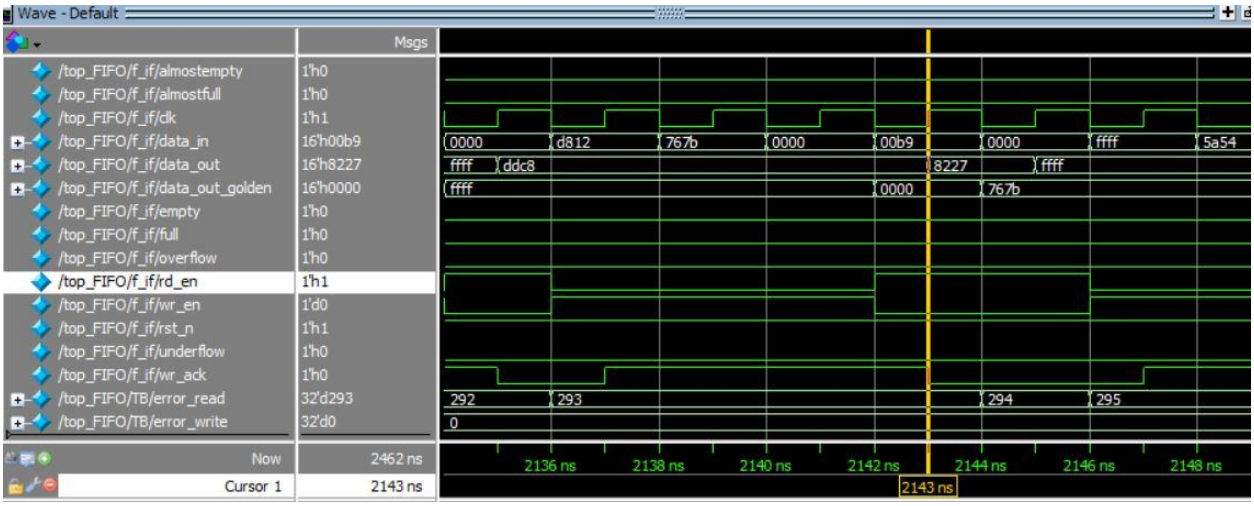
* test the output flags under different inputs

Randomization constrains :

* randomize the wr_en and rd_en with more probability to the write than the read operation .

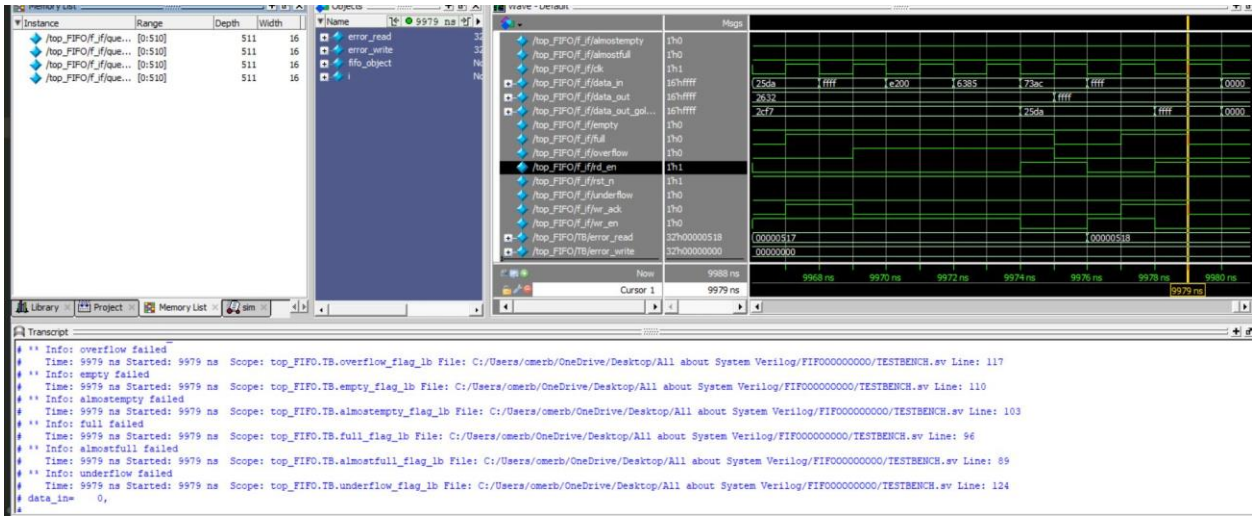
* randomization the data input with probability for bus of 1’s and 0’s and random values .

General overview

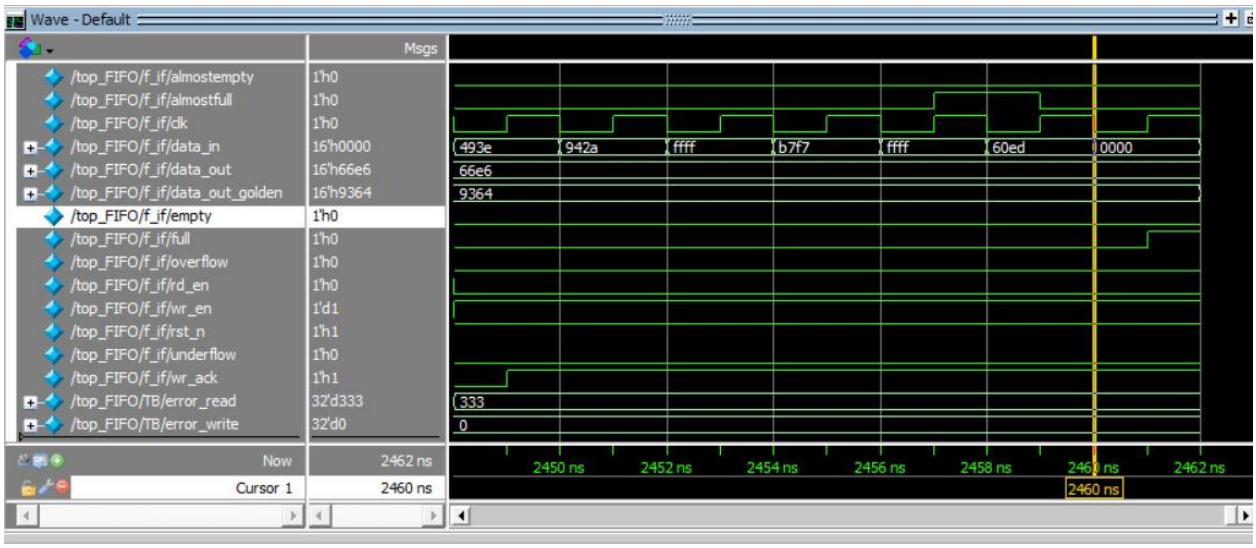


FIFO IS BUGGY at the read operation almost nothing works correctly and even all assertions fire at any read operation

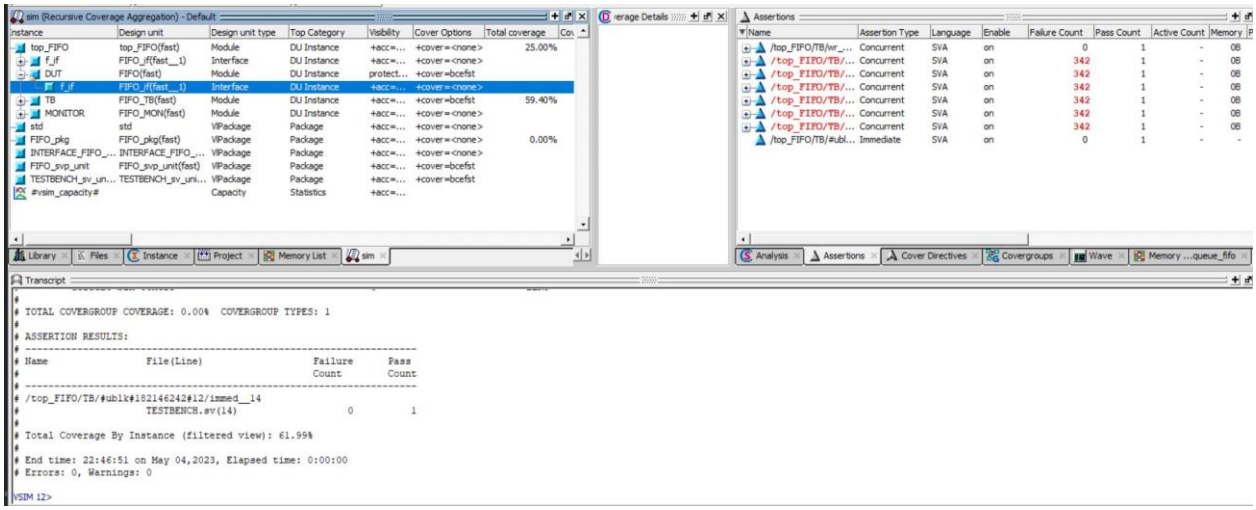
Note the write counter is 0 after 5000 iteration so the write operations works correctly .

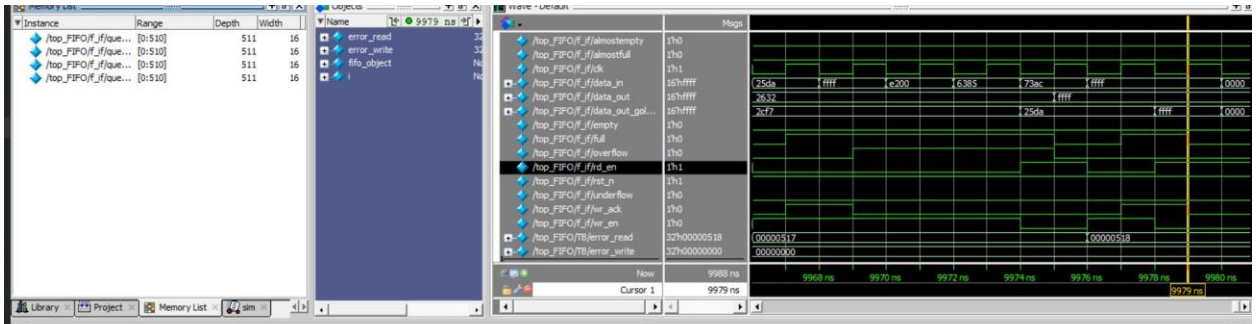


Almost full is delayed by 1 clock cycle



- all about the assertions like I said it fires mainly at the read operations





```
# ** Info: overflow failed
#    Time: 9979 ns Started: 9979 ns  Scope: top_FIFO.TB.overflow_flag_lb File: C:/Users/omerb/OneDrive/Desktop/All about System Verilog/FIFO000000000/TESTBENCH.sv Line: 117
# ** Info: empty failed
#    Time: 9979 ns Started: 9979 ns  Scope: top_FIFO.TB.empty_flag_lb File: C:/Users/omerb/OneDrive/Desktop/All about System Verilog/FIFO000000000/TESTBENCH.sv Line: 110
# ** Info: almostempty failed
#    Time: 9979 ns Started: 9979 ns  Scope: top_FIFO.TB.almostempty_flag_lb File: C:/Users/omerb/OneDrive/Desktop/All about System Verilog/FIFO000000000/TESTBENCH.sv Line: 103
# ** Info: full failed
#    Time: 9979 ns Started: 9979 ns  Scope: top_FIFO.TB.full_flag_lb File: C:/Users/omerb/OneDrive/Desktop/All about System Verilog/FIFO000000000/TESTBENCH.sv Line: 96
# ** Info: almostfull failed
#    Time: 9979 ns Started: 9979 ns  Scope: top_FIFO.TB.almostfull_flag_lb File: C:/Users/omerb/OneDrive/Desktop/All about System Verilog/FIFO000000000/TESTBENCH.sv Line: 89
# ** Info: underflow failed
#    Time: 9979 ns Started: 9979 ns  Scope: top_FIFO.TB.underflow_flag_lb File: C:/Users/omerb/OneDrive/Desktop/All about System Verilog/FIFO000000000/TESTBENCH.sv Line: 124
# data_in=    0,
#
#                       wr_ack = 1
# wr_ack PASS
# error message in read operation                9986 :data_out_design = 9566, data_out_golden = 982b
# data_in=13773,
#
#                       wr_en=1 ,
#
#                       rd_en =   ,
#
#                       rst_n = 1,
#
#                       underflow = 0,
#
#                       wr_ack = 0
# overflow PASS
# empty PASS
# almostempty PASS
# full PASS
# almostfull PASS
# underflow PASS
# ** Note: $stop    : C:/Users/omerb/OneDrive/Desktop/All about System Verilog/FIFO000000000/TESTBENCH.sv(54)
#    Time: 9988 ns  Iteration: 1  Instance: /top_FIFO/TB
# Break in Module FIFO_TB at C:/Users/omerb/OneDrive/Desktop/All about System Verilog/FIFO000000000/TESTBENCH.sv line 54

VSIM 147>
```

The coverage report which is not good due to bugs

```
#         default bin others                                0                    -    ZERO
#
# COVERGROUP COVERAGE:
# ----------------------------------------------------------------------------------------------------------------
# Covergroup                                              Metric       Goal       Bins    Status
#
# ----------------------------------------------------------------------------------------------------------------
#  TYPE /FIFO_pkg/FIFO_CLASS/CovCode                      0.00%        100          -    ZERO
#     covered/total bins:                                     0          2          -
#     missing/total bins:                                     2          2          -
#     % Hit:                                              0.00%        100          -
#     Coverpoint data_in_cp                               0.00%        100          -    ZERO
#         covered/total bins:                                 0          2          -
#         missing/total bins:                                 2          2          -
#         % Hit:                                          0.00%        100          -
#         bin max                                             0          1          -    ZERO
#         bin zero                                            0          1          -    ZERO
#         default bin others                                  0                     -    ZERO
#
# TOTAL COVERGROUP COVERAGE: 0.00%  COVERGROUP TYPES: 1
#
# ASSERTION RESULTS:
# ---------------------------------------------------------------------
# Name                 File(Line)                   Failure      Pass
#                                                   Count        Count
# ---------------------------------------------------------------------
# /top_FIFO/TB/#ublk#182146242#12/immed__14
#                      TESTBENCH.sv(14)                    0          1
#
# Total Coverage By Instance (filtered view): 61.99%
#
# End time: 22:46:51 on May 04,2023, Elapsed time: 0:00:00
```

```
# === Instance: /FIFO_pkg
# === Design Unit: work.FIFO_pkg
# ================================================================================
#
# Covergroup Coverage:
#     Covergroups                    1        na        na     0.00%
#         Coverpoints/Crosses        1        na        na       na
#             Covergroup Bins        2         0         2     0.00%
# ----------------------------------------------------------------------------------------------------------------
# Covergroup                                              Metric       Goal       Bins    Status
#
# ----------------------------------------------------------------------------------------------------------------
#  TYPE /FIFO_pkg/FIFO_CLASS/CovCode                      0.00%        100          -    ZERO
#     covered/total bins:                                     0          2          -
#     missing/total bins:                                     2          2          -
#     % Hit:                                              0.00%        100          -
#     Coverpoint data_in_cp                               0.00%        100          -    ZERO
#         covered/total bins:                                 0          2          -
#         missing/total bins:                                 2          2          -
#         % Hit:                                          0.00%        100          -
#         bin max                                             0          1          -    ZERO
#         bin zero                                            0          1          -    ZERO
#         default bin others                                  0                     -    ZERO
#
# COVERGROUP COVERAGE:
# ----------------------------------------------------------------------------------------------------------------
# Covergroup                                              Metric       Goal       Bins    Status
#
# ----------------------------------------------------------------------------------------------------------------
#  TYPE /FIFO_pkg/FIFO_CLASS/CovCode                      0.00%        100          -    ZERO
```

```
# ================================Toggle Details================================
#
# Toggle Coverage for instance /top_FIFO/TB --
#
#                                                  Node       1H->0L       0L->1H  "Coverage"
#                                                  ----------------------------------------
#                                      error_read[0-9]            1            1       100.00
#                                       error_read[10]            0            1        50.00
#                                     error_read[11-31]           0            0         0.00
#                                     error_write[0-31]           0            0         0.00
#                                             i[0-11]             1            1       100.00
#                                               i[12]             0            1        50.00
#                                            i[13-31]             0            0         0.00
#
# Total Node Count     =          96
# Toggled Node Count   =          22
# Untoggled Node Count =          74
#
# Toggle Coverage      =      23.95% (46 of 192 bins)
#
# ============================================================================================
# === Instance: /FIFO_pkg
# === Design Unit: work.FIFO_pkg
# ============================================================================================
#    58                                     // testing write operation
#
#    59                                     if(f_if.wr_en && (f_if.queue_fifo.size() <= FIFO_DEPTH)) begin
#
#    60                                       if (f_if.data_in != f_if.queue_fifo[$])begin
#
#    61            1                ***0***          $display("error message in write operation %t :data_in = %h, last_item_in_queue = %h",$time ,f_if.data_in,f_if.queue_fifo[$]);
#
#    62            1                ***0***          error_write++ ;
#
#    63                                       end
#
#    64                                     end
#
#    65                                     // testing read operation
#
#    66                                     else if (f_if.rd_en && (f_if.queue_fifo.size() != 0))begin
#
#    67                                      if (f_if.data_out != f_if.data_out_golden) begin
#
#    68            1                   1305        $display("error message in read operation %t :data_out_design = %h, data_out_golden = %h",$time ,f_if.data_out ,f_if.data_out_golden);
#
#    69            1                   1305        error_read++ ;
#
#
# Toggle Coverage:
#     Enabled Coverage             Bins     Hits   Misses  Coverage
#     ----------------             ----     ----   ------  --------
#     Toggles                       192       46      146    23.95%
#
#
# ----------------Focused Condition View--------------------
# Line       67 Item    1  (f_if.data_out != f_if.data_out_golden)
# Condition totals: 1 of 1 input term covered = 100.00%
#
#                                Input Term   Covered  Reason for no coverage   Hint
#                               -----------  --------  ----------------------  --------------
#   (f_if.data_out != f_if.data_out_golden)         Y
#
#      Rows:       Hits  FEC Target                                 Non-masking condition(s)
#  ---------  ---------  --------------------                      -------------------------
#   Row   1:          1  (f_if.data_out != f_if.data_out_golden)_0  -
#   Row   2:          1  (f_if.data_out != f_if.data_out_golden)_1  -
#
#
# Statement Coverage:
#     Enabled Coverage              Bins      Hits    Misses  Coverage
#     ----------------              ----      ----    ------  --------
#     Statements                      26        24         2    92.30%
#
# ================================Statement Details================================
#
# Statement Coverage for instance /top_FIFO/TB --
# NOTE: The modification timestamp for source file 'TESTBENCH.sv' has been altered since compilation.
#
#     Line         Item                      Count     Source
```

```
#   Row   4:          1  (f_if.queue_fifo.size() < FIFO_DEPTH)_1  f_if.wr_en
#
# ----------------Focused Condition View-------------------
# Line       60 Item    1  (f_if.data_in != f_if.queue_fifo[$])
# Condition totals: 0 of 1 input term covered = 0.00%
#
#                            Input Term   Covered  Reason for no coverage   Hint
#                           -----------  --------  ----------------------  --------------
#   (f_if.data_in != f_if.queue_fifo[$])         N  '_1' not hit            Hit '_1'
#
#      Rows:       Hits  FEC Target                                 Non-masking condition(s)
#  ---------  ---------  --------------------                       -------------------------
#   Row   1:          1  (f_if.data_in != f_if.queue_fifo[$])_0  -
#   Row   2:    ***0***  (f_if.data_in != f_if.queue_fifo[$])_1  -
#
# ----------------Focused Condition View-------------------
# Line       66 Item    1  (f_if.rd_en && (f_if.queue_fifo.size() != 0))
# Condition totals: 1 of 2 input terms covered = 50.00%
#
#                     Input Term   Covered  Reason for no coverage   Hint
#                    -----------  --------  ----------------------  --------------
#                     f_if.rd_en         Y
#   (f_if.queue_fifo.size() != 0)         N  '_0' not hit            Hit '_0'
#
#      Rows:       Hits  FEC Target                          Non-masking condition(s)
#  ---------  ---------  --------------------                ------------------------
#   Row   1:          1  f_if.rd_en_0                        -
#   Row   2:          1  f_if.rd_en_1                        (f_if.queue_fifo.size() != 0)
#   Row   3:    ***0***  (f_if.queue_fifo.size() != 0)_0  f_if.rd_en
#   Row   4:          1  (f_if.queue_fifo.size() != 0)_1  f_if.rd_en
#
# ----------------Focused Condition View-------------------
# Line       67 Item    1  (f_if.data_out != f_if.data_out_golden)
# Condition totals: 1 of 1 input term covered = 100.00%
#
# ----------------Focused Condition View-------------------
# Line       45 Item    1  (f_if.rd_en && (f_if.queue_fifo.size() != 0))
# Condition totals: 1 of 2 input terms covered = 50.00%
#
#                     Input Term   Covered  Reason for no coverage   Hint
#                    -----------  --------  ----------------------  --------------
#                     f_if.rd_en         Y
#   (f_if.queue_fifo.size() != 0)         N  '_0' not hit            Hit '_0'
#
#      Rows:       Hits  FEC Target                          Non-masking condition(s)
#  ---------  ---------  --------------------                ------------------------
#   Row   1:          1  f_if.rd_en_0                        -
#   Row   2:          1  f_if.rd_en_1                        (f_if.queue_fifo.size() != 0)
#   Row   3:    ***0***  (f_if.queue_fifo.size() != 0)_0  f_if.rd_en
#   Row   4:          1  (f_if.queue_fifo.size() != 0)_1  f_if.rd_en
#
# ----------------Focused Condition View-------------------
# Line       59 Item    1  (f_if.wr_en && (f_if.queue_fifo.size() < FIFO_DEPTH))
# Condition totals: 2 of 2 input terms covered = 100.00%
#
#                       Input Term   Covered  Reason for no coverage   Hint
#                      -----------  --------  ----------------------  --------------
#                       f_if.wr_en         Y
#   (f_if.queue_fifo.size() < FIFO_DEPTH)         Y
#
#      Rows:       Hits  FEC Target                            Non-masking condition(s)
#  ---------  ---------  --------------------                  ------------------------
#   Row   1:          1  f_if.wr_en_0                          -
#   Row   2:          1  f_if.wr_en_1                          (f_if.queue_fifo.size() < FIFO_DEPTH)
#   Row   3:          1  (f_if.queue_fifo.size() < FIFO_DEPTH)_0  f_if.wr_en
#   Row   4:          1  (f_if.queue_fifo.size() < FIFO_DEPTH)_1  f_if.wr_en
#
```

```
#                                          2241     All False Count
# Branch totals: 3 hits of 3 branches = 100.00%
#
# ------------------------------------IF Branch------------------------------------
#     60                                   1315     Count coming in to IF
#     60              1                   ***0***         if (f_if.data_in != f_if.queue_fifo[$])begin
#
#                                          1315     All False Count
# Branch totals: 1 hit of 2 branches = 50.00%
#
# ------------------------------------IF Branch------------------------------------
#     67                                   1437     Count coming in to IF
#     67              1                    1305        if (f_if.data_out != f_if.data_out_golden) begin
#
#                                           132     All False Count
# Branch totals: 2 hits of 2 branches = 100.00%
#
#
# Condition Coverage:
#     Enabled Coverage              Bins   Covered    Misses  Coverage
#     ----------------              ----      ----    ------  --------
#     Conditions                      10         7         3    70.00%
#
# ================================Condition Details================================
#
# Condition Coverage for instance /top_FIFO/TB --
# NOTE: The modification timestamp for source file 'TESTBENCH.sv' has been altered since compilation.
#
#   File TESTBENCH.sv
# ----------------Focused Condition View-------------------
# Line       40 Item    1  (f_if.wr_en && (f_if.queue_fifo.size() < FIFO_DEPTH))
# Condition totals: 2 of 2 input terms covered = 100.00%
#
#                             Input Term   Covered  Reason for no coverage   Hint
#     ----         ----                     -----     ------
#   File TESTBENCH.sv
# ------------------------------------IF Branch------------------------------------
#     33                                   5000     Count coming in to IF
#     33              1                       7        if(~f_if.rst_n) begin
#
#     37              1                    4993        else begin
#
# Branch totals: 2 hits of 2 branches = 100.00%
#
# ------------------------------------IF Branch------------------------------------
#     40                                   4993     Count coming in to IF
#     40              1                    1948          if(f_if.wr_en && (f_if.queue_fifo.size() <= FIFO_DEPTH))begin
#
#     44              1                    3045          else if (~f_if.empty)begin // read operation
#
#                                        ***0***     All False Count
# Branch totals: 2 hits of 3 branches = 66.66%
#
# ------------------------------------IF Branch------------------------------------
#     45                                   3045     Count coming in to IF
#     45              1                    1437           if (f_if.rd_en && (f_if.queue_fifo.size() != 0))begin
#
#                                          1608     All False Count
# Branch totals: 2 hits of 2 branches = 100.00%
#
# ------------------------------------IF Branch------------------------------------
#     59                                   4993     Count coming in to IF
#     59              1                    1315       if(f_if.wr_en && (f_if.queue_fifo.size() <= FIFO_DEPTH)) begin
#
#     66              1                    1437       else if (f_if.rd_en && (f_if.queue_fifo.size() != 0))begin
#
```

```
# vcover report top_FIFO.ucdb -details -annotate -all
# Coverage Report by instance with details
#
# ================================================================================
# === Instance: /top_FIFO/TB
# === Design Unit: work.FIFO_TB
# ================================================================================
#
# Assertion Coverage:
#     Assertions                        1         1         0   100.00%
# --------------------------------------------------------------------
# Name                 File(Line)                    Failure      Pass
#                                                    Count        Count
# --------------------------------------------------------------------
# /top_FIFO/TB/#ublk#182146242#12/immed__14
#                      TESTBENCH.sv(14)                    0          1
# Branch Coverage:
#     Enabled Coverage              Bins      Hits    Misses  Coverage
#     ----------------              ----      ----    ------  --------
#     Branches                        14        12         2    85.71%
#
# ================================Branch Details================================
#
# Branch Coverage for instance /top_FIFO/TB
```

Feature	ASSERTION
If write operation is done the the wr_ack flag is set within 2 clk cycles	@(posedge f_if.clk)(~f_if.full && f_if.wr_en && (f_if.queue_fifo.size() < FIFO_DEPTH))|-> ##[0:2] f_if.wr_ack;
If the fifo is written with 511 element then almostfull flag is set	@(posedge f_if.clk)(f_if.queue_fifo.size() == FIFO_DEPTH-1)|-> f_if.almostfull ;
If the fifo is written with 512 element then full flag is set	@(posedge f_if.clk)(f_if.queue_fifo.size() == FIFO_DEPTH)|-> f_if.full ;
If the fifo is written with 1 element then almostempty flag is set	@(posedge f_if.clk)(f_if.queue_fifo.size() == 1)|-> f_if.almostempty ;
If the fifo is written with 0 element then aempty flag is set	@(posedge f_if.clk)(f_if.queue_fifo.size() == 0)|-> f_if.empty ;
When the fifo is full and a write operation is requested then the overflow flag is set	@(posedge f_if.clk)(f_if.full && f_if.wr_en)|-> f_if.overflow ;

When the fifo is empty and a read operation is requested then the underflow flag is set	@(posedge f_if.clk)(f_if.empty && f_if.rd_en)|-> f_if.underflow ;

The codes are in the files 😊