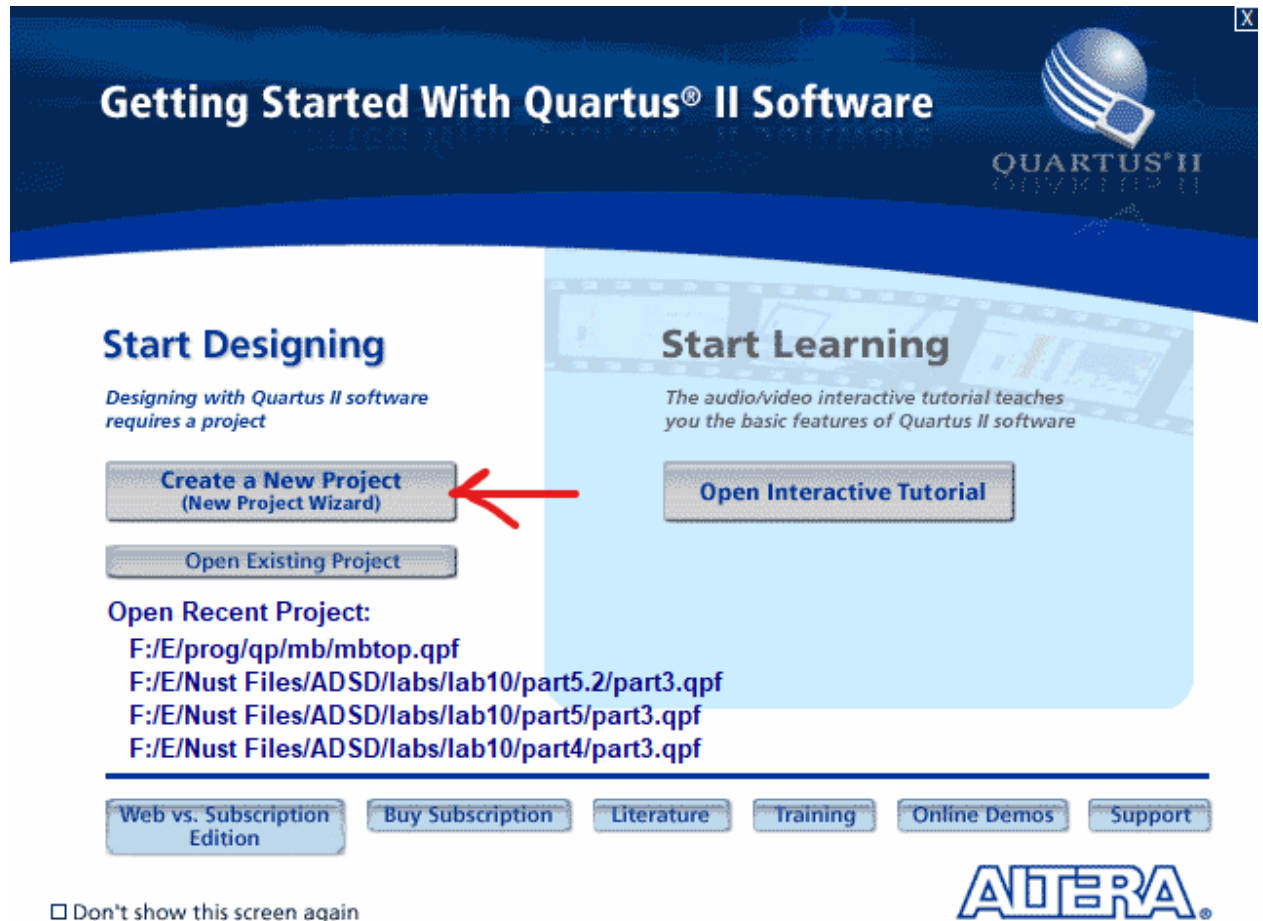


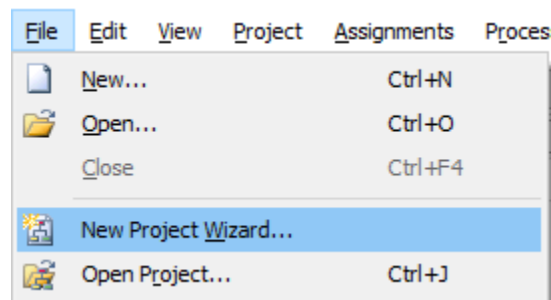
Creating a new project

Click the new project wizard button on the welcome screen



OR

Go to File > New Project Wizard



Click Next if an intro page opens

New Project Wizard

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

F:\projects\my_project_foo\

What is the name of this project?

foo

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

module_foo

Use Existing Project Settings...

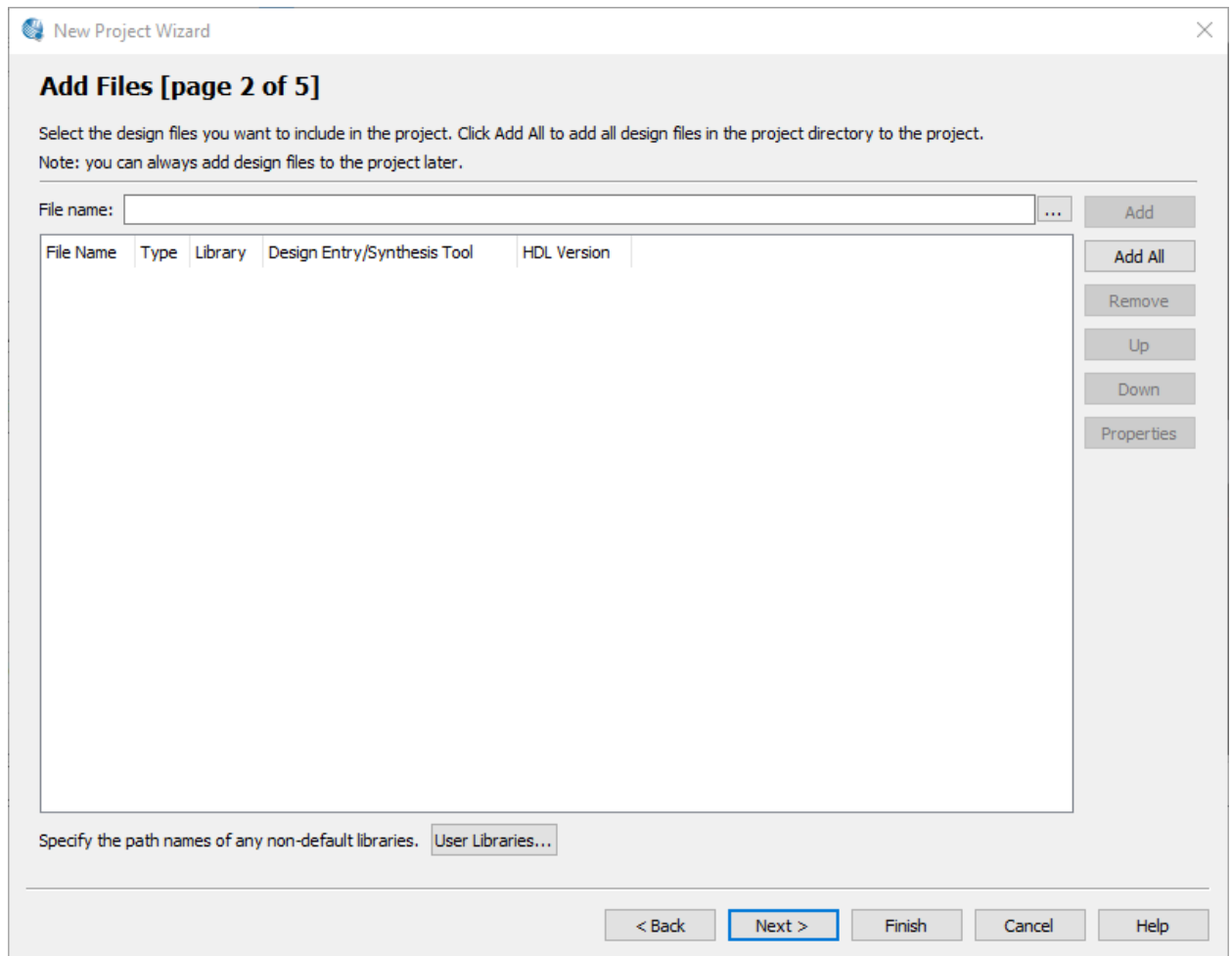
< Back Next > Finish Cancel Help

Enter path of your project.

Enter the name.

Enter the module name. (NOTE: This **must** match with the Verilog module you will write)

Click Next



Use this page to add any existing Verilog files to your project. If there are none, click Next

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

Device family

Family: Cyclone II

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter: 20f484c7

☒ Show advanced devices ☐ HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	Global
EP2C20F484C7	1.2V	18752	315	239616	52	4	16

Companion device

HardCopy:

☐ Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel Help

Set the family to "Cyclone II"

In the name filter type "20f484C7", which is the code for the FPGA on our board

Select the device in the list

Click Next

New Project Wizard

EDA Tool Settings [page 4 of 5]

Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	Verilog HDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel Help

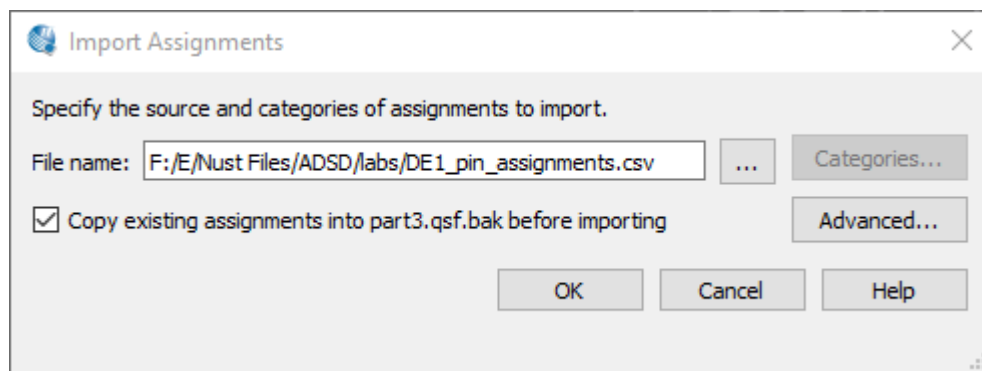
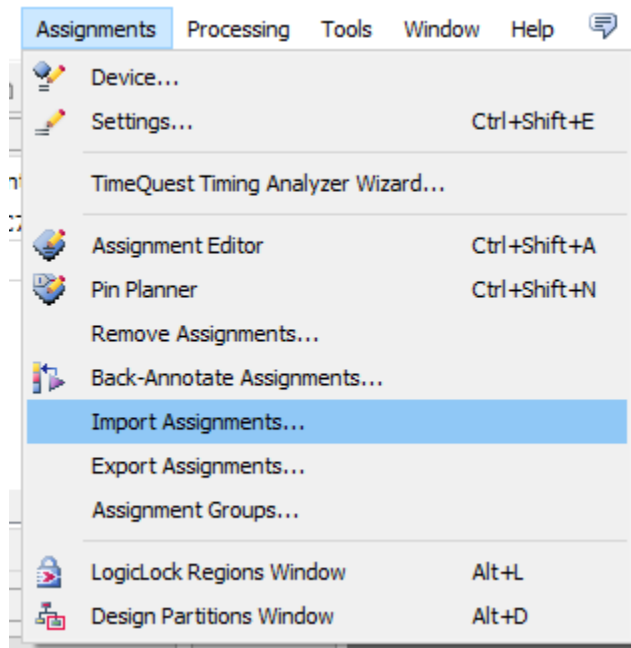
Set the simulation tool to “ModelSim-Altera” and language to “Verilog-HDL”

Click Next

After that, click Finish on the Summary page

Now you need to add pin assignment file so that Quartus knows which FPGA pins are mapped to the peripherals on the board. For more information about this, view the user manual document.

To add pin assignments, go to Assignments > Import Assignments



Give the path to the assignment file and click Ok.

Now you are ready to start coding.

To add a new Verilog file, go to File > New > Verilog HDL file

A blank file will open, write your code in this file and save it in the project directory.