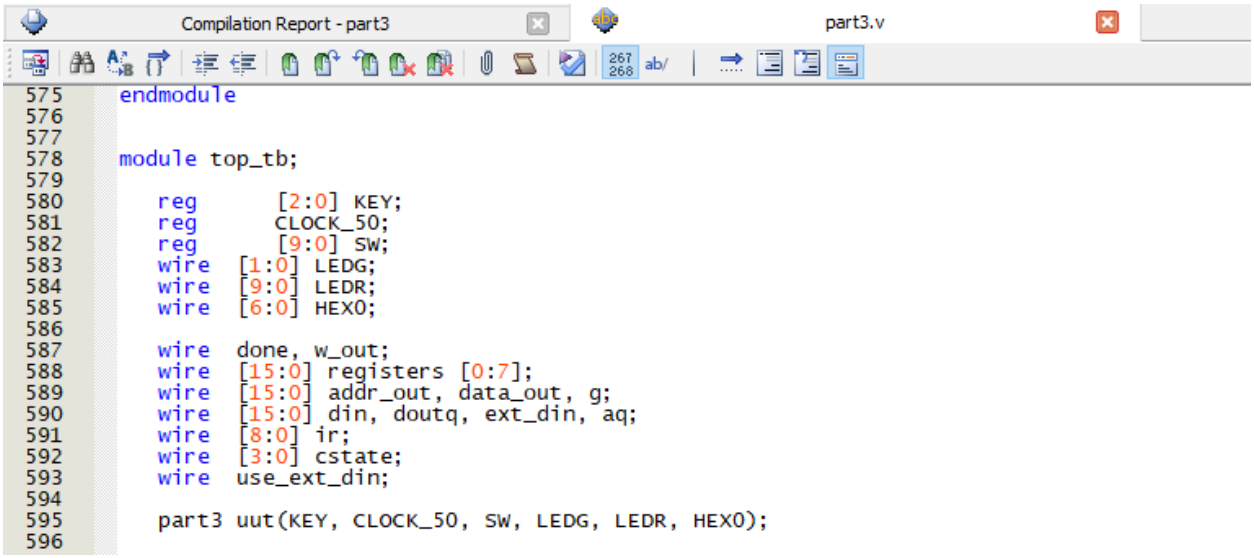
Using ModelSim with Quartus II

1. WRITE AN APPROPRIATE TESTBENCH

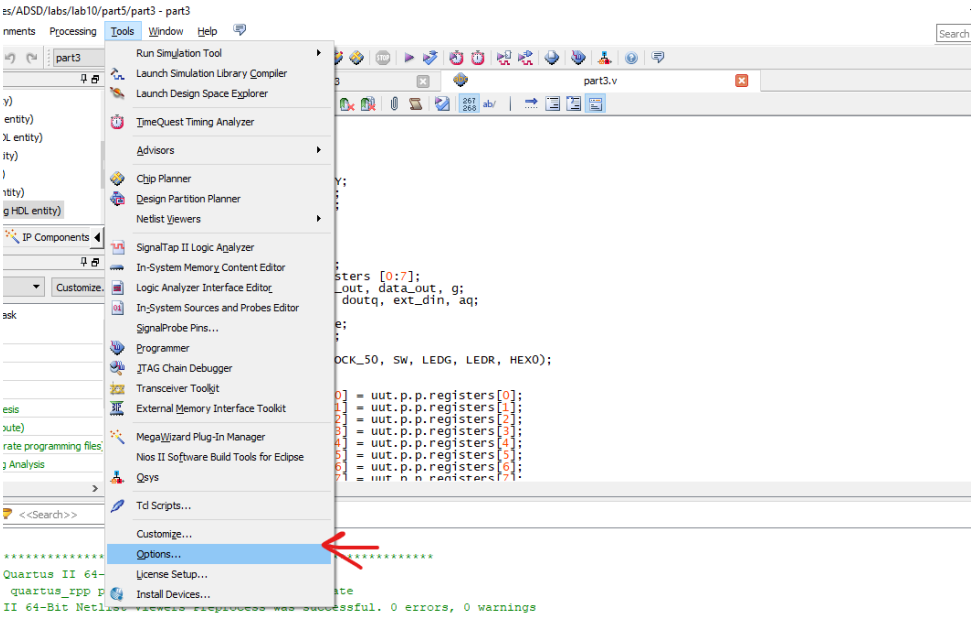
Create a testbench for your design. You may use a separate file or this or keep it in the same file.

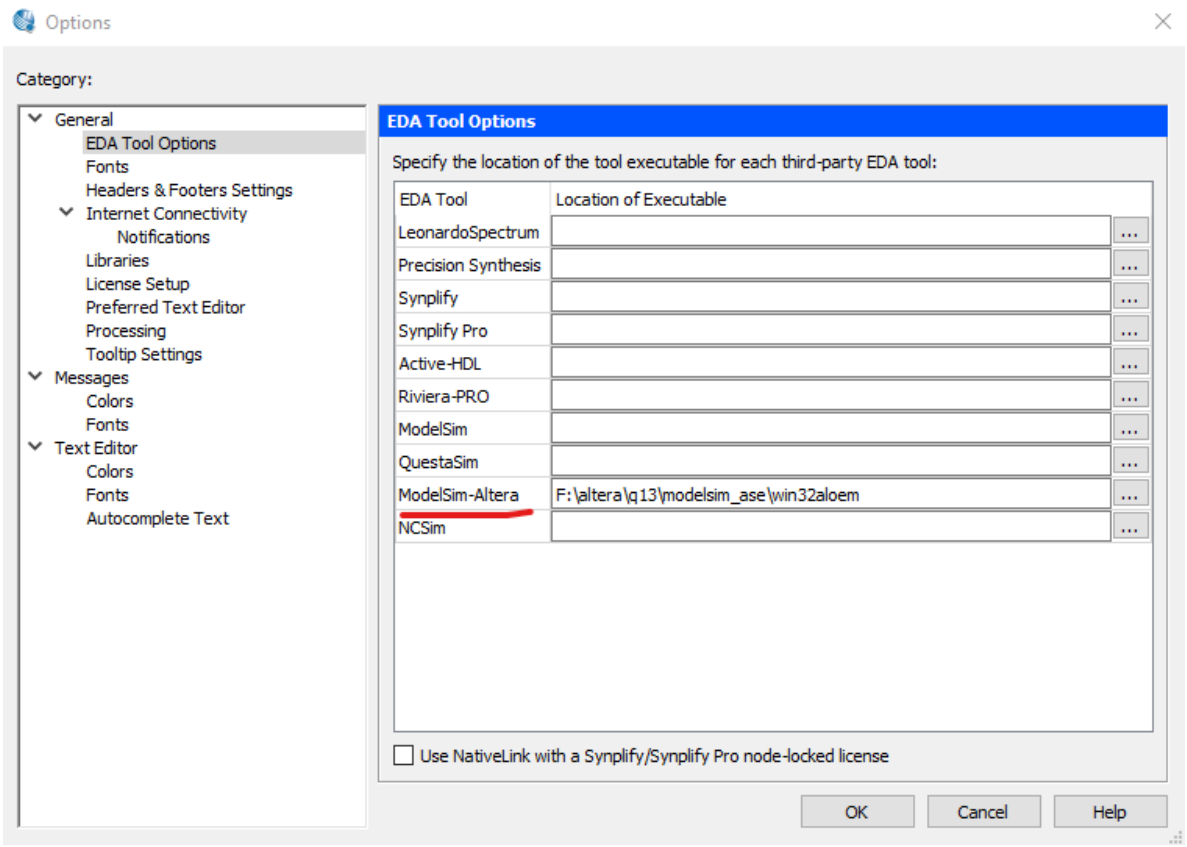



```
575   endmodule
576
577
578   module top_tb;
579
580      reg      [2:0] KEY;
581      reg      CLOCK_50;
582      reg      [9:0] SW;
583      wire  [1:0] LEDG;
584      wire  [9:0] LEDR;
585      wire  [6:0] HEX0;
586
587      wire  done, w_out;
588      wire  [15:0] registers [0:7];
589      wire  [15:0] addr_out, data_out, g;
590      wire  [15:0] din, doutq, ext_din, aq;
591      wire  [8:0] ir;
592      wire  [3:0] cstate;
593      wire  use_ext_din;
594
595      part3 uut(KEY, CLOCK_50, SW, LEDG, LEDR, HEX0);
596
```

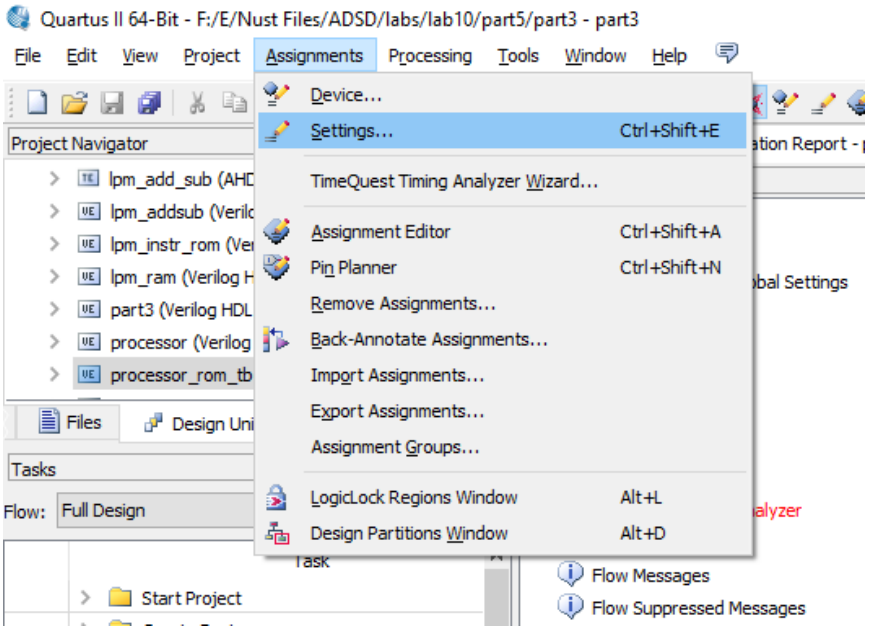
2. MAKE SURE QUARTUS KNOWS THE LOCATION OF MODELSIM EXECUTABLE

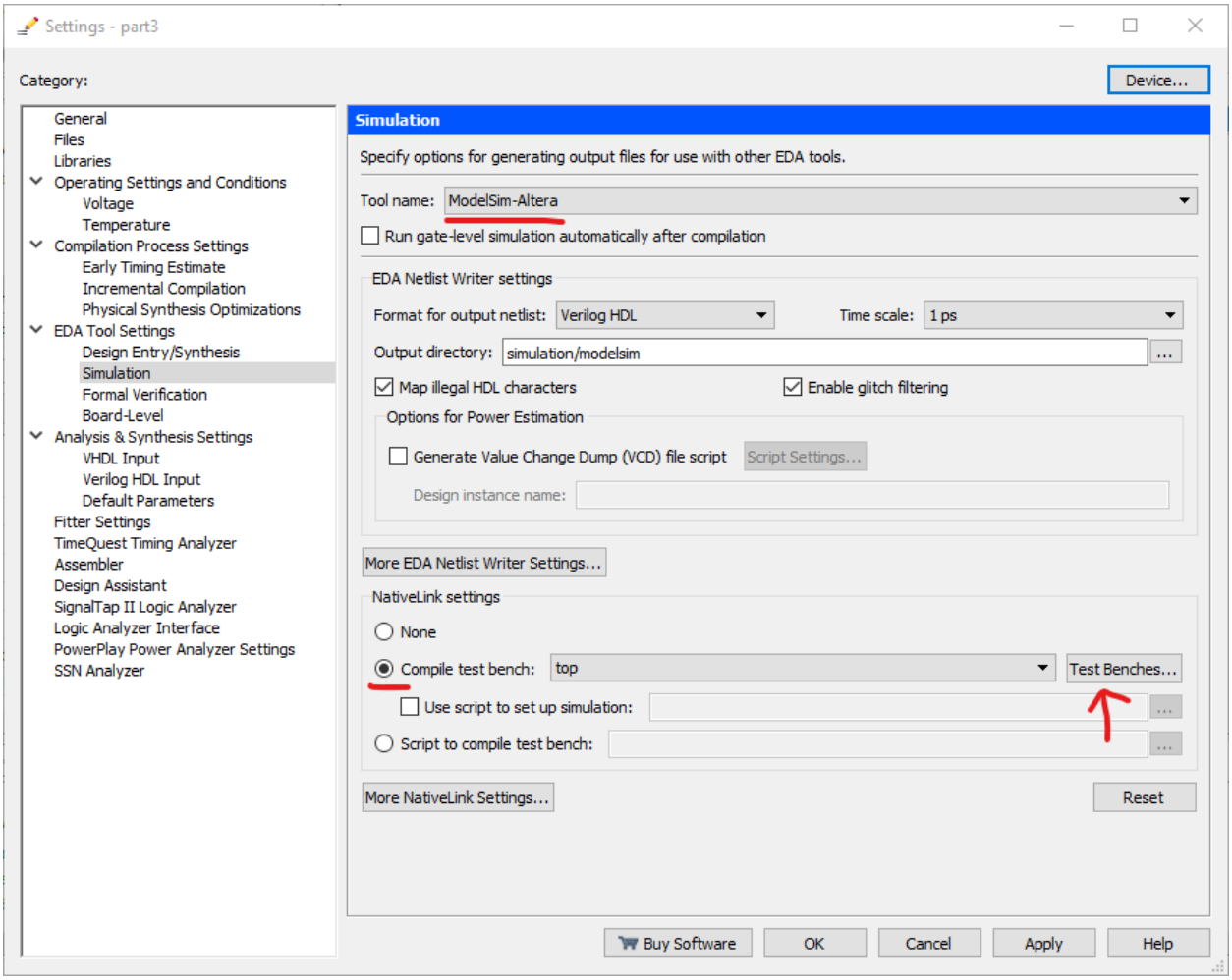
You only need to do this once.

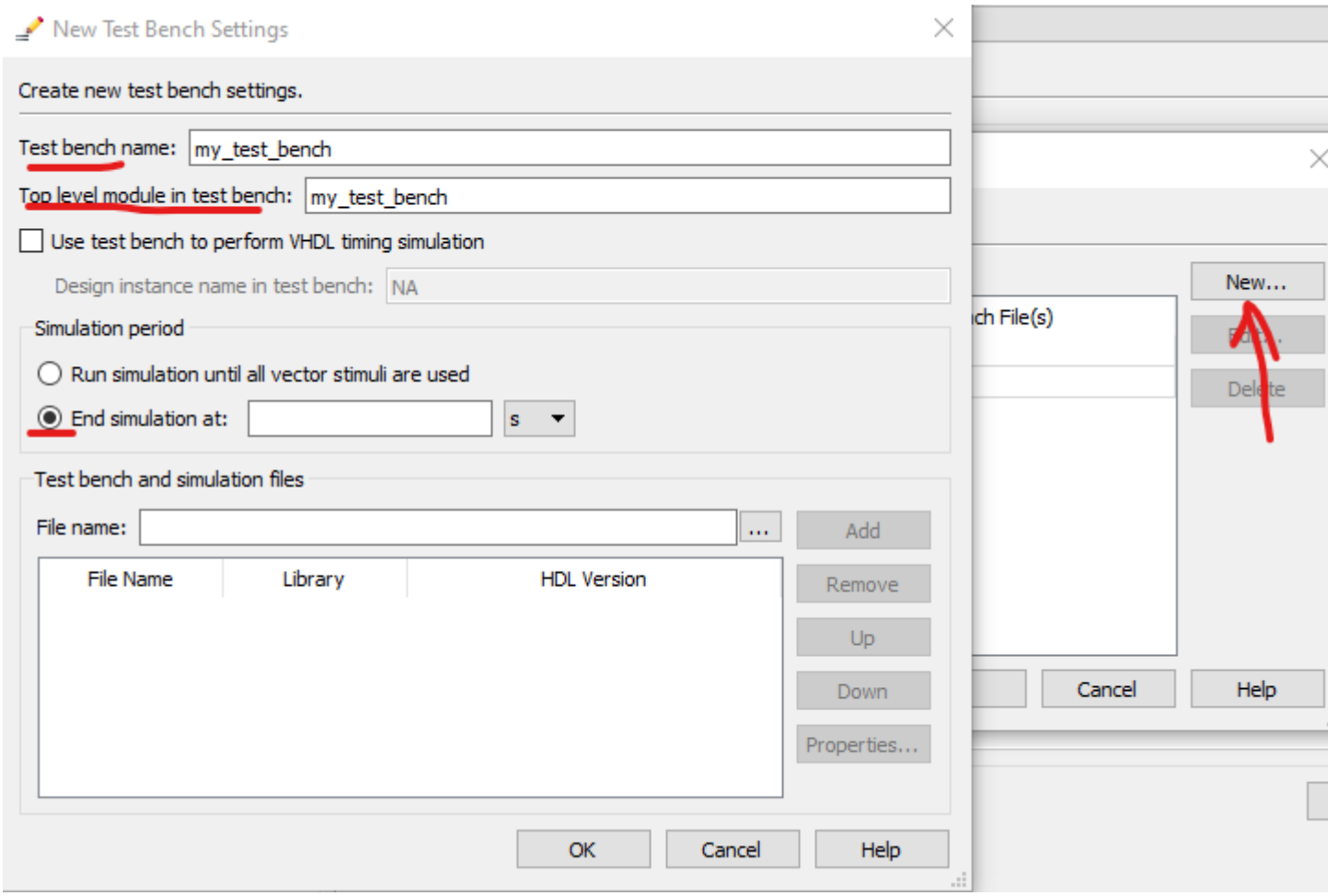




3. TELL QUARTUS ABOUT YOUR TESTBENCH







In the field Test bench name, name your test bench.

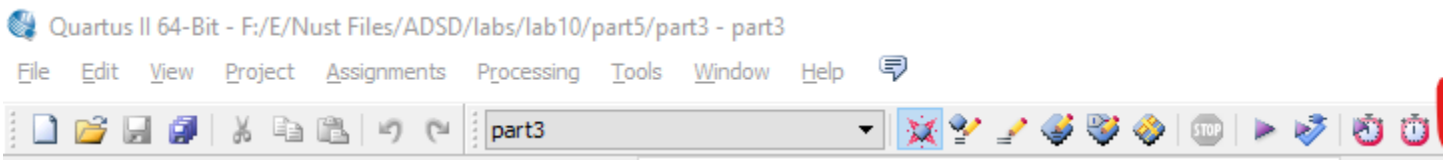
In the field Top level module in test bench, write the name of the Verilog module of your test bench

The field End Simulation at, write 1000 ps. You can change this number but 1000 ps is enough for most cases.

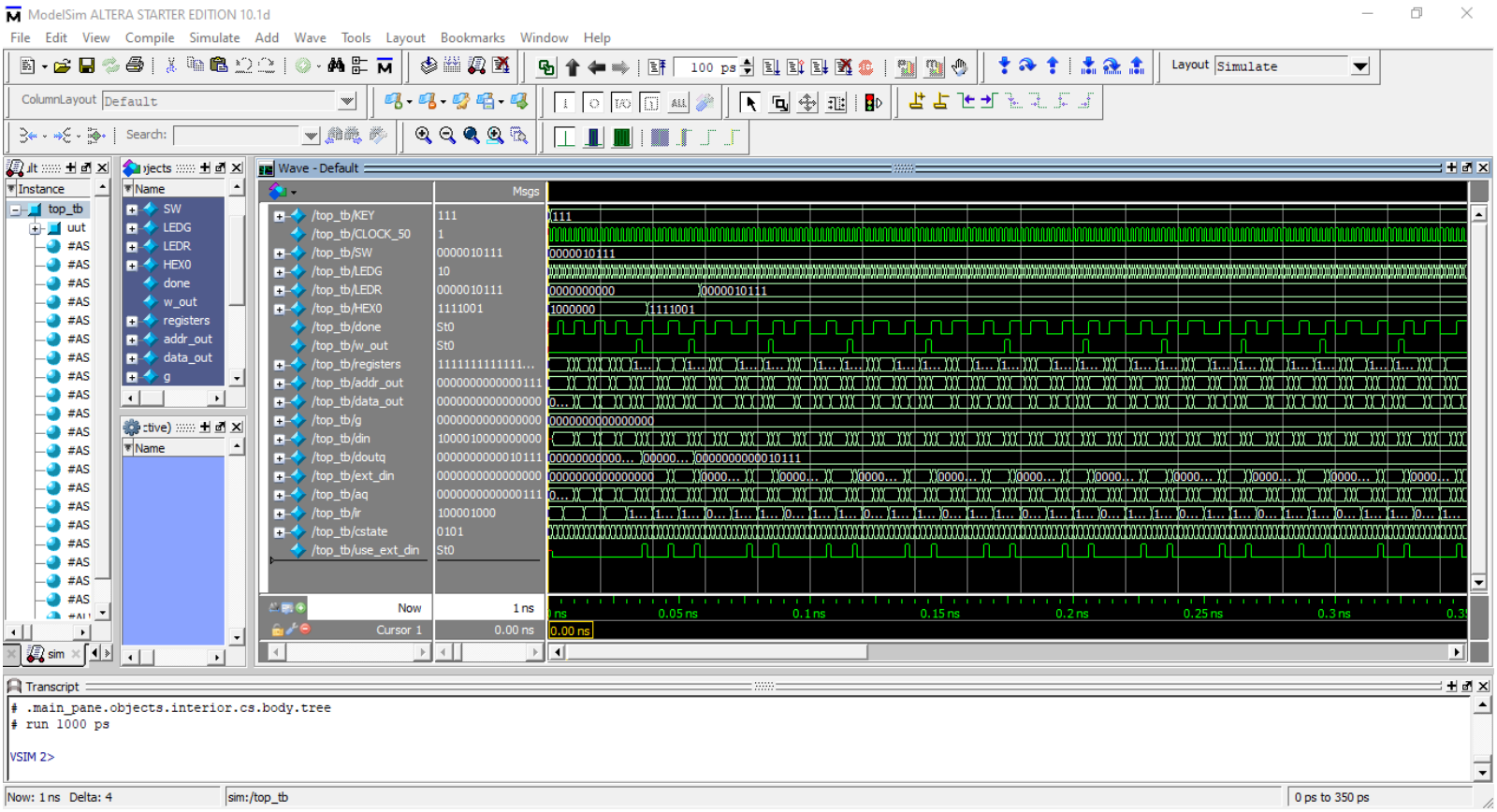
In the filename field, browse for the Verilog file that has the test bench and click Add button.

Click ok and return to Quartus.

4. LAUNCH SIMULATION



Click the launch RTL simulation button and ModelSim will open up.


ModelSim ALTERA STARTER EDITION 10.1d
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
Msgs
/top_tb/KEY
/top_tb/CLOCK_50
/top_tb/SW
/top_tb/LEDG
/top_tb/LEDR
/top_tb/HEX0
/top_tb/done
/top_tb/w_out
/top_tb/registers
/top_tb/addr_out
/top_tb/data_out
/top_tb/g
/top_tb/din
/top_tb/doutq
/top_tb/ext_din
/top_tb/aq
/top_tb/ir
/top_tb/cstate
/top_tb/use_ext_din
Now
Cursor 1
Transcript
.main_pane.objects.interior.cs.body.tree
run 1000 ps
VSIM 2>
Now: 1 ns Delta: 4
sim:/top_tb
0 ps to 350 ps