- ***Show the circuits connection on the transistor level using VISIO or any other software tool.***
- ***Deadline due to May 25, 2019.***
- ***The group can be out of 2-3 students.***

## Problem 1

Design AU (Arithmetic Unit) using any preferred transistor level logic design.
This AU must do the following:

a) It has two inputs A and B 3-bit each (for example A "010", B "110").
b) The arithmetic circuit performs Multiplication "A*B" using 3-bit adder.

## Problem 2 (Bonus)

Design Synchronous up/down counter (The flip flops in counter must designed using another preferred transistor level logic design than used in Problem 1).

***Simulate this design on Multisim.***

***Good Luck***