2-Operand

OP-Code				Add Mode			Src Reg			Add Mode			Dest Reg		

Instruction	Op-Code
MOV	0000
ADD	0001
ADC	0010
SUB	0011
SBC	0100
AND	0101
OR	0110
XNOR	0111
CMP	1000

1-Operand

						OP-Code				Add Mode			Src		
1	1	0	X	X	X										

Instruction	Op-Code
INC	0000
DEC	0001
CLR	0010
INV	0011
LSR	0100
RDR	0101
RRC	0110
ASR	0111
LSL	1000

ROL	1001
RLC	1010

Branch

OPCODE :: 8 Bits , Offset :: 8 Bits

Instructions	OPCODE(Binary)
BR (Branch unconditionally)	10100 000
BEQ (Branch if equal)	10100 001
BNE (Branch if not equal)	10100 010
BLO (Branch if Lower)	10100 011
BLS (Branch if Lower or same)	10100 100
BHI (Branch if Higher)	10100 101
BHS (Branch if Higher or same)	10100 110

No operand

OPCODE :: 5 Bits and 11 don’t care

Instructions	OPCODE(Binary)
HLT (Halt)	1110 0 00000000000
NOP (No Operation)	1110 1 00000000000

Jump Sub-Routine

OPCODE :: 6 Bits

Instructions	OPCODE(Binary)
JSR (Jump to subroutine)	1111 00
RTS (Return from subroutine)	1111 01

INTERRUPT	1111 10
IRET	1111 11