Control Store

000000	**SUB/CMP**	F = A-B,Zin,Src-out BA: 011000 => ((umar0 + (IR3'.IR4'.IR5')).(sub),umar1+(cmp))	
000001	**ADD**	F= A+B,Zin,Src-out	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
000010	**ADC**	F =A+B+Cin,Zin,Src-out	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
000011	**MOV**	F = BUS (B) , Zin ,Src-out	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
000100	**SBC**	F = A -B-Cin,Zin,Src-out	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
000101	**AND**	F= A and B,Zin,Src-out	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
000110	**OR**	F = A or B, Zin ,Src-out	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
000111	**Xnor**	F = A xnor B, Zin ,Src-out	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
001000	**INC**	F = INC DEST(B) , Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
001001	**DEC**	F = DEC DEST (B) , Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
001010	CLR	F = 0, Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
001011	INV	F = not [DEST(B)] , Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
001100	LSR	F = LSR B, Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
001101	ROR	F =ROR B, Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
001110	RRC	F= RRC B, Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
001111	ASR	F= ASR B, Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
010000	LSL	F= LSL B, Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
010001	ROL	F=ROL B, Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
010010	RLC	F=RLC B, Zin	BA: 011000 => (umar0 + (IR3'.IR4'.IR5'))
010011	BR1	Pcout-bus ,Yin	010100
010100	BR2	IRaddressfld-out ,F=A+B,Zin	010101
010101	BR3	Zout,Pcin-bus	011010
010110	HLT		010110
010111	NOP		011010
011000	SAVE1	MDR-in,Zout,WR	011010

011001	SAVE2	Rdst-in,Zout	011010
011010	Fetch	Pcout,Pcout-inc,M ARin,Rd	011011
011011	Decode	Pcin-inc,MDRout,IRin	Wide branch
011100			
011101			
011110			
011111			
100000	Rdst-out,Yin	000000 => (2op.(umar0,1,2+ir12,13,14)+1op.(umar0,1,2,3,4 + ir6,7,8,9',9))	
100001	Rdst-out, MARin,Rd, F=INC Bus ,Zin		100101
100010	Rdst-out,F=DEC Bus,Zin		100110
100011	Pcout,Pcout-inc,MARin,Rd		100111
100100	Rdsout,MAR-in,Rd		101011
100101	Zout,Rdst-in		101010 => (umar0 + IR5')
100110	Zout,Rdst-in,MAR-in,Rd		101010 => (umar0 + IR5')
100111	Pcin-inc,MDR-out,Yin		101000
101000	Rdstout, F=A+B,Zin		101001
101001	Zout,MAR-in,Rd		101010 => (umar0 + IR5')
101010	MDR-out,MARin		101011
101011	MDR-out,Yin,Rd	000000 => (2op.(umar0,1,2+ir12,13,14)+1op.(umar0,1,2,3,4 + ir6,7,8,9',9))	
101100			
101101			
101110			
101111			
110000			
110001			
110010			
110011			

110100	Rsrcout,Src-in	100000 => (umar0,1 + ir3,4 , umar2 +(reg indirect))
110101	Rsrcout,MAR-in,Rd	111111
110110	Rsrcout,MAR-in,Rd, F=INC Bus,Zin	110111
110111	Zout,Rsrc-in	111110=> (umar0+(IR11'))
111000	Rsrcout,DEC Bus,Zin	111001
111001	Zout,Rsrcin,MAR-in,Rd	111110=> (umar0+(IR11'))
111010	Pcout,MAR-in,Rd,Pcout-inc	111011
111011	Pcin-inc,MDR-out,Yin	111100
111100	Rsrc-out, F=A+B,Zin	111101
111101	Zout,MAR-in,Rd	111110=> (umar0+(IR11'))
111110	MDR-out,MARin	111111
111111	MDR-out, Src-in,Rd	100000 => (umar0,1 + ir3,4 , umar2 +(reg indirect))