Project-3: Designing a 16-bit Adder

Omar Ali Elayat  
Electrical and Computer Engineering DepartmentUniversity of Waterloo

*Abstract*— This project focuses on design exploration, analysis, and optimization of 16-bit adders architectures using 65nm technology. The objectives include detailed circuit design, and performance evaluation through functional and corner simulations. This study aims to enhance our understanding of full adder circuit behavior in modern semiconductor technology by investigating the impact of power-supply voltage on power-delay and energy-delay products.

Keywords—CMOS Technology, Arithmetic Units, Corner Simulation, RCA, CSAsq, KSA, CBA, PDP, EDP.

# Introduction

This project explores and optimizes four 16-bit adder architectures—Ripple Carry Adder (RCA), Square Root Carry Select Adder (CSAsq), Carry Bypass Adder (CBA), and Kogge-Stone Adder (KSA) using 65nm technology. The selected architectures offer unique trade-offs in terms of speed, area, and power consumption. The primary objectives of this study encompass four key aspects. First, the project entails the detailed transistor-level design and optimizations of the 16-bit adder circuits. Subsequently, We set an objective function as a benchmark and the most optimized circuit is chosen and functionally verified against three test vectors that puts the adders in extreme propagate (P) and/or generate (G) conditions. The chosen adder delay/power/PDP/EDP vs power supply is also assessed. The rest of the report is organized as follows: Chapter II describes in detail the design and optimization of the adders. Chapter III discusses functional simulations, Chapter IV discusses global mismatch simulations and power-supply sweep for the chosen adder, and finally Chapter V is the conclusion.

# Adders design and optimization

## 1 -Bit Full adder Design and Optimization

To design a highly optimized 16-bit adder, CMOS and PTL FA adders were designed and optimized to fit our design requirements.

* 1. *CMOS Mirrored Full Adder*

A Mirrored Logic Full Adder is considered advantageous compared to a normal CMOS adder due to its symmetric structure. The mirrored design enhances performance by ensuring balanced signal paths, resulting in improved speed and reduced power consumption. The symmetry in layout contributes to better signal propagation, making mirrored logic full adders suitable for high carry propagation chains.

The pull-down network (PDN) and pull-up network (PUN) of the adder was mapped to minimum-size inverters to provide equal drive strengths, symmetric rise and fall times, and power efficiency while simplifying the design and reducing sensitivity to manufacturing variations. In this design, Wn was fixed at 200 nm and using ADE L parametric analysis, Wp was swept in the range from 1 to 5 to find the ratio that equates TpLH to TpHL. According to the sweep, ≅2 yield a TpLH = TpHL ≅ 5.4ps. Accordingly, of the adder is fixed at 2:1.

After sizing the PDN and PUN to min. sized inverter, the critical path (Cin Cout) was sized up for minimum path effort of Eq. (1) & Eq. (2) hence, minimizing the critical delay adder.

(1)

(2)

For maximum performance, the path effort (PE) should be close to 4 [1]. Since the logical effort (LE) is 2, 2. For a two cascaded minimum-sized 1-bit FA of Fig. (2), the total load on carry gate, CL. Where Cci is the input capacitance of carry-in signal. Solving for Cci yields PUNci : PDNci = 14:7.

The critical path is further minimized by eliminating inverters in the carry chain, as in Fig. (3), thus, reducing inverting stages through exploiting the adder’s inversion property.

* 1. *PTL Full adder*

CBA and KSA adders utilized the outputs of the setup block (P, G) and Ci signals to compute the sum (S) and carry-out (Co) instead of A and B according to Eq.(3) & Eq.(4).

(3)

(4)

The used gates are non-inverting by nature. Thus, PTL designs in Fig. (2) were proven to be cheaper in silicon than their CMOS counterparts by eliminating the output inversion. Transmission gates were used to ensure full output swing, and low propagation delay. Moreover, appropriate buffering was placed along the PTL carry chains to break the exponential growth of the Elmore chain every M switch. Obviously, the number of switches per segment grows with increasing values of tbuff. In current technologies, Mopt is typically around 3 [1].

## Ripple Carry Adder

A 16-bit RCA, Fig. (1), was constructed by cascading three 6-bit RCA, Fig. (3), where every 6-bit RCA is composed of six CMOS FA chained in series. As the inversion property was used, all the odd S outputs {1,3,5, … ,15} were inverted. According to Eq. (5) & Eq. (6), the worst cade delay of RCA is typically linear with the number of bits (N).

(5)

(6)

Where tcarry is the carry delay, and tsum is the sum delay.

## Carry Bypass Adder

Similar to RCA, a 16-bit CBA, Fig (1), is constructed from a 4-unit series chain of 4-bit CBA, Fig (3). The 4-bit RCA is composed of 3 stages, from top to bottom: Setup, addition, and Multiplexing. The inputs of the 4-bit CBA are the Cin and A[3:0] and B[3:0] vectors. Then, the next block takes an offset of M bits from both vectors, where M is 4 in our case. We will use the notation Ai|Bi pair to refer to the A and B inputs of a given blocki. The working principle is to directly forward the Cin if all the Ai|Bi to Am-1Bm-1 pairs propagates the Cin block input. Thus, blocki+1 can start the addition immediately without waiting for the Co from Am-1Bm-1 of blocki-1. Initially, the setup block of each Ai|Bi generates a propagate (P) and generate (G) pair (Pi|Gi) according to Eq. (7) & Eq. (8). Then, Pi|Gi and Cin is fed to the PTL P|G adder as discussed earlier. The vector S[0:3] is driven directly from the adders, however, the Co has to be multiplexed with Cin to decide whether to bypass the carry or kill/generate according to the mux signal Sel from Eq. (9).

(7)

(8)

(9)

According to Eq. (10) & Eq. (11), the worst cade delay of CBA is typically linear with the number of bits (N), however it should have a lower slope than RCA because of division by M stages.

(10)

(11)

Where tsetup is the setup block delay of each stage, and tbypass is the Multiplexing delay.

## Square Root Carry Select Adder

RSAsq is another approach to beat the adders linear dependency on N. It’s architecture is simply constructed from the optimized RCA discussed earlier in addition to an extra multiplexing stage. The working principle behind a 16-RSAsq is, similar to CBA, to divide the N bits into M blocks, where each addition unit in each block computes the Si and Coi of both Ci = 0 and Ci = 1 in parallel. Then, the two Si and two Coi output of each addition unit is multiplexed based on the signal Cin. Accordingly, Cin=0, Si/1 and Coi/1 is flushed, Cin=1, Si/0 and Coi/0 are propagated, and vice versa. In a sense, the adder will still linearly dependent on N, just like CBA. However, RSAsq overcomes this linear dependency by accounting for the multiplexing delay when constructing the arithmetic blocks by progressively increasing the number of bits/group. In other words, assuming the first block has an M=4, the critical delay will be tdelay=RCA4+tmux. Thus, the next block will have an M=5, so by the time the carry is multiplexed, an extra bit will be computed. Similarly, the third block will have an M=6 and so on.

(12)

(13)

According to Eq. (12) & Eq. (13), RSAsq has a square dependency on N.

## Radix-2 Kogge-Stone Adder

KSA is a parallel prefix form carry look ahead where carries are computed fast by computing them in parallel at the cost of increased area. KSA is composed of three stages: setup, look ahead network, and post-processing. The setup stage is the same as in CBA. The look-ahead network stage involves computation of carries corresponding to each bit. A hierarchy carry chain is built by dividing the addend into two parts, a higher part (H) and a lower part (L). The G|P function is expressed in Eq. (15) & Eq. (16).

(14)

(15)

(16)

(17)

Given the value of the carry-in of the least significant bits, we also generate the carries for every adder by considering the G and P of all the least significant bits as in Eq. (16). Finally, in the post-processing phase, the sum vector and Co is computed at one shot according to Eq. (17) & Eq. (3) respectively. Appropriate two stage buffers were placed intra-stages to handle the stages high-fanout. There are only 4 stages in carry generation tree, the worst-case propagation is typically four times than a 1-bit adder. Thus, td ~ log2(N).

# Functional Simulations

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Description automatically generated with medium confidenceFunctional simulations were performed on the adders using the test vectors provided. The vectors assert different P|G combinations. All the simulation settings adhered to the provided project specifications. As shown in Fig. (4), All the adders are functioning as expected. The Input/Output vectors had to be grouped in vector buses, with appropriate labels, to meet the report space constraints. A summary of the worst-case delay, average power, power-delay-product (PDP), and energy-delay-product of all adders across the three test vectors can be found in Table (1) & Table (2). None of the vectors causes a falling Co edge. Thus, results were collected in the form of only the worst-case TpLHco, TpHLs(15), and TpLHs(15). Where worst-case delay is based on TpLHco only since it will be the one scaling with N. According to Table (2), RCA exhibits the highest worst-case delay, followed by CBA. Surprisingly, KSA had higher delay than CSAsq, although tKSA tCSA ~ td, which can be explained by the effect of high branching overhead of KSA. Since we are optimizing for performance, EDP was proven to be the best metric for choosing an adder since it puts more emphasis on the delay part of the equation. Thus, CSAsq was chosen as the best architecture for our application.

# global mismatch and power-supply sweep

CSAsq performance was assessed under two extreme process corners (ff & ss) and extreme temperature (-25°C and 85°C). The results were compared to the typical condition (tt) under typical temperature (27°C). Table (3) provides a comprehensive summary for the critical delay, average power, PDP, and EDP for all three vector bitstreams. As expected CSAsq had 21.9% delay, 5.1% power, 17.7% PDP, 35.8% EDP performance improvement at ff/-25°C, and 31.2% delay, 2.8% power, 27.5% PDP, and 67.4% EDP overhead at ss/85°C. At high temperatures, carrier mobility decreases and effective resistance increases, thus delay decreases and power dissipation increases. CSAsq design has shown its corner process and temperature tolerance, as it abides by the timing constraints thoroughly.

Similarly, a power-supply (VDD) sweep under tt (27°C) with vector A was performed to verify the adder’s tolerance to VDD variations. As shown in Fig. (5), Power dissipation is increasing quadratically with VDD, while delay is decreasing exponentially when the transistors are ON (VDD > 0.7v). This variation is translated to an exponential decay in both PDP and EDP. To ensure that the adder meets the timing constraints of 400ps, VDD has to be a minimum of 0.7v which results in a TpLHCo 400ps, Power 36.2 , PDP 14.5fJ, and EDP 5.79 yJs of vector A in isolation.

# Conclusion

We have designed, optimized and analyzed four different adders. The CSAsq emerged as the optimal choice among the four architectures with an offset of 1.8% EDP to its nearest competitor, CBA. It exhibited a 48.4% improvement in EDP compared to the RCA. Under extreme conditions (ff/-25°C and ss/85°C), CSAsq was abiding by the design timing constraints with 31% delay overhead in the worst-case scenario, highlighting its robust performance. Power-supply sweep analysis confirmed CSAsq tolerance to VDD variations, with a minimum VDD of 0.7v to meet timing constraints.

##### References

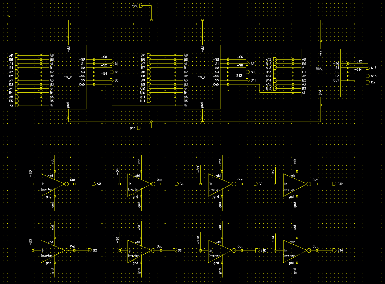
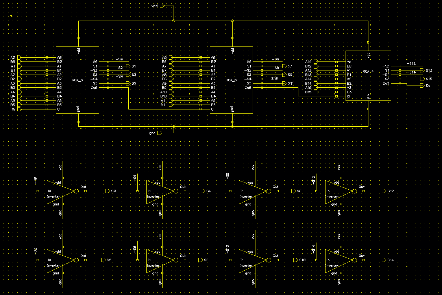
[1] J. M. Rabaey, A. Chandrakasan, and B. Nikoli´c, Digital Integrated Circuits: A Design Perspective, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2003

1. A screenshot of a table

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   Description automatically generated Delay, Power, PDP & EDP of the adders at tt 27°C
3. A table with numbers and letters

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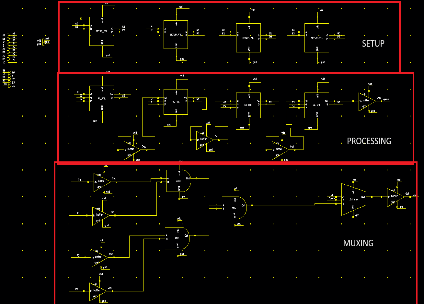
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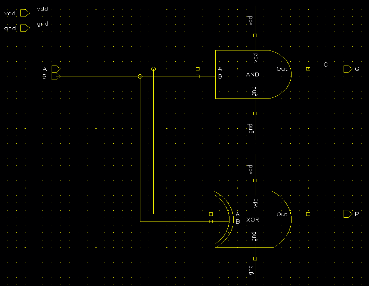
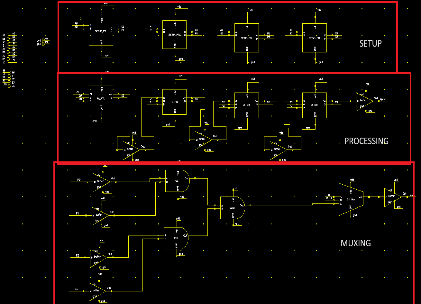
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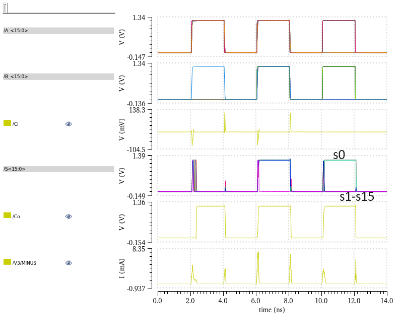
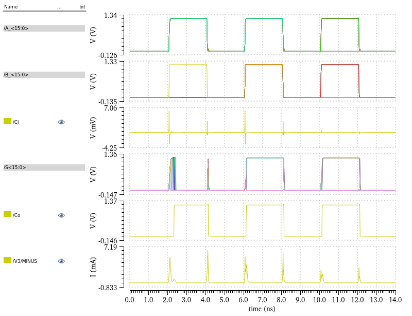
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