UART_RX

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TEST CASES:

First, testing with no Errors :

Prescale = 8

- TEST 1 : is testing normal frame with no errors
- TEST 2 : is testing consequent frames with no errors

Prescale = 16

- TEST 3 : is testing normal frame with no errors
- TEST 4 : is testing consequent frames with no errors

Prescale = 32

- TEST 5: is testing normal frame with no errors
- TEST 6 : is testing consequent frames with no errors

Second, testing Errors :

Prescale = 8

- TEST 7: testing start glitch Error
- TEST 8: (8.1) testing odd parity error

  (8.2) testing even parity error
- TEST 9 : testing stop error

Prescale = 16

- TEST 10: testing start glitch Error
- TEST 11: (11.1) testing odd parity error

  (11.2) testing even parity error
- TEST 12 : testing stop error

Prescale = 32

- TEST 10: testing start glitch Error
- TEST 11: (11.1) testing odd parity error

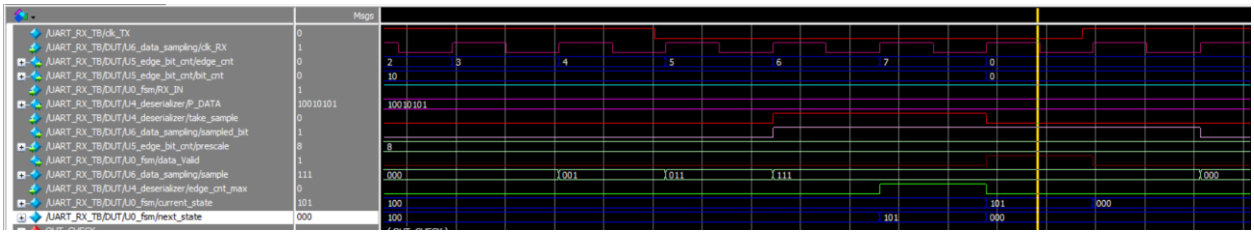
  (11.2) testing even parity error
- TEST 12 : testing stop error

Transipt output:

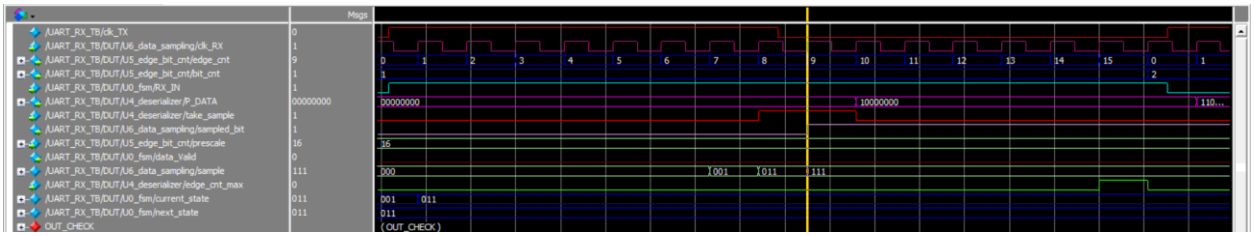
```
#
# ================================  TEST 1 ================================
#  Serial RX_IN = 10100101010
#   TEST1: Prescale = 8, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  1 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 0
# ================================ TEST 2 ================================
#  Serial RX_IN = 11100110010
#   TEST2: Prescale = 8, PAR_EN = 1, PAR_TYP = 0,
#
# ********************** test  2 PASSED, with CORRECT error report ,output data = 10011001 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 0
#  Serial RX_IN = 10100110010
#   TEST2: Prescale = 8, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  2 PASSED, with CORRECT error report ,output data = 10011001 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 0
# consequent frames: TEST 2 Finished
# ================================ TEST 3 ================================
#  Serial RX_IN = 10100101010
#   TEST3: Prescale = 16, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  3 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR GLITCH = 0 , PAR ERR = 0 , STP ERR = 0

# ================================  TEST 4 ================================
#  Serial RX_IN = 11100110010
#   TEST4: Prescale = 16, PAR_EN = 1, PAR_TYP = 0,
#
# ********************** test  4 PASSED, with CORRECT error report ,output data = 10011001 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 0
#  Serial RX_IN = 10100110010
#   TEST4: Prescale = 8, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  4 PASSED, with CORRECT error report ,output data = 10011001 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 0
# consequent frames: TEST 4 Finished
# ================================  TEST 5 ================================
#  Serial RX_IN = 10100101010
#   TEST5: Prescale = 32, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  5 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 0
# ================================ TEST 6 ================================
#  Serial RX_IN = 11100110010
#   TEST6: Prescale = 32, PAR_EN = 1, PAR_TYP = 0,
#
# ********************** test  6 PASSED, with CORRECT error report ,output data = 10011001 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 0
#  Serial RX_IN = 10100110010
#   TEST6: Prescale = 32, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  6 PASSED, with CORRECT error report ,output data = 10011001 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 0
# consequent frames: TEST 6 Finished
```

```
#
#  ====================================================================
# ================================ Prescale =8 ============================
#  TESTING with ERRORS
# ================================ TEST 7 ================================
# start_glitch error test
# Test 7 PASSED: str_glitch =1
# ================================   TEST 8 ================================
# TEST 8.1
#  odd par_err test
#  Serial RX_IN = 11100101010
#   TEST8: Prescale = 8, PAR_EN = 1, PAR_TYP = 1,
#
# ********************* test  8 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 1 , STP_ERR = 0
# TEST 8.2
#  even par_err test
#  Serial RX_IN = 10100101010
#   TEST8: Prescale = 8, PAR_EN = 1, PAR_TYP = 0,
#
# ********************* test  8 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 1 , STP_ERR = 0
# ================================ TEST 9 ================================
# stp_err test
#  Serial RX_IN = 100101010
#   TEST9: Prescale = 8, PAR_EN = 1, PAR_TYP = 1,
#
# ********************* test  9 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 1
#
#  ____________________________________________________________________
```

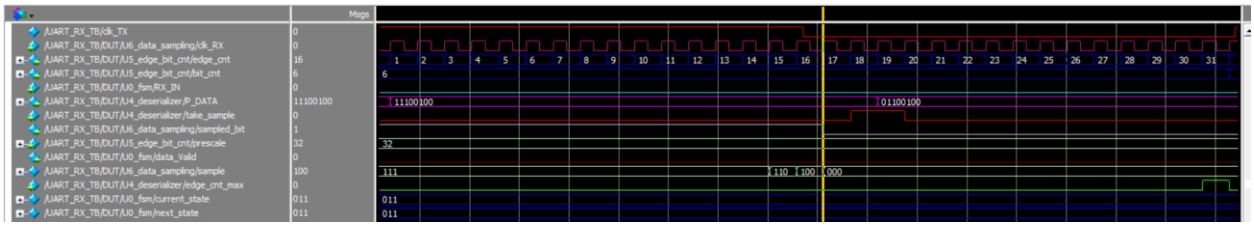
```
#
#  ====================================================================
#  TESTING with ERRORS
# ================================ Prescale =16 ============================
# ================================== TEST 10 ================================
# start_glitch error test
# Test 10 PASSED: str_glitch =1
# ==================================   TEST 11 ================================
# TEST 11.1
#  odd par_err test
#  Serial RX_IN = 11100101010
#   TEST11: Prescale = 16, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  11 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 1 , STP_ERR = 0
# TEST 11.2
#  even  par_err test
#  Serial RX_IN = 10100101010
#   TEST11: Prescale = 16, PAR_EN = 1, PAR_TYP = 0,
#
# ********************** test  11 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 1 , STP_ERR = 0
# ================================== TEST 12 ================================
# stp_err test
#  Serial RX_IN = 100101010
#   TEST12: Prescale = 16, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  12 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 1
#
#  ====================================================================
#  TESTING with ERRORS
# ============================== Prescale =32 ==============================
# ================================ TEST 13 ================================
# start_glitch error test
# Test 13 PASSED: str_glitch =1
# ==================================   TEST 14 ================================
# TEST 14.1
#  odd par_err test
#  Serial RX_IN = 11100101010
#   TEST14: Prescale = 32, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  14 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 1 , STP_ERR = 0
# TEST 14.2
#  even  par_err test
#  Serial RX_IN = 10100101010
#   TEST14: Prescale = 32, PAR_EN = 1, PAR_TYP = 0,
#
# ********************** test  14 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 1 , STP_ERR = 0
# ================================ TEST 15 ================================
# stp_err test
#  Serial RX_IN = 100101010
#   TEST15: Prescale = 32, PAR_EN = 1, PAR_TYP = 1,
#
# ********************** test  15 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 1
# Testing a frame without sending a parity bit --> PAR_EN =0
# ==================================  TEST 16 ================================
#  Serial RX_IN = 1100101010
#   TEST16: Prescale = 8, PAR_EN = 0, PAR_TYP = 0,
#
# ********************** test  16 PASSED, with CORRECT error report ,output data = 10010101 **********************
#
#   STR_GLITCH = 0 , PAR_ERR = 0 , STP_ERR = 0
# ** Note: $stop    : C:/Digital IC Design_Eltimsah/systems/UART_RX/project_final_TB/UART_RX_TB.v(343)
#    Time: 2330580 ns  Iteration: 1  Instance: /UART_RX_TB
# Break in Module UART_RX_TB at C:/Digital IC Design_Eltimsah/systems/UART_RX/project_final_TB/UART_RX_TB.v line 343
```



- Wave form of last bit in TEST 1
- You can see that samples are taken at edge = 4,5,6 and sampled bit is determined at 6
- Data valid is high for a clock cycle after stop bit



- At prescale = 16



- At prescale = 32