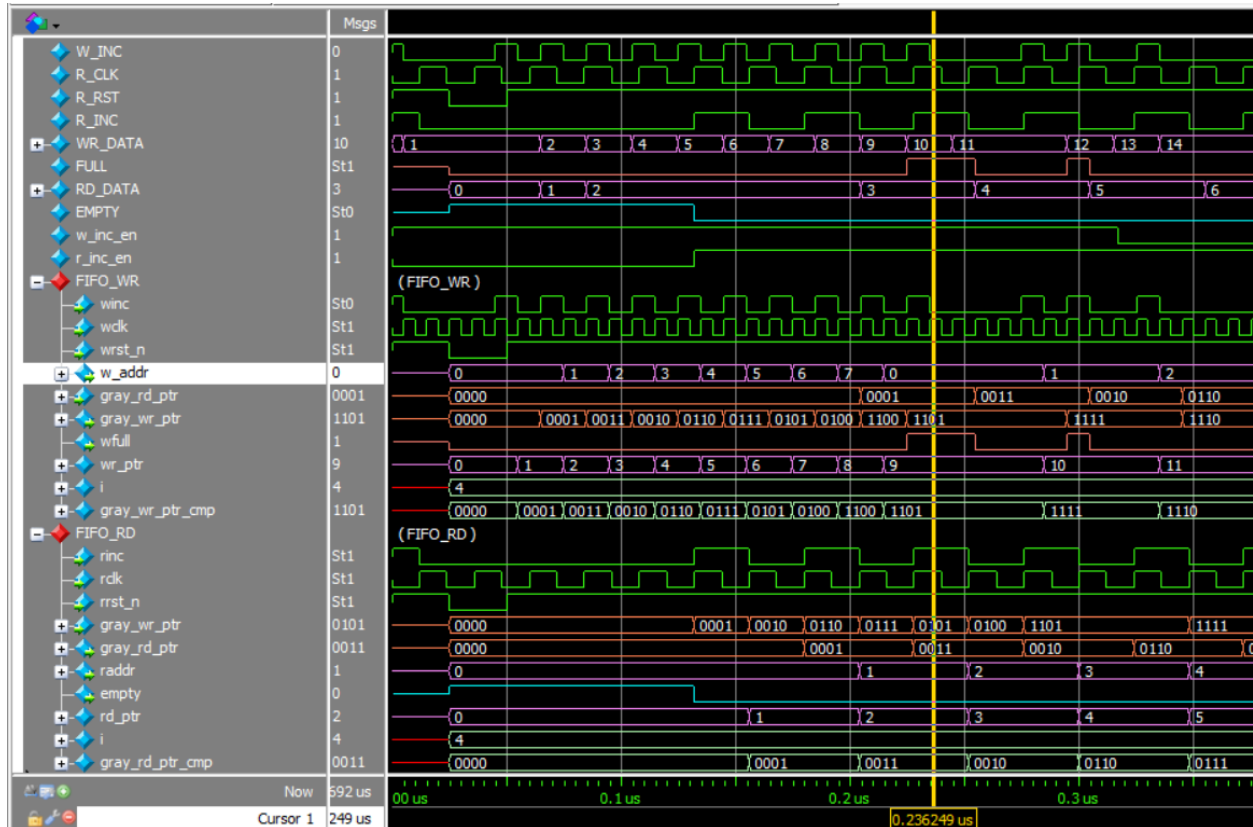


FIFO

Test case 1: testing FIFO full case



IN FIFO_WR BLOCK:

WR_PTR = 9 → gray_wr_ptr = 1101

RD_PTR = 1 → gray_rd_ptr = 0001

- At this point, FIFO FULL flag is up to prevent overwriting data.
- Also reading operation didn't stop and when FULL flag is down writing operation started again

The timing diagram displays various digital signals over time. A yellow vertical line is positioned at 0.672342 us. The signals shown include:

- W_INK**: Signal 0, value 0.
- R_CLK**: Signal 1, value 1.
- R_RST**: Signal 1, value 1.
- R_INK**: Signal 1, value 1.
- WR_DATA**: Signal 14, values 13, 15, 16, 17, 18, 19, 20, 21, 22, 23.
- RD_DATA**: Signal 4, values 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14.
- FIFO_WR**: Signal 0, value 0.
- FIFO_RD**: Signal 0, value 0.
- gray_wr_ptr**: Signal 11, values 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23.
- gray_rd_ptr**: Signal 11, values 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23.
- gray_wr_ptr_cmp**: Signal 4, value 4.
- gray_rd_ptr_cmp**: Signal 4, value 4.

The time scale at the bottom shows markers from 0.3 us to 0.9 us, with a specific point marked at 0.672342 us.

- IN FIFO_RD BLOCK:**

RD_PTR = 11 \rightarrow gray_rd_ptr = 1110

- At this point, FIFO empty flag is up to prevent reading wrong data.
- Also we can see writing operation begin again after I raised `wr_inc_en` And then empty flag down again.