Omar Abdelrazek Sobh Mohammed

Personal Information

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Date of birth: 7/12/2001

Education

Senior student, Faculty of Engineering Cairo University

- **Department:** Electronics and communication Engineering.
- **Cumulative Grade:** Excellent (85.02%)
- **Graduation Year :** 2024
- **Graduation Project - Sponsored by Si-Vision**
  - **implementing CXL 2.0 Link layer, Transaction layers and Register file**
    - **Main Features :**
      1- Configurable operation modes: Device, Host and Dual Mode.
      2- Configurable Transaction/Application Layer clock frequency.
      3- Data path integrity (ECC code)**.**
    - CXL controller interface with the application layer through 2 different options:
      1- ARM AMBA CXS Interface.
      2- CXL native interface.
    - CXL controller link layer interface with the Physical layer according to LPIF specifications.
    - Register file interface with the application layer through AMBA APB Protocol and CDC handling between Register file and CXL main controller

Courses & Workshops

Current – May2024

- **AUC Training for employment in Electronics Sector**
  - **Content: -**
    1. **Fundamental Module**
       - Introduction to Digital Design.
       - Introduction to silicon process & VLSI.
       - Introduction to Analog Design
    2. **Advanced Module-Digital IC Design**
       - Advanced Digital Design.
       - Advanced Full Custom VLSI Design.
       - Digital Testing and Verification.

Jul2023 - Sep2023

- **Digital IC Design Diploma (**Under supervision of **Eng. Ali El-Temsah)**

Internships

Jul 2023 – Oct 2023

- **ST "computer architecture" training course at STMicroelectronics**
  - **Content :** Topics from TextBook "Digital Design ,2nd Edition David Harris and Sarah L.Harris"
    - Architecture "Chapter6"
    - Microarchitecture "Chapter7"
    - Memory and I/O Systems "Chapter8**"**

Related Projects

Jul 2023 – Sep 2023

- **"RTL to GDS Implementation of Low Power Configurable Multi Clock Digital System"**
  - **Description:** It is responsible of receiving commands through UART receiver to do different system functions as register file reading/writing or doing some processing using ALU block and send result as well as CRC bits of result using 4 bytes frame through UART transmitter communication protocol.

Aug 2023

- **Multi Cycles MIPS**
  - **Description:** Synthesizable RTL of Full 32-bits multicycles MIPS performing instructions in different cycles based on the type of instruction :
    R-Type , J-Type , load , store
  - **Project phases: -**
    1. RTL Design from Scratch of system blocks (Control-Unit, ALU, Register File, Memory, PC)
    2. Implementing external multiply division block based on basic algorithms which need 32 cycles
    3. Synthesize on **Cyclon IV** FPGA using Quartus prime tool

Feb 2023

- **32-bit Single Cycle Micro architecture RISC-V processor based on Harvard Architecture**

Dec 2023

- **VLSI flow for random number generator**
  - **Description :** VLSI flow including the schematic entry, symbol creation, building the test design, creating the layout view, checking DRC, LVS verification, parasitic extraction, and post-layout simulation.
- **"DSP48E1 slice within Xilinx 7 series FPGAs for digital signal processing (DSP) tasks " RTL implementation**

Other Projects

- Design and implement UART protocol in Verilog testing it with FPGA .
- Design Ring oscillator based on inverters from transistor level using cadence virtuoso
- Implementing a meeting planner in C++.

Extracurricular Activities:

Sep 2020 – MAR2021

- Robotics academic member in Kvector student activity at Cairo University.

JAN 2023

- IEEE participant digital workshop.

Technical Skills

• **Programming Languages**	C	C++	Assembly
• **Scripting Languages**	MATLAB	Python	TCl
• **Hardware Description Languages**	Verilog	System Verilog	
• **Tools**	Multisim Arduino IDE	Cadence	ModelSim Tanner Quartus Synopsys Asic tools

Soft Skills

Team Work	Presentation Skills	Communication Skills

Languages Skills

- Arabic — Native Language
- English — Very Good