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ESCUELA SUPERIOR DE INGENIERÍA MECÁNICA Y ELÉCTRICA

UNIDAD PROFESIONAL ADOLFO LÓPEZ MATEOS

DEPARTAMENTO DE INGENIERÍA EN COMUNICACIONES Y
ELECTRÓNICA

"PROYECTO VENUS: AUTOMATIZACIÓN DEL HOGAR (DOMÓTICA)"

PROYECTO FINAL

UNIDAD DE APRENDIZAJE

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OBJETIVOS

- Proponer un proyecto de emprendimiento con tecnologías de bajo costo para su producción en cadena.
- Analizar y comprender el funcionamiento de nuevas tecnologías emergentes en el sector de la automatización remota.
- Comparar los aspectos positivos y negativos entre la tecnología llamada MQTT y los conceptos vistos en clase con referencia a *html* y *sockets*
- Diseñar y elaborar un proyecto en el cual se integren conceptos vistos en clase con ayuda de servidores

INTRODUCCIÓN

La automatización consiste en usar la tecnología para realizar tareas con muy poca intervención humana. Se puede implementar en cualquier sector en el que se lleven a cabo tareas repetitivas. Sin embargo, es más común en aquellos relacionados con la fabricación, la robótica y los automóviles, así como en el mundo de la tecnología: en el software para la toma de decisiones empresariales y los sistemas de TI.

La robótica posee una rama de aprendizaje, que en los últimos años ha tomado fuerza ya que es aplicada a la vida cotidiana y reforma las casas con una nueva estructura; la domótica.

La domótica es la aplicación de la tecnología a la automatización del hogar y de edificios. Se utiliza para controlar y gestionar diferentes sistemas y dispositivos en el hogar o edificio de forma automatizada. Estos sistemas pueden incluir iluminación, calefacción, aire acondicionado, sistemas de seguridad y cámaras de vigilancia, sistemas de entretenimiento y otros dispositivos domésticos. Es una tecnología que permite automatizar y controlar de forma remota diferentes sistemas y dispositivos en el hogar o edificio, utilizando una red de dispositivos conectados y un sistema central de control.

A través de la programación, hacemos que las máquinas imiten un comportamiento complejo siguiendo secuencias de instrucciones simples. Utilizar lenguajes de programación textual como Asamby, C, Python y JavaScript, es una de las formas principales de hacerlo. Los diseñadores de estos lenguajes de programación han pasado horas y horas tratando de hacer que la experiencia de los programas de escritura sean lo más fácil posible a través de una sintaxis expresiva, fuertes construcciones de programación y cadenas de herramientas poderosas. Sin embargo, todos estos lenguajes de programación comparten un rasgo común: el código fuente textual.

Escribir programas en texto funciona y en la mayoría de los casos funciona bien. Sin embargo, la capacidad de expresar programas visualmente es a menudo deseable. Ser capaz de diseñar el flujo de información a través de diversos componentes de un sistema más grande es normalmente todo lo que se necesita. Las herramientas visuales de programación también son indulgentes con cualquier persona que sea nuevo en la programación y que les es difícil manejar diversos conceptos como las variables, indicadores, señales, alcances, y así sucesivamente.

Node-RED es una herramienta de programación visual. Muestra visualmente las relaciones y funciones, y permite al usuario programar sin tener que escribir una lengua. Node-RED es un editor de flujo basado en el navegador donde se puede añadir o eliminar nodos y conectarlos entre sí con el fin de hacer que se comuniquen entre ellos.

En Node-RED, cada nodo es uno de los siguientes dos tipos: un nodo de inyección o un nodo de función. Los nodos de inyección producen un mensaje sin necesidad de entrada y lanzan el mensaje al siguiente nodo conectado a éste. Los nodos de función, por el contrario, tienen una entrada y realizan algún trabajo en él. Con una gran cantidad de estos nodos para elegir, Node-RED hace que el conectar los dispositivos de hardware, APIs y servicios en línea sea más fácil que nunca.

DESARROLLO

Marco Teórico

¿Qué es MQTT?

MQTT es un protocolo de mensajería basado en estándares, o un conjunto de reglas, que se utiliza para la comunicación de un equipo a otro. Los sensores inteligentes, los dispositivos portátiles y otros dispositivos de Internet de las cosas (IoT) generalmente tienen que transmitir y recibir datos a través de una red con recursos restringidos y un ancho de banda limitado. Estos dispositivos IoT utilizan MQTT para la transmisión de datos, ya que resulta fácil de implementar y puede comunicar datos IoT de manera eficiente. MQTT admite la mensajería entre dispositivos a la nube y la nube al dispositivo. El protocolo MQTT se inventó en 1999 para su uso en la industria del petróleo y el gas. Los ingenieros necesitaban un protocolo para un ancho de banda mínimo y una pérdida de batería mínima para supervisar los oleoductos vía satélite. Inicialmente, el protocolo se conocía como transporte de telemetría de Message Queue Server debido al producto de IBM MQ Series que admitió por primera vez su fase inicial. En 2010, IBM lanzó MQTT 3.1 como un protocolo gratuito y abierto para que cualquiera pudiera implementarlo, que después, en 2013, se envió al organismo de especificación de la Organización para el Avance de Estándares de Información Estructurada (OASIS) para su mantenimiento. En 2019, OASIS lanzó una versión 5 de MQTT actualizada. Ahora MQTT ya no es un acrónimo sino que se considera el nombre oficial del protocolo.

¿Por qué es importante el protocolo MQTT?

El protocolo MQTT se ha convertido en un estándar para la transmisión de datos de IoT, ya que ofrece los siguientes beneficios:

Ligero y eficiente. La implementación de MQTT en el dispositivo IoT requiere recursos mínimos, por lo que se puede usar incluso en pequeños microcontroladores. Por ejemplo, un mensaje de control MQTT mínimo puede tener tan solo dos bytes de datos. Los encabezados de los mensajes MQTT también son pequeños para poder optimizar el ancho de banda de la red.

Escalable. La implementación de MQTT requiere una cantidad mínima de código que consume muy poca energía en las operaciones. El protocolo también tiene funciones integradas para admitir la comunicación con una gran cantidad de dispositivos IoT. Por tanto, puede implementar el protocolo MQTT para conectarse con millones de estos dispositivos.

Fiable. Muchos dispositivos IoT se conectan a través de redes celulares poco fiables con bajo ancho de banda y alta latencia. MQTT tiene funciones integradas que reducen el tiempo que tarda el dispositivo IoT en volver a conectarse con la nube. También define tres niveles diferentes de calidad de servicio a fin de garantizar la fiabilidad para los casos de uso de IoT: como máximo una vez (0), al menos una vez (1) y exactamente una vez (2).

Seguro. MQTT facilita a los desarrolladores el cifrado de mensajes y la autenticación de dispositivos y usuarios mediante protocolos de autenticación modernos, como OAuth, TLS1.3, certificados administrados por el cliente, etc.

Admitido. Varios lenguajes, como Python, tienen un amplio soporte para la implementación del protocolo MQTT. Por lo tanto, los desarrolladores pueden implementarlo rápidamente con una codificación mínima en cualquier tipo de aplicación.

¿Cuál es el principio en el que se basa MQTT?

El protocolo MQTT funciona según los principios del modelo de publicación o suscripción. En la comunicación de red tradicional, los clientes y servidores se comunican directamente entre sí. Los clientes solicitan recursos o datos del servidor, a continuación el servidor procesa y envía una respuesta. Sin embargo, MQTT utiliza un patrón de publicación o suscripción para desacoplar el remitente del mensaje (editor) del receptor del mensaje (suscriptor). En lugar de ello, un tercer componente, denominado agente de mensajes, controla la comunicación entre editores y suscriptores. El trabajo del agente consiste en filtrar todos los mensajes entrantes de los editores y distribuirlos correctamente a los suscriptores. El agente desacopla los editores y suscriptores de la siguiente manera:

Desacoplamiento espacial. El editor y el suscriptor no conocen la ubicación de la red del otro y no intercambian información como direcciones IP o números de puerto.

Desacoplamiento de tiempo. El editor y el suscriptor no se ejecutan ni tienen conectividad de red al mismo tiempo.

Desacoplamiento de sincronización. Tanto los editores como los suscriptores pueden enviar o recibir mensajes sin interrumpirse entre sí. Por ejemplo, el suscriptor no tiene que esperar a que el editor envíe un mensaje.

¿Qué son los componentes MQTT?

MQTT implementa el modelo de publicación o suscripción mediante la definición de clientes y agentes, tal y como se muestra a continuación.

Cliente MQTT. Un cliente MQTT es cualquier dispositivo, desde un servidor hasta un microcontrolador, que ejecuta una biblioteca MQTT. Si el cliente envía mensajes, actúa como editor, y si recibe mensajes, actúa como receptor. Básicamente, cualquier dispositivo que se comunique mediante MQTT a través de una red puede denominarse dispositivo cliente MQTT.

Agente MQTT. El agente MQTT es el sistema de back-end que coordina los mensajes entre los diferentes clientes. Las responsabilidades del agente incluyen recibir y filtrar mensajes, identificar a los clientes suscritos a cada mensaje y enviarles los mensajes. También se encarga de otras tareas como:

- La autorización y autenticación de clientes MQTT
- Pasar mensajes a otros sistemas para su posterior análisis
- El control de mensajes perdidos y sesiones de clientes

Conexión MQTT. Los clientes y los agentes comienzan a comunicarse mediante una conexión MQTT. Los clientes inician la conexión al enviar un mensaje CONECTAR al agente MQTT. El agente confirma que se ha establecido una conexión al responder con un mensaje

CONNACK. Tanto el cliente MQTT como el agente requieren una pila TCP o IP para comunicarse. Los clientes nunca se conectan entre sí, solo con el agente.

¿Cómo funciona MQTT?

A continuación se proporciona una descripción general del funcionamiento de MQTT.

1. Un cliente MQTT establecer una conexión con el agente MQTT.
2. Una vez conectado, el cliente puede publicar mensajes, suscribirse a mensajes específicos o hacer ambas cosas.
3. Cuando el agente MQTT recibe un mensaje, lo reenvía a los suscriptores que están interesados.

Analicemos los detalles para una mayor comprensión.

Tema de MQTT. El término “tema” se refiere a las palabras clave que utiliza el agente MQTT a fin de filtrar mensajes para los clientes de MQTT. Los temas están organizados jerárquicamente, de forma similar a un directorio de archivos o carpetas. Por ejemplo, considere un sistema doméstico inteligente que opera en una casa de varios pisos que tiene diferentes dispositivos inteligentes en cada uno de ellos. En ese caso, es posible que el agente MQTT organice temas como:

ourhome/groundfloor/livingroom/light

ourhome/firstfloor/kitchen/temperature

Publicación MQTT. Los clientes MQTT publican mensajes que contienen el tema y los datos en formato de bytes. El cliente determina el formato de los datos, como datos de texto, datos binarios, archivos XML o JSON. Por ejemplo, es posible que una lámpara del sistema doméstico inteligente publique un mensaje sobre el tema salón o luz.

Suscripción MQTT. Los clientes MQTT envían un mensaje SUBSCRIBE (SUBSCRIBIRSE) al agente MQTT para recibir mensajes sobre temas de interés. Este mensaje contiene un identificador único y una lista de suscripciones. Por ejemplo, la aplicación de hogar inteligente en su teléfono quiere mostrar cuántas luces están encendidas en casa. Se suscribirá a la luz del tema y aumentará el contador para todos los mensajes activados.

ESP32

Creado y desarrollado por *Espressif Systems*, ESP32, una serie de microcontroladores de bajo costo y de bajo consumo con sistema en chip con Wi-Fi y Bluetooth de modo dual integrados, es un avance para los ingenieros de automatización que no quieren verse envueltos en los matices de la radiofrecuencia (RF) y el diseño inalámbrico. Como una radio combinada Wi-Fi/Bluetooth de bajo costo, la serie ha ganado popularidad no solo entre los aficionados sino también entre los desarrolladores de IoT. Su bajo consumo de energía, sus múltiples entornos de desarrollo de código abierto y sus bibliotecas la hacen perfectamente adecuada para desarrolladores de todo tipo.

El módulo ESP32 es una solución de Wi-Fi/Bluetooth todo en uno, integrada y certificada que proporciona no solo la radio inalámbrica, sino también un procesador integrado con interfaces para conectarse con varios periféricos. El procesador en realidad tiene dos núcleos de procesamiento cuyas frecuencias operativas pueden controlarse independientemente entre 80 megahercios (MHz) y 240 MHz. Los periféricos del procesador facilitan la conexión a una variedad de interfaces externas como:

- Interfaz periférica serial (SPI)
- I2C
- Transmisor receptor asíncrono universal (UART)
- I2S
- Ethernet
- Tarjetas SD
- Interfaces táctiles y capacitivas

Hay varios módulos ESP32 diferentes que un desarrollador puede seleccionar según sus necesidades de aplicación. El primer módulo ESP32 y el más popular es el ESP32-WROOM-32D, que funciona hasta 240 MHz (Figura 1). El módulo incluye una antena de rastreo de placa de CI, que simplifica la implementación. También evita tener que agregar el hardware adicional y la complejidad de diseño asociada con una antena conectada IPEX. Sin embargo, si se selecciona la opción de conector IPEX, hay muchas buenas opciones de antenas, como la W24P-U de Inventek Systems.



Figura 1: El módulo ESP32-WROOM-32D funciona a velocidades de hasta 240 MHz y contiene 8 MB de flash

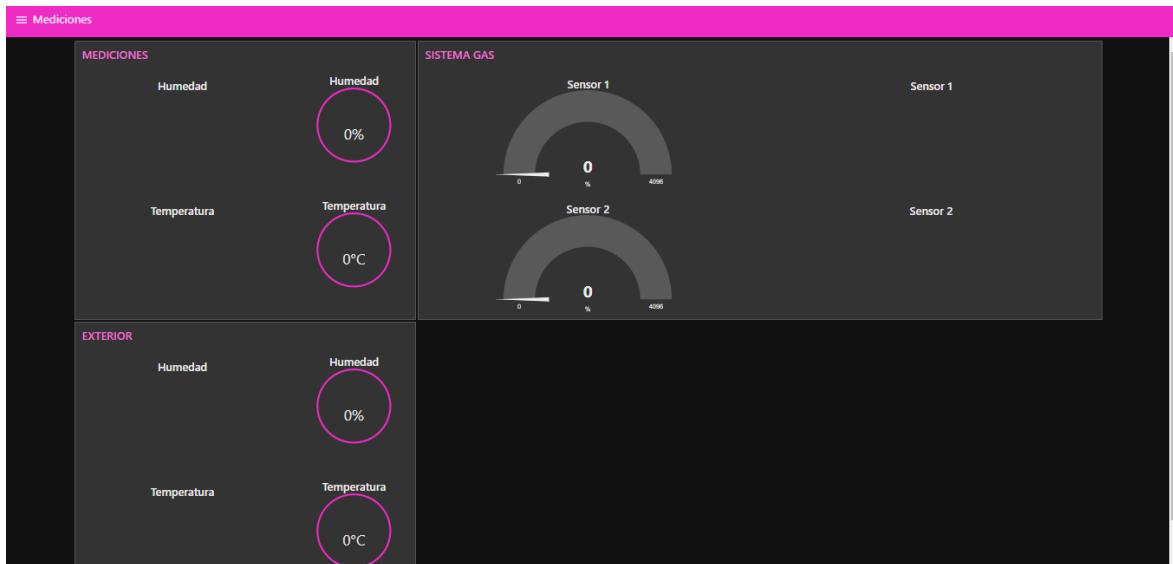
El módulo contiene 4 megabytes (MB) de flash y tiene 38 pines dispuestos para minimizar el tamaño del módulo, lo que lo hace casi cuadrado. De hecho, el WROOM-32D es completamente compatible con los pines del ESP-WROOM-32U (Figura 2). El WROOM-32U reemplaza la antena de rastreo integrada de la placa de CI con un conector IPEX, basado en el diseño U.FL de Hirose. Al hacerlo, el WROOM-32U ahorra espacio en la placa y permite a los desarrolladores conectar una antena externa que pueden colocar dentro de su producto para obtener características óptimas de RF.



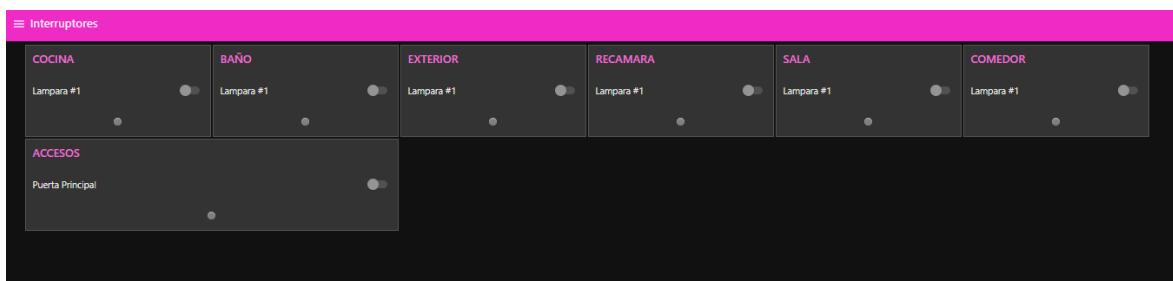
Figura 2: El ESP32-WROOM-32U es compatible con los pines del WROOM-32D, pero reemplaza la antena de rastreo integrada de este último con un conector IPEX para una antena externa, lo que permite obtener características de RF optimizadas. (Fuente de la imagen: Espressif Systems)

Interfaz de Usuario

Cuando el usuario abre el cliente desde cualquier dispositivo móvil se visualizará el siguiente panel, donde mostrará los valores de los sensores, DHT22 y MQ2, valores que corresponden a Humedad relativa del ambiente, temperatura del ambiente y concentración de gas.



El siguiente menú, muestra los controles para los interruptores de lámparas y el acceso para una chapa eléctrica.

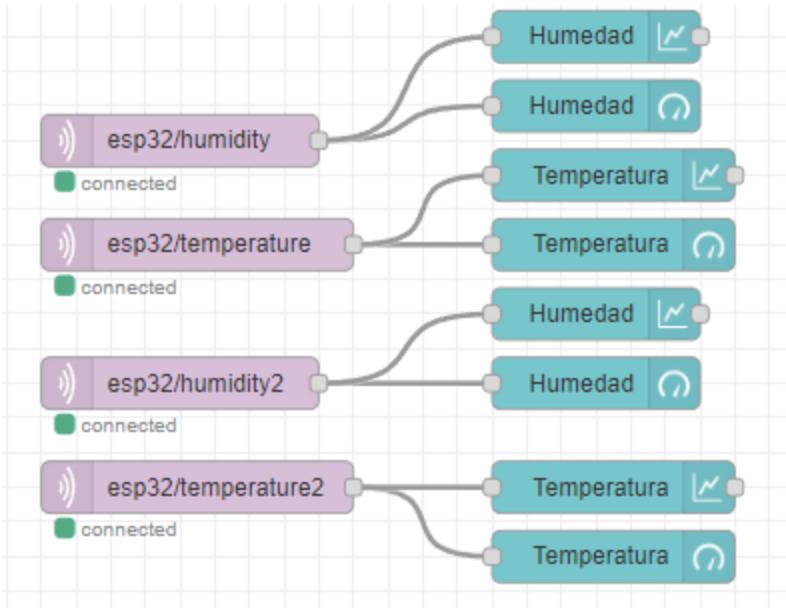


Este menú muestra la visualización en tiempo real del sistema de vigilancia, integrado por 3 módulos esp32 cam.

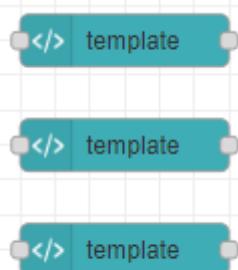
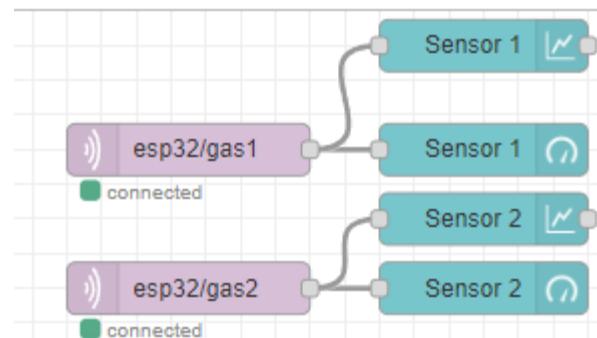


La navegación entre menús se hará con este submenú en donde el usuario podrá seleccionar el grupo de acciones que quiera monitorear, ya sean las mediciones de los sensores, la interacción entre interruptores y por último el sistema de vigilancia.

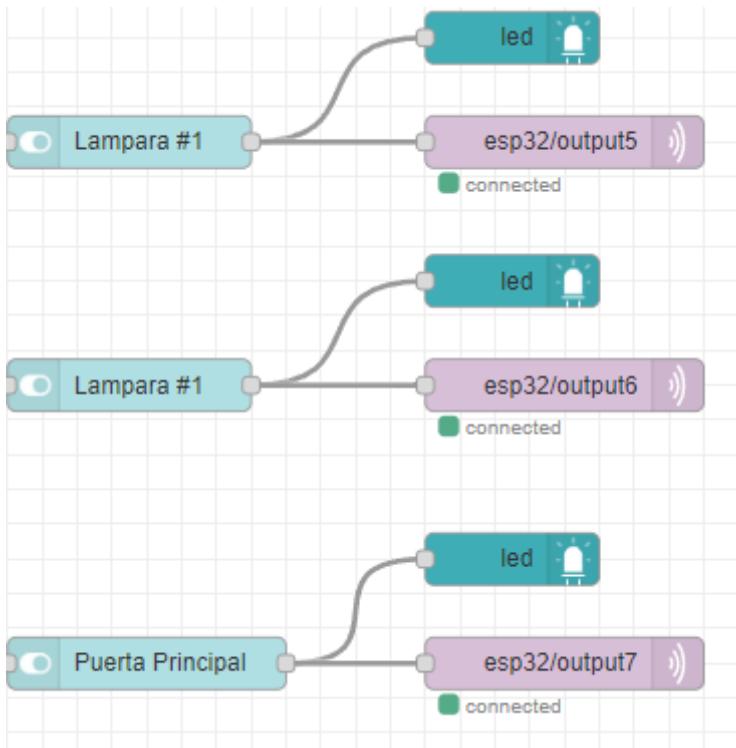
Programación del server



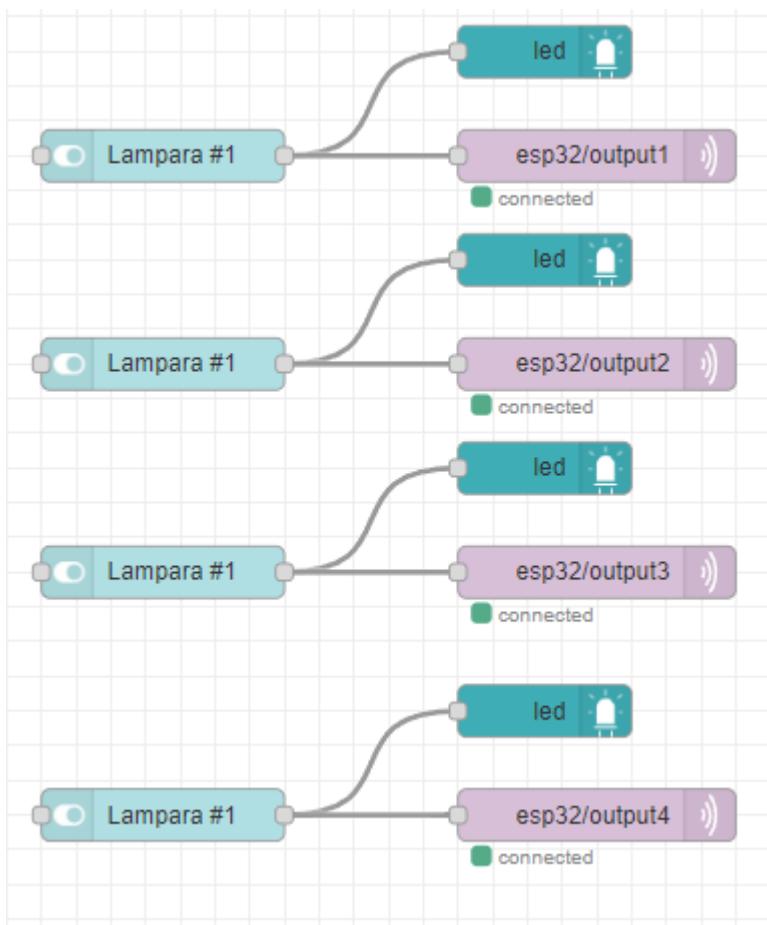
La programación es por bloques, en donde se colocarán las entradas del protocolo mqtt en donde por medio de un topic se designará una etiqueta de entrada, y dicha entrada se mandará a los medidores para su visualización, en este caso serán de los sensores.



En estos bloques se programará un frame en donde se mandarán a traer los servidores de las cámaras que son parte del sistema de vigilancia, ya que las cámaras no están integradas directamente al protocolo mqtt se harán por un servidor, el cuál se podrá acceder por medio de la dirección ip que el modem les asigne.



Estos bloques servirán para mandar datos o salidas del servidor mqtt, que recibirán los clientes, estos tendrán un topic específico. Los datos serán generados por un nodo llamado switch, quien estará mandando en cadena de texto los estados “on” y “off” para el encendido de los focos. Así mismo, el estado del nodo switch será recibido por un nodo interno llamado led, quién indicará en el cliente el estado de los focos.



Configuración de nodos de salida y de entrada

Edit mqtt out node

Delete Cancel Done

Properties

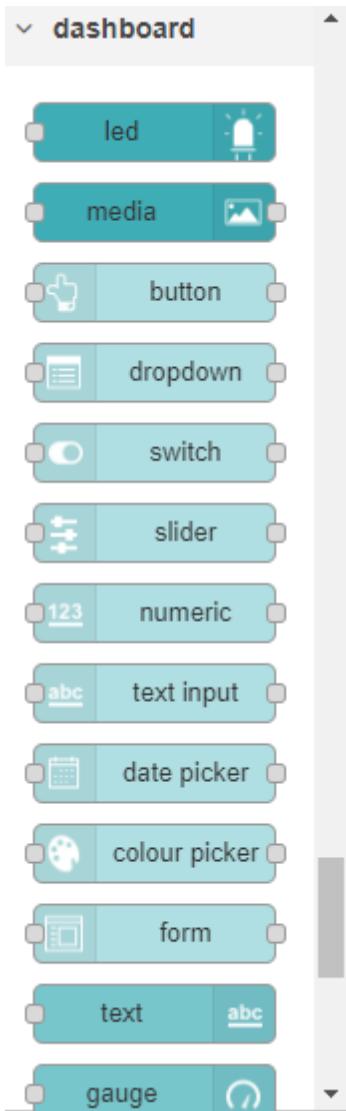
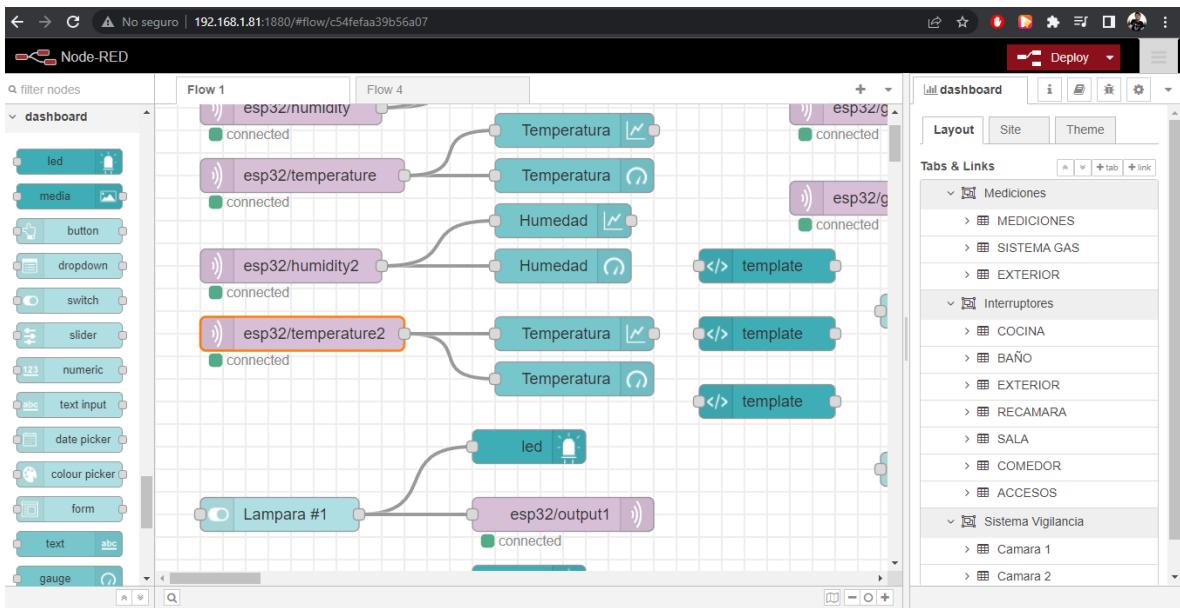
Server	localhost:1883	
Topic	esp32/output5	
QoS	1	Retain
Name	Name	

Edit mqtt in node

Delete Cancel Done

Properties

Server	localhost:1883	
Action	Subscribe to single topic	
Topic	esp32/temperature2	
QoS	0	
Output	auto-detect (parsed JSON object, string or buf	
Name	Name	



El diseño del dashboard debe considerarse como una cuadrícula. Cada elemento del grupo tiene un ancho: de forma predeterminada, 6 ‘unidades’ (una unidad tiene 48 píxeles de ancho de forma predeterminada con un espacio de 6 píxeles).

Cada widget del grupo también tiene un ancho: de forma predeterminada, ‘auto’, lo que significa que ocupará el ancho del grupo en el que se encuentra, pero puede establecerlo en un número fijo de unidades.

El algoritmo de diseño del tablero siempre trata de colocar elementos tan altos y a la izquierda como sea posible dentro de su contenedor; esto se aplica a cómo se posicionan los grupos en la página, así como a cómo se colocan los widgets en un grupo.

Dado un grupo con un ancho de 6, si agrega seis widgets, cada uno con un ancho de 2, se colocarán en dos filas, tres widgets en cada uno.

Si agrega dos grupos de ancho 6, siempre que la ventana de su navegador sea lo suficientemente ancha, se sentarán uno al lado del otro. Si encoge el navegador, en algún momento el segundo grupo cambiará para estar debajo del primero, en una columna.

Es posible utilizar múltiples grupos si es posible, en lugar de un gran grupo, para que la página pueda cambiar de tamaño dinámicamente en pantallas más pequeñas.

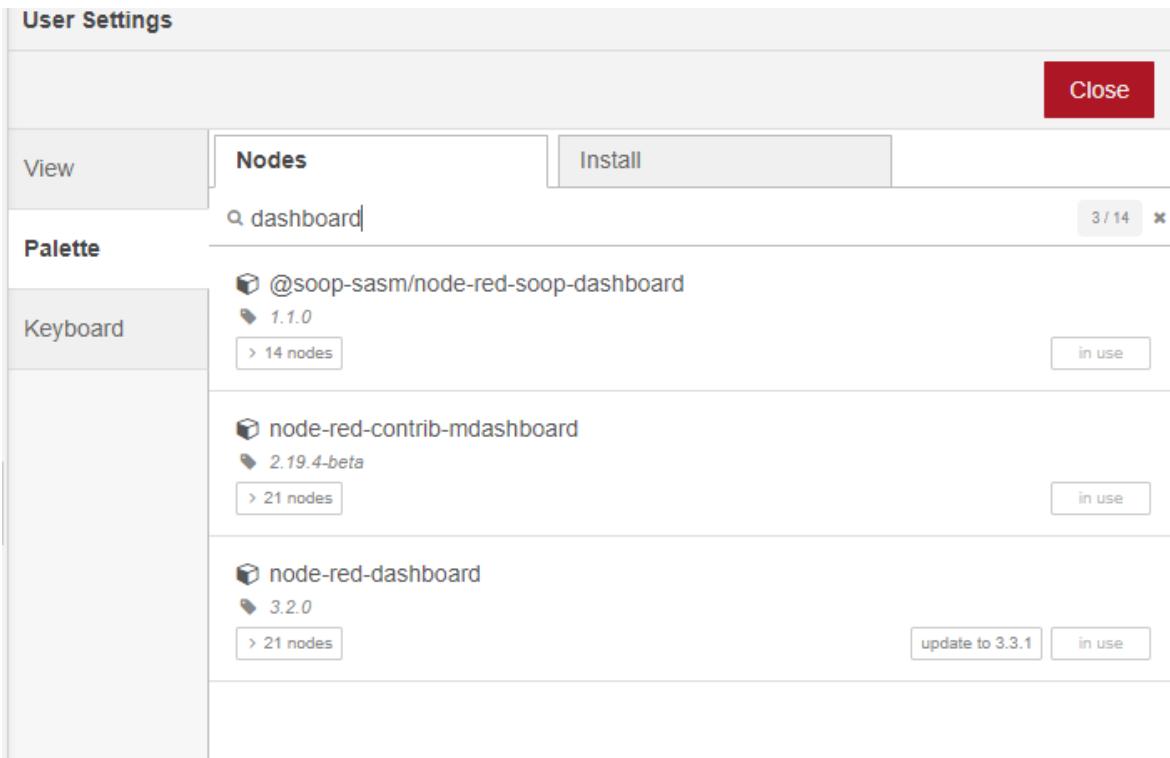


Diagrama MQTT

La raspberry será la encargada de gestionar el servidor por medio de un bróker, en donde las instrucciones serán mandadas por los clientes, en este caso la ESP32 y así mismo, estos podrán recibir instrucciones del servidor.

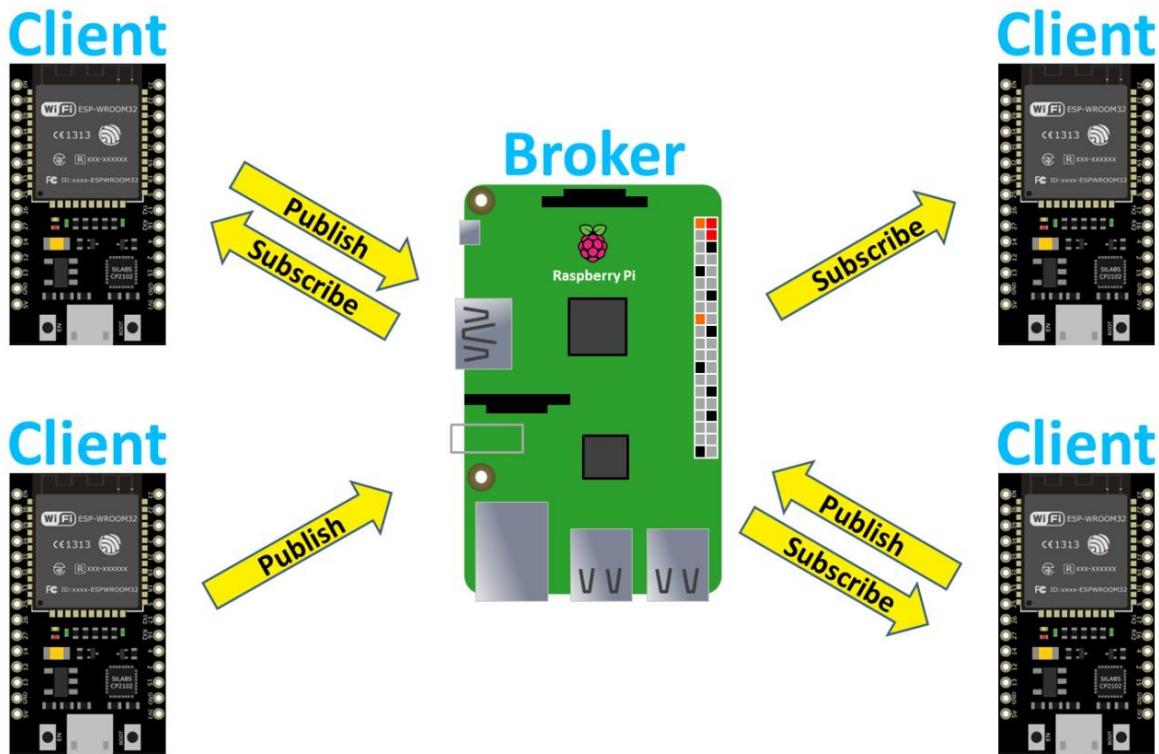


Diagrama eléctrico

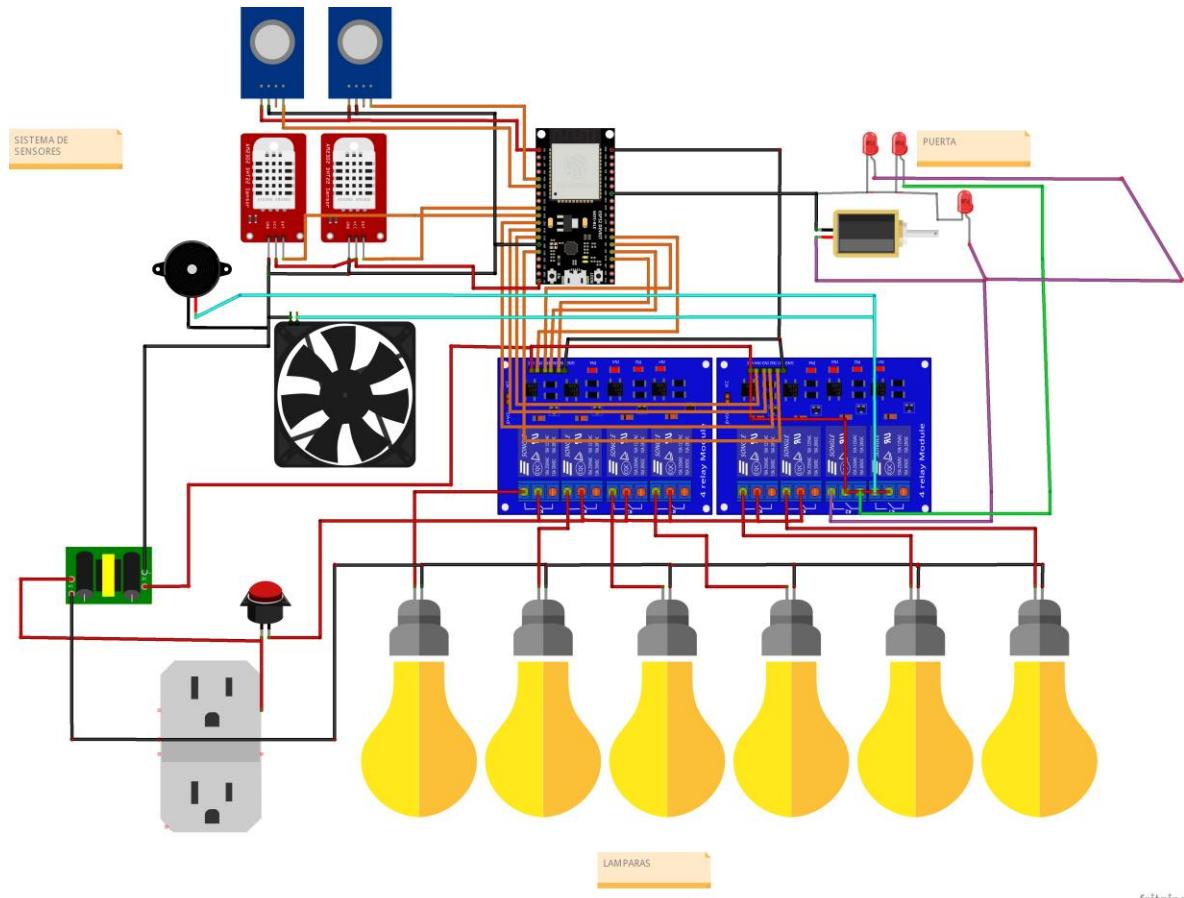
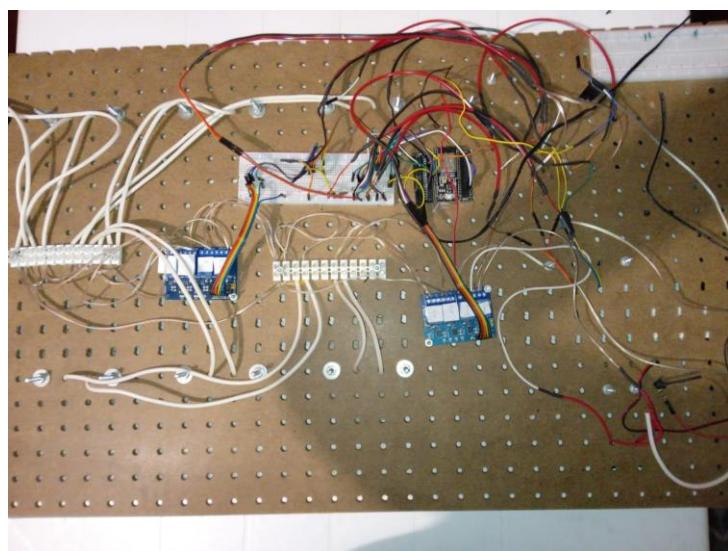


Diagrama físico



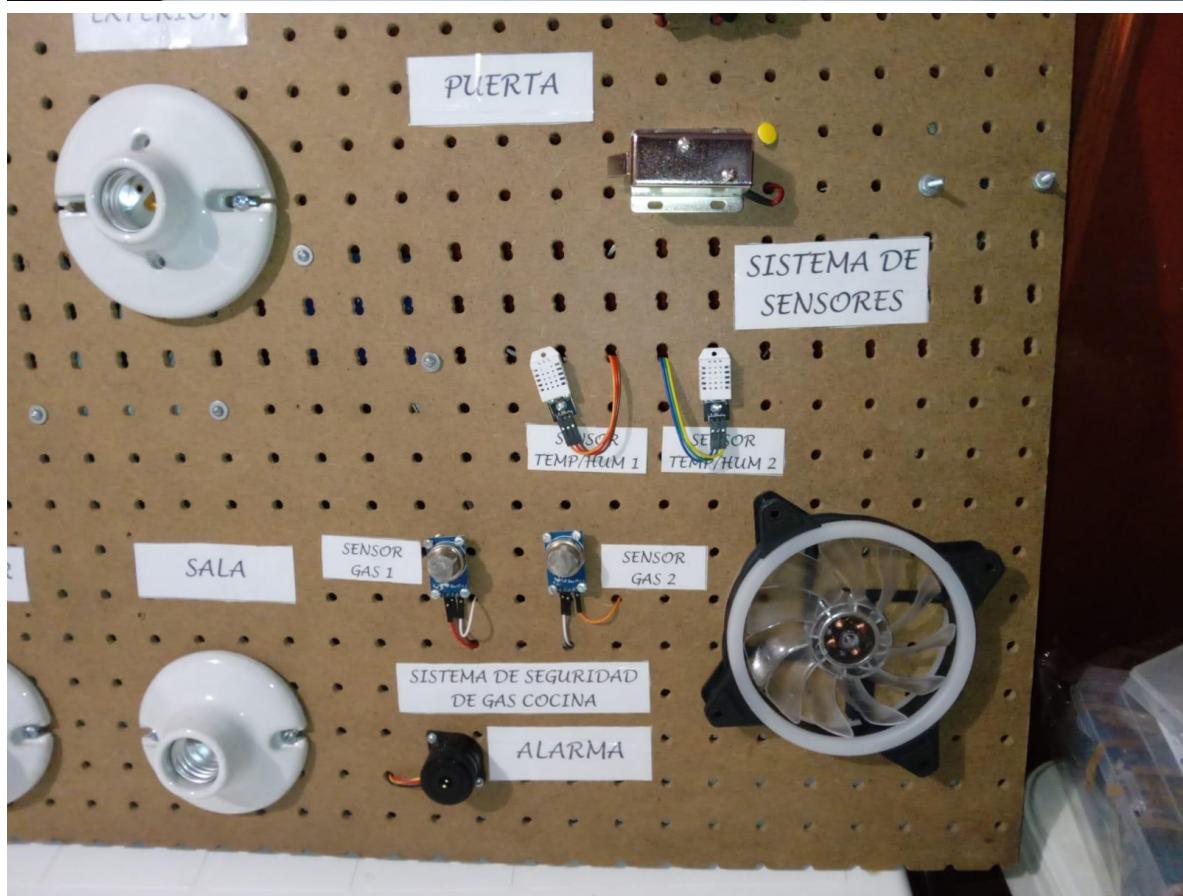
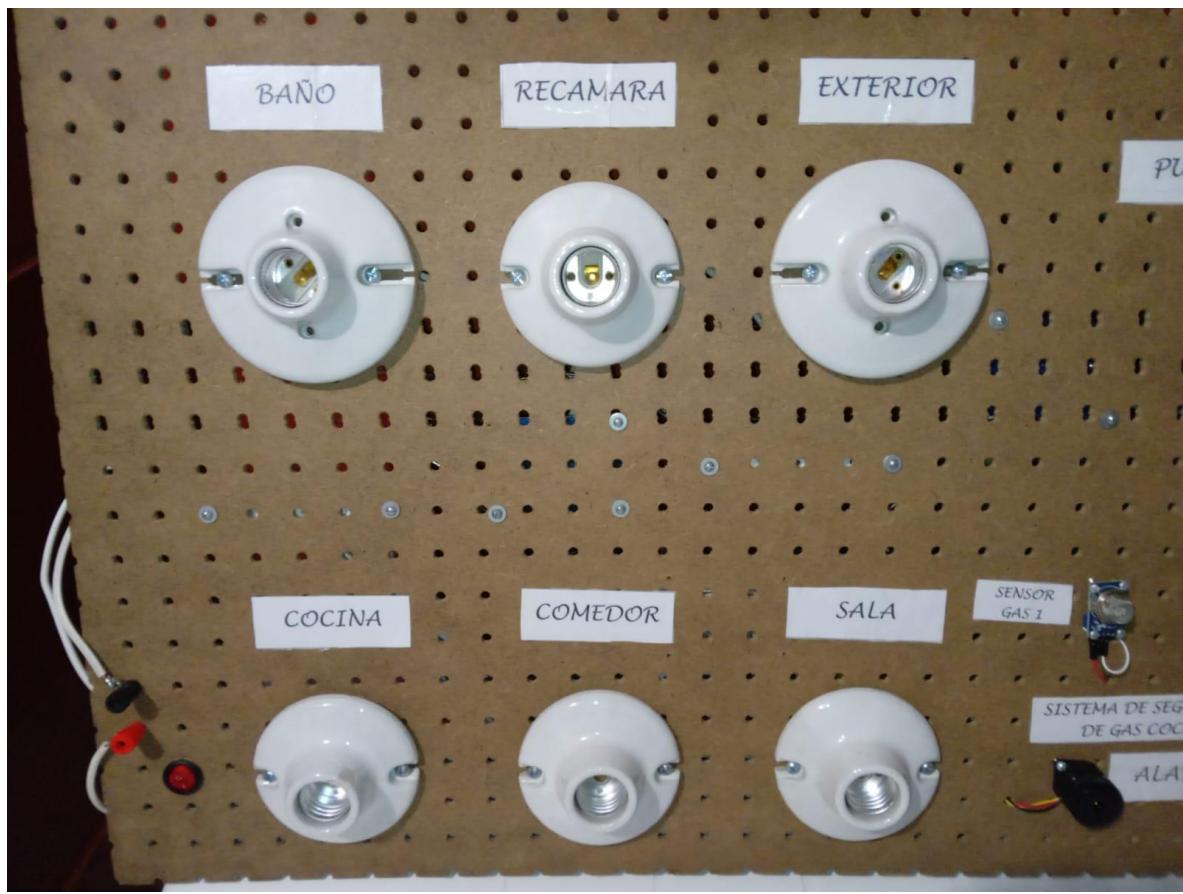
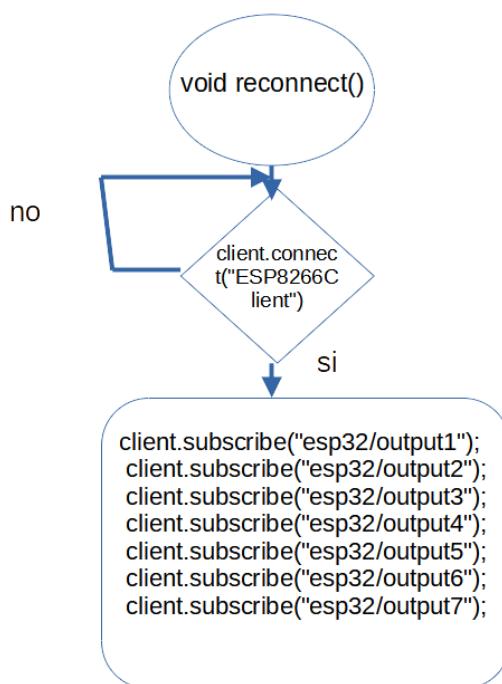
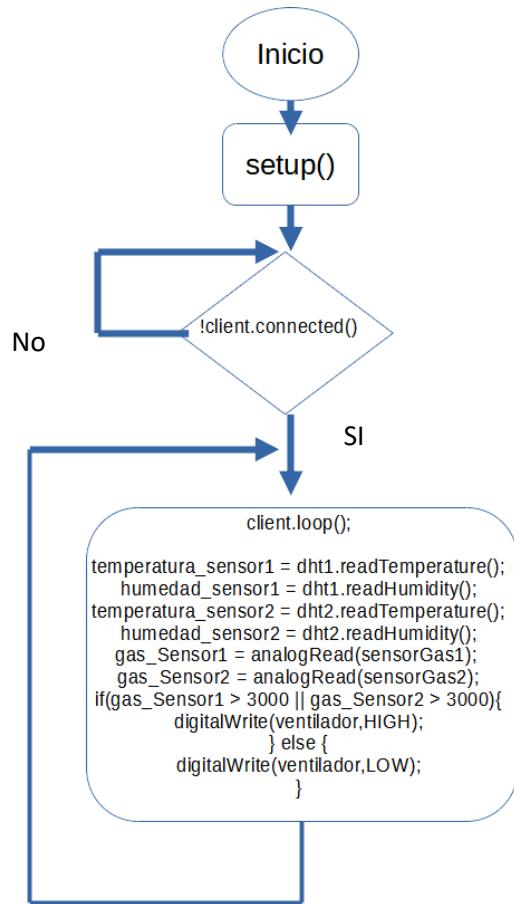
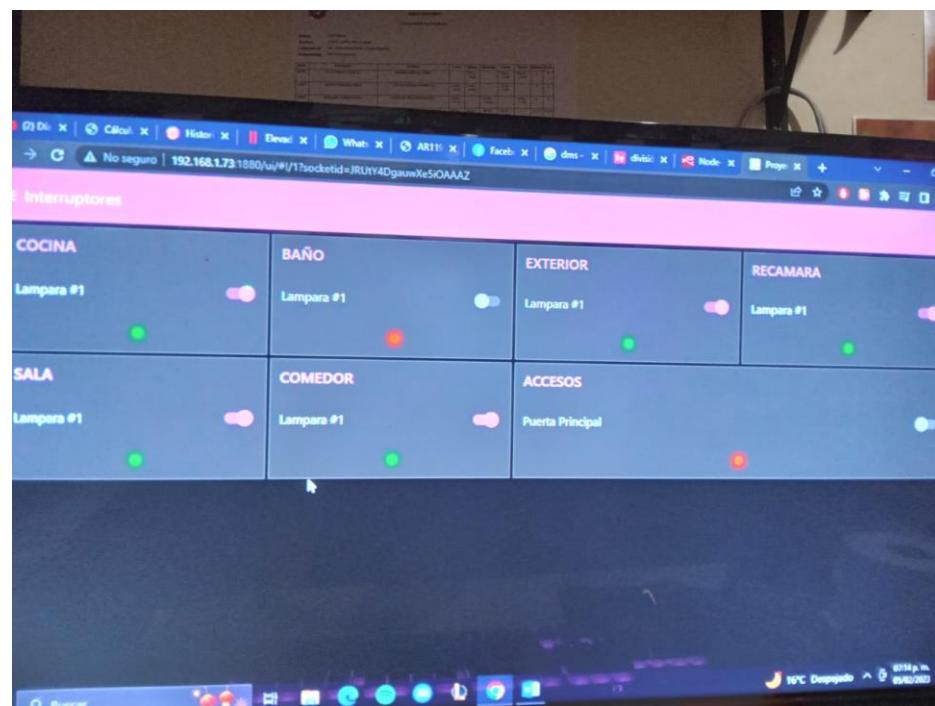
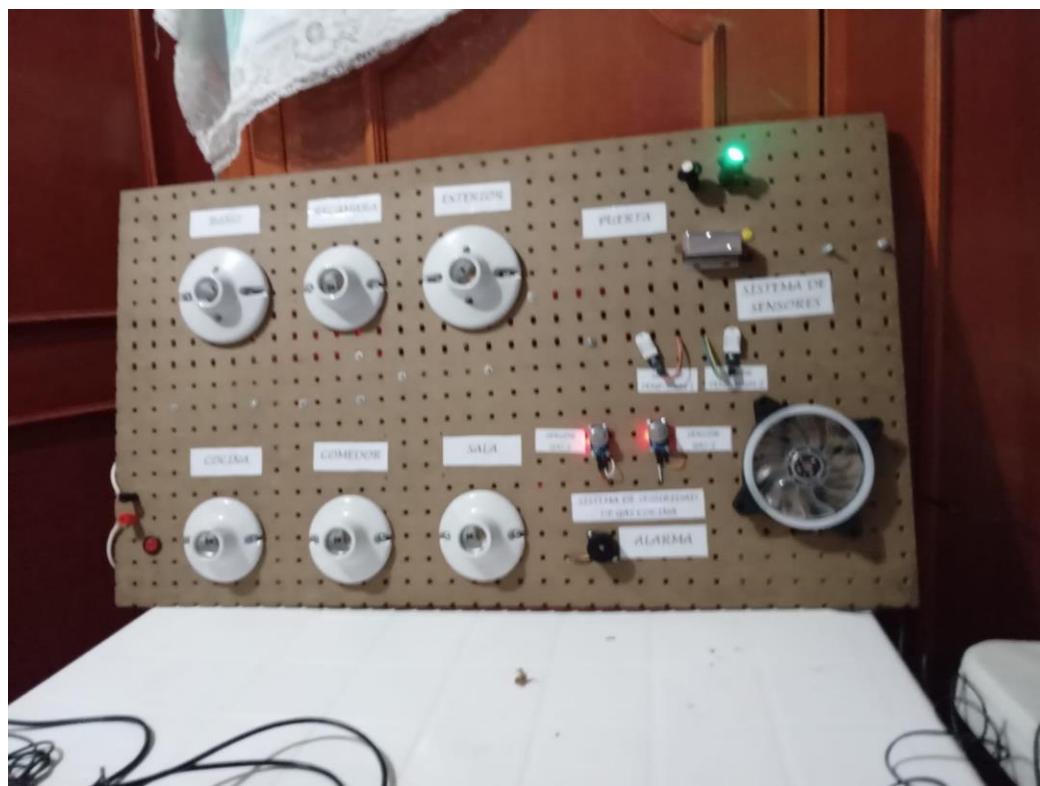


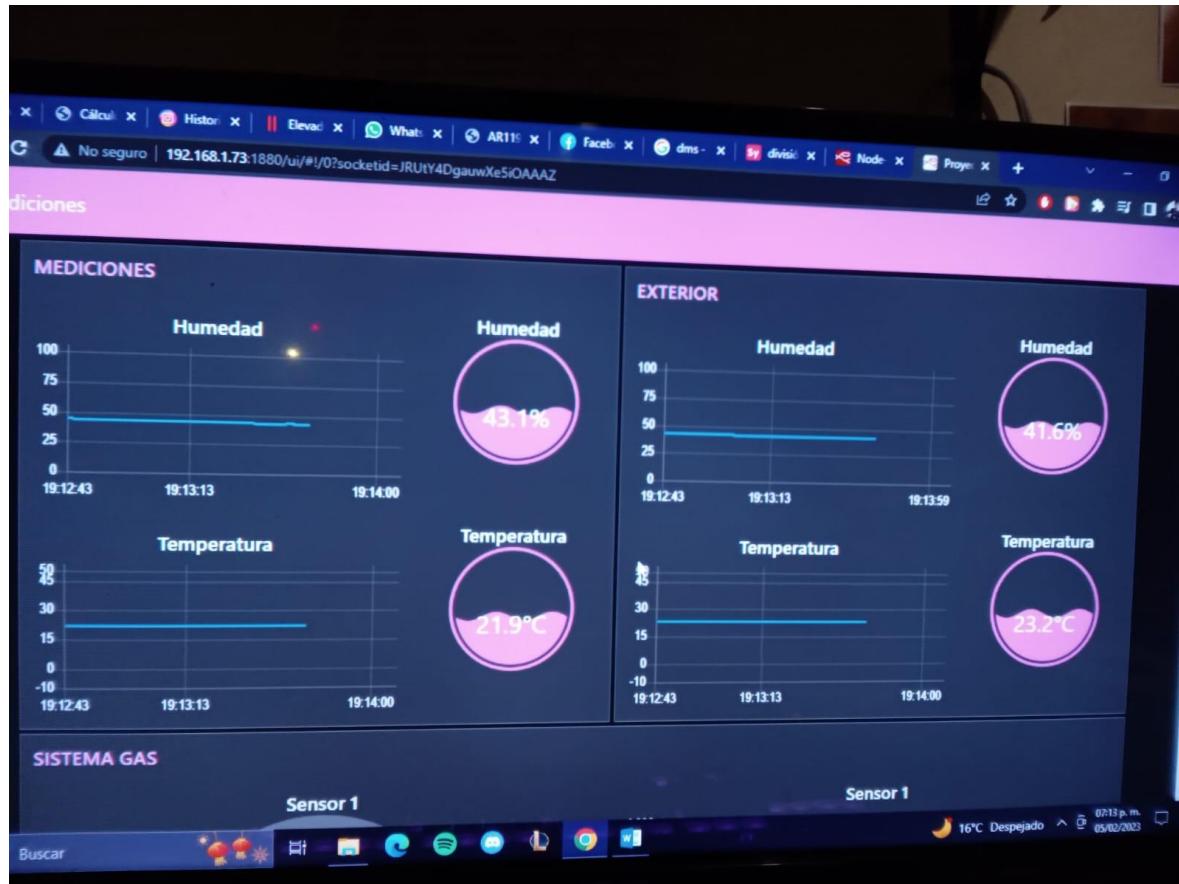
Diagrama de flujo

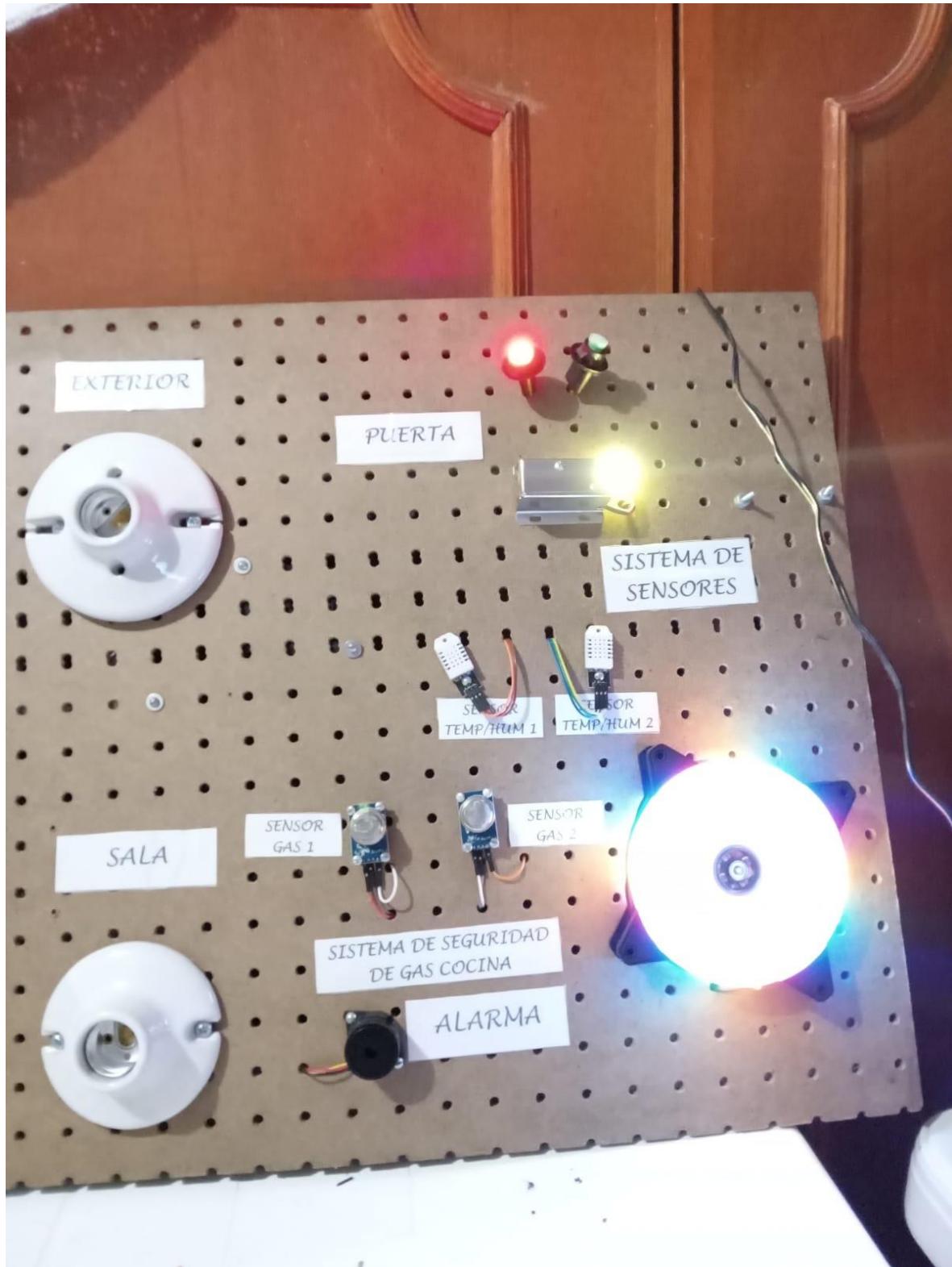
Arduino



Pruebas







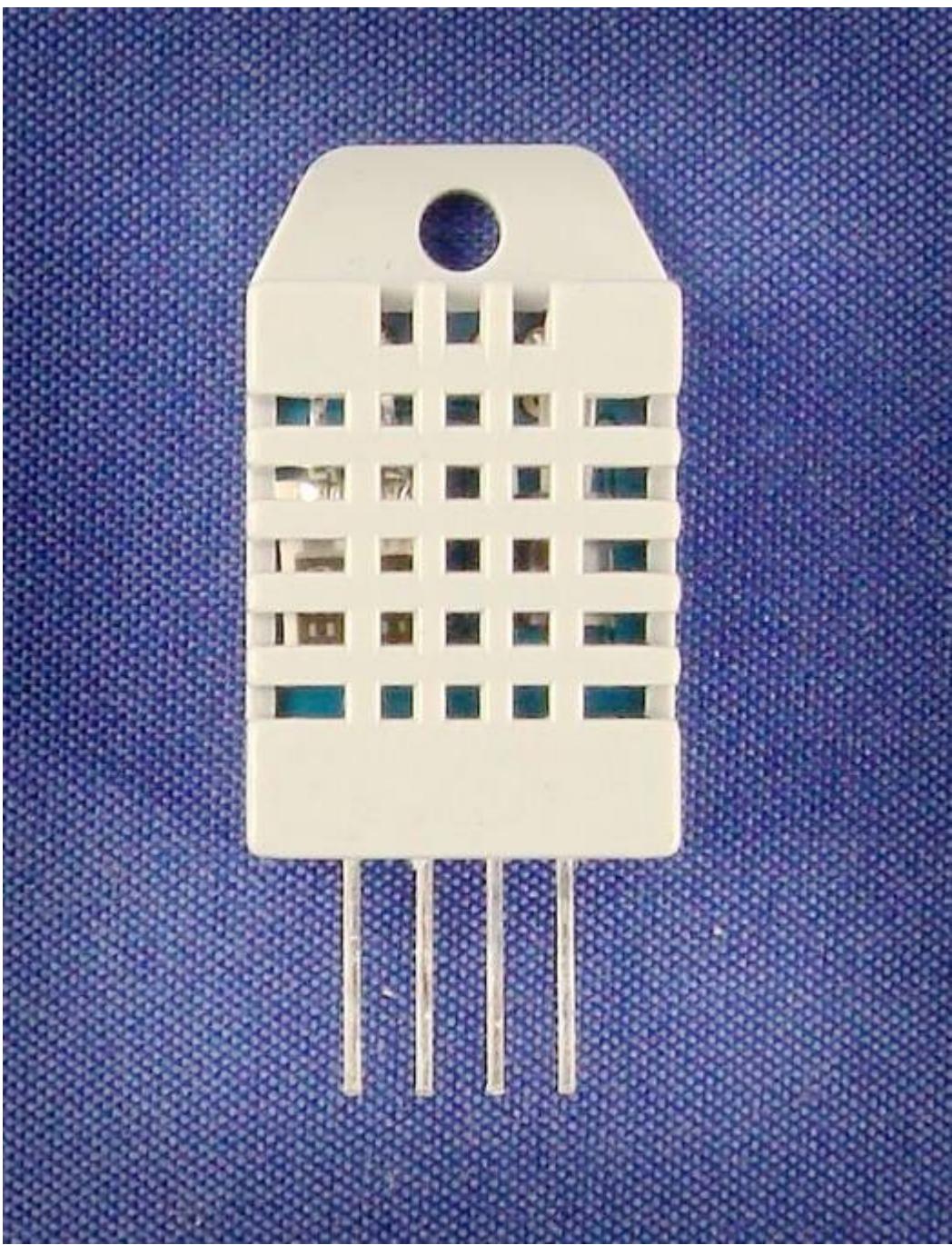
Anexos

Aosong Electronics Co.,Ltd

Your specialist in innovating humidity & temperature sensors

Digital-output relative humidity & temperature sensor/module

DHT22 (DHT22 also named as AM2302)



Capacitive-type humidity and temperature module/sensor

1

Thomas Liu (Business Manager)

Email: thomasliu198518@yahoo.com.cn

Aosong Electronics Co.,Ltd

Your specialist in innovating humidity & temperature sensors

1. Feature & Application:

- * Full range temperature compensated * Relative humidity and temperature measurement
- * Calibrated digital signal * Outstanding long-term stability * Extra components not needed
- * Long transmission distance * Low power consumption * 4 pins packaged and fully interchangeable

2. Description:

DHT22 output calibrated digital signal. It utilizes exclusive digital-signal-collecting-technique and humidity sensing technology, assuring its reliability and stability. Its sensing elements is connected with 8-bit single-chip computer.

Every sensor of this model is temperature compensated and calibrated in accurate calibration chamber and the calibration-coefficient is saved in type of programme in OTP memory, when the sensor is detecting, it will cite coefficient from memory.

Small size & low consumption & long transmission distance(20m) enable DHT22 to be suited in all kinds of harsh application occasions.

Single-row packaged with four pins, making the connection very convenient.

3. Technical Specification:

Model	DHT22	
Power supply	3.3-6V DC	
Output signal	digital signal via single-bus	
Sensing element	Polymer capacitor	
Operating range	humidity 0-100%RH; temperature -40~80Celsius	
Accuracy	humidity +/-2%RH(Max +/-5%RH); temperature <+/-0.5Celsius	
Resolution or sensitivity	humidity 0.1%RH; temperature 0.1Celsius	
Repeatability	humidity +/-1%RH; temperature +/-0.2Celsius	
Humidity hysteresis	+/-0.3%RH	
Long-term Stability	+/-0.5%RH/year	
Sensing period	Average: 2s	
Interchangeability	fully interchangeable	
Dimensions	small size 14*18*5.5mm;	big size 22*28*5mm

4. Dimensions: (unit----mm)

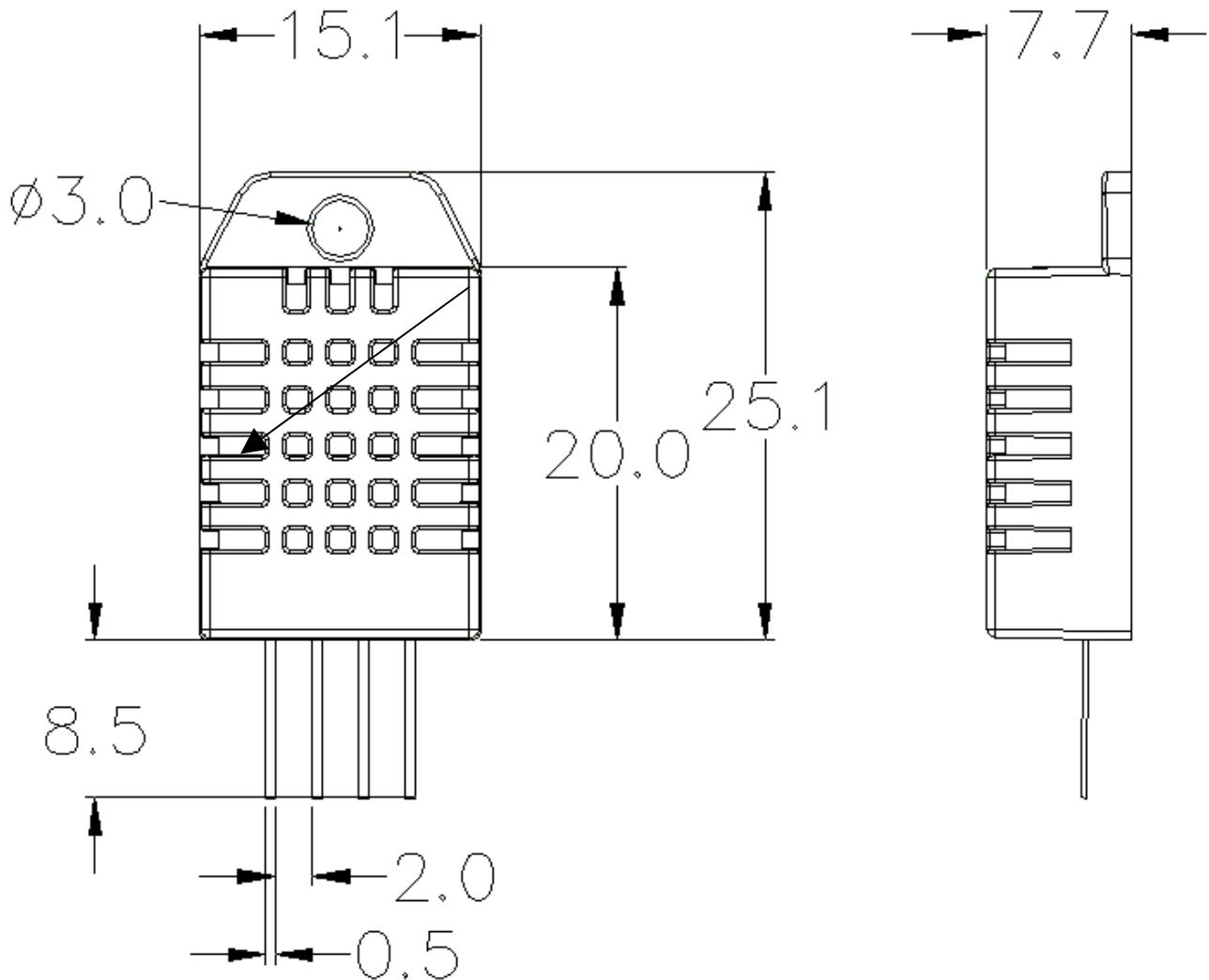
1) Small size dimensions: (unit----mm)

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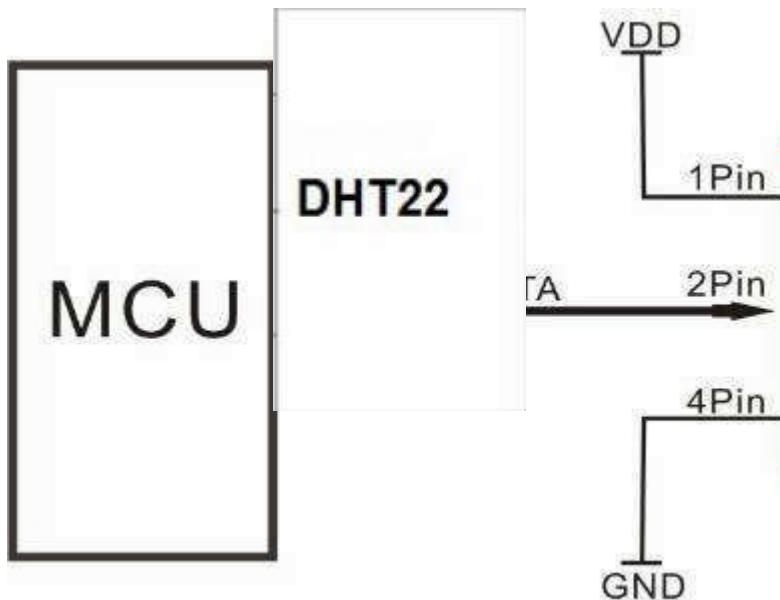
Pin sequence number: 1 2 3 4 (from left to right direction).

Pin	Function
1	VDD----power supply
2	DATA--signal
3	NULL
4	GND

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5. Electrical connection diagram:



3Pin---NC, AM2302 is another name for DHT22

6. Operating specifications:

(1) Power and Pins

Power's voltage should be 3.3-6V DC. When power is supplied to sensor, don't send any instruction to the sensor within one second to pass unstable status. One capacitor valued 100nF can be added between VDD and GND for wave filtering.

(2) Communication and signal

Single-bus data is used for communication between MCU and DHT22, it costs 5mS for single time communication.

Data is comprised of integral and decimal part, the following is the formula for data.

DHT22 send out higher data bit firstly!

DATA=8 bit integral RH data+8 bit decimal RH data+8 bit integral T data+8 bit decimal T data+8 bit check-sum
If the data transmission is right, check-sum should be the last 8 bit of "8 bit integral RH data+8 bit decimal RH data+8 bit integral T data+8 bit decimal T data".

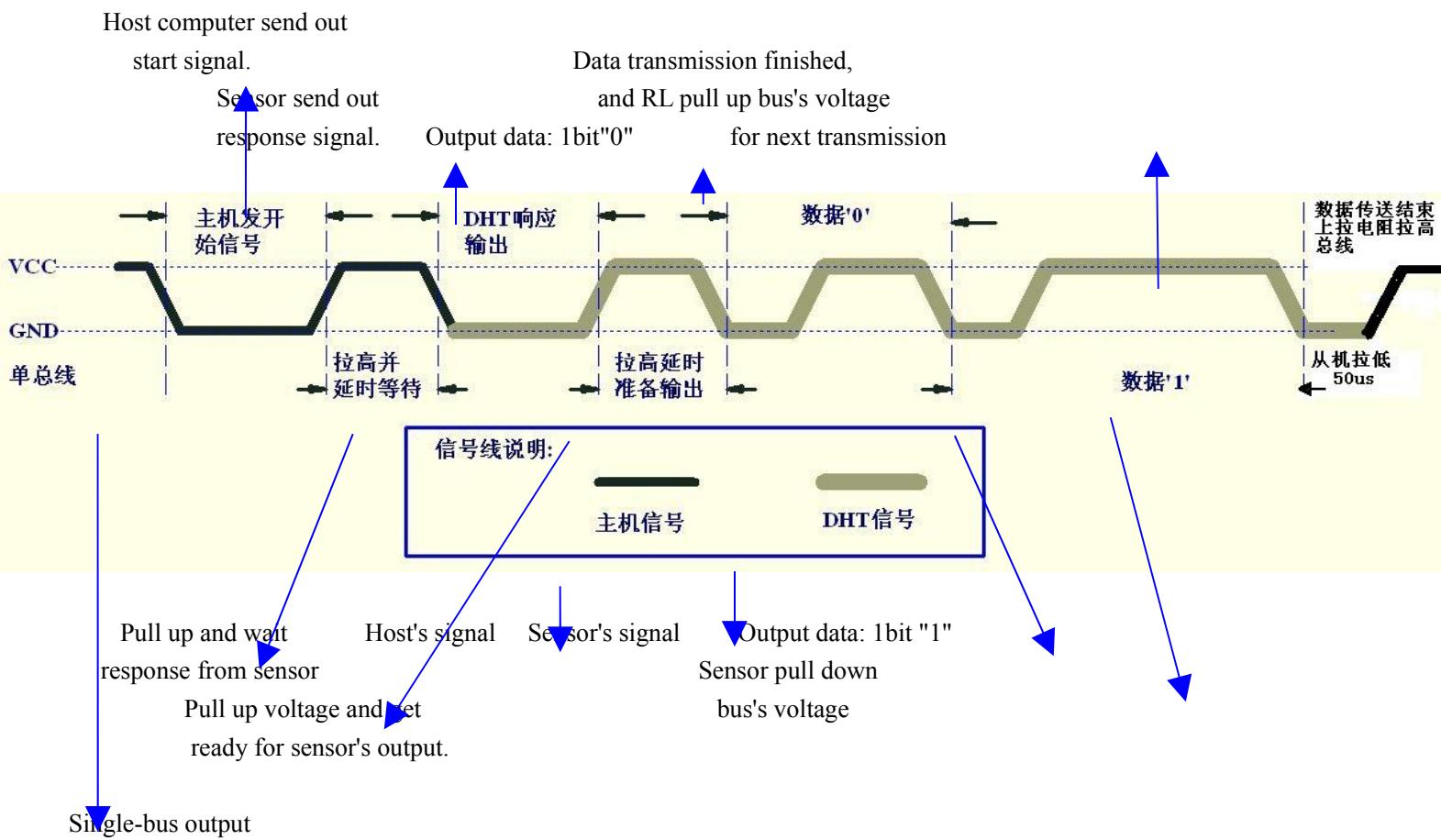
When MCU send start signal, DHT22 change from low-power-consumption-mode to running-mode. When MCU finishes sending the start signal, DHT22 will send response signal of 40-bit data that reflect the relative humidity

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and temperature information to MCU. Without start signal from MCU, DHT22 will not give response signal to MCU. One start signal for one time's response data that reflect the relative humidity and temperature information from DHT22. DHT22 will change to low-power-consumption-mode when data collecting finish if it don't receive start signal from MCU again.

1) Check bellow picture for overall communication process:



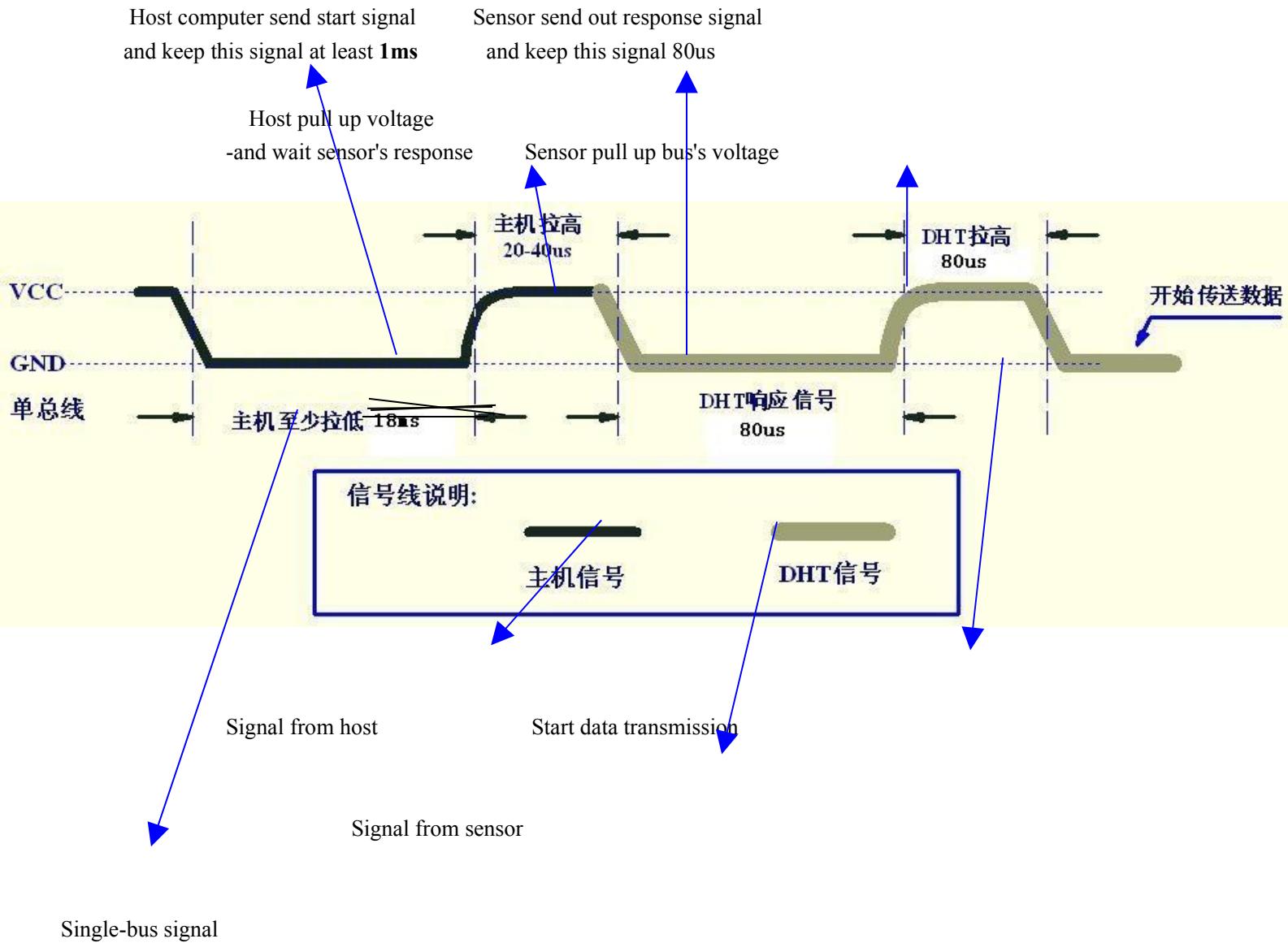
2) Step 1: MCU send out start signal to DHT22

Data-bus's free status is high voltage level. When communication between MCU and DHT22 begin, program of MCU will transform data-bus's voltage level from high to low level and this process must beyond at least 1ms to ensure DHT22 could detect MCU's signal, then MCU will wait 20-40us for DHT22's response.

Check bellow picture for step 1:

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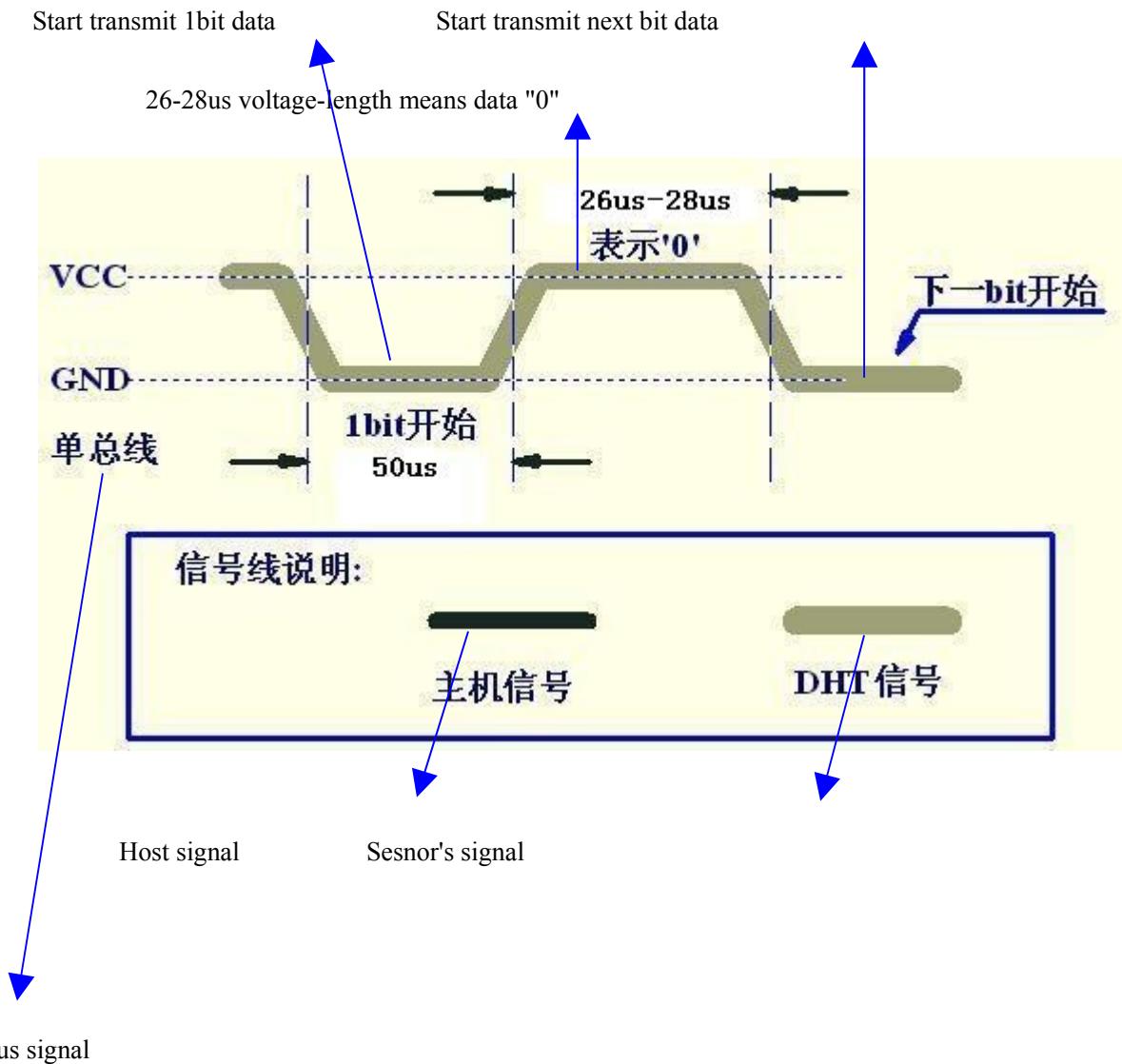
Step 2: DHT22 send response signal to MCU

When DHT22 detect the start signal, DHT22 will send out low-voltage-level signal and this signal last 80us as response signal, then program of DHT22 transform data-bus's voltage level from low to high level and last 80us for DHT22's preparation to send data.

Check bellow picture for step 2:

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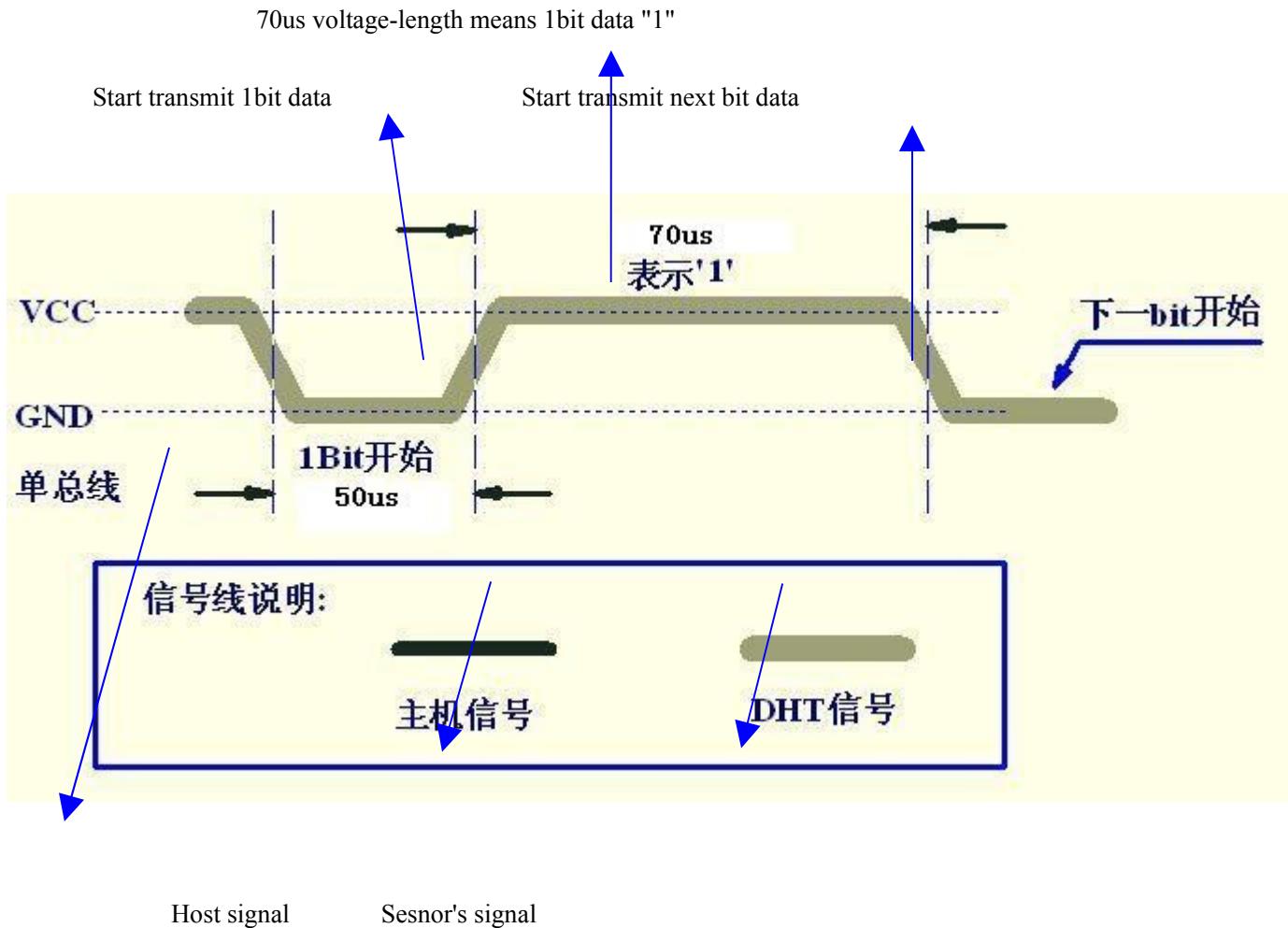
Step 3: DHT22 send data to MCU

When DHT22 is sending data to MCU, every bit's transmission begin with low-voltage-level that last 50us, the following high-voltage-level signal's length decide the bit is "1" or "0".

Check bellow picture for step 3:

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If signal from DHT22 is always high-voltage-level, it means DHT22 is not working properly, please check the electrical connection status.

7. Electrical Characteristics:

Item	Condition	Min	Typical	Max	Unit
Power supply	DC	3.3	5	6	V
Current supply	Measuring	1		1.5	mA
	Stand-by	40	Null	50	uA
Collecting period	Second		2		Second

*Collecting period should be : >2 second.

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8. Attentions of application:

(1) Operating and storage conditions

We don't recommend the applying RH-range beyond the range stated in this specification. The DHT22 sensor can recover after working in non-normal operating condition to calibrated status, but will accelerate sensors' aging.

(2) Attentions to chemical materials

Vapor from chemical materials may interfere DHT22's sensitive-elements and debase DHT22's sensitivity.

(3) Disposal when (1) & (2) happens

Step one: Keep the DHT22 sensor at condition of Temperature 50~60Celsius, humidity <10%RH for 2 hours;

Step two: After step one, keep the DHT22 sensor at condition of Temperature 20~30Celsius, humidity >70%RH for 5 hours.

(4) Attention to temperature's affection

Relative humidity strongly depend on temperature, that is why we use temperature compensation technology to ensure accurate measurement of RH. But it's still be much better to keep the sensor at same temperature when sensing.

DHT22 should be mounted at the place as far as possible from parts that may cause change to temperature.

(5) Attentions to light

Long time exposure to strong light and ultraviolet may debase DHT22's performance.

(6) Attentions to connection wires

The connection wires' quality will effect communication's quality and distance, high quality shielding-wire is recommended.

(7) Other attentions

* Welding temperature should be bellow 260Celsius.

* Avoid using the sensor under dew condition.

* Don't use this product in safety or emergency stop devices or any other occasion that failure of DHT22 may cause personal injury.

ESP32-WROOM-32D & ESP32-WROOM-32U

Datasheet



Version 1.9
Espressif Systems
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About This Document

This document provides the specifications for the ESP32-WROOM-32D and ESP32-WROOM-32U modules.

Revision History

For revision history of this document, please refer to the [last page](#).

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1. Overview

ESP32-WROOM-32D and ESP32-WROOM-32U are powerful, generic Wi-Fi+BT+BLE MCU modules that target a wide variety of applications, ranging from low-power sensor networks to the most demanding tasks, such as voice encoding, music streaming and MP3 decoding.

ESP32-WROOM-32U is different from ESP32-WROOM-32D in that ESP32-WROOM-32U integrates a U.FL connector. For detailed information of the U.FL connector please see Chapter 10. Note that the information in this data sheet is applicable to both modules. Any differences between them will be clearly specified in the course of this document. Table 1 lists the difference between ESP32-WROOM-32D and ESP32-WROOM-32U.

Table 1: ESP32-WROOM-32D vs. ESP32-WROOM-32U

Module	ESP32-WROOM-32D	ESP32-WROOM-32U
Core	ESP32-D0WD	ESP32-D0WD
SPI flash	32 Mbits, 3.3 V	32 Mbits, 3.3 V
Crystal	40 MHz	40 MHz
Antenna	onboard antenna	U.FL connector (which needs to be connected to an external IPEX antenna)
Dimensions (Unit: mm)	(18.00±0.10) × (25.50±0.10) × (3.10±0.10) (See Figure 6 for details)	(18.00±0.10) × (19.20±0.10) × (3.20±0.10) (See Figure 7 for details)
Schematics	See Figure 3 for details.	See Figure 4 for details.

At the core of the two modules is the ESP32-D0WD chip that belongs to the ESP32 series* of chips. The chip embedded is designed to be scalable and adaptive. There are two CPU cores that can be individually controlled, and the CPU clock frequency is adjustable from 80 MHz to 240 MHz. The user may also power off the CPU and make use of the low-power co-processor to constantly monitor the peripherals for changes or crossing of thresholds. ESP32 integrates a rich set of peripherals, ranging from capacitive touch sensors, Hall sensors, SD card interface, Ethernet, high-speed SPI, UART, I²S and I²C.

Note:

* For details on the part numbers of the ESP32 family of chips, please refer to the document [ESP32 Datasheet](#).

The integration of Bluetooth, Bluetooth LE and Wi-Fi ensures that a wide range of applications can be targeted, and that the module is all-around: using Wi-Fi allows a large physical range and direct connection to the Internet through a Wi-Fi router, while using Bluetooth allows the user to conveniently connect to the phone or broadcast low energy beacons for its detection. The sleep current of the ESP32 chip is less than 5 μ A, making it suitable for battery powered and wearable electronics applications. The module supports a data rate of up to 150 Mbps, and 20 dBm output power at the antenna to ensure the widest physical range. As such the module does offer industry-leading specifications and the best performance for electronic integration, range, power consumption, and connectivity.

The operating system chosen for ESP32 is freeRTOS with LwIP; TLS 1.2 with hardware acceleration is built in as well. Secure (encrypted) over the air (OTA) upgrade is also supported, so that users can upgrade their products even after their release, at minimum cost and effort.

Table 2 provides the specifications of ESP32-WROOM-32D and ESP32-WROOM-32U.

Table 2: ESP32-WROOM-32D and ESP32-WROOM-32U Specifications

Categories	Items	Specifications
Certification	RF Certification	FCC/CE-RED/IC/TELEC/KCC/SRRC/NCC
	Wi-Fi Certification	Wi-Fi Alliance
	Bluetooth certification	BQB
	Green Certification	REACH/RoHS
Test	Reliability	HTOL/HTSL/uHAST/TCT/ESD
Wi-Fi	Protocols	802.11 b/g/n (802.11n up to 150 Mbps)
		A-MPDU and A-MSDU aggregation and 0.4 μ s guard interval support
	Frequency range	2.4 GHz ~ 2.5 GHz
Bluetooth	Protocols	Bluetooth v4.2 BR/EDR and BLE specification
	Radio	NZIF receiver with -97 dBm sensitivity
		Class-1, class-2 and class-3 transmitter
		AFH
	Audio	CVSD and SBC
Hardware	Module interfaces	SD card, UART, SPI, SDIO, I ² C, LED PWM, Motor PWM, I ² S, IR, pulse counter, GPIO, capacitive touch sensor, ADC, DAC
	On-chip sensor	Hall sensor
	Integrated crystal	40 MHz crystal
	Integrated SPI flash ¹	4 MB
	Operating voltage/Power supply	3.0 V ~ 3.6 V
	Operating current	Average: 80 mA
	Minimum current delivered by power supply	500 mA
	Recommended operating temperature range ²	-40 °C ~ +85 °C
	Moisture sensitivity level (MSL)	Level 3

Notice:

1. ESP32-WROOM-32D and ESP32-WROOM-32U with 8 MB flash or 16 MB flash are available for custom order.
2. ESP32-WROOM-32D and ESP32-WROOM-32U with high temperature range (-40 °C ~ +105 °C) option are available for custom order. 4 MB SPI flash is supported on the high temperature range version.
3. For detailed ordering information, please see [Espressif Product Ordering Information](#).

2. Pin Definitions

2.1 Pin Layout

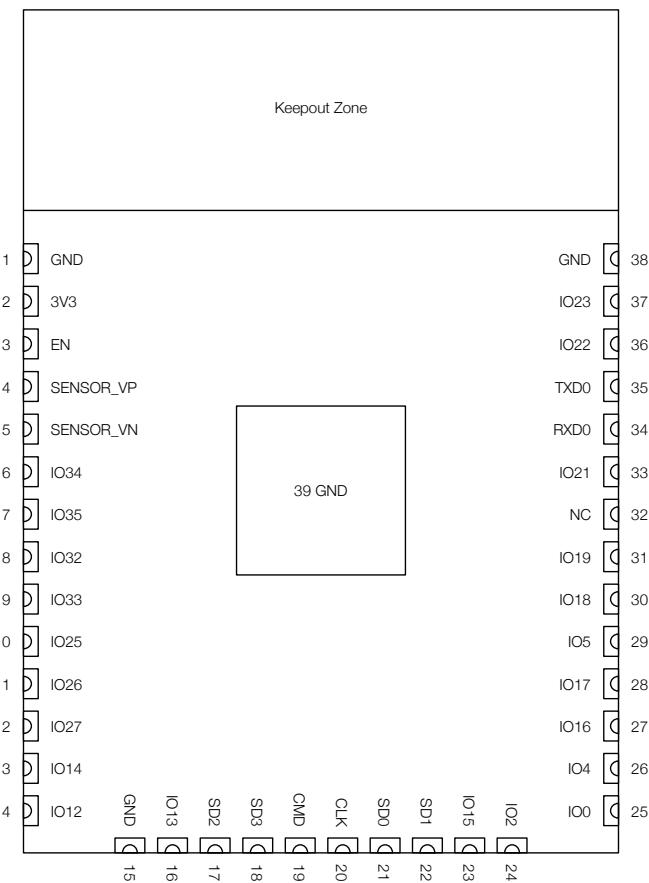


Figure 1: ESP32-WROOM-32D Pin Layout (Top View)

Note:

The pin layout of ESP32-WROOM-32U is the same as that of ESP32-WROOM-32D, except that ESP32-WROOM-32U has no keepout zone.

2.2 Pin Description

The ESP32-WROOM-32D and ESP32-WROOM-32U have 38 pins. See pin definitions in Table 3.

Table 3: Pin Definitions

Name	No.	Type	Function
GND	1	P	Ground
3V3	2	P	Power supply
EN	3	I	Module-enable signal. Active high.
SENSOR_VP	4	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_VN	5	I	GPIO39, ADC1_CH3, RTC_GPIO3
IO34	6	I	GPIO34, ADC1_CH6, RTC_GPIO4
IO35	7	I	GPIO35, ADC1_CH7, RTC_GPIO5

Name	No.	Type	Function
IO32	8	I/O	GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
IO33	9	I/O	GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
IO25	10	I/O	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
IO26	11	I/O	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1
IO27	12	I/O	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
IO14	13	I/O	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
IO12	14	I/O	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
GND	15	P	Ground
IO13	16	I/O	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
SHD/SD2*	17	I/O	GPIO9, SD_DATA2, SPIHD, HS1_DATA2, U1RXD
SWP/SD3*	18	I/O	GPIO10, SD_DATA3, SPIWP, HS1_DATA3, U1TXD
SCS/CMD*	19	I/O	GPIO11, SD_CMD, SPICS0, HS1_CMD, U1RTS
SCK/CLK*	20	I/O	GPIO6, SD_CLK, SPICLK, HS1_CLK, U1CTS
SDO/SD0*	21	I/O	GPIO7, SD_DATA0, SPIQ, HS1_DATA0, U2RTS
SDI/SD1*	22	I/O	GPIO8, SD_DATA1, SPID, HS1_DATA1, U2CTS
IO15	23	I/O	GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3
IO2	24	I/O	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
IO0	25	I/O	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
IO4	26	I/O	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER
IO16	27	I/O	GPIO16, HS1_DATA4, U2RXD, EMAC_CLK_OUT
IO17	28	I/O	GPIO17, HS1_DATA5, U2TXD, EMAC_CLK_OUT_180
IO5	29	I/O	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
IO18	30	I/O	GPIO18, VSPICLK, HS1_DATA7
IO19	31	I/O	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
NC	32	-	-
IO21	33	I/O	GPIO21, VSPIHD, EMAC_TX_EN
RXD0	34	I/O	GPIO3, U0RXD, CLK_OUT2
TXD0	35	I/O	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
IO22	36	I/O	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
IO23	37	I/O	GPIO23, VSPID, HS1_STROBE
GND	38	P	Ground

Notice:

* Pins SCK/CLK, SDO/SD0, SDI/SD1, SHD/SD2, SWP/SD3 and SCS/CMD, namely, GPIO6 to GPIO11 are connected to the integrated SPI flash integrated on the module and are not recommended for other uses.

2.3 Strapping Pins

ESP32 has five strapping pins, which can be seen in Chapter 6 Schematics:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the values of these five bits from register "GPIO_STRAPPING".

During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 4 for a detailed boot-mode configuration by strapping pins.

Table 4: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3 V	1.8 V		
MTDI	Pull-down	0	1		
Booting Mode					
Pin	Default	SPI Boot	Download Boot		
GPIO0	Pull-up	1	0		
GPIO2	Pull-down	Don't-care	0		
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
Pin	Default	U0TXD Active	U0TXD Silent		
MTDO	Pull-up	1	0		
Timing of SDIO Slave					
Pin	Default	Falling-edge Sampling Falling-edge Output	Falling-edge Sampling Rising-edge Output	Rising-edge Sampling Falling-edge Output	Rising-edge Sampling Rising-edge Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Note:

- Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave" after booting.
- Both ESP32-WROOM-32D and ESP32-WROOM-32U integrate a 3.3 V SPI flash, so the pin MTDI cannot be set to 1 when the modules are powered up.

3. Functional Description

This chapter describes the modules and functions integrated in ESP32-WROOM-32D and ESP32-WROOM-32U.

3.1 CPU and Internal Memory

ESP32-D0WD contains a dual-core Xtensa® 32-bit LX6 MCU. The internal memory includes:

- 448 KB of ROM for booting and core functions.
- 520 KB of on-chip SRAM for data and instructions.
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash-encryption and chip-ID.

3.2 External Flash and SRAM

ESP32 supports multiple external QSPI flash and SRAM chips. More details can be found in Chapter SPI in the [ESP32 Technical Reference Manual](#). ESP32 also supports hardware encryption/decryption based on AES to protect developers' programs and data in flash.

ESP32 can access the external QSPI flash and SRAM through high-speed caches.

- The external flash can be mapped into CPU instruction memory space and read-only memory space simultaneously.
 - When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU.
 - When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads are supported.
- External SRAM can be mapped into CPU data memory space. Up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads and writes are supported.

Both ESP32-WROOM-32D and ESP32-WROOM-32U integrate a 4 MB of external SPI flash. The integrated SPI flash is connected to GPIO6, GPIO7, GPIO8, GPIO9, GPIO10 and GPIO11. These six pins cannot be used as regular GPIOs.

3.3 Crystal Oscillators

The module uses a 40-MHz crystal oscillator.

3.4 RTC and Low-Power Management

With the use of advanced power-management technologies, ESP32 can switch between different power modes.

For details on ESP32's power consumption in different power modes, please refer to section "RTC and Low-Power Management" in [ESP32 Datasheet](#).

4. Peripherals and Sensors

Please refer to Section Peripherals and Sensors in [ESP32 Datasheet](#).

Note:

External connections can be made to any GPIO except for GPIOs in the range 6-11. These six GPIOs are connected to the module's integrated SPI flash. For details, please see Section 6 Schematics.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in Table 5 below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the [recommended operating conditions](#).

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	-0.3	3.6	V
I_{output}^1	Cumulative IO output current	-	1,100	mA
T_{store}	Storage temperature	-40	150	°C

1. The module worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to ground. Please note that pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.
2. Please see Appendix IO_MUX of [ESP32 Datasheet](#) for IO's power domain.

5.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	-	-	A
T	Operating temperature	-40	-	85	°C

5.3 DC Characteristics (3.3 V, 25 °C)

Table 7: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
C_{IN}	Pin capacitance		-	2	-	pF
V_{IH}	High-level input voltage		$0.75 \times VDD^1$	-	$VDD^1 + 0.3$	V
V_{IL}	Low-level input voltage		-0.3	-	$0.25 \times VDD^1$	V
I_{IH}	High-level input current		-	-	50	nA
I_{IL}	Low-level input current		-	-	50	nA
V_{OH}	High-level output voltage		$0.8 \times VDD^1$	-	-	V
V_{OL}	Low-level output voltage		-	-	$0.1 \times VDD^1$	V
I_{OH}	High-level source current ($VDD^1 = 3.3$ V, $V_{OH} \geq 2.64$ V, output drive strength set to the maximum)	VDD3P3_CPU power domain ^{1, 2}	-	40	-	mA
		VDD3P3_RTC power domain ^{1, 2}	-	40	-	mA
		VDD_SDIO power domain ^{1, 3}	-	20	-	mA

Symbol	Parameter	Min	Typ	Max	Unit
I_{OL}	Low-level sink current ($VDD^1 = 3.3$ V, $V_{OL} = 0.495$ V, output drive strength set to the maximum)	-	28	-	mA
R_{PU}	Resistance of internal pull-up resistor	-	45	-	k Ω
R_{PD}	Resistance of internal pull-down resistor	-	45	-	k Ω
V_{IL_nRST}	Low-level input voltage of CHIP_PU to power off the chip	-	-	0.6	V

Notes:

1. Please see Appendix IO_MUX of [ESP32 Datasheet](#) for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, $V_{OH}>=2.64$ V, as the number of current-source pins increases.
3. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

5.4 Wi-Fi Radio

Table 8: Wi-Fi Radio Characteristics

Parameter	Condition	Min	Typical	Max	Unit
Operating frequency range ^{note1}	-	2412	-	2484	MHz
Output impedance ^{note2}	-	-	<i>note 2</i>	-	Ω
TX power ^{note3}	11n, MCS7	12	13	14	dBm
	11b mode	17.5	18.5	20	dBm
Sensitivity	11b, 1 Mbps	-	-98	-	dBm
	11b, 11 Mbps	-	-89	-	dBm
	11g, 6 Mbps	-	-92	-	dBm
	11g, 54 Mbps	-	-74	-	dBm
	11n, HT20, MCS0	-	-91	-	dBm
	11n, HT20, MCS7	-	-71	-	dBm
	11n, HT40, MCS0	-	-89	-	dBm
	11n, HT40, MCS7	-	-69	-	dBm
Adjacent channel rejection	11g, 6 Mbps	-	31	-	dB
	11g, 54 Mbps	-	14	-	dB
	11n, HT20, MCS0	-	31	-	dB
	11n, HT20, MCS7	-	13	-	dB

1. Device should operate in the frequency range allocated by regional regulatory authorities. Target operating frequency range is configurable by software.
2. For the modules that use IPEX antennas, the output impedance is 50 Ω . For other modules without IPEX antennas, users do not need to concern about the output impedance.
3. Target TX power is configurable based on device or certification requirements.

5.5 BLE Radio

5.5.1 Receiver

Table 9: Receiver Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	-	-	-97	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-5	-	dB
	F = F0 - 1 MHz	-	-5	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	-10	-	-	dBm
	2000 MHz ~ 2400 MHz	-27	-	-	dBm
	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-36	-	-	dBm

5.5.2 Transmitter

Table 10: Transmitter Characteristics – BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	-	-	0	-	dBm
Gain control step	-	-	3	-	dBm
RF power control range	-	-12	-	+9	dBm
Adjacent channel transmit power	F = F0 ± 2 MHz	-	-52	-	dBm
	F = F0 ± 3 MHz	-	-58	-	dBm
	F = F0 ± > 3 MHz	-	-60	-	dBm
Δ f1avg	-	-	-	265	kHz
Δ f2max	-	247	-	-	kHz
Δ f2avg/Δ f1avg	-	-	-0.92	-	-
ICFT	-	-	-10	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift	-	-	2	-	kHz

5.6 Reflow Profile

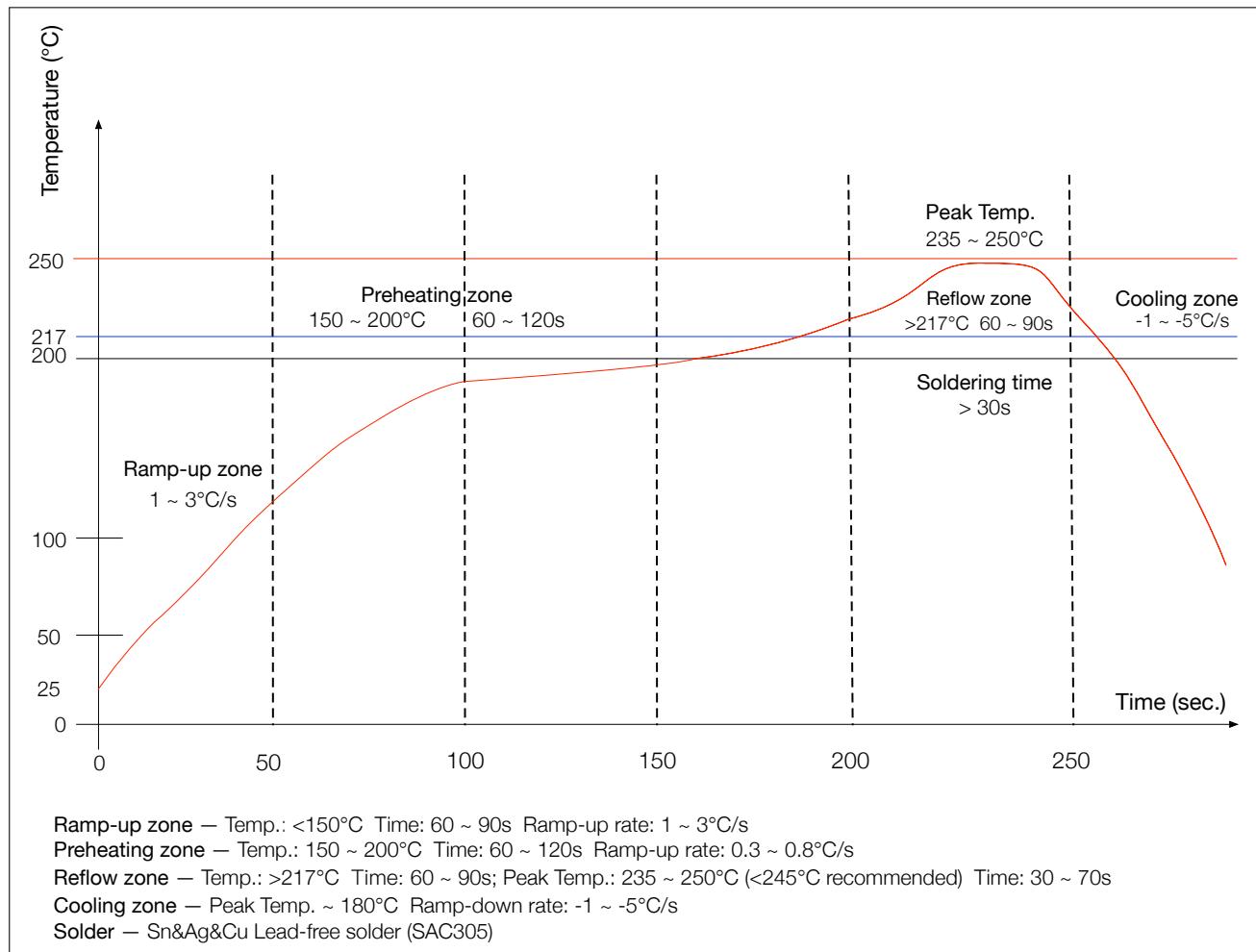


Figure 2: Reflow Profile

6. Schematics

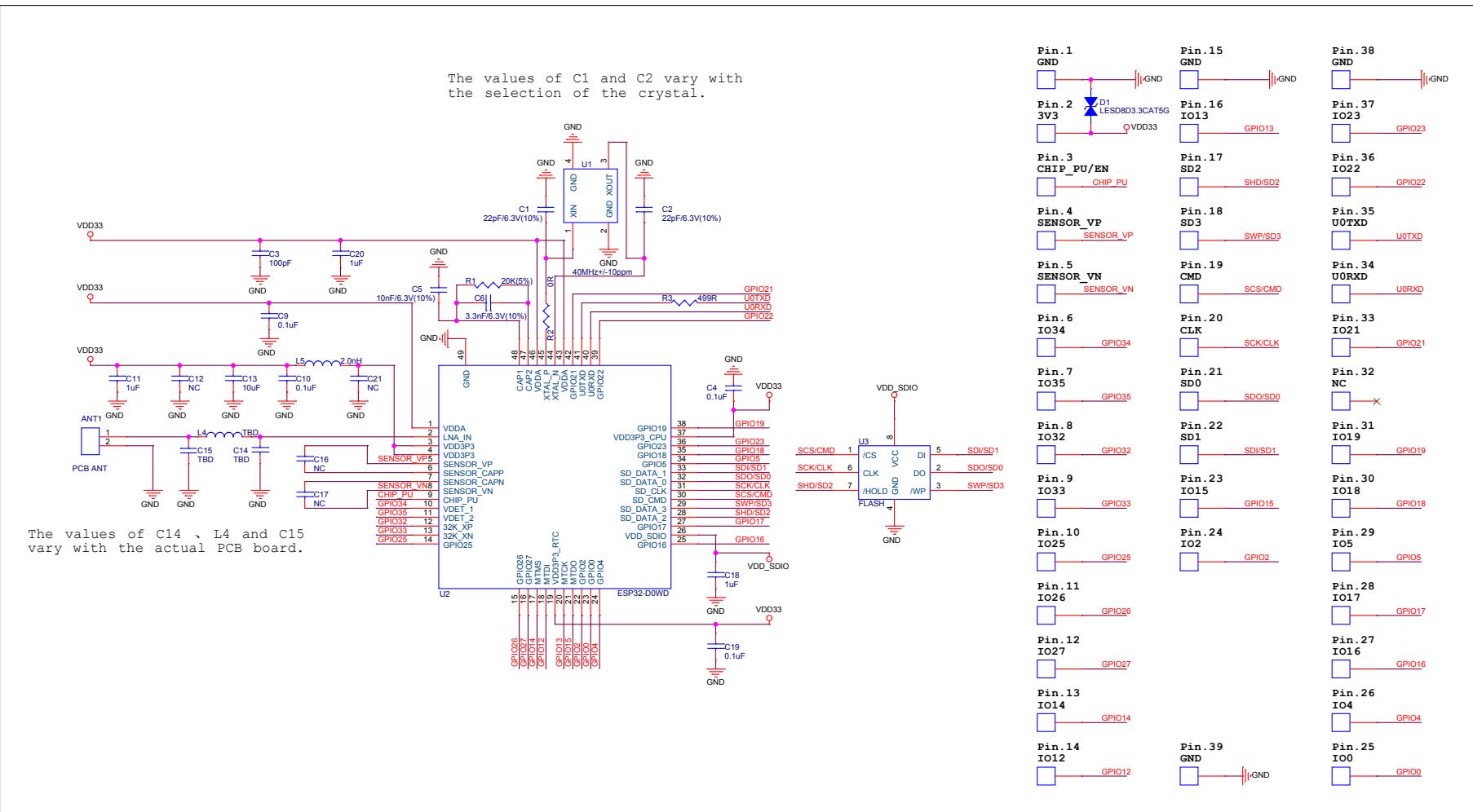


Figure 3: ESP32-WROOM-32D Schematics

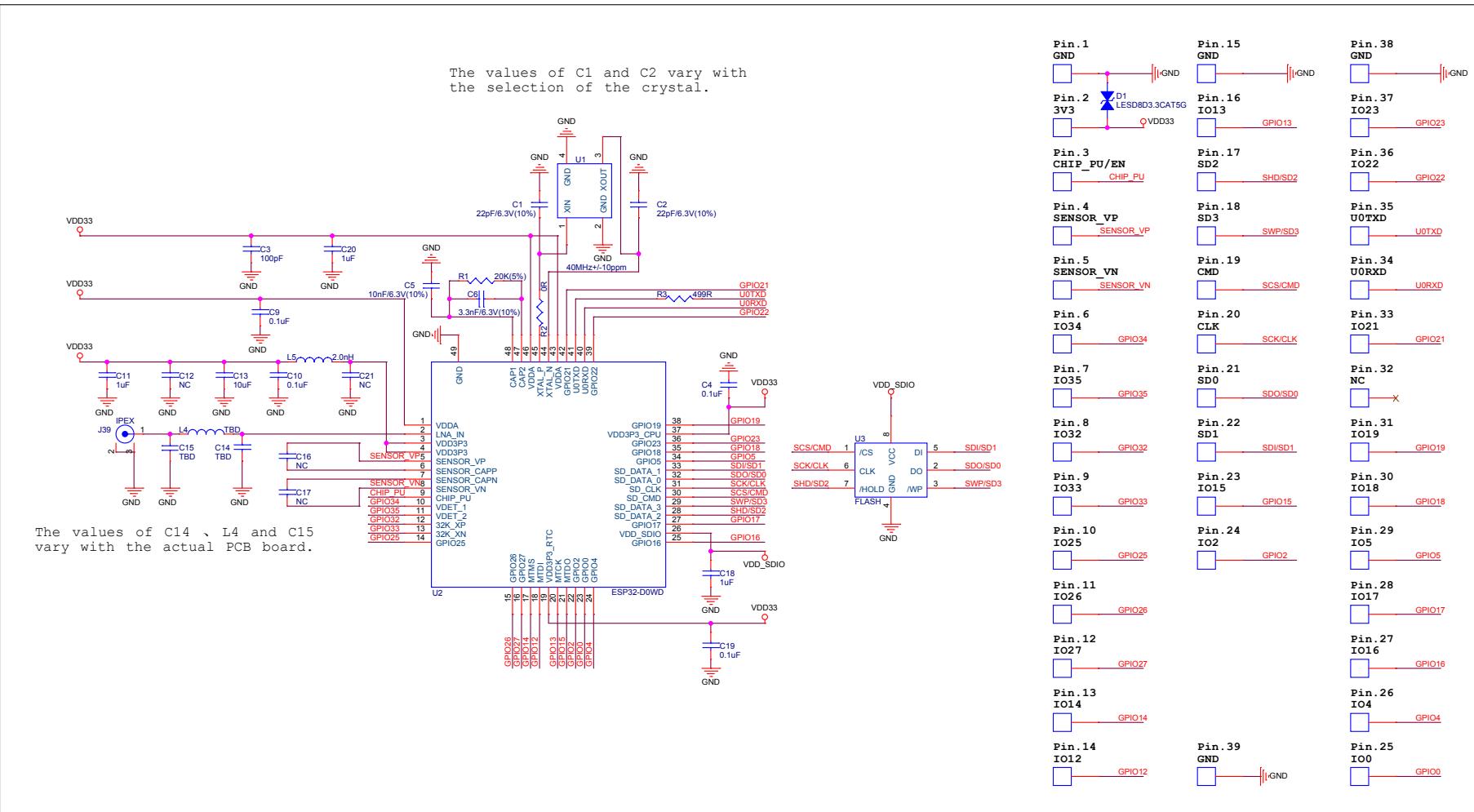


Figure 4: ESP32-WROOM-32U Schematics

7. Peripheral Schematics

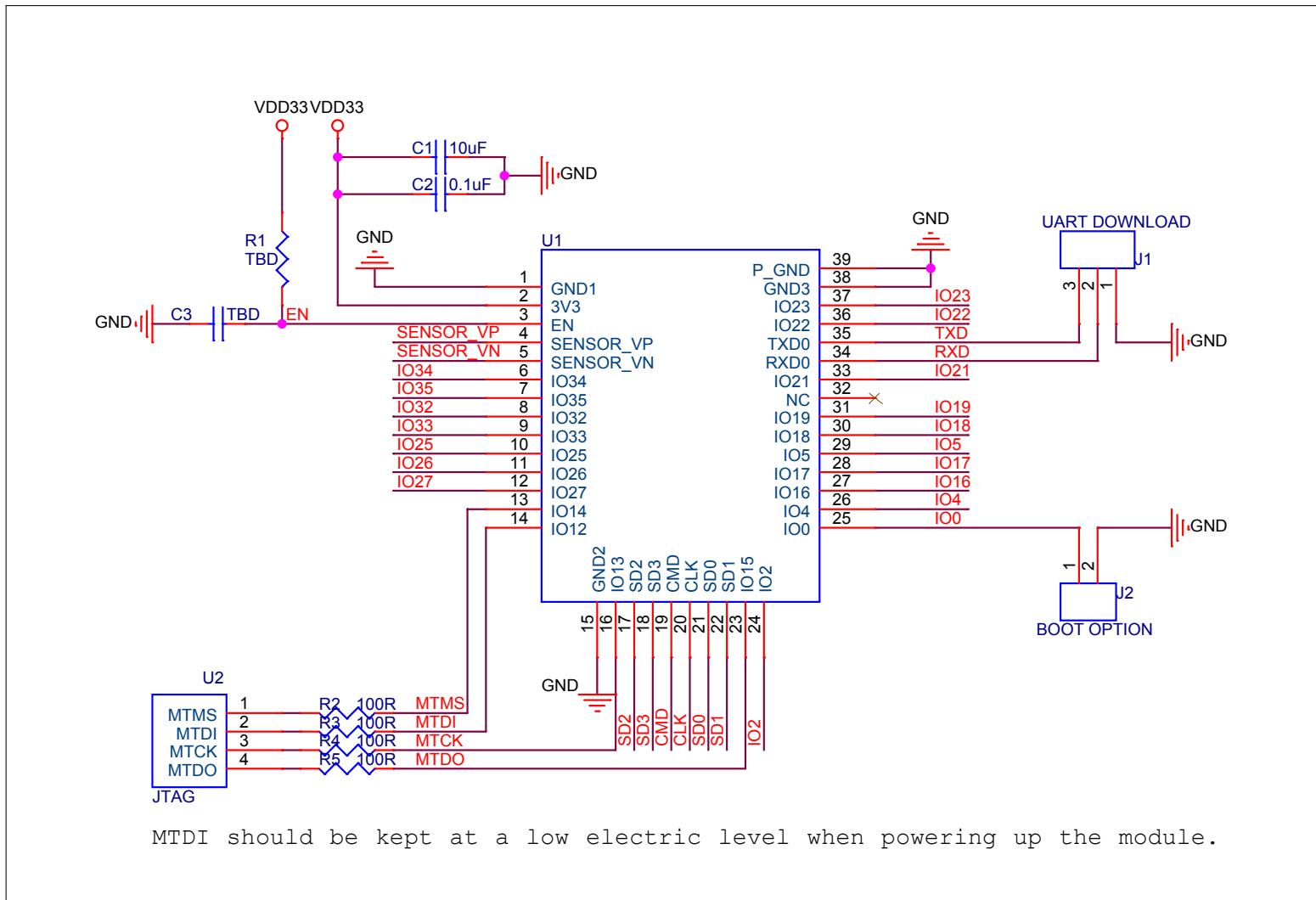


Figure 5: ESP32-WROOM-32D & ESP32-WROOM-32U Peripheral Schematics

Note:

- Soldering Pad 39 to the Ground is not necessary for a satisfactory thermal performance. If users do want to solder it, they need to ensure that the correct quantity of soldering paste is applied.
- When ESP32 is powered on and off repeatedly by switching the power rails, and there is a large capacitor on the 3V3 rail, a discharge circuit can be added to the 3V3 rail to ensure proper power-on-reset. Please find the discharge circuit in Chapter *Peripheral Schematics*, in [ESP32-WROOM-32 Datasheet](#).
- When battery is used as the power supply for ESP32 series of chips and modules, a supply voltage supervisor is recommended to avoid boot failure due to low voltage. Users are recommended to pull CHIP_PU low if the power supply for ESP32 is below 2.3 V. For the reset circuit, please refer to Chapter *Peripheral Schematics*, in [ESP32-WROOM-32 Datasheet](#).
- To ensure the power supply to the ESP32 chip during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually $R = 10 \text{ k}\Omega$ and $C = 0.1 \mu\text{F}$. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in [ESP32 Datasheet](#).

8. Physical Dimensions

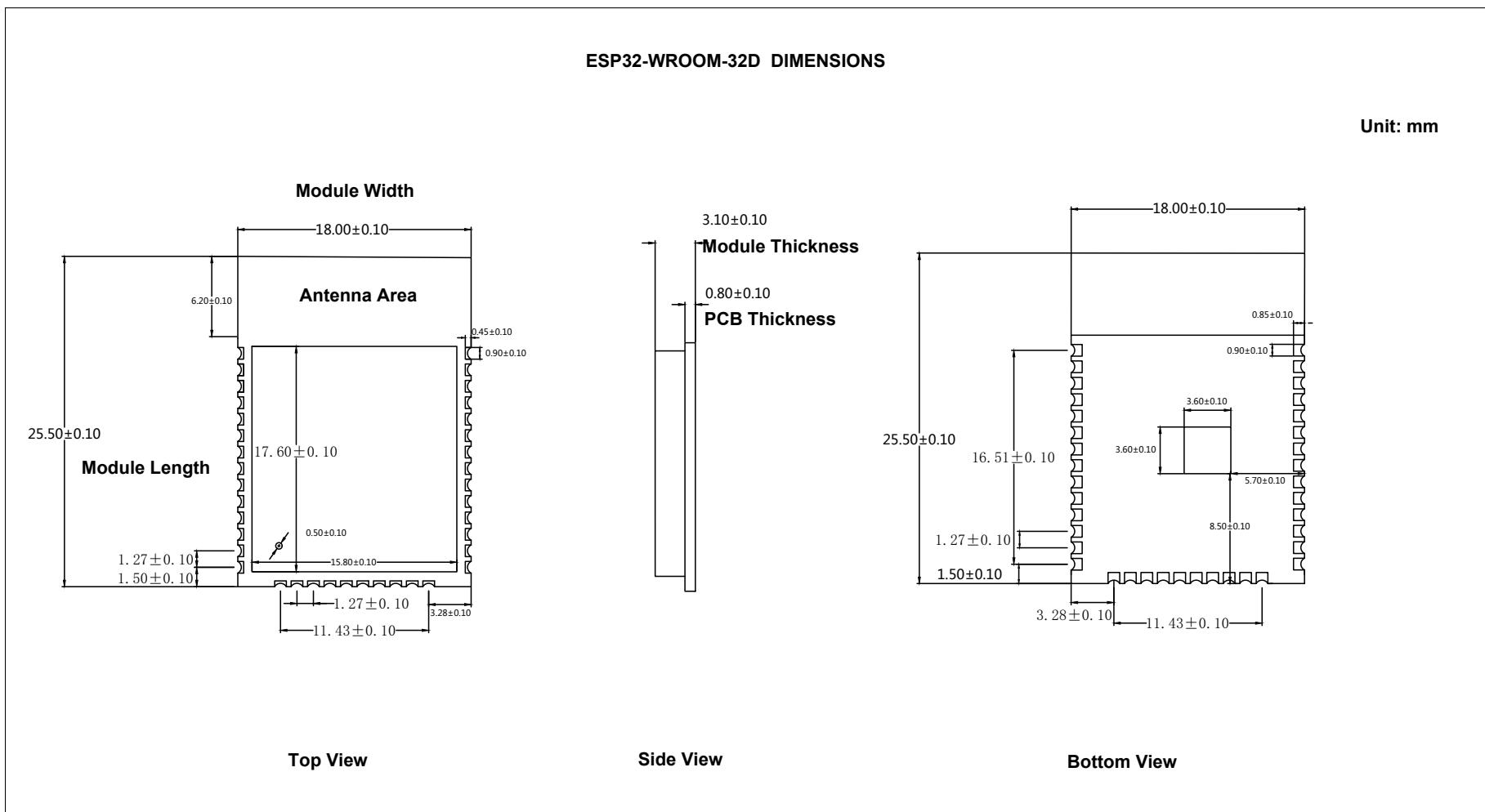


Figure 6: Physical Dimensions of ESP32-WROOM-32D

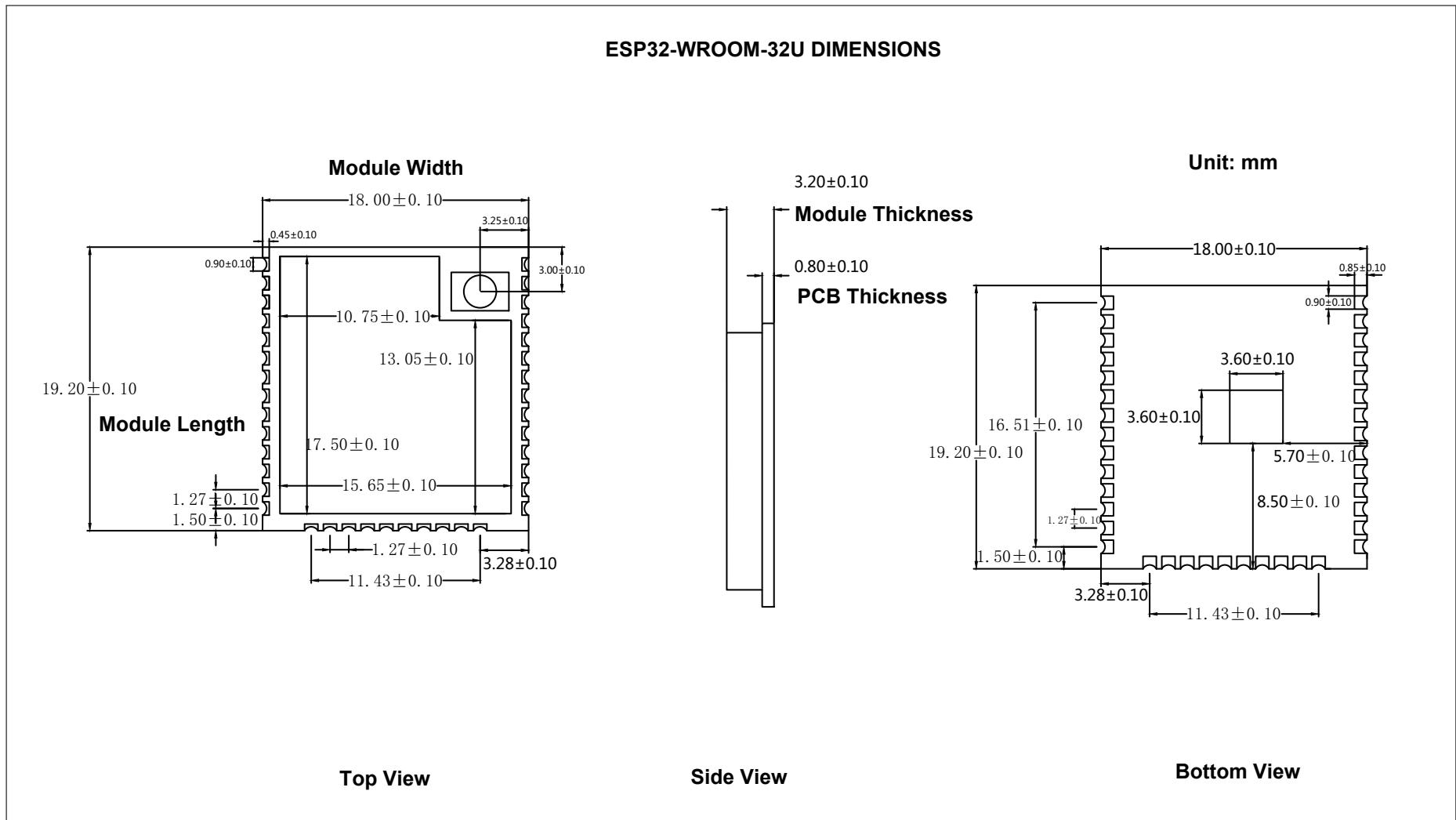


Figure 7: Physical Dimensions of ESP32-WROOM-32U

9. Recommended PCB Land Pattern

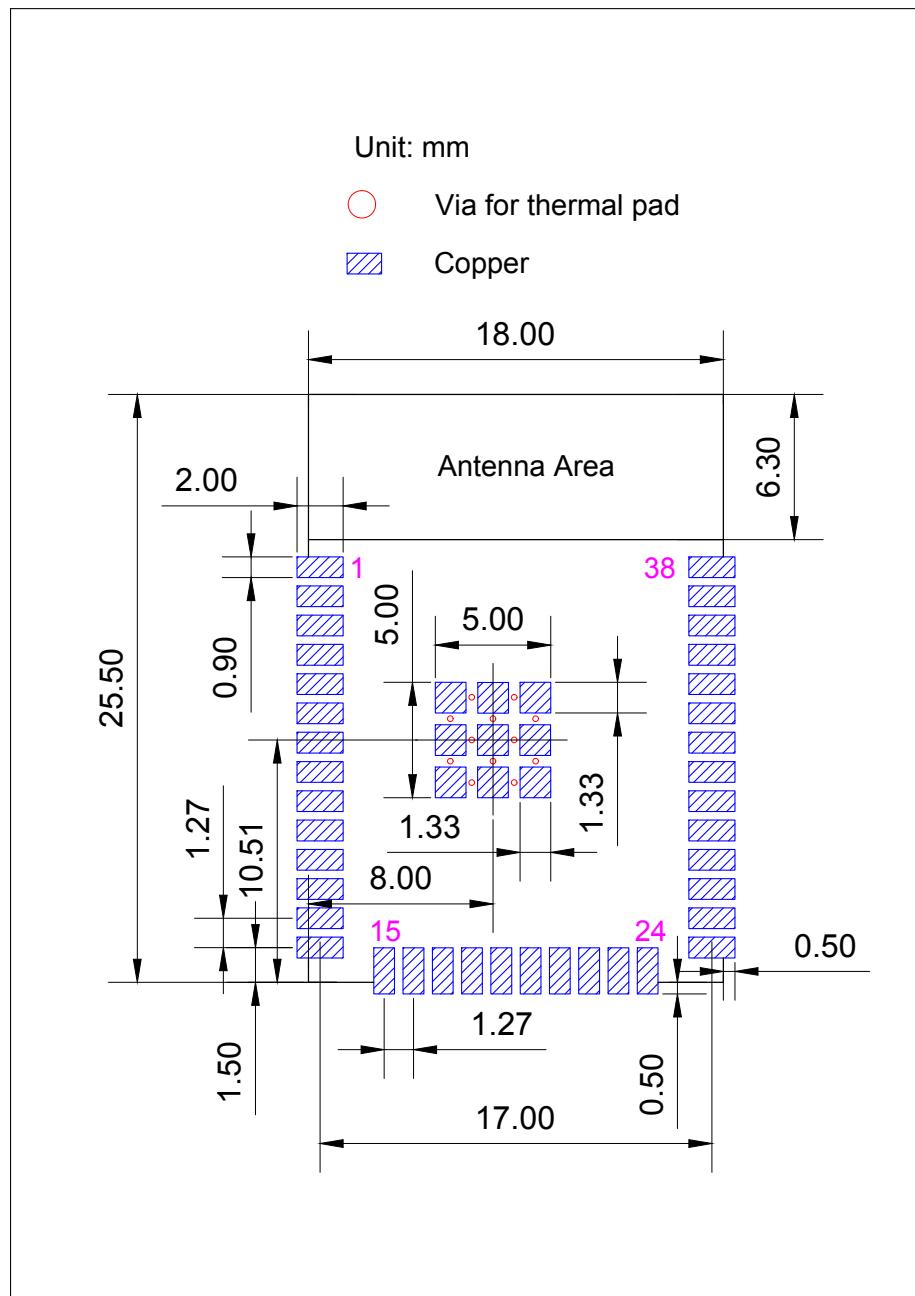


Figure 8: Recommended PCB Land Pattern of ESP32-WROOM-32D

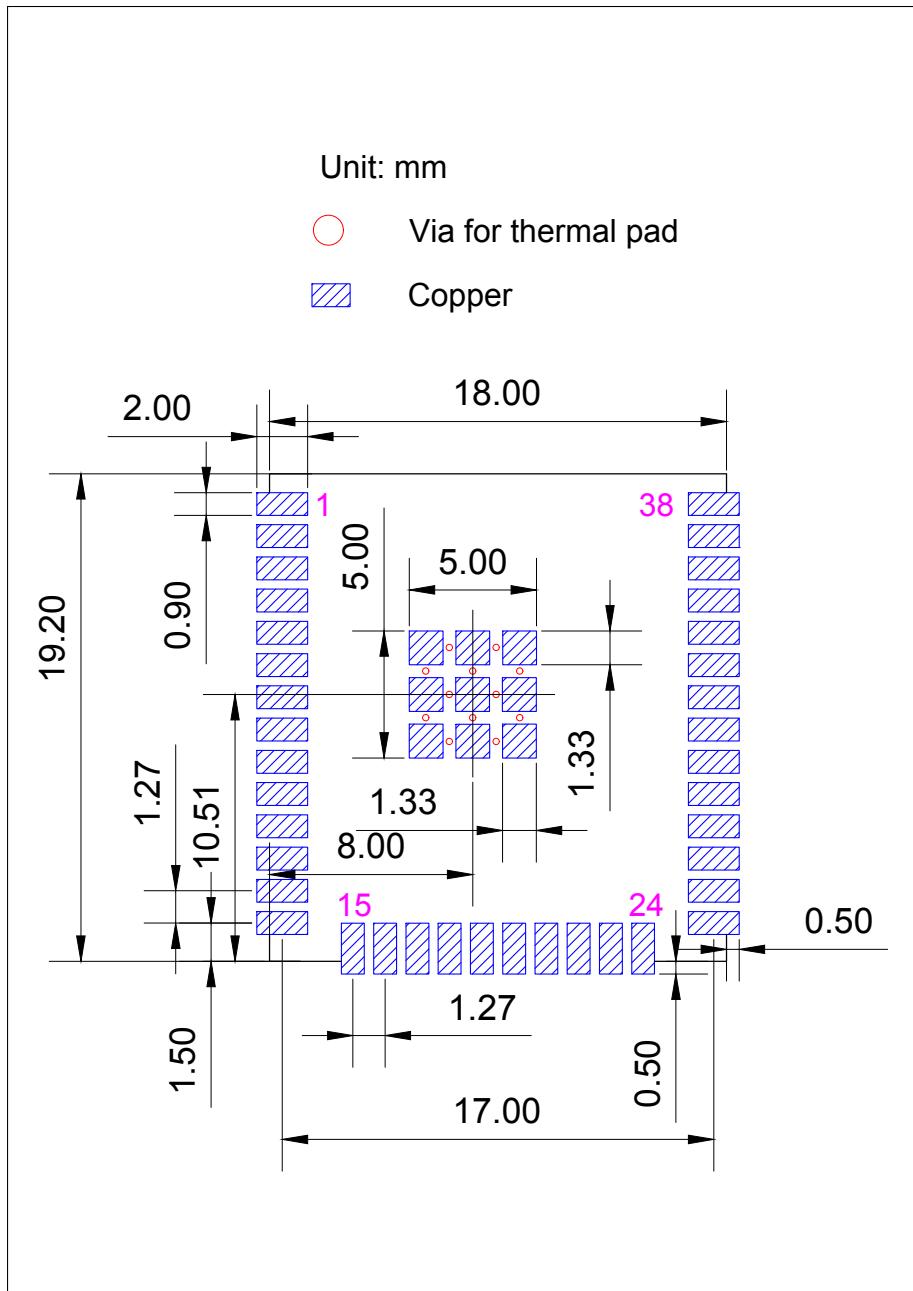


Figure 9: Recommended PCB Land Pattern of ESP32-WROOM-32U

10. U.FL Connector Dimensions

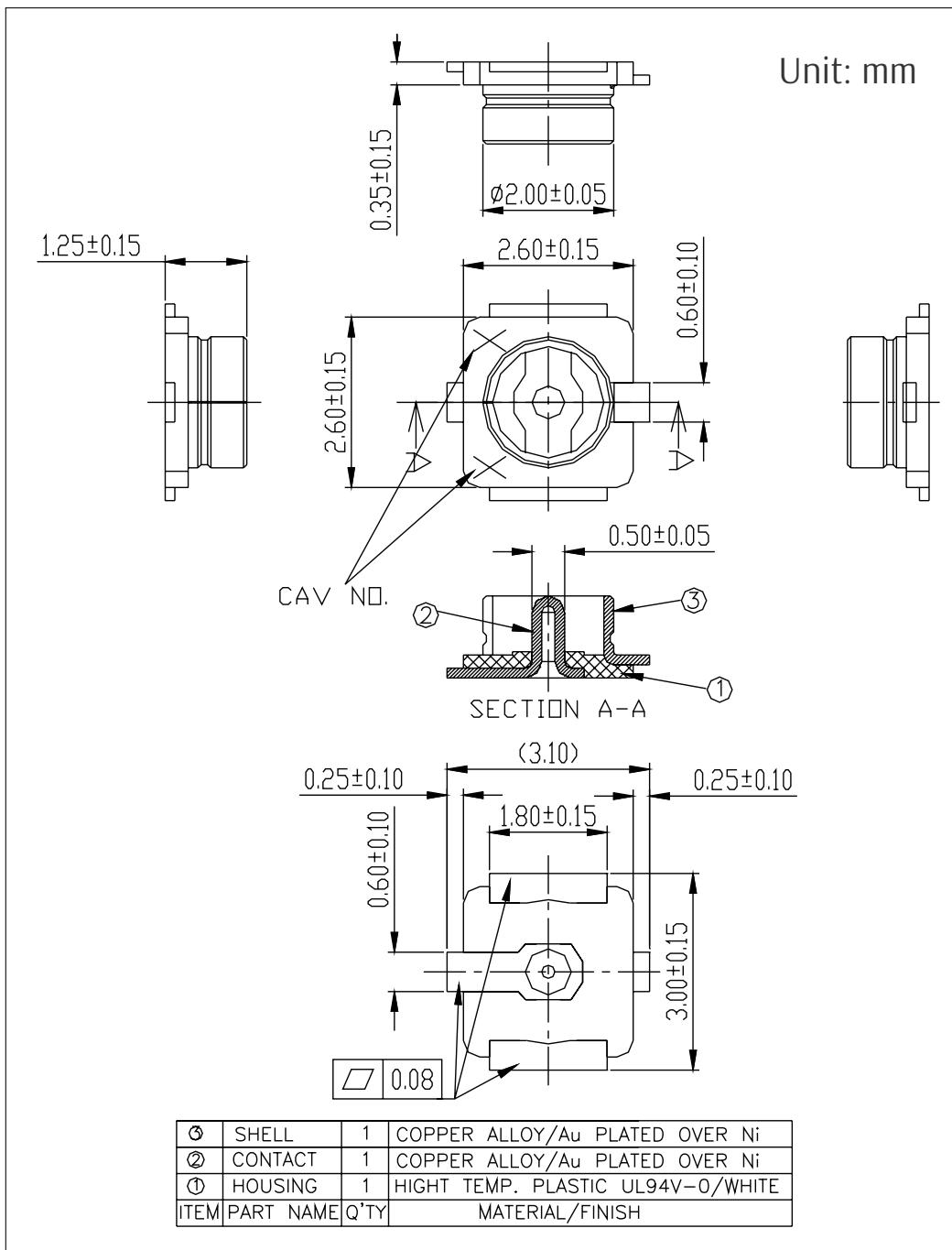


Figure 10: ESP32-WROOM-32U U.FL Dimensions

11. Learning Resources

11.1 Must-Read Documents

The following link provides documents related to ESP32.

- [ESP32 Datasheet](#)

This document provides an introduction to the specifications of the ESP32 hardware, including overview, pin definitions, functional description, peripheral interface, electrical characteristics, etc.

- [ESP-IDF Programming Guide](#)

It hosts extensive documentation for ESP-IDF ranging from hardware guides to API reference.

- [ESP32 Technical Reference Manual](#)

The manual provides detailed information on how to use the ESP32 memory and peripherals.

- [ESP32 Hardware Resources](#)

The zip files include the schematics, PCB layout, Gerber and BOM list of ESP32 modules and development boards.

- [ESP32 Hardware Design Guidelines](#)

The guidelines outline recommended design practices when developing standalone or add-on systems based on the ESP32 series of products, including the ESP32 chip, the ESP32 modules and development boards.

- [ESP32 AT Instruction Set and Examples](#)

This document introduces the ESP32 AT commands, explains how to use them, and provides examples of several common AT commands.

- [Espressif Products Ordering Information](#)

11.2 Must-Have Resources

Here are the ESP32-related must-have resources.

- [ESP32 BBS](#)

This is an Engineer-to-Engineer (E2E) Community for ESP32 where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

- [ESP32 GitHub](#)

ESP32 development projects are freely distributed under Espressif's MIT license on GitHub. It is established to help developers get started with ESP32 and foster innovation and the growth of general knowledge about the hardware and software surrounding ESP32 devices.

- [ESP32 Tools](#)

This is a webpage where users can download ESP32 Flash Download Tools and the zip file "ESP32 Certification and Test".

- [ESP-IDF](#)

This webpage links users to the official IoT development framework for ESP32.

- [ESP32 Resources](#)

This webpage provides the links to all available ESP32 documents, SDK and tools.

Revision History

Date	Version	Release notes
2019.09	V1.9	<ul style="list-style-type: none"> Changed the supply voltage range from 2.7 V ~ 3.6 V to 3.0 V ~ 3.6 V; Added Moisture sensitivity level (MSL) 3 in Table 2 <i>ESP32-WROOM-32D and ESP32-WROOM-32U Specifications</i>; Added notes about "Operating frequency range" and "TX power" under Table 8 <i>Wi-Fi Radio Characteristics</i>; Updated Section 7 <i>Peripheral Schematics</i> and added a note about RC delay circuit under it; Updated Figure 8 and Figure 9 <i>Recommended PCB Land Pattern</i>.
2019.01	V1.8	Changed the RF power control range in Table 10 from -12 ~ +12 to -12 ~ +9 dBm.
2018.10	V1.7	<p>Added notice on module custom options under Table 2;</p> <p>Added "Cumulative IO output current" entry to Table 5: Absolute Maximum Ratings;</p> <p>Added more parameters to Table 7: DC Characteristics.</p>
2018.09	V1.6	Updated the hole diameter in the shield from 1.00 mm to 0.50 mm, in Figure 6.
2018.08	V1.5	<ul style="list-style-type: none"> Added certifications and reliability test items the module has passed in Table 2: <i>ESP32-WROOM-32D and ESP32-WROOM-32U Specifications</i>, and removed software-specific information; Updated section 3.4: RTC and Low-Power Management; Changed the modules' dimensions; Updated Figure 8 and 7: Physical Dimensions; Updated Table 8: Wi-Fi Radio.
2018.06	V1.4	<ul style="list-style-type: none"> Deleted Temperature Sensor in Table 2: <i>ESP32-WROOM-32D & ESP32-WROOM-32U Specifications</i>; Updated Chapter 3: Functional Description; Added notes to Chapter 7: Peripheral Schematics; Added Chapter 8: Recommended PCB Land Pattern; <p>Changes to electrical characteristics:</p> <ul style="list-style-type: none"> Updated Table 5: Absolute Maximum Ratings; Added Table 6: Recommended Operating Conditions; Added Table 7: DC Characteristics; Updated the values of "Gain control step", "Adjacent channel transmit power" in Table 10: Transmitter Characteristics - BLE.
2018.04	V1.3	Updated Figure 4 <i>ESP32-WROOM-32U Schematics</i> and Figure 3 <i>ESP32-WROOM-32D Schematics</i> .
2018.02	V1.2	Update Figure 4 <i>ESP32-WROOM-32U Schematics</i> .
2018.02	V1.1	<p>Updated Chapter 6 Schematics.</p> <p>Deleted description of low-noise amplifier.</p> <p>Replaced the module name <i>ESP-WROOM-32D</i> with <i>ESP32-WROOM-32D</i>.</p> <p>Added information about module certification in Table 2.</p> <p>Updated the description of eFuse bits in Section 3.1.</p>
2017.11	V1.0	First release.

TECHNICAL DATA

MQ-2 GAS SENSOR

FEATURES

Wide detecting scope
Stable and long life

Fast response and High sensitivity
Simple drive circuit

APPLICATION

They are used in gas leakage detecting equipments in family and industry, are suitable for detecting of LPG, i-butane, propane, methane ,alcohol, Hydrogen, smoke.

SPECIFICATIONS

A. Standard work condition

Symbol	Parameter name	Technical condition	Remarks
V _c	Circuit voltage	5V±0.1	AC OR DC
V _H	Heating voltage	5V±0.1	ACOR DC
R _L	Load resistance	can adjust	
R _H	Heater resistance	33 Ω ±5%	Room Tem
P _H	Heating consumption	less than 800mw	

B. Environment condition

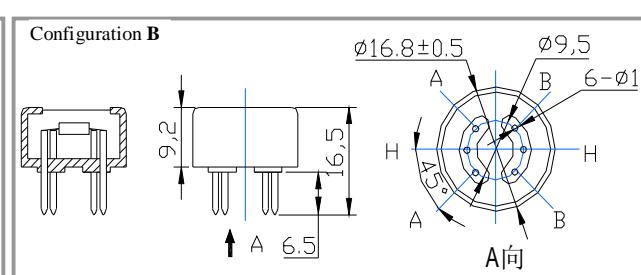
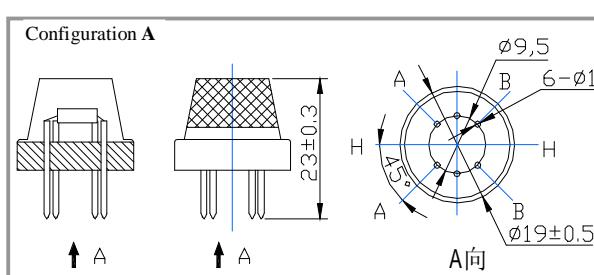
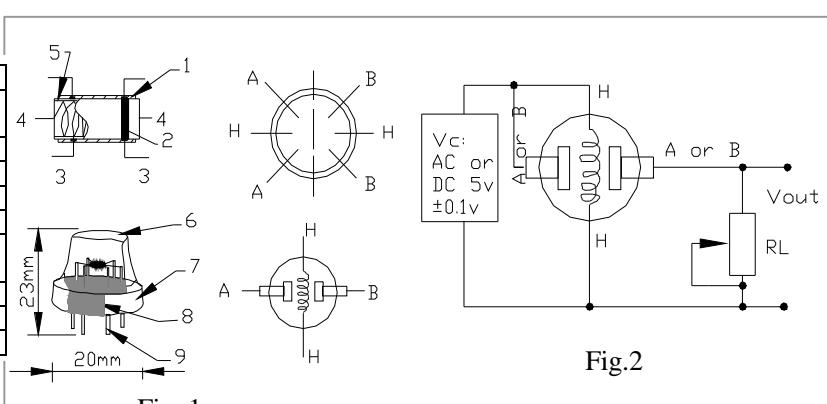
Symbol	Parameter name	Technical condition	Remarks
T _{ao}	Using Tem	-20°C-50°C	
T _{as}	Storage Tem	-20°C-70°C	
R _H	Related humidity	less than 95% Rh	
O ₂	Oxygen concentration	21%(standard condition)Oxygen concentration can affect sensitivity	minimum value is over 2%

C. Sensitivity characteristic

Symbol	Parameter name	Technical parameter	Remarks
R _s	Sensing Resistance	3K Ω -30K Ω (1000ppm iso-butane)	Detecting concentration scope: 200ppm-5000ppm LPG and propane 300ppm-5000ppm butane 5000ppm-20000ppm methane 300ppm-5000ppm H ₂ 100ppm-2000ppm Alcohol
a (3000/1000) isobutane	Concentration Slope rate	≤0.6	
Standard Detecting Condition	Temp: 20°C ±2°C Humidity: 65%±5%	V _c :5V±0.1 V _h : 5V±0.1	
Preheat time	Over 24 hour		

D. Structure and configuration, basic measuring circuit

Parts	Materials
1 Gas sensing layer	SnO ₂
2 Electrode	Au
3 Electrode line	Pt
4 Heater coil	Ni-Cr alloy
5 Tubular ceramic	Al ₂ O ₃
6 Anti-explosion network	Stainless steel gauze (SUS316 100-mesh)
7 Clamp ring	Copper plating Ni
8 Resin base	Bakelite
9 Tube Pin	Copper plating Ni



Structure and configuration of MQ-2 gas sensor is shown as Fig. 1 (Configuration A or B), sensor composed by micro AL₂O₃ ceramic tube, Tin Dioxide (SnO₂) sensitive layer, measuring electrode and heater are fixed into a

crust made by plastic and stainless steel net. The heater provides necessary work conditions for work of sensitive components. The enveloped MQ-2 have 6 pin ,4 of them are used to fetch signals, and other 2 are used for providing heating current.

Electric parameter measurement circuit is shown as Fig.2

E. Sensitivity characteristic curve

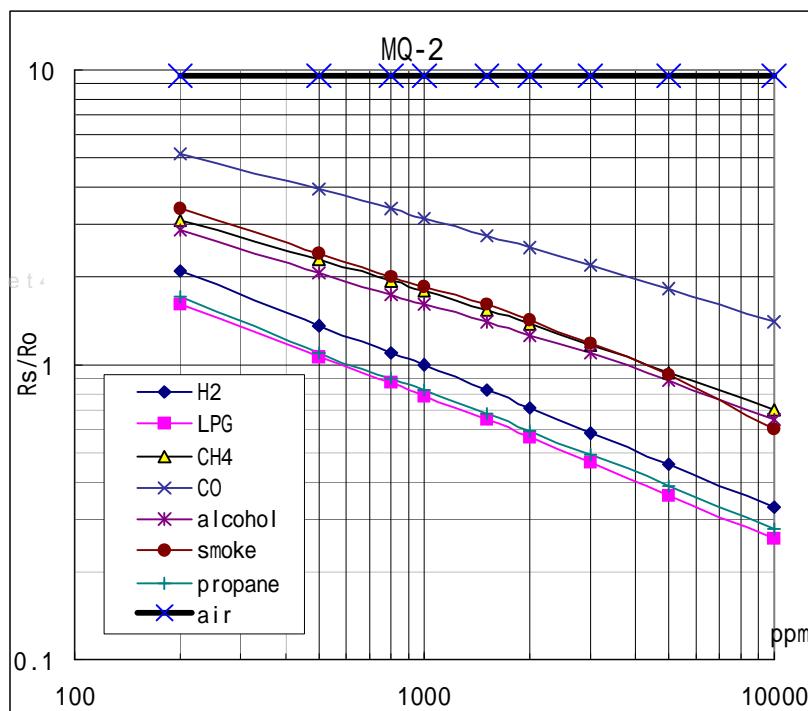


Fig.2 sensitivity characteristics of the MQ-2

Fig.3 is shows the typical sensitivity characteristics of the MQ-2 for several gases.

in their: Temp: 20°C、

Humidity: 65%、

O₂ concentration 21%

RL=5k Ω

Ro: sensor resistance at 1000ppm of H₂ in the clean air.

Rs: sensor resistance at various concentrations of gases.

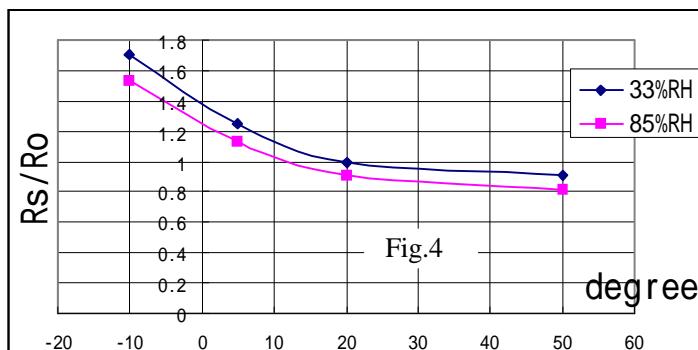


Fig.4 is shows the typical dependence of the MQ-2 on temperature and humidity.

Ro: sensor resistance at 1000ppm of H₂ in air at 33%RH and 20 degree.

Rs: sensor resistance at 1000ppm of H₂ at different temperatures and humidities.

SENSITVITY ADJUSTMENT

Resistance value of MQ-2 is difference to various kinds and various concentration gases. So, When using this components, sensitivity adjustment is very necessary. we recommend that you calibrate the detector for 1000ppm liquified petroleum gas<LPG>,or 1000ppm iso-butane<i-C₄H₁₀>concentration in air and use value of Load resistance that(R_L) about 20 K Ω (5K Ω to 47 K Ω).

When accurately measuring, the proper alarm point for the gas detector should be determined after considering the temperature and humidity influence.

SONGLE RELAY



RELAY ISO9002

SRD



1. MAIN FEATURES

- Switching capacity available by 10A in spite of small size design for high density P.C. board mounting technique.
- UL,CUL,TUV recognized.
- Selection of plastic material for high temperature and better chemical solution performance.
- Sealed types available.
- Simple relay magnetic circuit to meet low cost of mass production.

2. APPLICATIONS

- Domestic appliance, office machine, audio, equipment, automobile, etc.
(Remote control TV receiver, monitor display, audio equipment high rushing current use application.)

3. ORDERING INFORMATION

SRD	XX VDC	S	L	C
Model of relay	Nominal coil voltage	Structure	Coil sensitivity	Contact form
SRD	03、05、06、09、12、24、48VDC	S:Sealed type	L:0.36W	A:1 form A
		F:Flux free type	D:0.45W	B:1 form B C:1 form C

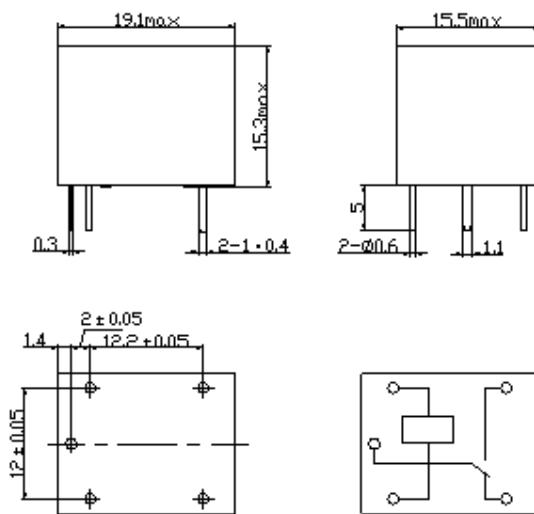
4. RATING

CCC	FILE NUMBER:CH0052885-2000	7A/240VDC
CCC	FILE NUMBER:CH0036746-99	10A/250VDC
UL/CUL	FILE NUMBER: E167996	10A/125VAC 28VDC
TUV	FILE NUMBER: R9933789	10A/240VAC 28VDC

5. DIMENSION (unit:mm)

DRILLING (unit:mm)

WIRING DIAGRAM



6. COIL DATA CHART (AT20°C)

Coil Sensitivity	Coil Voltage Code	Nominal Voltage (VDC)	Nominal Current (mA)	Coil Resistance (Ω) $\pm 10\%$	Power Consumption (W)	Pull-In Voltage (VDC)	Drop-Out Voltage (VDC)	Max-Allowable Voltage (VDC)
SRD (High Sensitivity)	03	03	120	25	abt. 0.36W	75% Max.	10% Min.	120%
	05	05	71.4	70				
	06	06	60	100				
	09	09	40	225				
	12	12	30	400				
	24	24	15	1600				
	48	48	7.5	6400				
SRD (Standard)	03	03	150	20	abt. 0.45W	75% Max.	10% Min.	110%
	05	05	89.3	55				
	06	06	75	80				
	09	09	50	180				
	12	12	37.5	320				
	24	24	18.7	1280				
	48	48	10	4500		abt. 0.51W		

7. CONTACT RATING

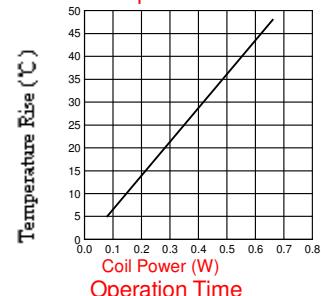
Item	Type	SRD	
	FORM C	FORM A	
Contact Capacity Resistive Load ($\cos\Phi=1$)	7A 28VDC 10A 125VAC 7A 240VAC	10A 28VDC 10A 240VAC	
Inductive Load ($\cos\Phi=0.4$ L/R=7msec)	3A 120VAC 3A 28VDC	5A 120VAC 5A 28VDC	
Max. Allowable Voltage	250VAC/110VDC	250VAC/110VDC	
Max. Allowable Power Force	800VAC/240W	1200VA/300W	
Contact Material	AgCdO	AgCdO	

8. PERFORMANCE (at initial value)

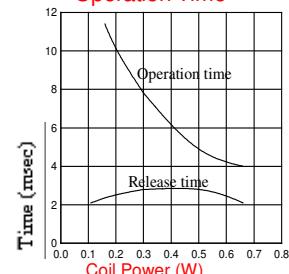
Item	Type	SRD	
	SRD	SRD	SRD
Contact Resistance	100m Ω Max.		
Operation Time	10msec Max.		
Release Time	5msec Max.		
Dielectric Strength Between coil & contact	1500VAC 50/60HZ (1 minute)		
Between contacts	1000VAC 50/60HZ (1 minute)		
Insulation Resistance	100 M Ω Min. (500VDC)		
Max. ON/OFF Switching			
Mechanically	300 operation/min		
Electrically	30 operation/min		
Ambient Temperature	-25°C to +70°C		
Operating Humidity	45 to 85% RH		
Vibration			
Endurance	10 to 55Hz Double Amplitude 1.5mm		
Error Operation	10 to 55Hz Double Amplitude 1.5mm		
Shock			
Endurance	100G Min.		
Error Operation	10G Min.		
Life Expectancy			
Mechanically	10^7 operations. Min. (no load)		
Electrically	10^5 operations. Min. (at rated coil voltage)		
Weight	abt. 10grs.		

9. REFERENCE DATA

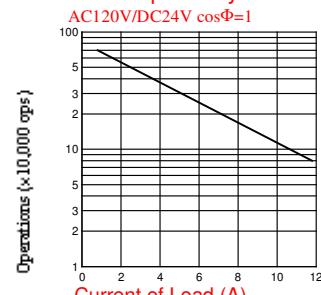
Coil Temperature Rise



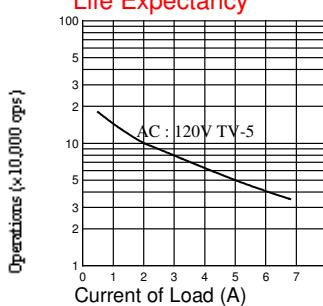
Coil Power (W) Operation Time



Release time Operation time



Life Expectancy AC 120V/DC24V cosΦ=1



ESP32 Series

Datasheet

Including:

ESP32-D0WD-V3

ESP32-D0WDR2-V3

ESP32-U4WDH

ESP32-S0WD – [Not Recommended for New Designs \(NRND\)](#)

ESP32-D0WD – [Not Recommended for New Designs \(NRND\)](#)

ESP32-D0WDQ6 – [Not Recommended for New Designs \(NRND\)](#)

ESP32-D0WDQ6-V3 – [Not Recommended for New Designs \(NRND\)](#)



Version 4.2
Espressif Systems
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About This Document

This document provides the specifications of ESP32 series of chips.

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Please always refer to the latest version on <https://www.espressif.com/en/support/download/documents>.

Revision History

For any changes to this document over time, please refer to the [last page](#).

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1 Overview

ESP32 is a single 2.4 GHz Wi-Fi-and-Bluetooth combo chip designed with the TSMC low-power 40 nm technology. It is designed to achieve the best power and RF performance, showing robustness, versatility and reliability in a wide variety of applications and power scenarios.

The ESP32 series of chips includes ESP32-D0WD-V3, ESP32-D0WDR2-V3, ESP32-U4WDH, ESP32-S0WD ([NRND](#)), ESP32-D0WDQ6-V3 ([NRND](#)), ESP32-D0WD ([NRND](#)), and ESP32-D0WDQ6 ([NRND](#)), among which,

- ESP32-S0WD ([NRND](#)), ESP32-D0WD ([NRND](#)), and ESP32-D0WDQ6 ([NRND](#)) are based on chip revision v1 or chip revision v1.1.
- ESP32-D0WD-V3, ESP32-D0WDR2-V3, ESP32-U4WDH, and ESP32-D0WDQ6-V3 ([NRND](#)) are based on chip revision v3.0 or chip revision v3.1.

For details on part numbers and ordering information, please refer to Section 7. For details on chip revisions, please refer to [ESP32 Chip Revision v3.0 User Guide](#) and [ESP32 Series SoC Errata](#).

1.1 Featured Solutions

1.1.1 Ultra-Low-Power Solution

ESP32 is designed for mobile, wearable electronics, and Internet-of-Things (IoT) applications. It features all the state-of-the-art characteristics of low-power chips, including fine-grained clock gating, multiple power modes, and dynamic power scaling. For instance, in a low-power IoT sensor hub application scenario, ESP32 is woken up periodically only when a specified condition is detected. Low-duty cycle is used to minimize the amount of energy that the chip expends. The output of the power amplifier is also adjustable, thus contributing to an optimal trade-off between communication range, data rate and power consumption.

Note:

For more information, refer to Section 3.7 *RTC and Low-Power Management*.

1.1.2 Complete Integration Solution

ESP32 is a highly-integrated solution for Wi-Fi-and-Bluetooth IoT applications, with around 20 external components. ESP32 integrates an antenna switch, RF balun, power amplifier, low-noise receive amplifier, filters, and power management modules. As such, the entire solution occupies minimal Printed Circuit Board (PCB) area.

ESP32 uses CMOS for single-chip fully-integrated radio and baseband, while also integrating advanced calibration circuitries that allow the solution to remove external circuit imperfections or adjust to changes in external conditions. As such, the mass production of ESP32 solutions does not require expensive and specialized Wi-Fi testing equipment.

1.2 Wi-Fi Key Features

- 802.11b/g/n

- 802.11n (2.4 GHz), up to 150 Mbps
- WMM
- TX/RX A-MPDU, RX A-MSDU
- Immediate Block ACK
- Defragmentation
- Automatic Beacon monitoring (hardware TSF)
- 4 × virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure Station, SoftAP, and Promiscuous modes
Note that when ESP32 is in Station mode, performing a scan, the SoftAP channel will be changed.
- Antenna diversity

1.3 Bluetooth Key Features

- Compliant with Bluetooth v4.2 BR/EDR and Bluetooth LE specifications
- Class-1, class-2 and class-3 transmitter without external power amplifier
- Enhanced Power Control
- +9 dBm transmitting power
- NZIF receiver with -94 dBm Bluetooth LE sensitivity
- Adaptive Frequency Hopping (AFH)
- Standard HCI based on SDIO/SPI/UART
- High-speed UART HCI, up to 4 Mbps
- Bluetooth 4.2 BR/EDR and Bluetooth LE dual mode controller
- Synchronous Connection-Oriented/Extended (SCO/eSCO)
- CVSD and SBC for audio codec
- Bluetooth Piconet and Scatternet
- Multi-connections in Classic Bluetooth and Bluetooth LE
- Simultaneous advertising and scanning

1.4 MCU and Advanced Features

1.4.1 CPU and Memory

- Xtensa® single-/dual-core 32-bit LX6 microprocessor(s)
- CoreMark® score:
 - 1 core at 240 MHz: 504.85 CoreMark; 2.10 CoreMark/MHz
 - 2 cores at 240 MHz: 994.26 CoreMark; 4.14 CoreMark/MHz
- 448 KB ROM

- 520 KB SRAM
- 16 KB SRAM in RTC
- QSPI supports multiple flash/SRAM chips

1.4.2 Clocks and Timers

- Internal 8 MHz oscillator with calibration
- Internal RC oscillator with calibration
- External 2 MHz ~ 60 MHz crystal oscillator (40 MHz only for Wi-Fi/Bluetooth functionality)
- External 32 kHz crystal oscillator for RTC with calibration
- Two timer groups, including 2 × 64-bit timers and 1 × main watchdog in each group
- One RTC timer
- RTC watchdog

1.4.3 Advanced Peripheral Interfaces

- 34 × programmable GPIOs
- 12-bit SAR ADC up to 18 channels
- 2 × 8-bit DAC
- 10 × touch sensors
- 4 × SPI
- 2 × I₂S
- 2 × I₂C
- 3 × UART
- 1 host (SD/eMMC/SDIO)
- 1 slave (SDIO/SPI)
- Ethernet MAC interface with dedicated DMA and IEEE 1588 support
- TWAI[®], compatible with ISO 11898-1 (CAN Specification 2.0)
- RMT (TX/RX)
- Motor PWM
- LED PWM up to 16 channels

1.4.4 Security

- Secure boot
- Flash encryption
- 1024-bit OTP, up to 768-bit for customers
- Cryptographic hardware acceleration:

- AES
- Hash (SHA-2)
- RSA
- ECC
- Random Number Generator (RNG)

1.5 Applications (A Non-exhaustive List)

- Generic Low-power IoT Sensor Hub
 - Agriculture robotics
- Generic Low-power IoT Data Loggers
 - Audio Applications
- Cameras for Video Streaming
 - Internet music players
- Over-the-top (OTT) Devices
 - Live streaming devices
- Speech Recognition
 - Internet radio players
- Image Recognition
 - Audio headsets
- Mesh Network
- Home Automation
 - Light control
 - Smart plugs
 - Smart door locks
- Smart Building
 - Smart lighting
 - Energy monitoring
- Industrial Automation
 - Industrial wireless control
 - Industrial robotics
- Smart Agriculture
 - Smart greenhouses
 - Smart irrigation
- Health Care Applications
 - Health monitoring
 - Baby monitors
- Wi-Fi-enabled Toys
 - Remote control toys
 - Proximity sensing toys
 - Educational toys
- Wearable Electronics
 - Smart watches
 - Smart bracelets
- Retail & Catering Applications
 - POS machines
 - Service robots

1.6 Block Diagram

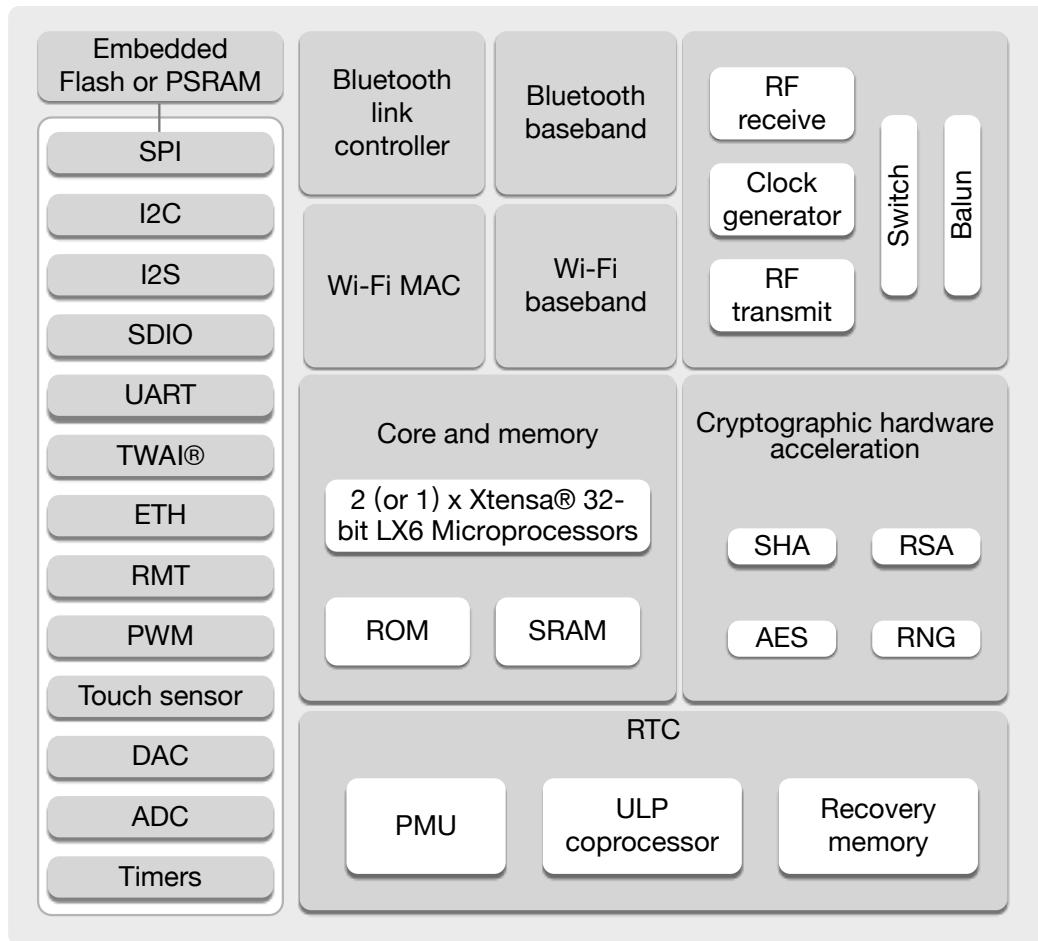


Figure 1: Functional Block Diagram

Note:

Products in the ESP32 series differ from each other in terms of their support for embedded flash or PSRAM and the number of CPUs they have. For details, please refer to Section [7 Part Number and Ordering Information](#).

2 Pin Definitions

2.1 Pin Layout

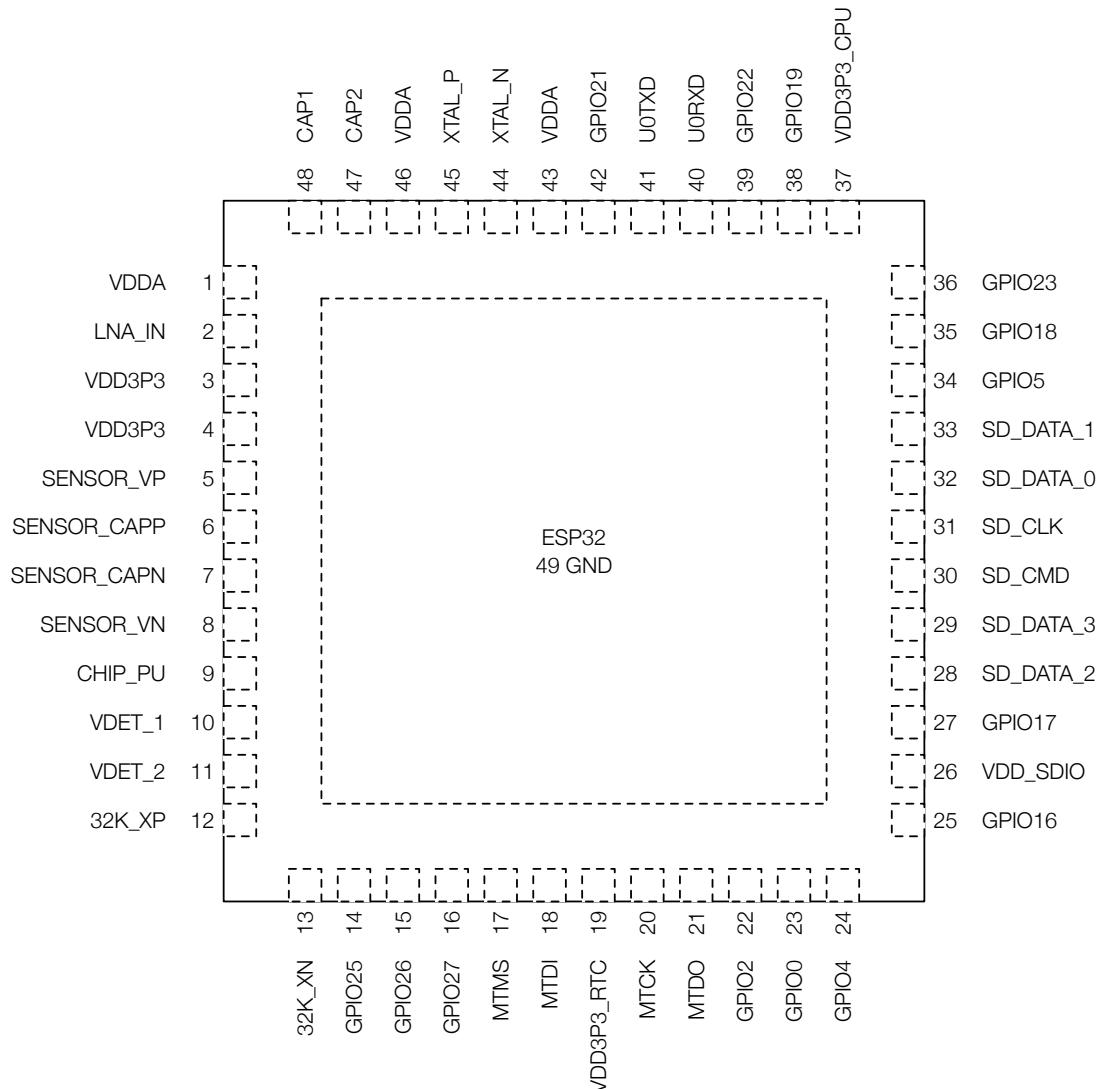


Figure 2: ESP32 Pin Layout (QFN 6*6, Top View)

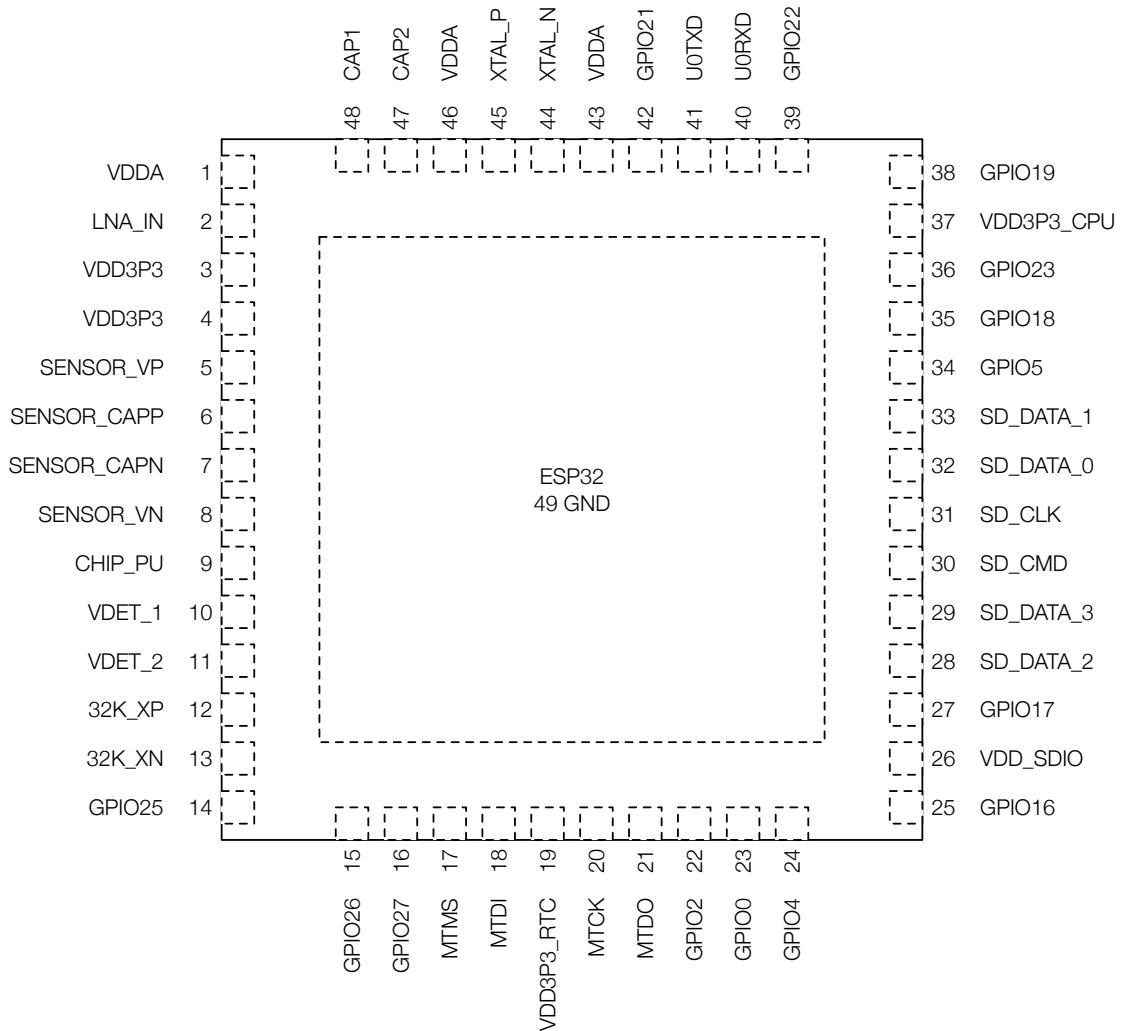


Figure 3: ESP32 Pin Layout (QFN 5*5, Top View)

Note:

For details on ESP32's part numbers and the corresponding packaging, please refer to Section [7 Part Number and Ordering Information](#).

2.2 Pin Description

Table 1: Pin Description

Name	No.	Type	Function
Analog			
VDDA	1	P	Analog power supply (2.3 V ~ 3.6 V)
LNA_IN	2	I/O	RF input and output
VDD3P3	3	P	Analog power supply (2.3 V ~ 3.6 V)
VDD3P3	4	P	Analog power supply (2.3 V ~ 3.6 V)
VDD3P3_RTC			
SENSOR_VP	5	I	GPIO36, ADC1_CH0, RTC_GPIO0
SENSOR_CAPP	6	I	GPIO37, ADC1_CH1, RTC_GPIO1
SENSOR_CAPN	7	I	GPIO38, ADC1_CH2, RTC_GPIO2
SENSOR_VN	8	I	GPIO39, ADC1_CH3, RTC_GPIO3
CHIP_PU	9	I	High: On; enables the chip Low: Off; the chip powers off Note: Do not leave the CHIP_PU pin floating.
VDET_1	10	I	GPIO34, ADC1_CH6, RTC_GPIO4
VDET_2	11	I	GPIO35, ADC1_CH7, RTC_GPIO5
32K_XP	12	I/O	GPIO32, ADC1_CH4, RTC_GPIO9, TOUCH9, 32K_XP (32.768 kHz crystal oscillator input)
32K_XN	13	I/O	GPIO33, ADC1_CH5, RTC_GPIO8, TOUCH8, 32K_XN (32.768 kHz crystal oscillator output)
GPIO25	14	I/O	GPIO25, ADC2_CH8, RTC_GPIO6, DAC_1, EMAC_RXD0
GPIO26	15	I/O	GPIO26, ADC2_CH9, RTC_GPIO7, DAC_2, EMAC_RXD1
GPIO27	16	I/O	GPIO27, ADC2_CH7, RTC_GPIO17, TOUCH7, EMAC_RX_DV
MTMS	17	I/O	GPIO14, ADC2_CH6, RTC_GPIO16, TOUCH6, EMAC_TXD2, HSPICLK, SD_CLK, MTMS
MTDI	18	I/O	GPIO12, ADC2_CH5, RTC_GPIO15, TOUCH5, EMAC_TXD3, HSPIQ, HS2_DATA2, SD_DATA2, MTDI
VDD3P3_RTC	19	P	Input power supply for RTC IO (2.3 V ~ 3.6 V)
MTCK	20	I/O	GPIO13, ADC2_CH4, RTC_GPIO14, TOUCH4, EMAC_RX_ER, HSPID, HS2_DATA3, SD_DATA3, MTCK
MTDO	21	I/O	GPIO15, ADC2_CH3, RTC_GPIO13, TOUCH3, EMAC_RXD3, HSPICS0, HS2_CMD, SD_CMD, MTDO

Name	No.	Type	Function			
GPIO2	22	I/O	GPIO2, ADC2_CH2, RTC_GPIO12, TOUCH2,		HSPIWP, HS2_DATA0, SD_DATA0	
GPIO0	23	I/O	GPIO0, ADC2_CH1, RTC_GPIO11, TOUCH1,	EMAC_TX_CLK, CLK_OUT1,		
GPIO4	24	I/O	GPIO4, ADC2_CH0, RTC_GPIO10, TOUCH0,	EMAC_TX_ER, HSPIHD, HS2_DATA1, SD_DATA1		VDD_SDIO
GPIO16	25	I/O	GPIO16, HS1_DATA4, U2RXD,	EMAC_CLK_OUT		
VDD_SDIO	26	P	Output power supply: 1.8 V or the same voltage as VDD3P3_RTC			
GPIO17	27	I/O	GPIO17, HS1_DATA5, U2TXD,	EMAC_CLK_OUT_180		
SD_DATA_2	28	I/O	GPIO9, HS1_DATA2, U1RXD,	SD_DATA2, SPIHD		
SD_DATA_3	29	I/O	GPIO10, HS1_DATA3, U1TXD,	SD_DATA3, SPIWP		
SD_CMD	30	I/O	GPIO11, HS1_CMD, U1RTS,	SD_CMD, SPICS0		
SD_CLK	31	I/O	GPIO6, HS1_CLK, U1CTS,	SD_CLK, SPICLK		
SD_DATA_0	32	I/O	GPIO7, HS1_DATA0, U2RTS,	SD_DATA0, SPIQ		
SD_DATA_1	33	I/O	GPIO8, HS1_DATA1, U2CTS,	SD_DATA1, SPID		VDD3P3_CPU
GPIO5	34	I/O	GPIO5, HS1_DATA6, VSPICS0,	EMAC_RX_CLK		
GPIO18	35	I/O	GPIO18, HS1_DATA7, VSPICLK			
GPIO23	36	I/O	GPIO23, HS1_STROBE, VSPIID			
VDD3P3_CPU	37	P	Input power supply for CPU IO (1.8 V ~ 3.6 V)			
GPIO19	38	I/O	GPIO19, U0CTS,	VSPIQ, EMAC_TXD0		
GPIO22	39	I/O	GPIO22, U0RTS,	VSPIWP, EMAC_TXD1		
U0RXD	40	I/O	GPIO3, U0RXD,	CLK_OUT2		
U0TXD	41	I/O	GPIO1, U0TXD,	CLK_OUT3, EMAC_RXD2		
GPIO21	42	I/O	GPIO21,	VSPIHD, EMAC_TX_EN		Analog
VDDA	43	P	Analog power supply (2.3 V ~ 3.6 V)			
XTAL_N	44	O	External crystal output			
XTAL_P	45	I	External crystal input			
VDDA	46	P	Analog power supply (2.3 V ~ 3.6 V)			
CAP2	47	I	Connects to a 3.3 nF (10%) capacitor and 20 kΩ resistor in parallel to CAP1			

Name	No.	Type	Function
CAP1	48	I	Connects to a 10 nF series capacitor to ground
GND	49	P	Ground

Note:

For a quick reference guide to using the IO_MUX, Ethernet MAC, and GPIO Matrix pins of ESP32, please refer to Appendix [ESP32 Pin Lists](#).

Table 2 lists the pin-to-pin mapping between the chip and the embedded flash/PSRAM. The chip pins listed here are not recommended for other usage. For the data port connection between ESP32 and external flash/PSRAM please refer to Table 3.

Table 2: Pin-to-Pin Mapping Between Chip and Embedded Flash/PSRAM

ESP32-U4WDH	Embedded Flash (4 MB)
SD_DATA_1	IO0/DI
GPIO17	IO1/DO
SD_DATA_0	IO2/WP#
SD_CMD	IO3/HOLD#
SD_CLK	CLK
GPIO16	CS#
GND	VSS
VDD_SDIO	VDD
ESP32-D0WDR2-V3	Embedded PSRAM (2 MB)
SD_DATA_1	SIO0/SI
SD_DATA_0	SIO1/SO
SD_DATA_3	SIO2
SD_DATA_2	SIO3
SD_CLK	SCLK
GPIO16*	CE#
GND	VSS
VDD_SDIO	VDD

Table 3: Connection Between Chip and External Flash/PSRAM

Chip Pin	External Flash
SD_DATA_1/SPIID	IO0/DI
SD_DATA_0/SPIQ	IO1/DO
SD_DATA_3/SPIWP	IO2/WP#
SD_DATA_2/SPIHD	IO3/HOLD#
SD_CLK	CLK
SD_CMD	CS#
GND	VSS
VDD_SDIO	VDD
Chip Pin	External PSRAM
SD_DATA_1	SIO0/SI
SD_DATA_0	SIO1/SO
SD_DATA_3	SIO2
SD_DATA_2	SIO3
SD_CLK/GPIO17*	SCLK
GPIO16*	CE#
GND	VSS
VDD_SDIO	VDD

Note:

1. SD_CLK and GPIO17 pins are available to connect to the SCLK signal of external PSRAM.
 - If SD_CLK pin is selected, one GPIO (i.e., GPIO17) will be saved. The saved GPIO can be used for other purposes. This connection has passed internal tests, but relevant certification has not been completed.
 - Or GPIO17 pin is used to connect to the SCLK signal. This connection has passed relevant certification, see certificates for [ESP32-WROVER-E](#).Please select the proper pin for your specific applications.
2. If GPIO16 is used to connect to PSRAM's CE# signal, please add a pull-up resistor at the GPIO16 pin. See Figure: [Schematics of ESP32-WROVER-E](#).
3. As the embedded flash/PSRAM in ESP32-U4WDH/ESP32-D0WDR2-V3 operates at 3.3 V, VDD_SDIO must be powered by VDD3P3_RTC via a $6\ \Omega$ resistor. See Figure 4.

2.3 Power Scheme

ESP32's digital pins are divided into three different power domains:

- VDD3P3_RTC
- VDD3P3_CPU
- VDD_SDIO

VDD3P3_RTC is also the input power supply for RTC and CPU.

VDD3P3_CPU is also the input power supply for CPU.

VDD_SDIO connects to the output of an internal LDO whose input is VDD3P3_RTC. When VDD_SDIO is connected to the same PCB net together with VDD3P3_RTC, the internal LDO is disabled automatically. The power scheme diagram is shown below:

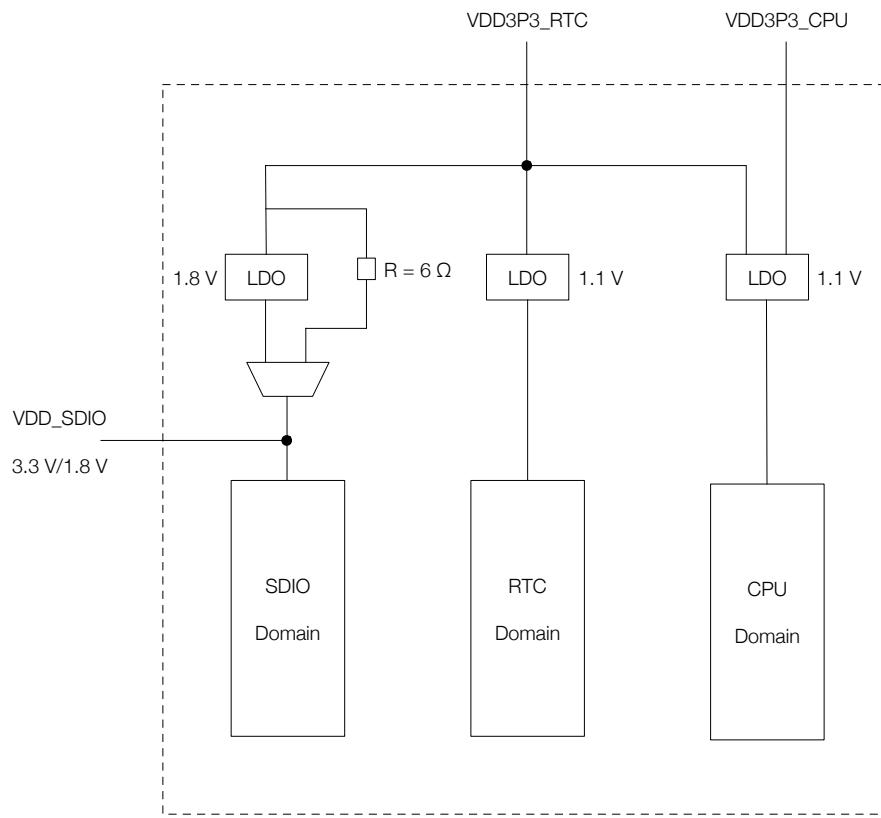


Figure 4: ESP32 Power Scheme

The internal LDO can be configured as having 1.8 V, or the same voltage as VDD3P3_RTC. It can be powered off via software to minimize the current of flash/SRAM during the Deep-sleep mode.

Notes on CHIP_PU:

- The illustration below shows the ESP32 power-up and reset timing. Details about the parameters are listed in Table 4.

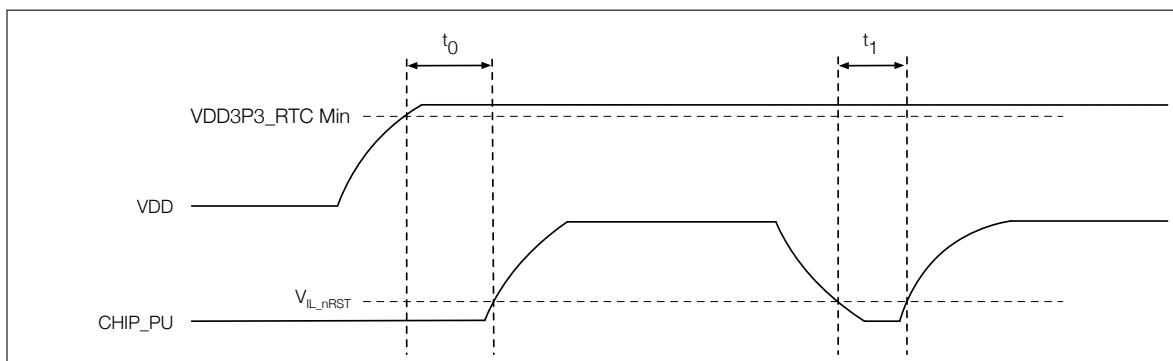


Figure 5: ESP32 Power-up and Reset Timing

Table 4: Description of ESP32 Power-up and Reset Timing Parameters

Parameters	Description	Min.	Unit
t_0	Time between the 3.3 V rails being brought up and CHIP_PU being activated	50	μs

Parameters	Description	Min.	Unit
t_1	Duration of CHIP_PU signal level $< V_{IL_nRST}$ (refer to its value in Table 15 DC Characteristics) to reset the chip	50	μs

- In scenarios where ESP32 is powered on and off repeatedly by switching the power rails, while there is a large capacitor on the VDD33 rail and CHIP_PU and VDD33 are connected, simply switching off the CHIP_PU power rail and immediately switching it back on may cause an incomplete power discharge cycle and failure to reset the chip adequately.
An additional discharge circuit may be required to accelerate the discharge of the large capacitor on rail VDD33, which will ensure proper power-on-reset when the ESP32 is powered up again.
- When a battery is used as the power supply for the ESP32 series of chips and modules, a supply voltage supervisor is recommended, so that a boot failure due to low voltage is avoided. Users are recommended to pull CHIP_PU low if the power supply for ESP32 is below 2.3 V.

Notes on power supply:

- The operating voltage of ESP32 ranges from 2.3 V to 3.6 V. When using a single-power supply, the recommended voltage of the power supply is 3.3 V, and its recommended output current is 500 mA or more.
- PSRAM and flash both are powered by VDD_SDIO. If the chip has an embedded flash, the voltage of VDD_SDIO is determined by the operating voltage of the embedded flash. If the chip also connects to an external PSRAM, the operating voltage of external PSRAM must match that of the embedded flash. This also applies if the chip has an embedded PSRAM but also connects to an external flash.
- When VDD_SDIO 1.8 V is used as the power supply for external flash/PSRAM, a $2 \text{ k}\Omega$ grounding resistor should be added to VDD_SDIO. For the circuit design, please refer to Figure **ESP32-WROVER Schematics**, in [ESP32-WROVER Datasheet](#).
- When the three digital power supplies are used to drive peripherals, e.g., 3.3 V flash, they should comply with the peripherals' specifications.

2.4 Strapping Pins

There are five strapping pins:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the values of these five bits from register "GPIO_STRAPPING".

During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on the chip.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 5 for a detailed boot-mode configuration by strapping pins.

Table 5: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3 V	1.8 V		
MTDI	Pull-down	0	1		
Booting Mode					
Pin	Default	SPI Boot	Download Boot		
GPIO0	Pull-up	1	0		
GPIO2	Pull-down	Don't-care	0		
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
Pin	Default	U0TXD Active	U0TXD Silent		
MTDO	Pull-up	1	0		
Timing of SDIO Slave					
Pin	Default	FE Sampling FE Output	FE Sampling RE Output	RE Sampling FE Output	RE Sampling RE Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Note:

- FE: falling-edge, RE: rising-edge.
- Firmware can configure register bits to change the settings of “Voltage of Internal LDO (VDD_SDIO)” and “Timing of SDIO Slave”, after booting.
- For ESP32 chips that contain an embedded flash or PSRAM, users need to note the logic level of MTDI. For example, ESP32-U4WDH contains an embedded flash that operates at 3.3 V, therefore, the MTDI should be low.

The illustration below shows the setup and hold times for the strapping pins before and after the CHIP_PU signal goes high. Details about the parameters are listed in Table 6.

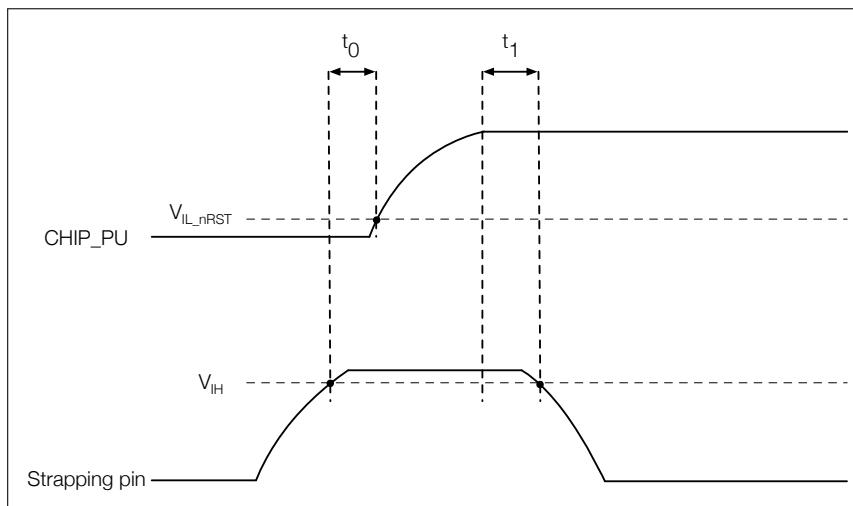


Figure 6: Setup and Hold Times for the Strapping Pins

Table 6: Parameter Descriptions of Setup and Hold Times for the Strapping Pins

Parameters	Description	Min.	Unit
t_0	Setup time before CHIP_PU goes from low to high	0	ms
t_1	Hold time after CHIP_PU goes high	1	ms

3 Functional Description

This chapter describes the functions integrated in ESP32.

3.1 CPU and Memory

3.1.1 CPU

ESP32 contains one or two low-power Xtensa® 32-bit LX6 microprocessor(s) with the following features:

- 7-stage pipeline to support the clock frequency of up to 240 MHz (160 MHz for ESP32-S0WD ([NRND](#)))
- 16/24-bit Instruction Set provides high code-density
- Support for Floating Point Unit
- Support for DSP instructions, such as a 32-bit multiplier, a 32-bit divider, and a 40-bit MAC
- Support for 32 interrupt vectors from about 70 interrupt sources

The single-/dual-CPU interfaces include:

- Xtensa RAM/ROM Interface for instructions and data
- Xtensa Local Memory Interface for fast peripheral register access
- External and internal interrupt sources
- JTAG for debugging

For information about the Xtensa® Instruction Set Architecture, please refer to [Xtensa® Instruction Set Architecture \(ISA\) Summary](#).

3.1.2 Internal Memory

ESP32's internal memory includes:

- 448 KB of ROM for booting and core functions
- 520 KB of on-chip SRAM for data and instructions
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the ULP coprocessor during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash-encryption and chip-ID.
- Embedded flash or PSRAM

Note:

Products in the ESP32 series differ from each other, in terms of their support for embedded flash or PSRAM and the size of them. For details, please refer to Section [7 Part Number and Ordering Information](#).

3.1.3 External Flash and SRAM

ESP32 supports multiple external QSPI flash and SRAM chips. More details can be found in Chapter SPI in the [ESP32 Technical Reference Manual](#). ESP32 also supports hardware encryption/decryption based on AES to protect developers' programs and data in flash.

ESP32 can access the external QSPI flash and SRAM through high-speed caches.

- Up to 16 MB of external flash can be mapped into CPU instruction memory space and read-only memory space simultaneously.
 - When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU.
 - When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads are supported.
- External SRAM can be mapped into CPU data memory space. SRAM up to 8 MB is supported and up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads and writes are supported.

Note:

After ESP32 is initialized, firmware can customize the mapping of external SRAM or flash into the CPU address space.

3.1.4 Memory Map

The structure of address mapping is shown in Figure 7. The memory and peripheral mapping of ESP32 is shown in Table 7.

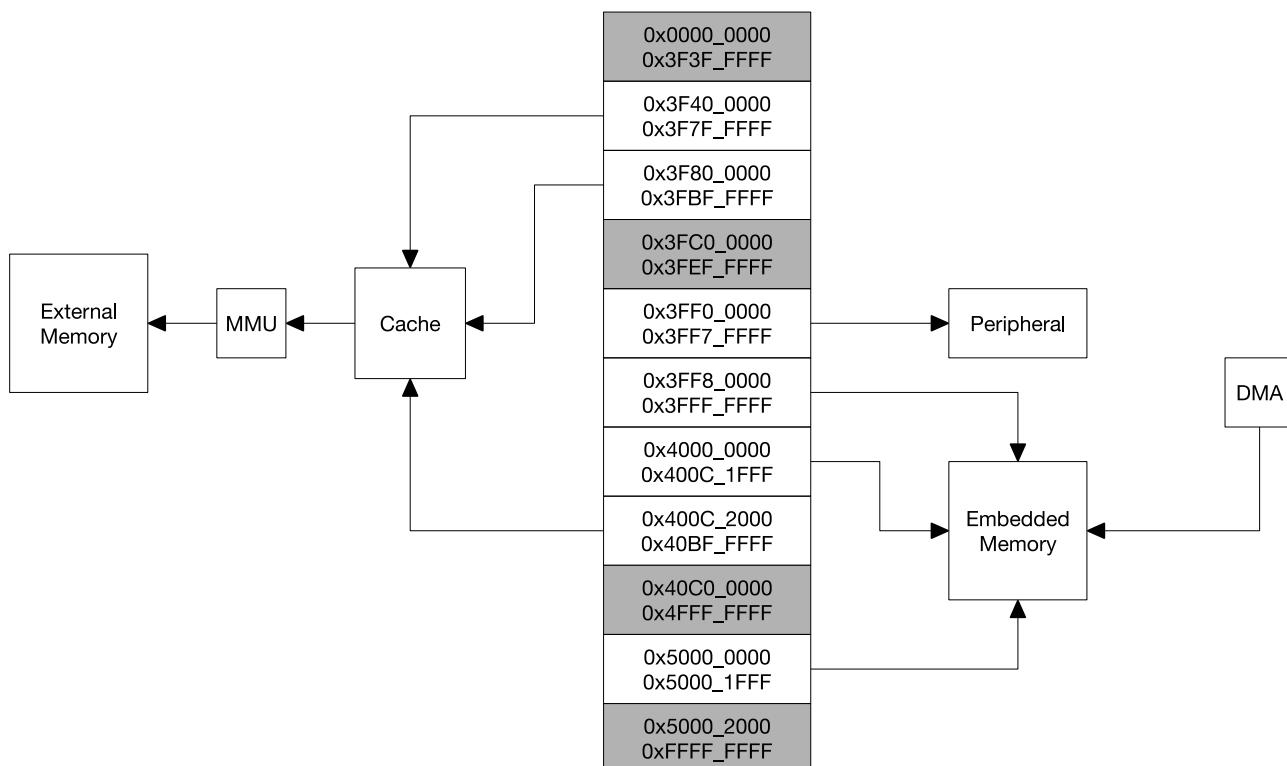


Figure 7: Address Mapping Structure

Table 7: Memory and Peripheral Mapping

Category	Target	Start Address	End Address	Size
Embedded Memory	Internal ROM 0	0x4000_0000	0x4005_FFFF	384 KB
	Internal ROM 1	0x3FF9_0000	0x3FF9_FFFF	64 KB
	Internal SRAM 0	0x4007_0000	0x4009_FFFF	192 KB
	Internal SRAM 1	0x3FFE_0000	0x3FFF_FFFF	128 KB
		0x400A_0000	0x400B_FFFF	
	Internal SRAM 2	0x3FFA_E000	0x3FFD_FFFF	200 KB
	RTC FAST Memory	0x3FF8_0000	0x3FF8_1FFF	8 KB
		0x400C_0000	0x400C_1FFF	
External Memory	RTC SLOW Memory	0x5000_0000	0x5000_1FFF	8 KB
	External Flash	0x3F40_0000	0x3F7F_FFFF	4 MB
		0x400C_2000	0x40BF_FFFF	11 MB+248 KB
Peripheral	External RAM	0x3F80_0000	0x3FBF_FFFF	4 MB
	DPort Register	0x3FF0_0000	0x3FF0_0FFF	4 KB
	AES Accelerator	0x3FF0_1000	0x3FF0_1FFF	4 KB
	RSA Accelerator	0x3FF0_2000	0x3FF0_2FFF	4 KB
	SHA Accelerator	0x3FF0_3000	0x3FF0_3FFF	4 KB
	Secure Boot	0x3FF0_4000	0x3FF0_4FFF	4 KB
	Cache MMU Table	0x3FF1_0000	0x3FF1_3FFF	16 KB
	PID Controller	0x3FF1_F000	0x3FF1_FFFF	4 KB
	UART0	0x3FF4_0000	0x3FF4_0FFF	4 KB
	SPI1	0x3FF4_2000	0x3FF4_2FFF	4 KB
	SPI0	0x3FF4_3000	0x3FF4_3FFF	4 KB
	GPIO	0x3FF4_4000	0x3FF4_4FFF	4 KB
	RTC	0x3FF4_8000	0x3FF4_8FFF	4 KB
	IO MUX	0x3FF4_9000	0x3FF4_9FFF	4 KB
	SDIO Slave	0x3FF4_B000	0x3FF4_BFFF	4 KB
	UDMA1	0x3FF4_C000	0x3FF4_CFFF	4 KB
	I2S0	0x3FF4_F000	0x3FF4_FFFF	4 KB
	UART1	0x3FF5_0000	0x3FF5_0FFF	4 KB
	I2C0	0x3FF5_3000	0x3FF5_3FFF	4 KB
	UDMA0	0x3FF5_4000	0x3FF5_4FFF	4 KB
	SDIO Slave	0x3FF5_5000	0x3FF5_5FFF	4 KB
	RMT	0x3FF5_6000	0x3FF5_6FFF	4 KB
	PCNT	0x3FF5_7000	0x3FF5_7FFF	4 KB
	SDIO Slave	0x3FF5_8000	0x3FF5_8FFF	4 KB
	LED PWM	0x3FF5_9000	0x3FF5_9FFF	4 KB
	eFuse Controller	0x3FF5_A000	0x3FF5_AFFF	4 KB
	Flash Encryption	0x3FF5_B000	0x3FF5_BFFF	4 KB
	PWM0	0x3FF5_E000	0x3FF5_EFFF	4 KB
	TIMG0	0x3FF5_F000	0x3FF5_FFFF	4 KB
	TIMG1	0x3FF6_0000	0x3FF6_0FFF	4 KB
	SPI2	0x3FF6_4000	0x3FF6_4FFF	4 KB
	SPI3	0x3FF6_5000	0x3FF6_5FFF	4 KB

Category	Target	Start Address	End Address	Size
Peripheral	SYSCON	0x3FF6_6000	0x3FF6_6FFF	4 KB
	I2C1	0x3FF6_7000	0x3FF6_7FFF	4 KB
	SDMMC	0x3FF6_8000	0x3FF6_8FFF	4 KB
	EMAC	0x3FF6_9000	0x3FF6_AFFF	8 KB
	TWAI	0x3FF6_B000	0x3FF6_BFFF	4 KB
	PWM1	0x3FF6_C000	0x3FF6_CFFF	4 KB
	I2S1	0x3FF6_D000	0x3FF6_DFFF	4 KB
	UART2	0x3FF6_E000	0x3FF6_EFFF	4 KB
	PWM2	0x3FF6_F000	0x3FF6_FFFF	4 KB
	PWM3	0x3FF7_0000	0x3FF7_0FFF	4 KB
	RNG	0x3FF7_5000	0x3FF7_5FFF	4 KB

3.2 Timers and Watchdogs

3.2.1 64-bit Timers

There are four general-purpose timers embedded in the chip. They are all 64-bit generic timers which are based on 16-bit prescalers and 64-bit auto-reload-capable up/down-timers.

The timers feature:

- A 16-bit clock prescaler, from 2 to 65536
- A 64-bit timer
- Configurable up/down timer: incrementing or decrementing
- Halt and resume of time-base counter
- Auto-reload at alarming
- Software-controlled instant reload
- Level and edge interrupt generation

For detailed information, please refer to Chapter [Timer Group \(TIMG\)](#) in *ESP32 Technical Reference Manual*.

3.2.2 Watchdog Timers

The chip has three watchdog timers: one in each of the two timer modules (called the Main Watchdog Timer, or MWDT) and one in the RTC module (called the RTC Watchdog Timer, or RWDT). These watchdog timers are intended to recover from an unforeseen fault causing the application program to abandon its normal sequence. A watchdog timer has four stages. Each stage may trigger one of three or four possible actions upon the expiry of its programmed time period, unless the watchdog is fed or disabled. The actions are: interrupt, CPU reset, core reset, and system reset. Only the RWDT can trigger the system reset, and is able to reset the entire chip, including the RTC itself. A timeout value can be set for each stage individually.

During flash boot the RWDT and the first MWDT start automatically in order to detect, and recover from, booting problems.

The watchdogs have the following features:

- Four stages, each of which can be configured or disabled separately
- A programmable time period for each stage
- One of three or four possible actions (interrupt, CPU reset, core reset, and system reset) upon the expiry of each stage
- 32-bit expiry counter
- Write protection that prevents the RWDT and MWDT configuration from being inadvertently altered
- SPI flash boot protection
 - If the boot process from an SPI flash does not complete within a predetermined time period, the watchdog will reboot the entire system.

For detailed information, please refer to Chapter [Watchdog Timers \(WDT\)](#) in *ESP32 Technical Reference Manual*.

3.3 System Clocks

3.3.1 CPU Clock

Upon reset, an external crystal clock source is selected as the default CPU clock. The external crystal clock source also connects to a PLL to generate a high-frequency clock (typically 160 MHz).

In addition, ESP32 has an internal 8 MHz oscillator. The application can select the clock source from the external crystal clock source, the PLL clock or the internal 8 MHz oscillator. The selected clock source drives the CPU clock directly, or after division, depending on the application.

3.3.2 RTC Clock

The RTC clock has five possible sources:

- external low-speed (32 kHz) crystal clock
- external crystal clock divided by 4
- internal RC oscillator (typically about 150 kHz, and adjustable)
- internal 8 MHz oscillator
- internal 31.25 kHz clock (derived from the internal 8 MHz oscillator divided by 256)

When the chip is in the normal power mode and needs faster CPU accessing, the application can choose the external high-speed crystal clock divided by 4 or the internal 8 MHz oscillator. When the chip operates in the low-power mode, the application chooses the external low-speed (32 kHz) crystal clock, the internal RC clock or the internal 31.25 kHz clock.

3.3.3 Audio PLL Clock

The audio clock is generated by the ultra-low-noise fractional-N PLL. For detailed information, please refer to Chapter [Reset and Clock](#) in *ESP32 Technical Reference Manual*.

3.4 Radio

The radio module consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch
- clock generator

3.4.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits and baseband filters are integrated in the chip.

3.4.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered Complementary Metal Oxide Semiconductor (CMOS) power amplifier. The use of digital calibration further improves the linearity of the power amplifier, enabling state-of-the-art performance in delivering up to +20.5 dBm of power for an 802.11b transmission and +18 dBm for an 802.11n transmission. Additional calibrations are integrated to cancel any radio imperfections, such as:

- Carrier leakage
- I/Q phase matching
- Baseband nonlinearities
- RF nonlinearities
- Antenna matching

These built-in calibration routines reduce the amount of time required for product testing, and render the testing equipment unnecessary.

3.4.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including all inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

3.5 Wi-Fi

ESP32 implements a TCP/IP and full 802.11 b/g/n Wi-Fi MAC protocol. It supports the Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF). Power management is handled with minimal host interaction to minimize the active-duty period.

3.5.1 Wi-Fi Radio and Baseband

The ESP32 Wi-Fi Radio and Baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 in both 20 MHz and 40 MHz bandwidth
- 802.11n MCS32 (RX)
- 802.11n 0.4 μ s guard-interval
- up to 150 Mbps of data rate
- Receiving STBC 2x1
- Up to 20.5 dBm of transmitting power
- Adjustable transmitting power
- Antenna diversity

ESP32 supports antenna diversity with an external RF switch. One or more GPIOs control the RF switch and selects the best antenna to minimize the effects of channel fading.

3.5.2 Wi-Fi MAC

The ESP32 Wi-Fi MAC applies low-level protocol functions automatically. They are as follows:

- 4 x virtual Wi-Fi interfaces
- Simultaneous Infrastructure BSS Station mode/SoftAP mode/Promiscuous mode
- RTS protection, CTS protection, Immediate Block ACK
- Defragmentation
- TX/RX A-MPDU, RX A-MSDU
- TXOP
- WMM
- CCMP (CBC-MAC, counter mode), TKIP (MIC, RC4), WAPI (SMS4), WEP (RC4) and CRC
- Automatic beacon monitoring (hardware TSF)

3.6 Bluetooth

The chip integrates a Bluetooth link controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packet processing, bit stream processing, frequency hopping, etc.

3.6.1 Bluetooth Radio and Baseband

The Bluetooth Radio and Baseband support the following features:

- Class-1, class-2 and class-3 transmit output powers, and a dynamic control range of up to 21 dB
- $\pi/4$ DQPSK and 8 DPSK modulation

- High performance in NZIF receiver sensitivity with a minimum sensitivity of -94 dBm
- Class-1 operation without external PA
- Internal SRAM allows full-speed data-transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- ACL, SCO, eSCO, and AFH
- A-law, μ -law, and CVSD digital audio CODEC in PCM interface
- SBC audio CODEC
- Power management for low-power applications
- SMP with 128-bit AES

3.6.2 Bluetooth Interface

- Provides UART HCI interface, up to 4 Mbps
- Provides SDIO/SPI HCI interface
- Provides PCM/I2S audio interface

3.6.3 Bluetooth Stack

The Bluetooth stack of the chip is compliant with the Bluetooth v4.2 BR/EDR and Bluetooth LE specifications.

3.6.4 Bluetooth Link Controller

The link controller operates in three major states: standby, connection and sniff. It enables multiple connections, and other operations, such as inquiry, page, and secure simple-pairing, and therefore enables Piconet and Scatternet. Below are the features:

- Classic Bluetooth
 - Device Discovery (inquiry, and inquiry scan)
 - Connection establishment (page, and page scan)
 - Multi-connections
 - Asynchronous data reception and transmission
 - Synchronous links (SCO/eSCO)
 - Master/Slave Switch
 - Adaptive Frequency Hopping and Channel assessment
 - Broadcast encryption
 - Authentication and encryption
 - Secure Simple-Pairing
 - Multi-point and scatternet management

- Sniff mode
- Connectionless Slave Broadcast (transmitter and receiver)
- Enhanced power control
- Ping
- Bluetooth Low Energy
 - Advertising
 - Scanning
 - Simultaneous advertising and scanning
 - Multiple connections
 - Asynchronous data reception and transmission
 - Adaptive Frequency Hopping and Channel assessment
 - Connection parameter update
 - Data Length Extension
 - Link Layer Encryption
 - LE Ping

3.7 RTC and Low-Power Management

With the use of advanced power-management technologies, ESP32 can switch between different power modes.

- Power modes
 - **Active mode:** The chip radio is powered on. The chip can receive, transmit, or listen.
 - **Modem-sleep mode:** The CPU is operational and the clock is configurable. The Wi-Fi/Bluetooth baseband and radio are disabled.
 - **Light-sleep mode:** The CPU is paused. The RTC memory and RTC peripherals, as well as the ULP coprocessor are running. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip.
 - **Deep-sleep mode:** Only the RTC memory and RTC peripherals are powered on. Wi-Fi and Bluetooth connection data are stored in the RTC memory. The ULP coprocessor is functional.
 - **Hibernation mode:** The internal 8 MHz oscillator and ULP coprocessor are disabled. The RTC recovery memory is powered down. Only one RTC timer on the slow clock and certain RTC GPIOs are active. The RTC timer or the RTC GPIOs can wake up the chip from the Hibernation mode.

Table 8: Power Consumption by Power Modes

Power mode	Description	Power Consumption
Active (RF working)	Wi-Fi Tx packet	Please refer to Table 17 for details.
	Wi-Fi/BT Tx packet	
	Wi-Fi/BT Rx and listening	

Power mode	Description			Power Consumption	
Modem-sleep	The CPU is powered on.	* 240 MHz	Dual-core chip(s)	30 mA ~ 68 mA	
			Single-core chip(s)	N/A	
		* 160 MHz	Dual-core chip(s)	27 mA ~ 44 mA	
			Single-core chip(s)	27 mA ~ 34 mA	
		Normal speed: 80 MHz	Dual-core chip(s)	20 mA ~ 31 mA	
			Single-core chip(s)	20 mA ~ 25 mA	
Light-sleep	-			0.8 mA	
Deep-sleep	The ULP coprocessor is powered on.			150 μ A	
	ULP sensor-monitored pattern			100 μ A @1% duty	
	RTC timer + RTC memory			10 μ A	
Hibernation	RTC timer only			5 μ A	
Power off	CHIP_PU is set to low level, the chip is powered off.			1 μ A	

Note:

- * Among the ESP32 series of SoCs, ESP32-D0WD-V3, ESP32-D0WDR2-V3, ESP32-U4WDH, ESP32-D0WD ([NRND](#)), ESP32-D0WDQ6 ([NRND](#)), and ESP32-D0WDQ6-V3 ([NRND](#)) have a maximum CPU frequency of 240 MHz, ESP32-S0WD ([NRND](#)) has a maximum CPU frequency of 160 MHz.
- When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, power consumption changes accordingly.
- In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.
- During Deep-sleep, when the ULP coprocessor is powered on, peripherals such as GPIO and RTC I2C are able to operate.
- When the system works in the ULP sensor-monitored pattern, the ULP coprocessor works with the ULP sensor periodically and the ADC works with a duty cycle of 1%, so the power consumption is 100 μ A.

4 Peripherals and Sensors

4.1 Descriptions of Peripherals and Sensors

4.1.1 General Purpose Input/Output Interface (GPIO)

ESP32 has 34 GPIO pins which can be assigned various functions by programming the appropriate registers. There are several kinds of GPIOs: digital-only, analog-enabled, capacitive-touch-enabled, etc. Analog-enabled GPIOs and Capacitive-touch-enabled GPIOs can be configured as digital GPIOs.

Most of the digital GPIOs can be configured as internal pull-up or pull-down, or set to high impedance. When configured as an input, the input value can be read through the register. The input can also be set to edge-trigger or level-trigger to generate CPU interrupts. Most of the digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the SDIO, UART, SPI, etc. (More details can be found in the Appendix, Table [IO_MUX](#).) For low-power operations, the GPIOs can be set to hold their states.

For more information, please refer to Chapter [IO MUX and GPIO Matrix \(GPIO, IO MUX\)](#) in *ESP32 Technical Reference Manual*.

4.1.2 Analog-to-Digital Converter (ADC)

ESP32 integrates two 12-bit SAR ADCs and supports measurements on 18 channels (analog-enabled pins). The ULP coprocessor in ESP32 is also designed to measure voltage, while operating in the sleep mode, which enables low-power consumption. The CPU can be woken up by a threshold setting and/or via other triggers.

With appropriate settings, the ADCs can be configured to measure voltage on 18 pins maximum.

Table 9 describes the ADC characteristics.

Table 9: ADC Characteristics

Parameter	Description	Min	Max	Unit
DNL (Differential nonlinearity)	RTC controller; ADC connected to an external 100 nF capacitor; DC signal input; ambient temperature at 25 °C; Wi-Fi&Bluetooth off	-7	7	LSB
INL (Integral nonlinearity)		-12	12	LSB
Sampling rate	RTC controller	-	200	kspS
	DIG controller	-	2	MspS

Notes:

- When atten = 3 and the measurement result is above 3000 (voltage at approx. 2450 mV), the ADC accuracy will be worse than described in the table above.
- To get better DNL results, users can take multiple sampling tests with a filter, or calculate the average value.
- The input voltage range of GPIO pins within VDD3P3_RTC domain should strictly follow the DC characteristics provided in Table 15. Otherwise, measurement errors may be introduced, and chip performance may be affected.

By default, there are ±6% differences in measured results between chips. ESP-IDF provides couple of [calibration](#)

[methods](#) for ADC1. Results after calibration using eFuse Vref value are shown in Table 10. For higher accuracy, users may apply other calibration methods provided in ESP-IDF, or implement their own.

Table 10: ADC Calibration Results

Parameter	Description	Min	Max	Unit
Total error	Atten = 0, effective measurement range of 100 ~ 950 mV	-23	23	mV
	Atten = 1, effective measurement range of 100 ~ 1250 mV	-30	30	mV
	Atten = 2, effective measurement range of 150 ~ 1750 mV	-40	40	mV
	Atten = 3, effective measurement range of 150 ~ 2450 mV	-60	60	mV

For more information, please refer to Chapter [On-Chip Sensors and Analog Signal Processing](#) in *ESP32 Technical Reference Manual*.

4.1.3 Digital-to-Analog Converter (DAC)

Two 8-bit DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and a buffer. This dual DAC supports power supply as input voltage reference. The two DAC channels can also support independent conversions.

For more information, please refer to Chapter [On-Chip Sensors and Analog Signal Processing](#) in *ESP32 Technical Reference Manual*.

4.1.4 Touch Sensor

ESP32 has 10 capacitive-sensing GPIOs, which detect variations induced by touching or approaching the GPIOs with a finger or other objects. The low-noise nature of the design and the high sensitivity of the circuit allow relatively small pads to be used. Arrays of pads can also be used, so that a larger area or more points can be detected. The 10 capacitive-sensing GPIOs are listed in Table 11.

Table 11: Capacitive-Sensing GPIOs Available on ESP32

Capacitive-Sensing Signal Name	Pin Name
T0	GPIO4
T1	GPIO0
T2	GPIO2
T3	MTDO
T4	MTCK
T5	MTDI
T6	MTMS
T7	GPIO27
T8	32K_XN
T9	32K_XP

For more information, please refer to Chapter [On-Chip Sensors and Analog Signal Processing](#) in *ESP32 Technical Reference Manual*.

Note:

ESP32 Touch Sensor has not passed the Conducted Susceptibility (CS) test for now, and thus has limited application scenarios.

4.1.5 Ultra-Low-Power (ULP) Coprocessor

The ULP coprocessor and RTC memory remain powered on during the Deep-sleep mode. Hence, the developer can store a program for the ULP coprocessor in the RTC slow memory to access the peripheral devices, internal timers and internal sensors during the Deep-sleep mode. This is useful for designing applications where the CPU needs to be woken up by an external event, or a timer, or a combination of the two, while maintaining minimal power consumption.

For more information, please refer to Chapter [ULP Coprocessor \(ULP\)](#) in *ESP32 Technical Reference Manual*.

4.1.6 Ethernet MAC Interface

An IEEE-802.3-2008-compliant Media Access Controller (MAC) is provided for Ethernet LAN communications. ESP32 requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to ESP32 through 17 signals of MII or nine signals of RMII. The following features are supported on the Ethernet MAC (EMAC) interface:

- 10 Mbps and 100 Mbps rates
- Dedicated DMA controller allowing high-speed transfer between the dedicated SRAM and Ethernet MAC
- Tagged MAC frame (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames)
- 32-bit CRC generation and removal
- Several address-filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 512 words (32-bit)
- Hardware PTP (Precision Time Protocol) in accordance with IEEE 1588 2008 (PTP V2)
- 25 MHz/50 MHz clock output

For more information, please refer to Chapter [Ethernet Media Access Controller \(MAC\)](#) in *ESP32 Technical Reference Manual*.

4.1.7 SD/SDIO/MMC Host Controller

An SD/SDIO/MMC host controller is available on ESP32, which supports the following features:

- Secure Digital memory (SD mem Version 3.0 and Version 3.01)
- Secure Digital I/O (SDIO Version 3.0)

- Consumer Electronics Advanced Transport Architecture (CE-ATA Version 1.1)
- Multimedia Cards (MMC Version 4.41, eMMC Version 4.5 and Version 4.51)

The controller allows up to 80 MHz clock output in three different data-bus modes: 1-bit, 4-bit, and 8-bit. It supports two SD/SDIO/MMC4.41 cards in a 4-bit data-bus mode. It also supports one SD card operating at 1.8 V.

For more information, please refer to Chapter [SD/MMC Host Controller](#) in *ESP32 Technical Reference Manual*.

4.1.8 SDIO/SPI Slave Controller

ESP32 integrates an SD device interface that conforms to the industry-standard SDIO Card Specification Version 2.0, and allows a host controller to access the SoC, using the SDIO bus interface and protocol. ESP32 acts as the slave on the SDIO bus. The host can access the SDIO-interface registers directly and can access shared memory via a DMA engine, thus maximizing performance without engaging the processor cores.

The SDIO/SPI slave controller supports the following features:

- SPI, 1-bit SDIO, and 4-bit SDIO transfer modes over the full clock range from 0 to 50 MHz
- Configurable sampling and driving clock edge
- Special registers for direct access by host
- Interrupts to host for initiating data transfer
- Automatic loading of SDIO bus data and automatic discarding of padding data
- Block size of up to 512 bytes
- Interrupt vectors between the host and the slave, allowing both to interrupt each other
- Supports DMA for data transfer

For more information, please refer to Chapter [SDIO Slave Controller](#) in *ESP32 Technical Reference Manual*.

4.1.9 Universal Asynchronous Receiver Transmitter (UART)

ESP32 has three UART interfaces, i.e., UART0, UART1, and UART2, which provide asynchronous communication (RS232 and RS485) and IrDA support, communicating at a speed of up to 5 Mbps. UART provides hardware management of the CTS and RTS signals and software flow control (XON and XOFF). All of the interfaces can be accessed by the DMA controller or directly by the CPU.

For more information, please refer to Chapter [UART Controller \(UART\)](#) in *ESP32 Technical Reference Manual*.

4.1.10 I2C Interface

ESP32 has two I2C bus interfaces which can serve as I2C master or slave, depending on the user's configuration. The I2C interfaces support:

- Standard mode (100 Kbit/s)
- Fast mode (400 Kbit/s)
- Up to 5 MHz, yet constrained by SDA pull-up strength

- 7-bit/10-bit addressing mode
- Dual addressing mode

Users can program command registers to control I2C interfaces, so that they have more flexibility.

For more information, please refer to Chapter [I2C Controller \(I2C\)](#) in *ESP32 Technical Reference Manual*.

4.1.11 I2S Interface

Two standard I2S interfaces are available in ESP32. They can be operated in master or slave mode, in full duplex and half-duplex communication modes, and can be configured to operate with an 8-/16-/32-/48-/64-bit resolution as input or output channels. BCK clock frequency, from 10 kHz up to 40 MHz, is supported. When one or both of the I2S interfaces are configured in the master mode, the master clock can be output to the external DAC/CODEC.

Both of the I2S interfaces have dedicated DMA controllers. PDM and BT PCM interfaces are supported.

For more information, please refer to Chapter [I2S Controller \(I2S\)](#) in *ESP32 Technical Reference Manual*.

4.1.12 Infrared Remote Controller (RMT)

The infrared remote controller supports eight channels of infrared remote transmission and receiving. By programming the pulse waveform, it supports various infrared protocols. Eight channels share a 512 x 32-bit block of memory to store the transmitting or receiving waveform.

For more information, please refer to Chapter [Remote Control Peripheral \(RMT\)](#) in *ESP32 Technical Reference Manual*.

4.1.13 Pulse Counter (PCNT)

The pulse counter captures pulse and counts pulse edges through seven modes. It has eight channels, each of which captures four signals at a time. The four input signals include two pulse signals and two control signals. When the counter reaches a defined threshold, an interrupt is generated.

For more information, please refer to Chapter [Pulse Count Controller \(PCNT\)](#) in *ESP32 Technical Reference Manual*.

4.1.14 Pulse Width Modulation (PWM)

The Pulse Width Modulation (PWM) controller can be used for driving digital motors and smart lights. The controller consists of PWM timers, the PWM operator and a dedicated capture sub-module. Each timer provides timing in synchronous or independent form, and each PWM operator generates a waveform for one PWM channel. The dedicated capture sub-module can accurately capture events with external timing.

For more information, please refer to Chapter [Motor Control PWM \(PWM\)](#) in *ESP32 Technical Reference Manual*.

4.1.15 LED PWM

The LED PWM controller can generate 16 independent channels of digital waveforms with configurable periods and duties.

The 16 channels of digital waveforms operate with an APB clock of 80 MHz. Eight of these channels have the option of using the 8 MHz oscillator clock. Each channel can select a 20-bit timer with configurable counting range, while its accuracy of duty can be up to 16 bits within a 1 ms period.

The software can change the duty immediately. Moreover, each channel automatically supports step-by-step duty increase or decrease, which is useful for the LED RGB color-gradient generator.

For more information, please refer to Chapter [LED PWM Controller \(LEDC\)](#) in *ESP32 Technical Reference Manual*.

4.1.16 Serial Peripheral Interface (SPI)

ESP32 features three SPIs (SPI, HSPI and VSPI) in slave and master modes in 1-line full-duplex and 1/2/4-line half-duplex communication modes. These SPIs also support the following general-purpose SPI features:

- Four modes of SPI transfer format, which depend on the polarity (CPOL) and the phase (CPHA) of the SPI clock
- Up to 80 MHz (The actual speed it can reach depends on the selected pads, PCB tracing, peripheral characteristics, etc.)
- up to 64-byte FIFO

All SPIs can also be connected to the external flash/SRAM and LCD. Each SPI can be served by DMA controllers.

For more information, please refer to Chapter [SPI Controller \(SPI\)](#) in *ESP32 Technical Reference Manual*.

4.1.17 TWAI Controller

ESP32 family has a TWAI® controller with the following features:

- compatible with ISO 11898-1 protocol (CAN Specification 2.0)
- standard frame format (11-bit ID) and extended frame format (29-bit ID)
- bit rates:
 - from 25 Kbit/s to 1 Mbit/s in chip revision v0.0/v1.0/v1.1
 - from 12.5 Kbit/s to 1 Mbit/s in chip revision v3.0/v3.1
- multiple modes of operation: Normal, Listen Only, and Self-Test
- 64-byte receive FIFO
- special transmissions: single-shot transmissions and self reception
- acceptance filter (single and dual filter modes)
- error detection and handling: error counters, configurable error interrupt threshold, error code capture, arbitration lost capture

For more information, please refer to Chapter [Two-wire Automotive Interface \(TWAI\)](#) in *ESP32 Technical Reference Manual*.

4.1.18 Accelerator

ESP32 is equipped with hardware accelerators of general algorithms, such as AES (FIPS PUB 197), SHA (FIPS PUB 180-4), RSA, and ECC, which support independent arithmetic, such as Big Integer Multiplication and Big Integer Modular Multiplication. The maximum operation length for RSA, ECC, Big Integer Multiply and Big Integer Modular Multiplication is 4096 bits.

The hardware accelerators greatly improve operation speed and reduce software complexity. They also support code encryption and dynamic decryption, which ensures that code in the flash will not be hacked.

4.2 Peripheral Pin Configurations

Table 12: Peripheral Pin Configurations

Interface	Signal	Pin	Function
ADC	ADC1_CH0	SENSOR_VP	Two 12-bit SAR ADCs
	ADC1_CH1	SENSOR_CAPP	
	ADC1_CH2	SENSOR_CAPN	
	ADC1_CH3	SENSOR_VN	
	ADC1_CH4	32K_XP	
	ADC1_CH5	32K_XN	
	ADC1_CH6	VDET_1	
	ADC1_CH7	VDET_2	
	ADC2_CH0	GPIO4	
	ADC2_CH1	GPIO0	
	ADC2_CH2	GPIO2	
	ADC2_CH3	MTDO	
	ADC2_CH4	MTCK	
	ADC2_CH5	MTDI	
	ADC2_CH6	MTMS	
	ADC2_CH7	GPIO27	
	ADC2_CH8	GPIO25	
	ADC2_CH9	GPIO26	
DAC	DAC_1	GPIO25	Two 8-bit DACs
	DAC_2	GPIO26	
Touch Sensor	TOUCH0	GPIO4	Capacitive touch sensors
	TOUCH1	GPIO0	
	TOUCH2	GPIO2	
	TOUCH3	MTDO	
	TOUCH4	MTCK	
	TOUCH5	MTDI	
	TOUCH6	MTMS	
	TOUCH7	GPIO27	
	TOUCH8	32K_XN	
	TOUCH9	32K_XP	
JTAG	MTDI	MTDI	JTAG for software debugging
	MTCK	MTCK	

Interface	Signal	Pin	Function
	MTMS	MTMS	
	MTDO	MTDO	

Interface	Signal	Pin	Function
SD/SDIO/MMC Host Controller	HS2_CLK	MTMS	Supports SD memory card V3.01 standard
	HS2_CMD	MTDO	
	HS2_DATA0	GPIO2	
	HS2_DATA1	GPIO4	
	HS2_DATA2	MTDI	
	HS2_DATA3	MTCK	
Motor PWM	PWM0_OUT0~2	Any GPIO Pins	Three channels of 16-bit timers generate PWM waveforms. Each channel has a pair of output signals, three fault detection signals, three event-capture signals, and three sync signals.
	PWM1_OUT_IN0~2		
	PWM0_FLT_IN0~2		
	PWM1_FLT_IN0~2		
	PWM0_CAP_IN0~2		
	PWM1_CAP_IN0~2		
	PWM0_SYNC_IN0~2		
	PWM1_SYNC_IN0~2		
SDIO/SPI Slave Controller	SD_CLK	MTMS	SDIO interface that conforms to the industry standard SDIO 2.0 card specification
	SD_CMD	MTDO	
	SD_DATA0	GPIO2	
	SD_DATA1	GPIO4	
	SD_DATA2	MTDI	
	SD_DATA3	MTCK	
UART	U0RXD_in	Any GPIO Pins	Three UART devices with hardware flow-control and DMA
	U0CTS_in		
	U0DSR_in		
	U0TXD_out		
	U0RTS_out		
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1TXD_out		
	U1RTS_out		
	U2RXD_in		
	U2CTS_in		
	U2TXD_out		
	U2RTS_out		
I2C	I2CEXT0_SCL_in	Any GPIO Pins	Two I2C devices in slave or master mode
	I2CEXT0_SDA_in		
	I2CEXT1_SCL_in		
	I2CEXT1_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
	I2CEXT1_SCL_out		
	I2CEXT1_SDA_out		
LED PWM	ledc_hs_sig_out0~7	Any GPIO Pins	16 independent channels @80 MHz clock/RTC CLK. Duty accuracy: 16 bits.
	ledc_ls_sig_out0~7		

Interface	Signal	Pin	Function
I2S	I2S0I_DATA_in0~15	Any GPIO Pins	Stereo input and output from/to the audio codec; parallel LCD data output; parallel camera data input.
	I2S0O_BCK_in		
	I2S0O_WS_in		
	I2S0I_BCK_in		
	I2S0I_WS_in		
	I2S0I_H_SYNC		
	I2S0I_V_SYNC		
	I2S0I_H_ENABLE		
	I2S0O_BCK_out		
	I2S0O_WS_out		
	I2S0I_BCK_out		
	I2S0I_WS_out		
	I2S0O_DATA_out0~23		
	I2S1I_DATA_in0~15		
	I2S1O_BCK_in		
	I2S1O_WS_in		
	I2S1I_BCK_in		
	I2S1I_WS_in		
	I2S1I_H_SYNC		
	I2S1I_V_SYNC		
	I2S1I_H_ENABLE		
	I2S1O_BCK_out		
	I2S1O_WS_out		
	I2S1I_BCK_out		
	I2S1I_WS_out		
	I2S1O_DATA_out0~23		
	I2S0_CLK	GPIO0, U0RXD, or U0TXD	Note: I2S0_CLK and I2S1_CLK can only be mapped to GPIO0, U0RXD (GPIO3), or U0TXD (GPIO1) via IO MUX by selecting GPIO functions CLK_OUT1, CLK_OUT2, and CLK_OUT3. For more information, see Table 4-3. IO MUX Pad Summary in ESP32 Technical Reference Manual .
	I2S1_CLK		
RMT	RMT_SIG_IN0~7	Any GPIO Pins	Eight channels for an IR transmitter and receiver of various waveforms
	RMT_SIG_OUT0~7		
General Purpose SPI	HSPIQ_in/_out	Any GPIO Pins	Standard SPI consists of clock, chip-select, MOSI and MISO. These SPIs can be connected to LCD and other external devices. They support the following features: <ul style="list-style-type: none">• Both master and slave modes;• Four sub-modes of the SPI transfer format;• Configurable SPI frequency;• Up to 64 bytes of FIFO and DMA.
	HSPID_in/_out		
	HSPICLK_in/_out		
	HSPI_CS0_in/_out		
	HSPI_CS1_out		
	HSPI_CS2_out		
	VSPIQ_in/_out		
	VSPID_in/_out		
	VSPICLK_in/_out		
	VSPI_CS0_in/_out		
	VSPI_CS1_out		
	VSPI_CS2_out		

Interface	Signal	Pin	Function
Parallel QSPI	SPIHD	SD_DATA_2	Supports Standard SPI, Dual SPI, and Quad SPI that can be connected to the external flash and SRAM
	SPIWP	SD_DATA_3	
	SPICS0	SD_CMD	
	SPICLK	SD_CLK	
	SPIQ	SD_DATA_0	
	SPID	SD_DATA_1	
	HSPICLK	MTMS	
	HSPICS0	MTDO	
	HSPIQ	MTDI	
	HSPID	MTCK	
	HSPIHD	GPIO4	
	HSPIWP	GPIO2	
	VSPICLK	GPIO18	
	VSPICS0	GPIO5	
	VSPIQ	GPIO19	
	VSPID	GPIO23	
	VSPIHD	GPIO21	
	VSPIWP	GPIO22	
EMAC	EMAC_TX_CLK	GPIO0	Ethernet MAC with MII/RMII interface
	EMAC_RX_CLK	GPIO5	
	EMAC_TX_EN	GPIO21	
	EMAC_TXD0	GPIO19	
	EMAC_TXD1	GPIO22	
	EMAC_TXD2	MTMS	
	EMAC_TXD3	MTDI	
	EMAC_RX_ER	MTCK	
	EMAC_RX_DV	GPIO27	
	EMAC_RXD0	GPIO25	
	EMAC_RXD1	GPIO26	
	EMAC_RXD2	U0TXD	
	EMAC_RXD3	MTDO	
	EMAC_CLK_OUT	GPIO16	
	EMAC_CLK_OUT_180	GPIO17	
	EMAC_TX_ER	GPIO4	
	EMAC_MDC_out	Any GPIO Pins	
	EMAC_MDI_in	Any GPIO Pins	
	EMAC_MDO_out	Any GPIO Pins	
	EMAC_CRS_out	Any GPIO Pins	
	EMAC_COL_out	Any GPIO Pins	

Interface	Signal	Pin	Function
Pulse Counter	pcnt_sig_ch0_in0	Any GPIO Pins	Operating in seven different modes, the pulse counter captures pulse and counts pulse edges.
	pcnt_sig_ch1_in0		
	pcnt_ctrl_ch0_in0		
	pcnt_ctrl_ch1_in0		
	pcnt_sig_ch0_in1		
	pcnt_sig_ch1_in1		
	pcnt_ctrl_ch0_in1		
	pcnt_ctrl_ch1_in1		
	pcnt_sig_ch0_in2		
	pcnt_sig_ch1_in2		
	pcnt_ctrl_ch0_in2		
	pcnt_ctrl_ch1_in2		
	pcnt_sig_ch0_in3		
	pcnt_sig_ch1_in3		
	pcnt_ctrl_ch0_in3		
	pcnt_ctrl_ch1_in3		
	pcnt_sig_ch0_in4		
	pcnt_sig_ch1_in4		
	pcnt_ctrl_ch0_in4		
	pcnt_ctrl_ch1_in4		
	pcnt_sig_ch0_in5		
	pcnt_sig_ch1_in5		
	pcnt_ctrl_ch0_in5		
	pcnt_ctrl_ch1_in5		
	pcnt_sig_ch0_in6		
	pcnt_sig_ch1_in6		
	pcnt_ctrl_ch0_in6		
	pcnt_ctrl_ch1_in6		
	pcnt_sig_ch0_in7		
	pcnt_sig_ch1_in7		
	pcnt_ctrl_ch0_in7		
	pcnt_ctrl_ch1_in7		
TWAI	twai_rx	Any GPIO Pins	Compatible with ISO 11898-1 protocol (CAN Specification 2.0)
	twai_tx		
	twai_bus_off_on		
	twai_clkout		

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the [recommended operating conditions](#).

Table 13: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO	Voltage applied to power supply pins per power domain	-0.3	3.6	V
I_{output}^*	Cumulative IO output current	-	1200	mA
T_{store}	Storage temperature	-40	150	°C

* The chip worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to ground.

5.2 Recommended Operating Conditions

Table 14: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDA, VDD3P3_RTC, ^{note 1} VDD3P3, VDD_SDIO (3.3 V mode) ^{note 2}	Voltage applied to power supply pins per power domain	2.3/3.0 ^{note 3}	3.3	3.6	V
VDD3P3_CPU	Voltage applied to power supply pin	1.8	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	-	-	A
T ^{note 4}	Operating temperature	-40	-	125	°C

1. When writing eFuse, VDD3P3_RTC should be at least 3.3 V.
2.
 - VDD_SDIO works as the power supply for the related IO, and also for an external device. Please refer to the Appendix [IO_MUX](#) of this datasheet for more details.
 - VDD_SDIO can be sourced internally by the ESP32 from the VDD3P3_RTC power domain:
 - When VDD_SDIO operates at 3.3 V, it is driven directly by VDD3P3_RTC through a $6\ \Omega$ resistor, therefore, there will be some voltage drop from VDD3P3_RTC.
 - When VDD_SDIO operates at 1.8 V, it can be generated from ESP32's internal LDO. The maximum current this LDO can offer is 40 mA, and the output voltage range is 1.65 V ~ 2.0 V.
 - VDD_SDIO can also be driven by an external power supply.
 - Please refer to Power Scheme, section [2.3](#), for more information.
3.
 - Chips with a 3.3 V flash or PSRAM embedded: this minimum voltage is 3.0 V;
 - Chips with no flash or PSRAM embedded: this minimum voltage is 2.3 V;
 - For more information, see Table [25 ESP32 Ordering Information](#).
4.
 - The operating temperature of ESP32-U4WDH ranges from -40 °C to 105 °C, due to the flash embedded in it.
 - The operating temperature of ESP32-D0WDR2-V3 ranges from -40 °C to 85 °C, due to the PSRAM embedded in it.
 - The other chips in this series have no embedded flash or PSRAM, so their range of operating temperatures is -40 °C ~ 125 °C.

5.3 DC Characteristics (3.3 V, 25 °C)

Table 15: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	-	2	-	pF
V_{IH}	High-level input voltage	$0.75 \times VDD^1$	-	$VDD^1 + 0.3$	V
V_{IL}	Low-level input voltage	-0.3	-	$0.25 \times VDD^1$	V
I_{IH}	High-level input current	-	-	50	nA
I_{IL}	Low-level input current	-	-	50	nA
V_{OH}	High-level output voltage	$0.8 \times VDD^1$	-	-	V
V_{OL}	Low-level output voltage	-	-	$0.1 \times VDD^1$	V
I_{OH}	High-level source current ($VDD^1 = 3.3$ V, $V_{OH} \geq 2.64$ V, output drive strength set to the maximum)	VDD3P3_CPU power domain 1, 2	-	40	-
		VDD3P3_RTC power domain 1, 2	-	40	-
		VDD_SDIO power domain 1, 3	-	20	-
I_{OL}	Low-level sink current ($VDD^1 = 3.3$ V, $V_{OL} = 0.495$ V, output drive strength set to the maximum)	-	28	-	mA
R_{PU}	Resistance of internal pull-up resistor	-	45	-	kΩ
R_{PD}	Resistance of internal pull-down resistor	-	45	-	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to power off the chip	-	-	0.6	V

Notes:

1. Please see Table [IO_MUX](#) for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, $V_{OH} \geq 2.64$ V, as the number of current-source pins increases.
3. For VDD_SDIO power domain, per-pin current sourced in the same domain is gradually reduced from around 30 mA to around 10 mA, $V_{OH} \geq 2.64$ V, as the number of current-source pins increases.

5.4 Reliability Qualifications

ESP32 chip series passed all reliability qualifications listed in Table 16.

Table 16: Reliability Qualifications

Test Item	Test Condition	Test Standard
HTOL (High Temperature Operating Life)	125 °C, 1000 hours	JESD22-A108
ESD (Electro-Static Discharge Sensitivity)	HBM (Human Body Mode) ¹ ± 2000 V	JESD22-A114
	CDM (Charge Device Mode) ² ± 500 V	JESD22-C101F
Latch up	Current trigger ± 200 mA	JESD78
	Voltage trigger $1.5 \times VDD_{max}$	
Preconditioning	Bake 24 hours @125 °C Moisture soak (level 3: 192 hours @30 °C, 60% RH) IR reflow solder: 260 + 0 °C, 20 seconds, three times	J-STD-020, JESD47, JESD22-A113

Test Item	Test Condition	Test Standard
TCT (Temperature Cycling Test)	-65 °C / 150 °C, 500 cycles	JESD22-A104
Autoclave Test	121 °C, 100% RH, 96 hours	JESD22-A102
uHAST (Highly Accelerated Stress Test, unbiased)	130 °C, 85% RH, 96 hours	JESD22-A118
HTSL (High Temperature Storage Life)	150 °C, 1000 hours	JESD22-A103

1. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

5.5 RF Power-Consumption Specifications

The power consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 50% duty cycle.

Table 17: RF Power-Consumption Specifications

Mode	Min	Typ	Max	Unit
Transmit 802.11b, DSSS 1 Mbps, POUT = +19.5 dBm	-	240	-	mA
Transmit 802.11g, OFDM 54 Mbps, POUT = +16 dBm	-	190	-	mA
Transmit 802.11n, OFDM MCS7, POUT = +14 dBm	-	180	-	mA
Receive 802.11b/g/n	-	95 ~ 100	-	mA
Transmit BT/BLE, POUT = 0 dBm	-	130	-	mA
Receive BT/BLE	-	95 ~ 100	-	mA

5.6 Wi-Fi Radio

Table 18: Wi-Fi Radio Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency range ^{note1}	-	2412	-	2484	MHz
Output impedance ^{note2}	-	-	<i>note 2</i>	-	Ω
TX power ^{note3}	11n, MCS7	12	13	14	dBm
	11b mode	18.5	19.5	20.5	dBm
Sensitivity	11b, 1 Mbps	-	-98	-	dBm
	11b, 11 Mbps	-	-88	-	dBm
	11g, 6 Mbps	-	-93	-	dBm
	11g, 54 Mbps	-	-75	-	dBm
	11n, HT20, MCS0	-	-93	-	dBm
	11n, HT20, MCS7	-	-73	-	dBm
	11n, HT40, MCS0	-	-90	-	dBm
	11n, HT40, MCS7	-	-70	-	dBm

Parameter	Condition	Min	Typ	Max	Unit
Adjacent channel rejection	11g, 6 Mbps	-	27	-	dB
	11g, 54 Mbps	-	13	-	dB
	11n, HT20, MCS0	-	27	-	dB
	11n, HT20, MCS7	-	12	-	dB

1. Device should operate in the frequency range allocated by regional regulatory authorities. Target operating frequency range is configurable by software.
2. The typical value of ESP32's Wi-Fi radio output impedance is different between chips in different QFN packages. For ESP32 chips with a QFN 6x6 package, the value is $30+j10 \Omega$. For ESP32 chips with a QFN 5x5 package, the value is $35+j10 \Omega$.
3. Target TX power is configurable based on device or certification requirements.

5.7 Bluetooth Radio

5.7.1 Receiver – Basic Data Rate

Table 19: Receiver Characteristics – Basic Data Rate

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity @0.1% BER	-	-90	-89	-88	dBm
Maximum received signal @0.1% BER	-	0	-	-	dBm
Co-channel C/I	-	-	+7	-	dB
Adjacent channel selectivity C/I	$F = F_0 + 1 \text{ MHz}$	-	-	-6	dB
	$F = F_0 - 1 \text{ MHz}$	-	-	-6	dB
	$F = F_0 + 2 \text{ MHz}$	-	-	-25	dB
	$F = F_0 - 2 \text{ MHz}$	-	-	-33	dB
	$F = F_0 + 3 \text{ MHz}$	-	-	-25	dB
	$F = F_0 - 3 \text{ MHz}$	-	-	-45	dB
Out-of-band blocking performance	$30 \text{ MHz} \sim 2000 \text{ MHz}$	-10	-	-	dBm
	$2000 \text{ MHz} \sim 2400 \text{ MHz}$	-27	-	-	dBm
	$2500 \text{ MHz} \sim 3000 \text{ MHz}$	-27	-	-	dBm
	$3000 \text{ MHz} \sim 12.5 \text{ GHz}$	-10	-	-	dBm
Intermodulation	-	-36	-	-	dBm

5.7.2 Transmitter – Basic Data Rate

Table 20: Transmitter Characteristics – Basic Data Rate

Parameter	Condition	Min	Typ	Max	Unit
RF transmit power (see note under Table 20)	-	-	0	-	dBm
Gain control step	-	-	3	-	dB
RF power control range	-	-12	-	+9	dBm
+20 dB bandwidth	-	-	0.9	-	MHz
Adjacent channel transmit power	$F = F_0 \pm 2 \text{ MHz}$	-	-47	-	dBm
	$F = F_0 \pm 3 \text{ MHz}$	-	-55	-	dBm

Parameter	Condition	Min	Typ	Max	Unit
	$F = F_0 \pm > 3 \text{ MHz}$	-	-60	-	dBm
$\Delta f_{1\text{avg}}$	-	-	-	155	kHz
$\Delta f_{2\text{max}}$	-	133.7	-	-	kHz
$\Delta f_{2\text{avg}}/\Delta f_{1\text{avg}}$	-	-	0.92	-	-
ICFT	-	-	-7	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift (DH1)	-	-	6	-	kHz
Drift (DH5)	-	-	6	-	kHz

Note:

There are in total eight power levels from level 0 to level 7, with transmit power ranging from -12 dBm to 9 dBm. When the power level rises by 1, the transmit power increases by 3 dB. Power level 4 is used by default and the corresponding transmit power is 0 dBm.

5.7.3 Receiver – Enhanced Data Rate

Table 21: Receiver Characteristics – Enhanced Data Rate

Parameter	Condition	Min	Typ	Max	Unit
$\pi/4$ DQPSK					
Sensitivity @0.01% BER	-	-90	-89	-88	dBm
Maximum received signal @0.01% BER	-	-	0	-	dBm
Co-channel C/I	-	-	11	-	dB
Adjacent channel selectivity C/I	$F = F_0 + 1 \text{ MHz}$	-	-7	-	dB
	$F = F_0 - 1 \text{ MHz}$	-	-7	-	dB
	$F = F_0 + 2 \text{ MHz}$	-	-25	-	dB
	$F = F_0 - 2 \text{ MHz}$	-	-35	-	dB
	$F = F_0 + 3 \text{ MHz}$	-	-25	-	dB
	$F = F_0 - 3 \text{ MHz}$	-	-45	-	dB
8DPSK					
Sensitivity @0.01% BER	-	-84	-83	-82	dBm
Maximum received signal @0.01% BER	-	-	-5	-	dBm
C/I c-channel	-	-	18	-	dB
Adjacent channel selectivity C/I	$F = F_0 + 1 \text{ MHz}$	-	2	-	dB
	$F = F_0 - 1 \text{ MHz}$	-	2	-	dB
	$F = F_0 + 2 \text{ MHz}$	-	-25	-	dB
	$F = F_0 - 2 \text{ MHz}$	-	-25	-	dB
	$F = F_0 + 3 \text{ MHz}$	-	-25	-	dB
	$F = F_0 - 3 \text{ MHz}$	-	-38	-	dB

5.7.4 Transmitter – Enhanced Data Rate

Table 22: Transmitter Characteristics – Enhanced Data Rate

Parameter	Condition	Min	Typ	Max	Unit
RF transmit power (see note under Table 20)	-	-	0	-	dBm
Gain control step	-	-	3	-	dB
RF power control range	-	-12	-	+9	dBm
$\pi/4$ DQPSK max w0	-	-	-0.72	-	kHz
$\pi/4$ DQPSK max wi	-	-	-6	-	kHz
$\pi/4$ DQPSK max lwi + w0l	-	-	-7.42	-	kHz
8DPSK max w0	-	-	0.7	-	kHz
8DPSK max wi	-	-	-9.6	-	kHz
8DPSK max lwi + w0l	-	-	-10	-	kHz
$\pi/4$ DQPSK modulation accuracy	RMS DEVM	-	4.28	-	%
	99% DEVM	-	100	-	%
	Peak DEVM	-	13.3	-	%
8 DPSK modulation accuracy	RMS DEVM	-	5.8	-	%
	99% DEVM	-	100	-	%
	Peak DEVM	-	14	-	%
In-band spurious emissions	$F = F_0 \pm 1$ MHz	-	-46	-	dBm
	$F = F_0 \pm 2$ MHz	-	-40	-	dBm
	$F = F_0 \pm 3$ MHz	-	-46	-	dBm
	$F = F_0 +/- > 3$ MHz	-	-	-53	dBm
EDR differential phase coding	-	-	100	-	%

5.8 Bluetooth LE Radio

5.8.1 Receiver

Table 23: Receiver Characteristics – Bluetooth LE

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity @30.8% PER	-	-94	-93	-92	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	$F = F_0 + 1$ MHz	-	-5	-	dB
	$F = F_0 - 1$ MHz	-	-5	-	dB
	$F = F_0 + 2$ MHz	-	-25	-	dB
	$F = F_0 - 2$ MHz	-	-35	-	dB
	$F = F_0 + 3$ MHz	-	-25	-	dB
	$F = F_0 - 3$ MHz	-	-45	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	-10	-	-	dBm
	2000 MHz ~ 2400 MHz	-27	-	-	dBm
	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-36	-	-	dBm

5.8.2 Transmitter

Table 24: Transmitter Characteristics – Bluetooth LE

Parameter	Condition	Min	Typ	Max	Unit
RF transmit power (see note under Table 20)	-	-	0	-	dBm
Gain control step	-	-	3	-	dB
RF power control range	-	-12	-	+9	dBm
Adjacent channel transmit power	$F = F_0 \pm 2 \text{ MHz}$	-	-52	-	dBm
	$F = F_0 \pm 3 \text{ MHz}$	-	-58	-	dBm
	$F = F_0 \pm > 3 \text{ MHz}$	-	-60	-	dBm
$\Delta f_{1\text{avg}}$	-	-	-	265	kHz
$\Delta f_{2\text{max}}$	-	247	-	-	kHz
$\Delta f_{2\text{avg}}/\Delta f_{1\text{avg}}$	-	-	0.92	-	-
ICFT	-	-	-10	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift	-	-	2	-	kHz

6 Package Information

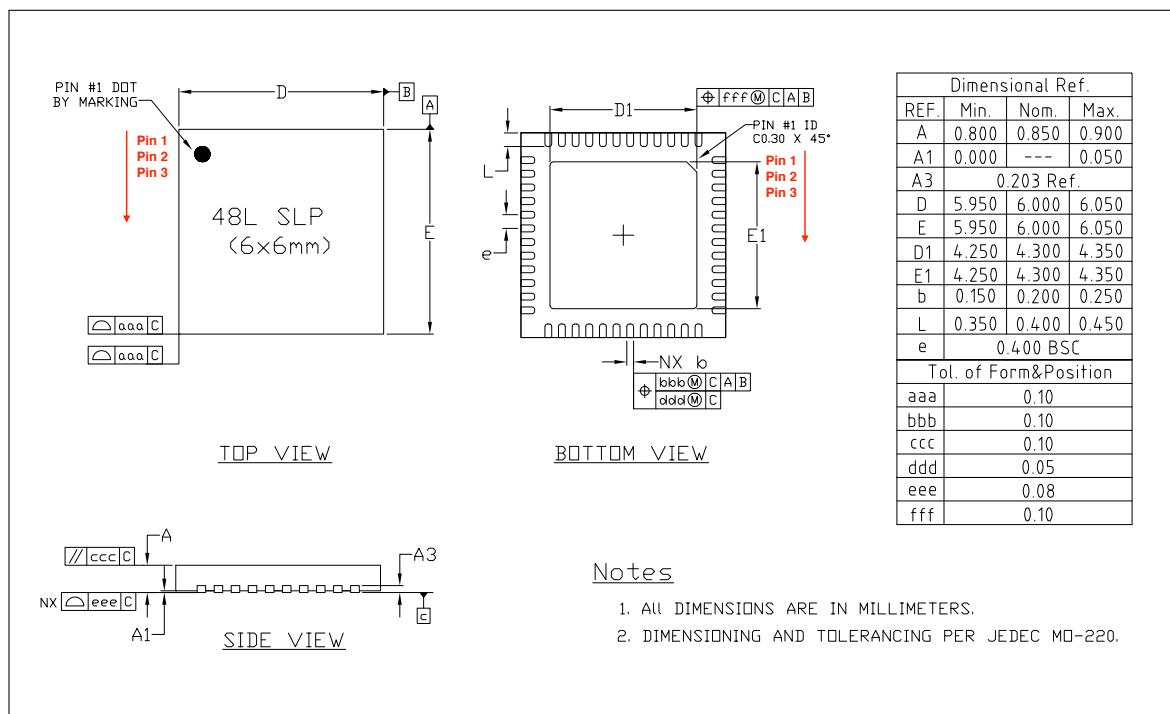


Figure 8: QFN48 (6x6 mm) Package

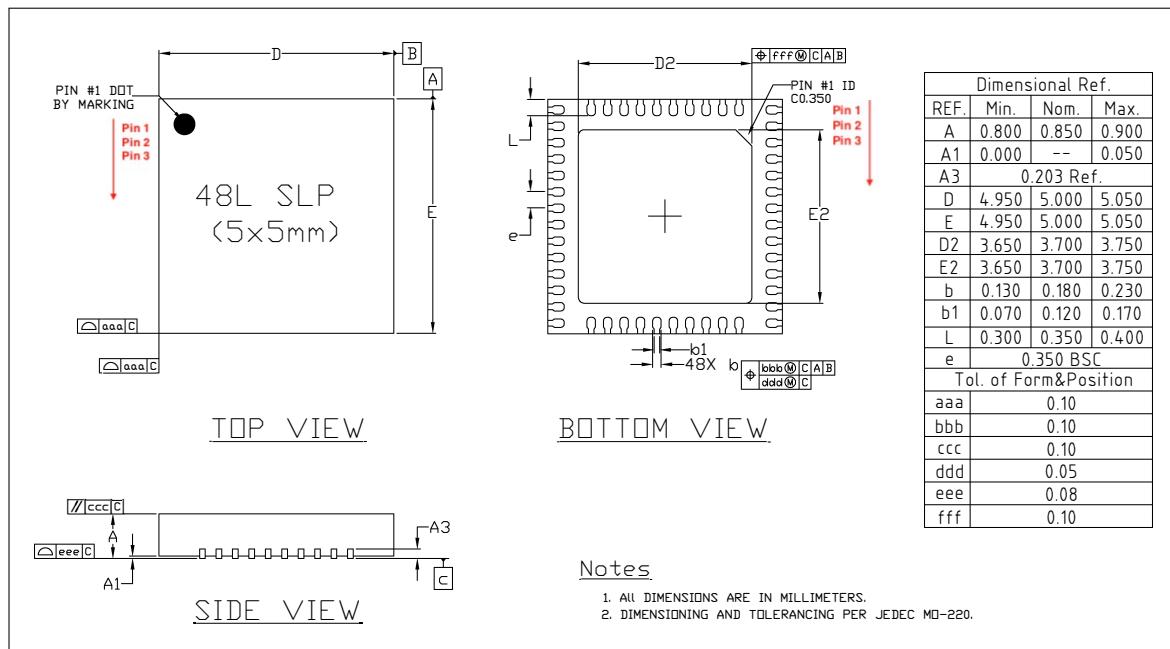


Figure 9: QFN48 (5x5 mm) Package

Note:

The pins of the chip are numbered in an anti-clockwise direction from Pin 1 in the top view. For information about tape, reel, and product marking, please refer to [Espressif Chip Package Information](#).

7 Part Number and Ordering Information

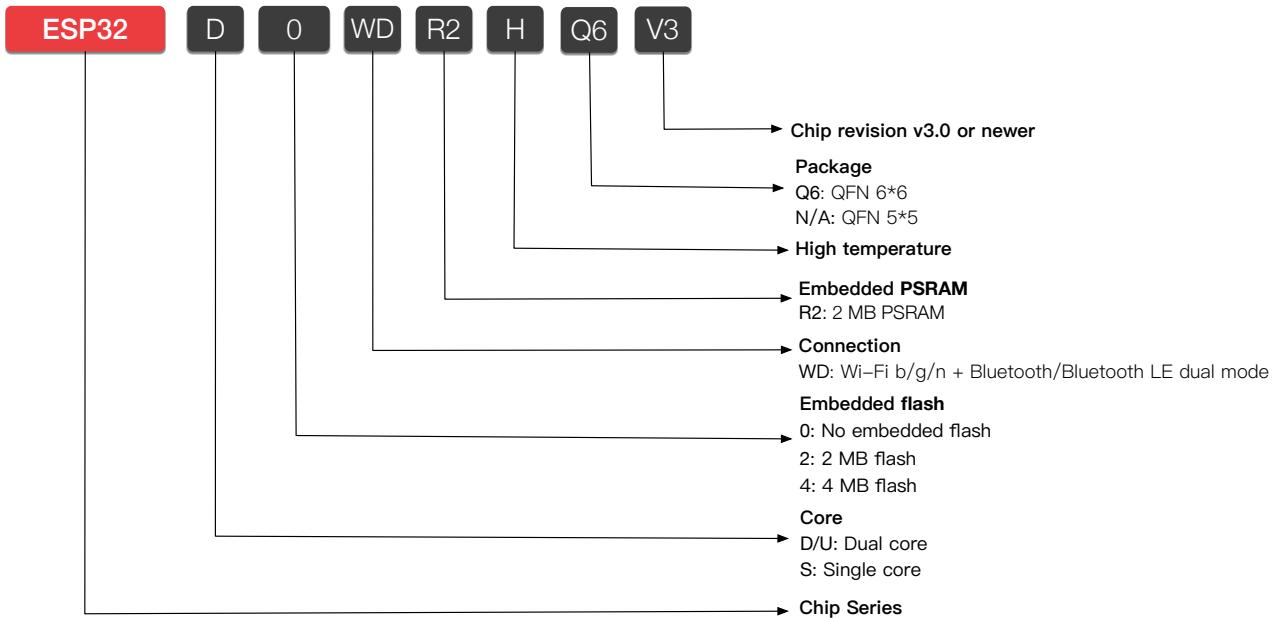


Figure 10: ESP32 Part Number Description

The table below provides the ordering information of the ESP32 series of chips.

Table 25: ESP32 Ordering Information

Ordering code ¹	Core	Chip Revision ²	Embedded flash/PSRAM	Package	VDD_SDIO voltage
ESP32-D0WD-V3	Dual core	v3.0/v3.1 ⁴	—	QFN 5*5	1.8 V/3.3 V
ESP32-D0WDR2-V3	Dual core	v3.0/v3.1 ⁴	2 MB PSRAM	QFN 5*5	3.3 V
ESP32-U4WDH	Dual core ³	v3.0/v3.1 ⁴	4 MB flash (80 MHz)	QFN 5*5	3.3 V
ESP32-D0WDQ6-V3 (NRND)	Dual core	v3.0/v3.1 ⁴	—	QFN 6*6	1.8 V/3.3 V
ESP32-D0WD (NRND)	Dual core	v1.0/v1.1 ⁵	—	QFN 5*5	1.8 V/3.3 V
ESP32-D0WDQ6 (NRND)	Dual core	v1.0/v1.1 ⁵	—	QFN 6*6	1.8 V/3.3 V
ESP32-S0WD (NRND)	Single core	v1.0/v1.1 ⁵	—	QFN 5*5	1.8 V/3.3 V

¹ All above chips support Wi-Fi b/g/n + Bluetooth/Bluetooth LE Dual Mode connection.

² The differences between ESP32 chip revisions and the way to distinguish the revisions used in each chip are described in [ESP32 Series SoC Errata](#).

³ ESP32-U4WDH will be produced as dual-core instead of single core. See [PCN-2021-021](#) for more details.

⁴ The chips will be produced with chip revision v3.1 inside. See [PCN20220901](#) for more details.

⁵ The chips will be produced with chip revision v1.1 inside. See [PCN20220901](#) for more details.

8 Related Documentation and Resources

Related Documentation

- [ESP32 Technical Reference Manual](#) – Detailed information on how to use the ESP32 memory and peripherals.
- [ESP32 Hardware Design Guidelines](#) – Guidelines on how to integrate the ESP32 into your hardware product.
- [ESP32 ECO and Workarounds for Bugs](#) – Correction of ESP32 design errors.
- [Certificates](#)
<http://espressif.com/en/support/documents/certificates>
- [ESP32 Product/Process Change Notifications \(PCN\)](#)
<http://espressif.com/en/support/documents/pcns>
- [ESP32 Advisories](#) – Information on security, bugs, compatibility, component reliability.
<http://espressif.com/en/support/documents/advisories>
- [Documentation Updates and Update Notification Subscription](#)
<http://espressif.com/en/support/download/documents>

Developer Zone

- [ESP-IDF Programming Guide for ESP32](#) – Extensive documentation for the ESP-IDF development framework.
- [ESP-IDF and other development frameworks on GitHub](#).
<http://github.com/espressif>
- [ESP32 BBS Forum](#) – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
<http://esp32.com/>
- [The ESP Journal](#) – Best Practices, Articles, and Notes from Espressif folks.
<http://blog.espressif.com/>
- See the tabs [SDKs and Demos](#), [Apps](#), [Tools](#), [AT Firmware](#).
<http://espressif.com/en/support/download/sdks-demos>

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- [ESP32 Series SoCs](#) – Browse through all ESP32 SoCs.
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<http://espressif.com/en/contact-us/sales-questions>

Appendix A – ESP32 Pin Lists

A.1. Notes on ESP32 Pin Lists

Table 26: Notes on ESP32 Pin Lists

No.	Description
1	In Table IO_MUX , the boxes highlighted in yellow indicate the GPIO pins that are input-only. Please see the following note for further details.
2	GPIO pins 34-39 are input-only. These pins do not feature an output driver or internal pull-up/pull-down circuitry. The pin names are: SENSOR_VP (GPIO36), SENSOR_CAPP (GPIO37), SENSOR_CAPN (GPIO38), SENSOR_VN (GPIO39), VDET_1 (GPIO34), VDET_2 (GPIO35).
3	The pins are grouped into four power domains: VDDA (analog power supply), VDD3P3_RTC (RTC power supply), VDD3P3_CPU (power supply of digital IOs and CPU cores), VDD_SDIO (power supply of SDIO IOs). VDD_SDIO is the output of the internal SDIO-LDO. The voltage of SDIO-LDO can be configured at 1.8 V or be the same as that of VDD3P3_RTC. The strapping pin and eFuse bits determine the default voltage of the SDIO-LDO. Software can change the voltage of the SDIO-LDO by configuring register bits. For details, please see the column “Power Domain” in Table IO_MUX .
4	The functional pins in the VDD3P3_RTC domain are those with analog functions, including the 32 kHz crystal oscillator, ADC, DAC, and the capacitive touch sensor. Please see columns “Analog Function 0 ~ 2” in Table IO_MUX .
5	These VDD3P3_RTC pins support the RTC function, and can work during Deep-sleep. For example, an RTC-GPIO can be used for waking up the chip from Deep-sleep.
6	The GPIO pins support up to six digital functions, as shown in columns “Function 0 ~ 5” In Table IO_MUX . The function selection registers will be set as “ <i>N</i> ”, where <i>N</i> is the function number. Below are some definitions: <ul style="list-style-type: none"> • SD_* is for signals of the SDIO slave. • HS1_* is for Port 1 signals of the SDIO host. • HS2_* is for Port 2 signals of the SDIO host. • MT* is for signals of the JTAG. • U0* is for signals of the UART0 module. • U1* is for signals of the UART1 module. • U2* is for signals of the UART2 module. • SPI* is for signals of the SPI01 module. • HSPI* is for signals of the SPI2 module. • VSPI* is for signals of the SPI3 module.

No.	Description
7	<p>Each column about digital “Function” is accompanied by a column about “Type”. Please see the following explanations for the meanings of “type” with respect to each “function” they are associated with. For each “Function-<i>N</i>”, “type” signifies:</p> <ul style="list-style-type: none"> • I: input only. If a function other than “Function-<i>N</i>” is assigned, the input signal of “Function-<i>N</i>” is still from this pin. • I1: input only. If a function other than “Function-<i>N</i>” is assigned, the input signal of “Function-<i>N</i>” is always “1”. • IO: input only. If a function other than “Function-<i>N</i>” is assigned, the input signal of “Function-<i>N</i>” is always “0”. • O: output only. • T: high-impedance. • I/O/T: combinations of input, output, and high-impedance according to the function signal. • I1/O/T: combinations of input, output, and high-impedance, according to the function signal. If a function is not selected, the input signal of the function is “1”. <p>For example, pin 30 can function as HS1_CMD or SD_CMD, where HS1_CMD is of an “I1/O/T” type. If pin 30 is selected as HS1_CMD, this pin’s input and output are controlled by the SDIO host. If pin 30 is not selected as HS1_CMD, the input signal of the SDIO host is always “1”.</p>
8	<p>Each digital output pin is associated with its configurable drive strength. Column “Drive Strength” in Table IO_MUX lists the default values. The drive strength of the digital output pins can be configured into one of the following four options:</p> <ul style="list-style-type: none"> • 0: ~5 mA • 1: ~10 mA • 2: ~20 mA • 3: ~40 mA <p>The default value is 2.</p> <p>The drive strength of the internal pull-up (wpu) and pull-down (wpd) is ~75 μA.</p>
9	<p>Column “At Reset” in Table IO_MUX lists the status of each pin during reset, including input-enable (ie=1), internal pull-up (wpu) and internal pull-down (wpd). During reset, all pins are output-disabled.</p>
10	<p>Column “After Reset” in Table IO_MUX lists the status of each pin immediately after reset, including input-enable (ie=1), internal pull-up (wpu) and internal pull-down (wpd). After reset, each pin is set to “Function 0”. The output-enable is controlled by digital Function 0.</p>
11	<p>Table Ethernet_MAC is about the signal mapping inside Ethernet MAC. The Ethernet MAC supports MII and RMII interfaces, and supports both the internal PLL clock and the external clock source. For the MII interface, the Ethernet MAC is with/without the TX_ERR signal. MDC, MDIO, CRS and COL are slow signals, and can be mapped onto any GPIO pin through the GPIO-Matrix.</p>
12	<p>Table GPIO Matrix is for the GPIO-Matrix. The signals of the on-chip functional modules can be mapped onto any GPIO pin. Some signals can be mapped onto a pin by both IO-MUX and GPIO-Matrix, as shown in the column tagged as “Same input signal from IO_MUX core” in Table GPIO Matrix.</p>

No.	Description
13	*In Table GPIO_Matrix the column “Default Value if unassigned” records the default value of the an input signal if no GPIO is assigned to it. The actual value is determined by register GPIO_FUNC m _IN_INV_SEL and GPIO_FUNC m _IN_SEL. (The value of m ranges from 1 to 255.)

A.2. GPIO_Matrix

Table 27: GPIO_Matrix

Signal No.	Input Signals	Default Value If Unassigned*	Same Input Signal from IO_MUX Core	Output Signals	Output Enable of Output Signals
0	SPICLK_in	0	yes	SPICLK_out	SPICLK_oe
1	SPIQ_in	0	yes	SPIQ_out	SPIQ_oe
2	SPID_in	0	yes	SPID_out	SPID_oe
3	SPIHD_in	0	yes	SPIHD_out	SPIHD_oe
4	SPIWP_in	0	yes	SPIWP_out	SPIWP_oe
5	SPICS0_in	0	yes	SPICS0_out	SPICS0_oe
6	SPICS1_in	0	no	SPICS1_out	SPICS1_oe
7	SPICS2_in	0	no	SPICS2_out	SPICS2_oe
8	HSPICLK_in	0	yes	HSPICLK_out	HSPICLK_oe
9	HSPIQ_in	0	yes	HSPIQ_out	HSPIQ_oe
10	HSPID_in	0	yes	HSPID_out	HSPID_oe
11	HSPICS0_in	0	yes	HSPICS0_out	HSPICS0_oe
12	HSPIHD_in	0	yes	HSPIHD_out	HSPIHD_oe
13	HSPIWP_in	0	yes	HSPIWP_out	HSPIWP_oe
14	U0RXD_in	0	yes	U0TXD_out	1'd1
15	U0CTS_in	0	yes	U0RTS_out	1'd1
16	U0DSR_in	0	no	U0DTR_out	1'd1
17	U1RXD_in	0	yes	U1TXD_out	1'd1
18	U1CTS_in	0	yes	U1RTS_out	1'd1
23	I2S0O_BCK_in	0	no	I2S0O_BCK_out	1'd1
24	I2S1O_BCK_in	0	no	I2S1O_BCK_out	1'd1
25	I2S0O_WS_in	0	no	I2S0O_WS_out	1'd1
26	I2S1O_WS_in	0	no	I2S1O_WS_out	1'd1
27	I2S0I_BCK_in	0	no	I2S0I_BCK_out	1'd1
28	I2S0I_WS_in	0	no	I2S0I_WS_out	1'd1
29	I2CEXT0_SCL_in	1	no	I2CEXT0_SCL_out	1'd1
30	I2CEXT0_SDA_in	1	no	I2CEXT0_SDA_out	1'd1
31	pwm0_sync0_in	0	no	sdio_tohost_int_out	1'd1
32	pwm0_sync1_in	0	no	pwm0_out0a	1'd1
33	pwm0_sync2_in	0	no	pwm0_out0b	1'd1
34	pwm0_f0_in	0	no	pwm0_out1a	1'd1

Signal No.	Input Signals	Default Value If Unassigned*	Same Input Signal from IO_MUX Core	Output Signals	Output Enable of Output Signals
35	pwm0_f1_in	0	no	pwm0_out1b	1'd1
36	pwm0_f2_in	0	no	pwm0_out2a	1'd1
37	-	0	no	pwm0_out2b	1'd1
39	pcnt_sig_ch0_in0	0	no	-	1'd1
40	pcnt_sig_ch1_in0	0	no	-	1'd1
41	pcnt_ctrl_ch0_in0	0	no	-	1'd1
42	pcnt_ctrl_ch1_in0	0	no	-	1'd1
43	pcnt_sig_ch0_in1	0	no	-	1'd1
44	pcnt_sig_ch1_in1	0	no	-	1'd1
45	pcnt_ctrl_ch0_in1	0	no	-	1'd1
46	pcnt_ctrl_ch1_in1	0	no	-	1'd1
47	pcnt_sig_ch0_in2	0	no	-	1'd1
48	pcnt_sig_ch1_in2	0	no	-	1'd1
49	pcnt_ctrl_ch0_in2	0	no	-	1'd1
50	pcnt_ctrl_ch1_in2	0	no	-	1'd1
51	pcnt_sig_ch0_in3	0	no	-	1'd1
52	pcnt_sig_ch1_in3	0	no	-	1'd1
53	pcnt_ctrl_ch0_in3	0	no	-	1'd1
54	pcnt_ctrl_ch1_in3	0	no	-	1'd1
55	pcnt_sig_ch0_in4	0	no	-	1'd1
56	pcnt_sig_ch1_in4	0	no	-	1'd1
57	pcnt_ctrl_ch0_in4	0	no	-	1'd1
58	pcnt_ctrl_ch1_in4	0	no	-	1'd1
61	HSPICS1_in	0	no	HSPICS1_out	HSPICS1_oe
62	HSPICS2_in	0	no	HSPICS2_out	HSPICS2_oe
63	VSPICLK_in	0	yes	VSPICLK_out_mux	VSPICLK_oe
64	VSPIQ_in	0	yes	VSPIQ_out	VSPIQ_oe
65	VSPID_in	0	yes	VSPID_out	VSPID_oe
66	VSPIHD_in	0	yes	VSPIHD_out	VSPIHD_oe
67	VSPIWP_in	0	yes	VSPIWP_out	VSPIWP_oe
68	VSPICS0_in	0	yes	VSPICS0_out	VSPICS0_oe
69	VSPICS1_in	0	no	VSPICS1_out	VSPICS1_oe
70	VSPICS2_in	0	no	VSPICS2_out	VSPICS2_oe
71	pcnt_sig_ch0_in5	0	no	ledc_hs_sig_out0	1'd1
72	pcnt_sig_ch1_in5	0	no	ledc_hs_sig_out1	1'd1
73	pcnt_ctrl_ch0_in5	0	no	ledc_hs_sig_out2	1'd1
74	pcnt_ctrl_ch1_in5	0	no	ledc_hs_sig_out3	1'd1
75	pcnt_sig_ch0_in6	0	no	ledc_hs_sig_out4	1'd1
76	pcnt_sig_ch1_in6	0	no	ledc_hs_sig_out5	1'd1
77	pcnt_ctrl_ch0_in6	0	no	ledc_hs_sig_out6	1'd1
78	pcnt_ctrl_ch1_in6	0	no	ledc_hs_sig_out7	1'd1

Signal No.	Input Signals	Default Value If Unassigned*	Same Input Signal from IO_MUX Core	Output Signals	Output Enable of Output Signals
79	pcnt_sig_ch0_in7	0	no	ledc_ls_sig_out0	1'd1
80	pcnt_sig_ch1_in7	0	no	ledc_ls_sig_out1	1'd1
81	pcnt_ctrl_ch0_in7	0	no	ledc_ls_sig_out2	1'd1
82	pcnt_ctrl_ch1_in7	0	no	ledc_ls_sig_out3	1'd1
83	rmt_sig_in0	0	no	ledc_ls_sig_out4	1'd1
84	rmt_sig_in1	0	no	ledc_ls_sig_out5	1'd1
85	rmt_sig_in2	0	no	ledc_ls_sig_out6	1'd1
86	rmt_sig_in3	0	no	ledc_ls_sig_out7	1'd1
87	rmt_sig_in4	0	no	rmt_sig_out0	1'd1
88	rmt_sig_in5	0	no	rmt_sig_out1	1'd1
89	rmt_sig_in6	0	no	rmt_sig_out2	1'd1
90	rmt_sig_in7	0	no	rmt_sig_out3	1'd1
91	-	-	-	rmt_sig_out4	1'd1
92	-	-	-	rmt_sig_out6	1'd1
94	twai_rx	1	no	rmt_sig_out7	1'd1
95	I2CEXT1_SCL_in	1	no	I2CEXT1_SCL_out	1'd1
96	I2CEXT1_SDA_in	1	no	I2CEXT1_SDA_out	1'd1
97	host_card_detect_n_1	0	no	host_ccmd_od_pullup_en_n	1'd1
98	host_card_detect_n_2	0	no	host_RST_n_1	1'd1
99	host_card_write_prt_1	0	no	host_RST_n_2	1'd1
100	host_card_write_prt_2	0	no	gpio_sd0_out	1'd1
101	host_card_int_n_1	0	no	gpio_sd1_out	1'd1
102	host_card_int_n_2	0	no	gpio_sd2_out	1'd1
103	pwm1_sync0_in	0	no	gpio_sd3_out	1'd1
104	pwm1_sync1_in	0	no	gpio_sd4_out	1'd1
105	pwm1_sync2_in	0	no	gpio_sd5_out	1'd1
106	pwm1_f0_in	0	no	gpio_sd6_out	1'd1
107	pwm1_f1_in	0	no	gpio_sd7_out	1'd1
108	pwm1_f2_in	0	no	pwm1_out0a	1'd1
109	pwm0_cap0_in	0	no	pwm1_out0b	1'd1
110	pwm0_cap1_in	0	no	pwm1_out1a	1'd1
111	pwm0_cap2_in	0	no	pwm1_out1b	1'd1
112	pwm1_cap0_in	0	no	pwm1_out2a	1'd1
113	pwm1_cap1_in	0	no	pwm1_out2b	1'd1
114	pwm1_cap2_in	0	no	pwm2_out1h	1'd1
115	pwm2_fta	1	no	pwm2_out1l	1'd1
116	pwm2_ftb	1	no	pwm2_out2h	1'd1
117	pwm2_cap1_in	0	no	pwm2_out2l	1'd1
118	pwm2_cap2_in	0	no	pwm2_out3h	1'd1
119	pwm2_cap3_in	0	no	pwm2_out3l	1'd1
120	pwm3_fta	1	no	pwm2_out4h	1'd1

Signal No.	Input Signals	Default Value If Unassigned*	Same Input Signal from IO_MUX Core	Output Signals	Output Enable of Output Signals
121	pwm3_fltb	1	no	pwm2_out4l	1'd1
122	pwm3_cap1_in	0	no	-	1'd1
123	pwm3_cap2_in	0	no	twai_tx	1'd1
124	pwm3_cap3_in	0	no	twai_bus_off_on	1'd1
125	-	-	-	twai_clkout	1'd1
140	I2S0I_DATA_in0	0	no	I2S0O_DATA_out0	1'd1
141	I2S0I_DATA_in1	0	no	I2S0O_DATA_out1	1'd1
142	I2S0I_DATA_in2	0	no	I2S0O_DATA_out2	1'd1
143	I2S0I_DATA_in3	0	no	I2S0O_DATA_out3	1'd1
144	I2S0I_DATA_in4	0	no	I2S0O_DATA_out4	1'd1
145	I2S0I_DATA_in5	0	no	I2S0O_DATA_out5	1'd1
146	I2S0I_DATA_in6	0	no	I2S0O_DATA_out6	1'd1
147	I2S0I_DATA_in7	0	no	I2S0O_DATA_out7	1'd1
148	I2S0I_DATA_in8	0	no	I2S0O_DATA_out8	1'd1
149	I2S0I_DATA_in9	0	no	I2S0O_DATA_out9	1'd1
150	I2S0I_DATA_in10	0	no	I2S0O_DATA_out10	1'd1
151	I2S0I_DATA_in11	0	no	I2S0O_DATA_out11	1'd1
152	I2S0I_DATA_in12	0	no	I2S0O_DATA_out12	1'd1
153	I2S0I_DATA_in13	0	no	I2S0O_DATA_out13	1'd1
154	I2S0I_DATA_in14	0	no	I2S0O_DATA_out14	1'd1
155	I2S0I_DATA_in15	0	no	I2S0O_DATA_out15	1'd1
156	-	-	-	I2S0O_DATA_out16	1'd1
157	-	-	-	I2S0O_DATA_out17	1'd1
158	-	-	-	I2S0O_DATA_out18	1'd1
159	-	-	-	I2S0O_DATA_out19	1'd1
160	-	-	-	I2S0O_DATA_out20	1'd1
161	-	-	-	I2S0O_DATA_out21	1'd1
162	-	-	-	I2S0O_DATA_out22	1'd1
163	-	-	-	I2S0O_DATA_out23	1'd1
164	I2S1I_BCK_in	0	no	I2S1I_BCK_out	1'd1
165	I2S1I_WS_in	0	no	I2S1I_WS_out	1'd1
166	I2S1I_DATA_in0	0	no	I2S1O_DATA_out0	1'd1
167	I2S1I_DATA_in1	0	no	I2S1O_DATA_out1	1'd1
168	I2S1I_DATA_in2	0	no	I2S1O_DATA_out2	1'd1
169	I2S1I_DATA_in3	0	no	I2S1O_DATA_out3	1'd1
170	I2S1I_DATA_in4	0	no	I2S1O_DATA_out4	1'd1
171	I2S1I_DATA_in5	0	no	I2S1O_DATA_out5	1'd1
172	I2S1I_DATA_in6	0	no	I2S1O_DATA_out6	1'd1
173	I2S1I_DATA_in7	0	no	I2S1O_DATA_out7	1'd1
174	I2S1I_DATA_in8	0	no	I2S1O_DATA_out8	1'd1
175	I2S1I_DATA_in9	0	no	I2S1O_DATA_out9	1'd1

Signal No.	Input Signals	Default Value If Unassigned*	Same Input Signal from IO_MUX Core	Output Signals	Output Enable of Output Signals
176	I2S1I_DATA_in10	0	no	I2S1O_DATA_out10	1'd1
177	I2S1I_DATA_in11	0	no	I2S1O_DATA_out11	1'd1
178	I2S1I_DATA_in12	0	no	I2S1O_DATA_out12	1'd1
179	I2S1I_DATA_in13	0	no	I2S1O_DATA_out13	1'd1
180	I2S1I_DATA_in14	0	no	I2S1O_DATA_out14	1'd1
181	I2S1I_DATA_in15	0	no	I2S1O_DATA_out15	1'd1
182	-	-	-	I2S1O_DATA_out16	1'd1
183	-	-	-	I2S1O_DATA_out17	1'd1
184	-	-	-	I2S1O_DATA_out18	1'd1
185	-	-	-	I2S1O_DATA_out19	1'd1
186	-	-	-	I2S1O_DATA_out20	1'd1
187	-	-	-	I2S1O_DATA_out21	1'd1
188	-	-	-	I2S1O_DATA_out22	1'd1
189	-	-	-	I2S1O_DATA_out23	1'd1
190	I2S0I_H_SYNC	0	no	pwm3_out1h	1'd1
191	I2S0I_V_SYNC	0	no	pwm3_out1l	1'd1
192	I2S0I_H_ENABLE	0	no	pwm3_out2h	1'd1
193	I2S1I_H_SYNC	0	no	pwm3_out2l	1'd1
194	I2S1I_V_SYNC	0	no	pwm3_out3h	1'd1
195	I2S1I_H_ENABLE	0	no	pwm3_out3l	1'd1
196	-	-	-	pwm3_out4h	1'd1
197	-	-	-	pwm3_out4l	1'd1
198	U2RXD_in	0	yes	U2TXD_out	1'd1
199	U2CTS_in	0	yes	U2RTS_out	1'd1
200	emac_mdc_i	0	no	emac_mdc_o	emac_mdc_oe
201	emac_mdi_i	0	no	emac_mdo_o	emac_mdo_o_e
202	emac_crs_i	0	no	emac_crs_o	emac_crs_oe
203	emac_col_i	0	no	emac_col_o	emac_col_oe
204	pcmfsync_in	0	no	bt_audio0_irq	1'd1
205	pcmclk_in	0	no	bt_audio1_irq	1'd1
206	pcmdin	0	no	bt_audio2_irq	1'd1
207	-	-	-	ble_audio0_irq	1'd1
208	-	-	-	ble_audio1_irq	1'd1
209	-	-	-	ble_audio2_irq	1'd1
210	-	-	-	pcmfsync_out	pcmfsync_en
211	-	-	-	pcmclk_out	pcmclk_en
212	-	-	-	pcmdout	pcmdout_en
213	-	-	-	ble_audio_sync0_p	1'd1
214	-	-	-	ble_audio_sync1_p	1'd1
215	-	-	-	ble_audio_sync2_p	1'd1
224	-	-	-	sig_in_func224	1'd1

Signal No.	Input Signals	Default Value If Unassigned*	Same Input Signal from IO_MUX Core	Output Signals	Output Enable of Output Signals
225	-	-	-	sig_in_func225	1'd1
226	-	-	-	sig_in_func226	1'd1
227	-	-	-	sig_in_func227	1'd1
228	-	-	-	sig_in_func228	1'd1

A.3. Ethernet_MAC

Table 28: Ethernet_MAC

Pin Name	Function6	MII (int_osc)	MII (ext_osc)	RMII (int_osc)	RMII (ext_osc)
GPIO0	EMAC_TX_CLK	TX_CLK (I)	TX_CLK (I)	CLK_OUT(O)	EXT_OSC_CLK(I)
GPIO5	EMAC_RX_CLK	RX_CLK (I)	RX_CLK (I)	-	-
GPIO21	EMAC_TX_EN	TX_EN(O)	TX_EN(O)	TX_EN(O)	TX_EN(O)
GPIO19	EMAC_TXD0	TXD[0](O)	TXD[0](O)	TXD[0](O)	TXD[0](O)
GPIO22	EMAC_TXD1	TXD[1](O)	TXD[1](O)	TXD[1](O)	TXD[1](O)
MTMS	EMAC_TXD2	TXD[2](O)	TXD[2](O)	-	-
MTDI	EMAC_TXD3	TXD[3](O)	TXD[3](O)	-	-
MTCK	EMAC_RX_ER	RX_ER(I)	RX_ER(I)	-	-
GPIO27	EMAC_RX_DV	RX_DV(I)	RX_DV(I)	CRS_DV(I)	CRS_DV(I)
GPIO25	EMAC_RXD0	RXD[0](I)	RXD[0](I)	RXD[0](I)	RXD[0](I)
GPIO26	EMAC_RXD1	RXD[1](I)	RXD[1](I)	RXD[1](I)	RXD[1](I)
U0TXD	EMAC_RXD2	RXD[2](I)	RXD[2](I)	-	-
MTDO	EMAC_RXD3	RXD[3](I)	RXD[3](I)	-	-
GPIO16	EMAC_CLK_OUT	CLK_OUT(O)	-	CLK_OUT(O)	-
GPIO17	EMAC_CLK_OUT_180	CLK_OUT_180(O)	-	CLK_OUT_180(O)	-
GPIO4	EMAC_TX_ER	TX_ERR(O)*	TX_ERR(O)*	-	-
In GPIO Matrix*	-	MDC(O)	MDC(O)	MDC(O)	MDC(O)
In GPIO Matrix*	-	MDIO(IO)	MDIO(IO)	MDIO(IO)	MDIO(IO)
In GPIO Matrix*	-	CRS(I)	CRS(I)	-	-
In GPIO Matrix*	-	COL(I)	COL(I)	-	-

*Notes: 1. The GPIO Matrix can be any GPIO. 2. The TX_ERR (O) is optional.

A.4. IO_MUX

For the list of IO_MUX pins, please see the next page.

IO_MUX																								
Pin No.	Power Supply Pin	Analog Pin	Digital Pin	Power Domain	Analog Function0	Analog Function1	Analog Function2	RTC Function0	RTC Function1	Function0	Type	Function1	Type	Function2	Type	Function3	Type	Function4	Type	Function5	Type	Drive Strength (2'd2: 20 mA)	At Reset	After Reset
1	VDDA			VDDA supply in																				
2		LNA_IN		VDD3P3																				
3	VDD3P3			VDD3P3 supply in																				
4	VDD3P3			VDD3P3 supply in																				
5		SENSOR_VP	VDD3P3_RTC		ADC1_CH0	RTC_GPIO0		GPIO36	I		GPIO36	I											oe=0, ie=0	oe=0, ie=0
6		SENSOR_CAPP	VDD3P3_RTC		ADC1_CH1	RTC_GPIO1		GPIO37	I		GPIO37	I											oe=0, ie=0	oe=0, ie=0
7		SENSOR_CAPN	VDD3P3_RTC		ADC1_CH2	RTC_GPIO2		GPIO38	I		GPIO38	I											oe=0, ie=0	oe=0, ie=0
8		SENSOR_VN	VDD3P3_RTC		ADC1_CH3	RTC_GPIO3		GPIO39	I		GPIO39	I											oe=0, ie=0	oe=0, ie=0
9		CHIP_PU	VDD3P3_RTC																					
10		VDET_1	VDD3P3_RTC		ADC1_CH6	RTC_GPIO4		GPIO34	I		GPIO34	I											oe=0, ie=0	oe=0, ie=0
11		VDET_2	VDD3P3_RTC		ADC1_CH7	RTC_GPIO5		GPIO35	I		GPIO35	I											oe=0, ie=0	oe=0, ie=0
12		32K_XP	VDD3P3_RTC	XTAL_32K_P	ADC1_CH4	TOUCH9	RTC_GPIO9	GPIO32	I/O/T		GPIO32	I/O/T										2'd2	oe=0, ie=0	oe=0, ie=0
13																								
14																								
15																								
16																								
17																								
18																								
19																								
20																								
21																								
22																								
23																								
24																								
25																								
26	VDD_SDIO	GPIO16	VDD_SDIO							GPIO16	I/O/T		GPIO16	I/O/T	HS1_DATA4	I/O/T	U2RXD	I	EMAC_CLK_OUT	O	2'd2	oe=0, ie=0	oe=0, ie=1	
27			VDD_SDIO	supply out/in																				
28																								
29																								
30																								
31																								
32																								
33																								
34																								
35																								
36																								
37																								
38																								
39																								
40																								
41																								
42																								
43	VDDA																							
44		XTAL_N	VDDA																					
45		XTAL_P	VDDA																					
46	VDDA																							
47			CAP2	VDDA																				
48			CAP1	VDDA																				
Total Number	8	14	26																					

Notes:

- wpu: weak pull-up;
- wpd: weak pull-down;
- ie: input enable;
- oe: output enable;

•

Please see Table: Notes on ESP32 Pin Lists for more information. (请参考表：管脚清单说明。)

Revision History

Date	Version	Release Notes
2023.01	v4.2	<p>Major updates:</p> <ul style="list-style-type: none"> Removed contents about hall sensor according to PCN20221202 <p>Other Updates:</p> <ul style="list-style-type: none"> Added a note about limited applications of touch sensor in Section 4.1.4 <i>Touch Sensor</i>
2022.12	v4.1	<p>Added link to Xtensa® Instruction Set Architecture (ISA) Summary in Section 3.1.1: <i>CPU</i></p> <p>Updated the description about chip revision upgrade under Table 25</p>
2022.10	v4.0	<p>Updated the description in Section 1</p> <p>Added two notes below Table 3</p> <p>Added a new item to “Notes on power supply” in Section 2.3</p> <p>Updated Figure 10</p> <p>Added a new column “VDD_SDIO Voltage” in Table 25</p> <p>Updated the bit rates in Section 4.1.17</p> <p>Added Not Recommended for New Designs (NRND) label to the ESP32-S0WD variant</p>
2022.03	v3.9	<p>Added a new chip variant ESP32-D0WDR2-V3</p> <p>Added Table 2: <i>Pin-to-Pin Mapping Between Chip and Embedded Flash/PSRAM</i> and Table 3: <i>Connection Between Chip and External Flash/PSRAM</i></p> <p>Updated Figure 9: <i>QFN48 (5x5 mm) Package</i></p> <p>Updated Appendix A.4. IO_MUX</p> <p>Updated Table 12: <i>Peripheral Pin Configurations</i></p> <p>Provided links to ESP32 Technical Reference Manual in Section 3: <i>Functional Description</i></p>
2021.10	v3.8	<p>Upgraded ESP32-U4WDH variant from single-core to dual-core, see PCN-2021-021 (estimated effective date: December 2, 2021). The single-core version coexists with the new dual-core version around December 2, 2021. The physical product is subject to batch tracking.</p> <p>Added CoreMark® score in Section 1.4: <i>MCU and Advanced Features</i></p> <p>Updated the description to TWAI in Section 4.1.17: <i>TWAI Controller</i></p> <p>Added Not Recommended for New Designs (NRND) label to the ESP32-D0WDQ6-V3 variant</p> <p>Provided a link to Espressif Chip Package Information in Section 6: <i>Package Information</i></p> <p>Updated Section 1.3: <i>Bluetooth Key Features</i></p>
2021.07	v3.7	<p>Removed ESP32-D2WD variant</p> <p>Updated the wording in Section 3.6.1</p> <p>Updated pin function numbers starting from Function0</p> <p>Added Not Recommended for New Designs (NRND) label to ESP32-D0WD and ESP32-D0WDQ6 variants</p>

Date	Version	Release Notes
2021.03	V3.6	<p>Updated Figure 1: <i>Functional Block Diagram</i></p> <p>Updated Table 16: <i>Reliability Qualifications</i></p> <p>Updated Figure 4: <i>ESP32 Power Scheme</i></p> <p>Updated Table 14: <i>Recommended Operating Conditions</i></p> <p>Updated the notes below Table 4: <i>Description of ESP32 Power-up and Reset Timing Parameters</i></p> <p>Provided more information about TWAI® in Table 7, Table 12, Table 8, and Section 4.1</p>
2021.01	V3.5	<p>Updated the description for CAP2 from 3 nF to 3.3 nF</p> <p>Added TWAI® in Section 1.4.3: <i>Advanced Peripheral Interfaces</i></p> <p>Updated Figure 1: <i>Functional Block Diagram</i></p> <p>Updated the reset values for MTCK, MTMS, GPIO27 in Appendix IO_MUX</p>
2020.04	V3.4	<p>Added one chip variant: ESP32-U4WDH</p> <p>Updated some figures in Table 8, 18, 19, 21, 23, 24</p> <p>Added a note under Table 20</p>
2020.01	V3.3	<p>Added two chip variants: ESP32-D0WD-V3 and ESP32-D0WDQ6-V3.</p> <p>Added a note under Table 9.</p>
2019.10	V3.2	Updated Figure 5: <i>ESP32 Power-up and Reset Timing</i> .
2019.07	V3.1	<p>Added pin-pin mapping between ESP32-D2WD and the embedded flash under Table 1 <i>Pin Description</i>;</p> <p>Updated Figure 10 <i>ESP32 Part Number</i>.</p>
2019.04	V3.0	Added information about the setup and hold times for the strapping pins in Section 2.4: <i>Strapping Pins</i> .
2019.02	V2.9	<p>Applied new formatting to Table 1: <i>Pin Description</i>;</p> <p>Fixed typos with respect to the ADC1 channel mappings in Table 12: <i>Peripheral Pin Configurations</i>.</p>
2019.01	V2.8	<p>Changed the RF power control range in Table 20, Table 22 and Table 24 from –12 ~ +12 to –12 ~ +9 dBm;</p> <p>Small text changes.</p>
2018.11	V2.7	<p>Updated Section 1.5;</p> <p>Updated pin statuses at reset and after reset in Table IO_MUX.</p>
2018.10	V2.6	Updated QFN package drawings in Chapter 6: <i>Package Information</i> .
2018.08	V2.5	<ul style="list-style-type: none"> Added "Cumulative IO output current" entry to Table 13: <i>Absolute Maximum Ratings</i>; Added more parameters to Table 15: <i>DC Characteristics</i>; Changed the power domain names in Table IO_MUX to be consistent with the pin names.
2018.07	V2.4	<ul style="list-style-type: none"> Deleted information on Packet Traffic Arbitration (PTA); Added Figure 5: <i>ESP32 Power-up and Reset Timing</i> in Section 2.3: <i>Power Scheme</i>; Added the power consumption of dual-core SoCs in Table 8: <i>Power Consumption by Power Modes</i>; Updated section 4.1.2: <i>Analog-to-Digital Converter (ADC)</i>.

Date	Version	Release Notes
2018.06	V2.3	<p>Added the power consumption at CPU frequency of 160 MHz in Table 8: Power Consumption by Power Modes.</p>
2018.05	V2.2	<ul style="list-style-type: none"> • Changed the voltage range of VDD3P3_RTC from 1.8-3.6V to 2.3-3.6V in Table 1: Pin Description; • Updated Section 2.3: Power Scheme; • Updated Section 3.1.3: External Flash and SRAM; • Updated Table 8: Power Consumption by Power Modes; • Deleted content about temperature sensor; <p>Changes to electrical characteristics:</p> <ul style="list-style-type: none"> • Updated Table 13: Absolute Maximum Ratings; • Added Table 14: Recommended Operating Conditions; • Added Table 15: DC Characteristics; • Added Table 16: Reliability Qualifications; • Updated the values of "Gain control step" and "Adjacent channel transmit power" in Table 20: Transmitter Characteristics - Basic Data Rate; • Updated the values of "Gain control step", "$\pi/4$ DQPSK modulation accuracy", "8 DPSK modulation accuracy" and "In-band spurious emissions" in Table 22: Transmitter Characteristics – Enhanced Data Rate; • Updated the values of "Gain control step", "Adjacent channel transmit power" in Table 24: Transmitter Characteristics - BLE.
2018.01	V2.1	<ul style="list-style-type: none"> • Deleted software-specific features; • Deleted information on LNA pre-amplifier; • Specified the CPU speed and flash speed of ESP32-D2WD; • Added notes to Section 2.3: Power Scheme.
2017.12	V2.0	Added a note on the sequence of pin number in Chapter 6.
2017.10	V1.9	<ul style="list-style-type: none"> • Updated the description of the pin CHIP_PU in Table 1; • Added a note to Section 2.3: Power Scheme; • Updated the description of the chip's system reset in Section 2.4: Strapping Pins; • Added a description of antenna diversity and selection to Section 3.5.1; • Deleted "Association sleep pattern" in Table 8 and added notes to Active sleep and Modem-sleep.
2017.08	V1.8	<ul style="list-style-type: none"> • Added Table 4.2 in Section 4; • Corrected a typo in Figure 1.

Date	Version	Release Notes
2017.08	V1.7	<ul style="list-style-type: none"> Changed the transmitting power to +12 dBm; the sensitivity of NZIF receiver to -97 dBm in Section 1.3; Added a note to Table 1 Pin Description; Added 160 MHz clock frequency in section 3.1.1; Changed the transmitting power from 21 dBm to 20.5 dBm in Section 3.5.1; Changed the dynamic control range of class-1, class-2 and class-3 transmit output powers to "up to 24 dBm"; and changed the dynamic range of NZIF receiver sensitivity to "over 97 dB" in Section 3.6.1; Updated Table 8: Power Consumption by Power Modes, and added two notes to it; Updated sections 4.1.1, 4.1.8; Updated Table 13: Absolute Maximum Ratings; Updated Table 17: RF Power Consumption Specifications, and changed the duty cycle on which the transmitters' measurements are based by 50%. Updated Table 18: Wi-Fi Radio Characteristics and added a note on "Output impedance" to it; Updated parameter "Sensitivity" in Table 19, 21, 23; Updated parameters "RF transmit power" and "RF power control range", and added parameter "Gain control step" in Table 20, 22, 24; Deleted Chapters: "Touch Sensor" and "Code Examples"; Added a link to certification download.
2017.06	V1.6	<p>Corrected two typos:</p> <ul style="list-style-type: none"> Changed the number of external components to 20 in Section 1.1.2; Changed the number of GPIO pins to 34 in Section 4.1.1.
2017.06	V1.5	<ul style="list-style-type: none"> Changed the power supply range in Section: 1.4.1 CPU and Memory; Updated the note in Section 2.3: Power Scheme; Updated Table 13: Absolute Maximum Ratings; Changed the drive strength values of the digital output pins in Note 8, in Table 26: Notes on ESP32 Pin Lists; Added the option to subscribe for notifications of documentation changes.
2017.05	V1.4	<ul style="list-style-type: none"> Added a note to the frequency of the external crystal oscillator in Section 1.4.2: Clocks and Timers; Added a note to Section 2.4: Strapping Pins; Updated Section 3.7: RTC and Low-Power Management; Changed the maximum driving capability from 12 mA to 80 mA, in Table 13: Absolute Maximum Ratings; Changed the input impedance value of 50Ω, in Table 18: Wi-Fi Radio Characteristics, to output impedance value of $30+j10 \Omega$; Added a note to No.8 in Table 26: Notes on ESP32 Pin Lists; Deleted GPIO20 in Table IO_MUX.
2017.04	V1.3	<ul style="list-style-type: none"> Added Appendix: ESP32 Pin Lists; Updated Table: Wi-Fi Radio Characteristics; Updated Figure: ESP32 Pin Layout (for QFN 5*5).

Date	Version	Release Notes
2017.03	V1.2	<ul style="list-style-type: none">• Added a note to Table: Pin Description;• Updated the note in Section: Internal Memory.
2017.02	V1.1	<ul style="list-style-type: none">• Added Chapter: Part Number and Ordering Information;• Updated Section: MCU and Advanced Features;• Updated Section: Block Diagram;• Updated Chapter: Pin Definitions;• Updated Section: CPU and Memory;• Updated Section: Audio PLL Clock;• Updated Section: Absolute Maximum Ratings;• Updated Chapter: Package Information;• Updated Chapter: Learning Resources.
2016.08	V1.0	First release.



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