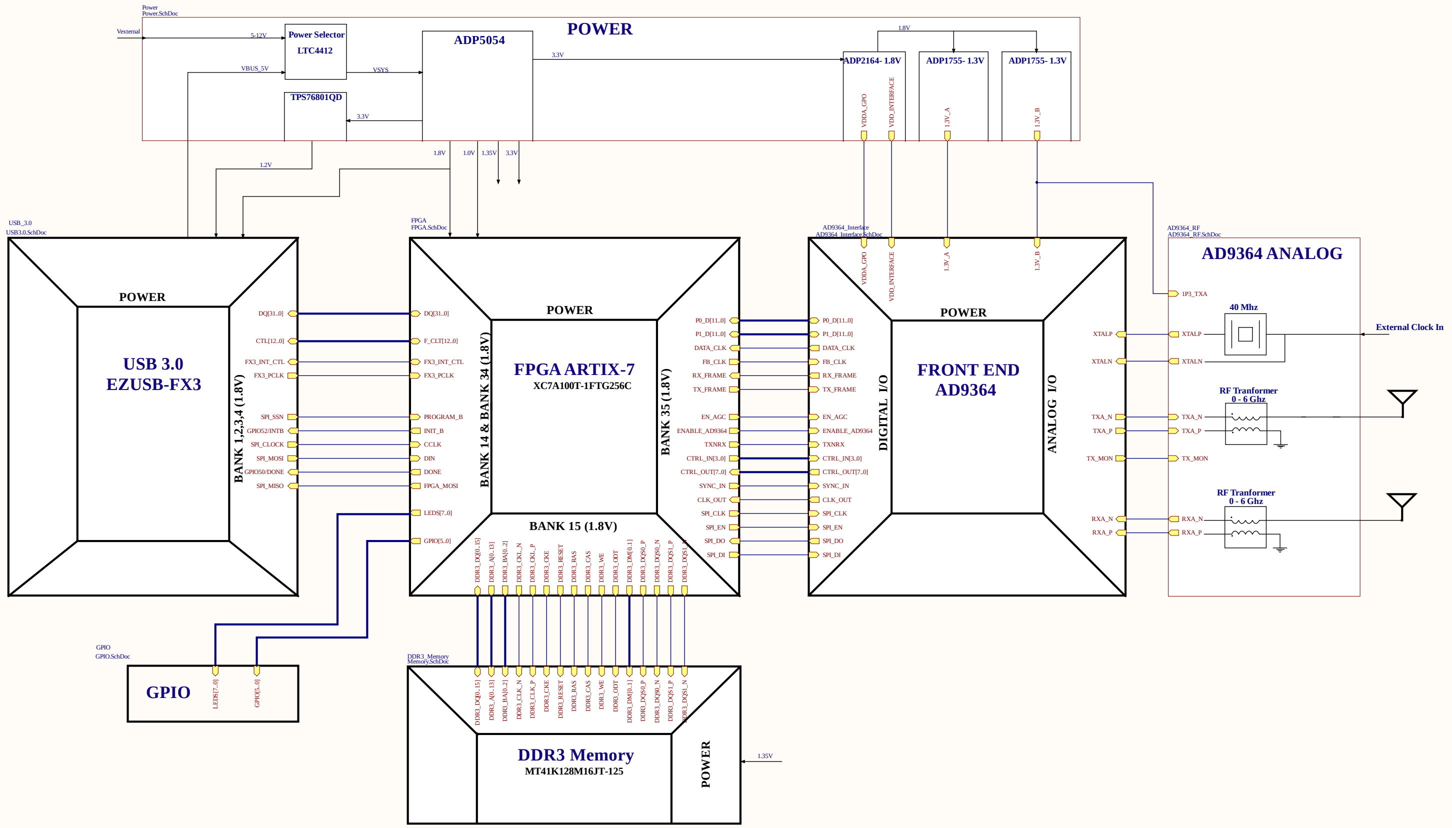
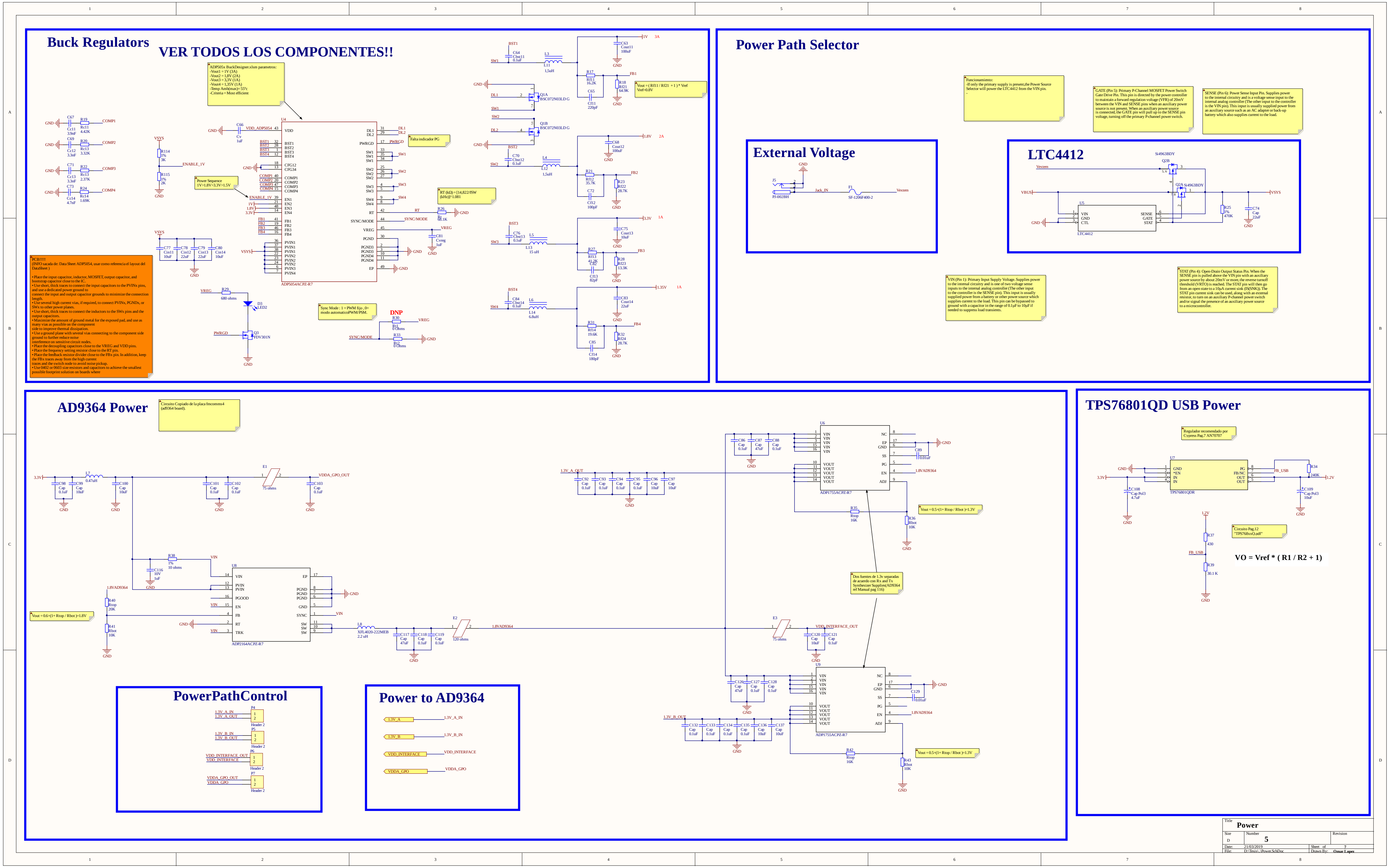


Title
Block Diagram

Size	Number	Revision
D	**0**	

Date: 21/03/2019 Sheet of 7
File: D:\Tesis\..\Intro.SchDoc Drawn By: **Omar Lopez**



Buck Regulators

VER TODOS LOS COMPONENTES!!

ADP505x BuckDesigner.xlsm parametros:
-Vout1 = 1V (3A)
-Vout2 = 1,8V (2A)
-Vout3 = 3,3V (1A)
-Vout4 = 1,35V (1A)
-Temp Amb(max)= 55°c
-Criteria = Most efficient

Power Sequence
1V>1.8V>3.3V>1.5V

Falta indicador PG

RT (kΩ) = [14,822/fSW (kHz)]^1.081

Vout = (Rf11 / Rf21 + 1) * Vref
Vref=0.8V

Sync Mode : 1 = PWM fijo , 0= modo automaticoPWM/PSM.

PCB!!!!!
(INFO sacada de: Data Sheet ADP5054, usar como referencia el layout del DataSheet)

- Place the input capacitor, inductor, MOSFET, output capacitor, and bootstrap capacitor close to the IC.
- Use short, thick traces to connect the input capacitors to the PVINx pins, and use a dedicated power ground to connect the input and output capacitor grounds to minimize the connection length.
- Use several high current vias, if required, to connect PVINx, PGNDx, or SWx to other power planes.
- Use short, thick traces to connect the inductors to the SWx pins and the output capacitors.
- Maximize the amount of ground metal for the exposed pad, and use as many vias as possible on the component side to improve thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Place the decoupling capacitors close to the VREG and VDD pins.
- Place the frequency setting resistor close to the RT pin.
- Place the feedback resistor divider close to the FBx pin. In addition, keep the FBx traces away from the high current traces and the switch node to avoid noise pickup.
- Use 0402 or 0603 size resistors and capacitors to achieve the smallest possible footprint solution on boards where

Power Path Selector

Funcionamiento:
-If only the primary supply is present,the Power Source Selector will power the LTC4412 from the VIN pin.
-

GATE (Pin 5): Primary P-Channel MOSFET Power Switch Gate Drive Pin. This pin is directed by the power controller to maintain a forward regulation voltage (VFR) of 20mV between the VIN and SENSE pins when an auxiliary power source is not present. When an auxiliary power source is connected, the GATE pin will pull up to the SENSE pin voltage, turning off the primary P-channel power switch.

SENSE (Pin 6): Power Sense Input Pin. Supplies power to the internal circuitry and is a voltage sense input to the internal analog controller (The other input to the controller is the VIN pin). This input is usually supplied power from an auxiliary source such as an AC adapter or back-up battery which also supplies current to the load.

External Voltage

LTC4412

VIN (Pin 1): Primary Input Supply Voltage. Supplies power to the internal circuitry and is one of two voltage sense inputs to the internal analog controller (The other input to the controller is the SENSE pin). This input is usually supplied power from a battery or other power source which supplies current to the load. This pin can be bypassed to ground with a capacitor in the range of 0.1µF to 10µF if needed to suppress load transients.

STAT (Pin 4): Open-Drain Output Status Pin. When the SENSE pin is pulled above the VIN pin with an auxiliary power source by about 20mV or more, the reverse turnoff threshold (VRTO) is reached. The STAT pin will then go from an open state to a 10µA current sink (IS(SNK)). The STAT pin current sink can be used, along with an external resistor, to turn on an auxiliary P-channel power switch and/or signal the presence of an auxiliary power source to a microcontroller.

AD9364 Power

Circuito Copiado de la placa fmcomms4 (ad9364 board).

Vout = 0.6×(1+ Rtop / Rbot)=1.8V

Vout = 0.5×(1+ Rtop / Rbot)=1.3V

Dos fuentes de 1.3v separadas de acuerdo con Rx and Tx Synthesizer Supplies(AD9364 ref Manual pag 116)

Vout = 0.5×(1+ Rtop / Rbot)=1.3V

PowerPathControl

Power to AD9364

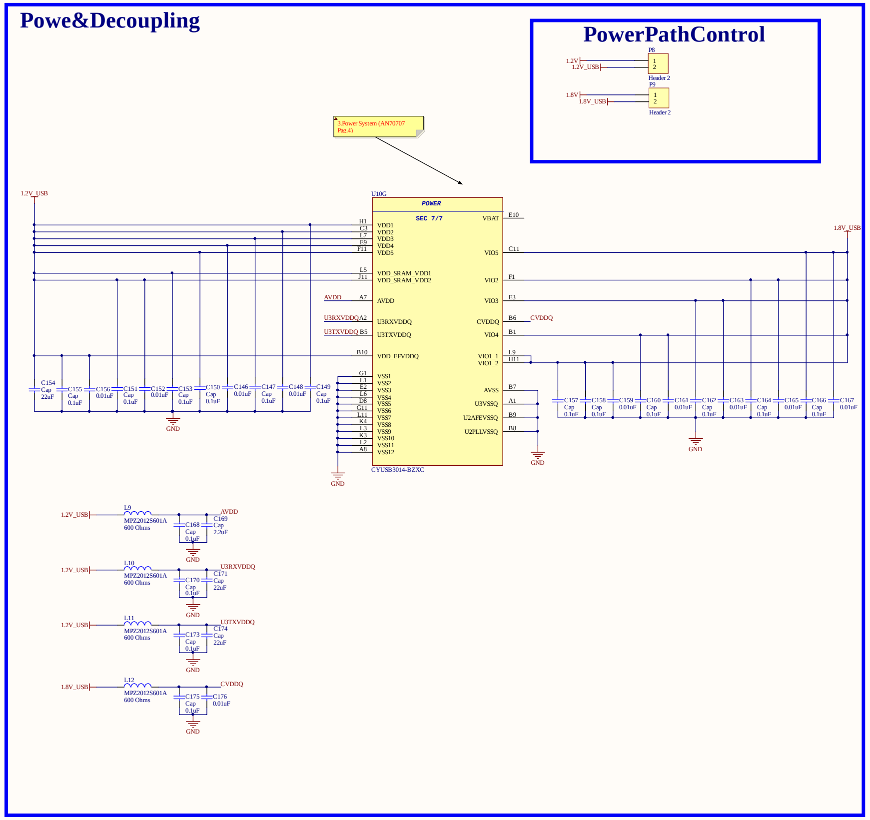
TPS76801QD USB Power

Regulador recomendado por Cypress Pag.7 AN70707

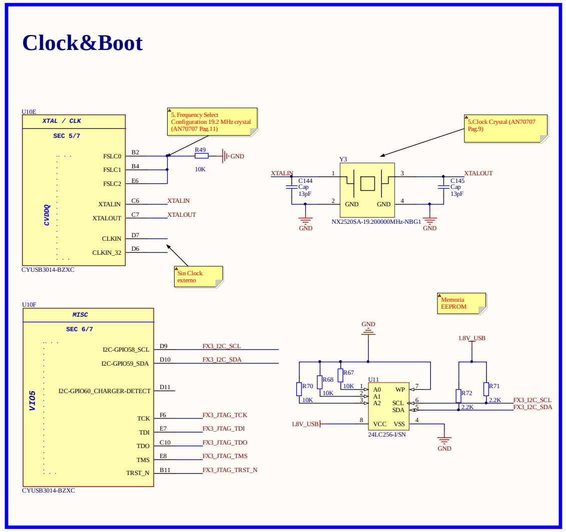
Circuito Pag.12 "TPS768xxQ.pdf"

VO = Vref * (R1 / R2 + 1)

Title	Power	
Size: D	Number: 5	Revision
Date: 21/03/2019		Sheet of 7
File: D:\Tesis\..\Power.SchDoc		Drawn By: **Omar Lopez**



3.Power System (AN70707 Pag.4)

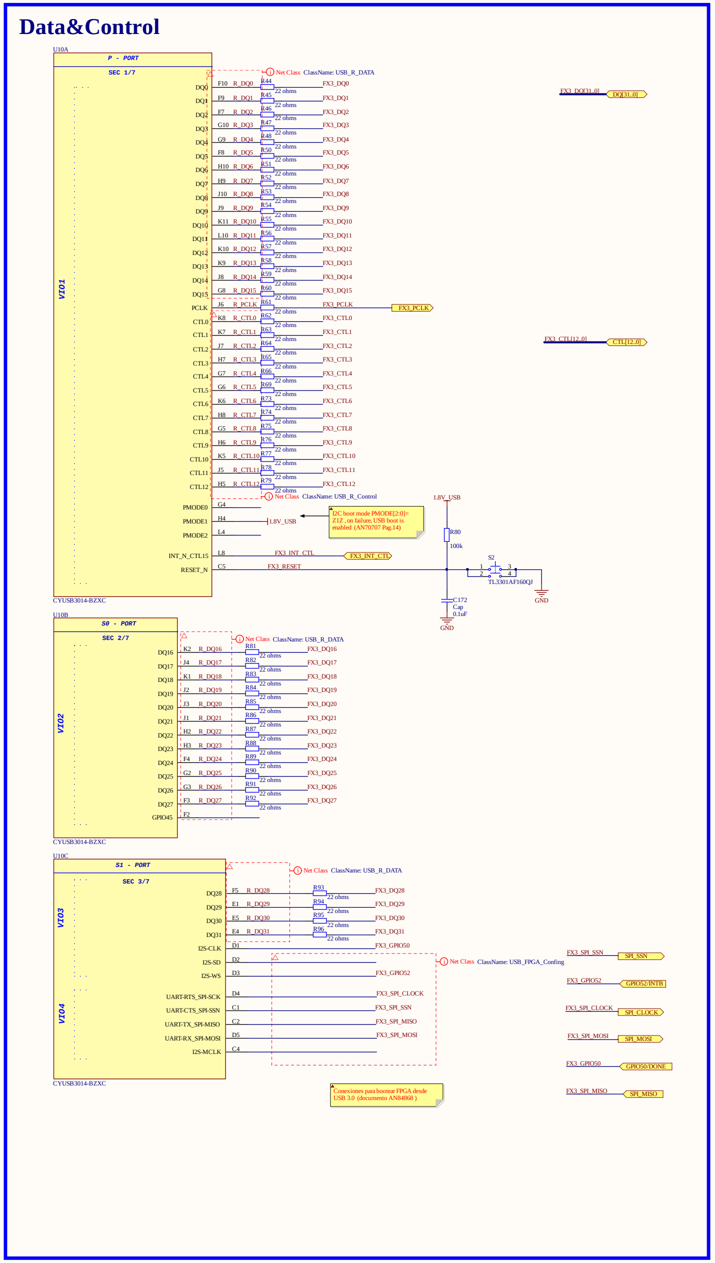


5. Frequency Select Configuration 19.2 MHz crystal (AN70707 Pag.11)

5.Clock Crystal (AN70707 Pag.9)

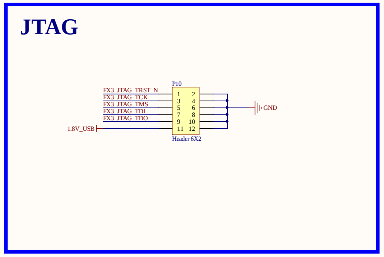
Sin Clock externo

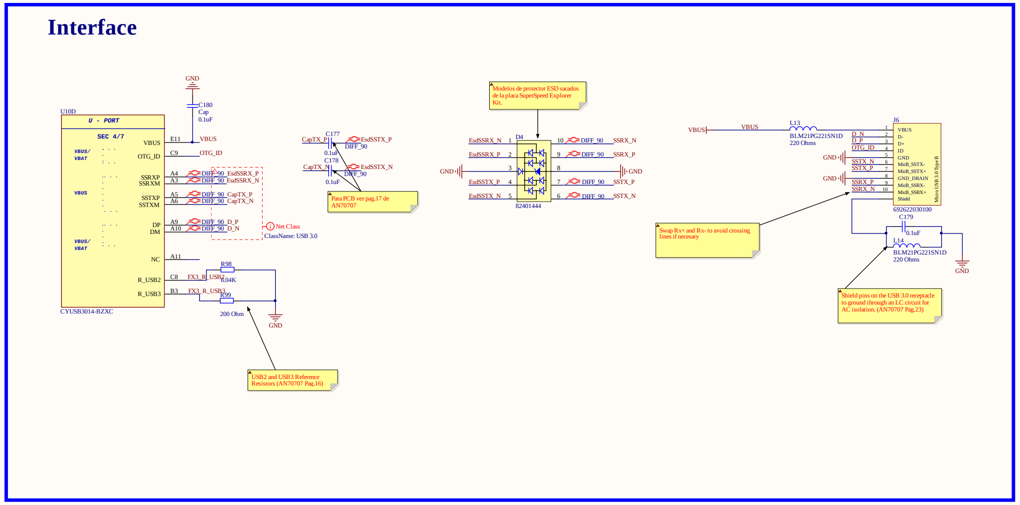
Memoria EEPROM



I2C boot mode PMODE[2:0]= Z1Z , on failure, USB boot is enabled (AN70707 Pag.14)

Conexiones para bootear FPGA desde USB 3.0 (documento AN84868)





USB2 and USB3 Reference Resistors (AN70707 Pag.16)

Para PCB ver pag.17 de AN70707

Modelos de protector ESD sacados de la placa SuperSpeed Explorer Kit.

Swap Rx+ and Rx- to avoid crossing lines if necessary

Shield pins on the USB 3.0 receptacle to ground through an LC circuit for AC isolation. (AN70707 Pag.23)

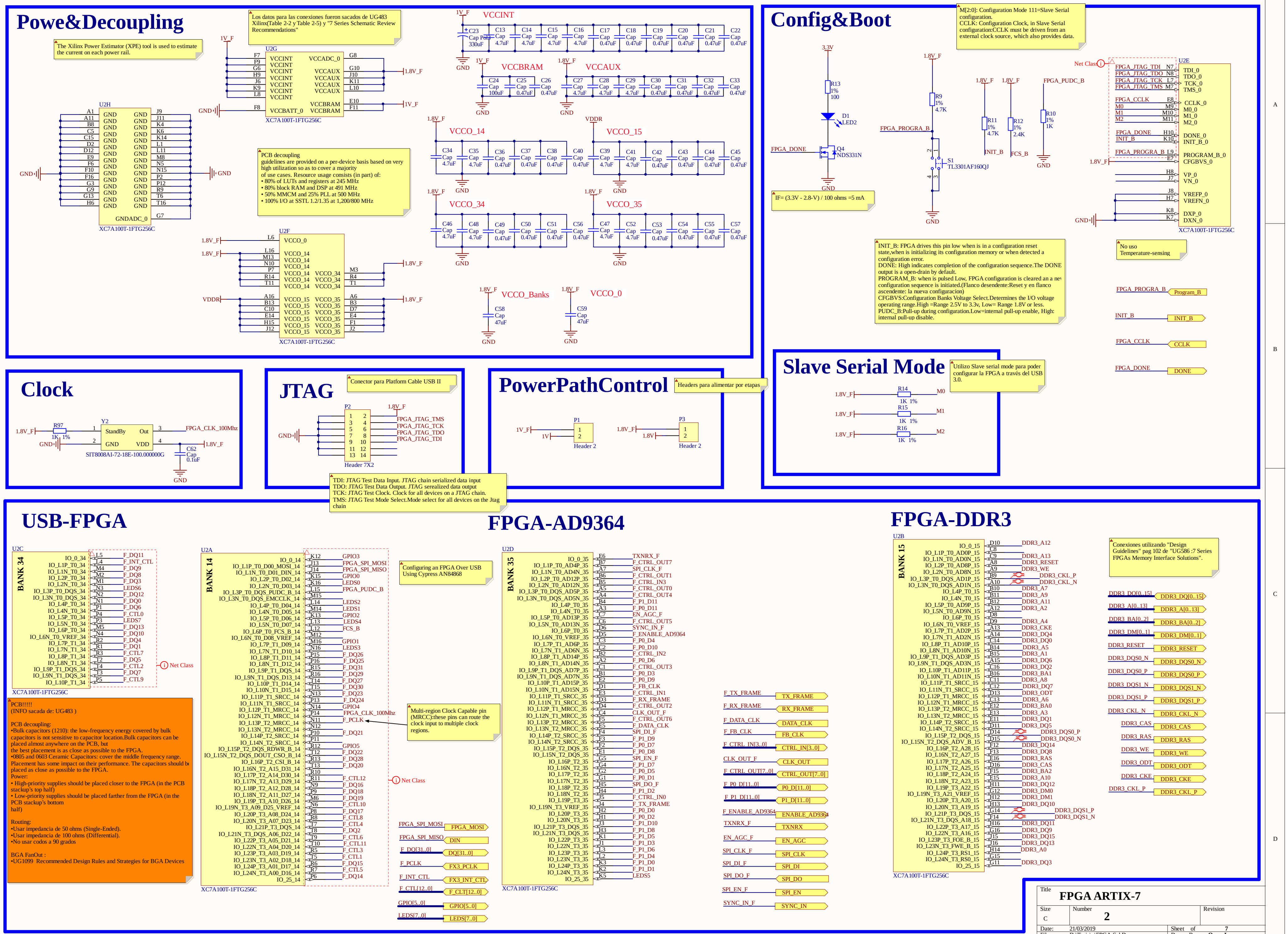
PCB!!!!!
(INFO sacada de: EZ-USB® FX3™/FX3S™ Hardware Design Guidelines and Schematic Checklist AN70707)

- The polarity can be swapped on the USB 3.0 differential pair
- Keep the crystal trace as short as possible. Place the crystal within 2 cm from FX3.
- Keep the power traces away from Hi-Speed data and clock lines.
- Keep power traces as short as possible. Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.
- Use split planes on the powerlayer for different power domains.
- The number of layers on the PCB should at least be four. To maintain 90 Ω differential impedance, use a solid reference power plane.
- At least one immediate plane underneath these AC coupling capacitors should have a cut out in the shape of these capacitors to avoid extra capacitance on the lines because of the capacitor pads

Routing:

- Power trace widths should be ≥25 mils to reduce inductance.
- Keep the USB signal line impedance at 90 Ω differential (±7%).
- Minimize the trace length of USB lines as much as possible (<3 inches).
- All data lines, command, and clock lines should be length-matched.
- The maximum frequency of the GPIF II interface is 100 MHz. It is recommended that all lines on the GPIF II bus could be length matched within 500 mils

Title	USB 3.0		
Size D	Number 1		Revision
Date:	21/03/2019	Sheet of	7
File:	D:\Tesis\..\USB3.0.SchDoc	Drawn By:	**Omar Lopez**



Los datos para las conexiones fueron sacados de UG483 Xilinx(Table 2-2 y Table 2-5) y "7 Series Schematic Review Recommendations"

The Xilinx Power Estimator (XPE) tool is used to estimate the current on each power rail.

PCB decoupling
guidelines are provided on a per-device basis based on very high utilization so as to cover a majority
of use cases. Resource usage consists (in part) of:
- 80% of LUTs and registers at 245 MHz
- 80% block RAM and DSP at 491 MHz
- 50% MMCM and 25% PLL at 500 MHz
- 100% I/O at SSTL 1.2/1.35 at 1,200/800 MHz

M[2:0]: Configuration Mode 111=Slave Serial configuration.
CCLK: Configuration Clock, in Slave Serial configuration:CCLK must be driven from an external clock source, which also provides data.

IF= (3.3V - 2.8-V) / 100 ohms =5 mA

INIT_B: FPGA drives this pin low when is in a configuration reset state,when is initializing its configuration memory or when detected a configuration error.
DONE: High indicates completion of the configuration sequence.The DONE output is a open-drain by default.
PROGRAM_B: when is pulsed Low, FPGA configuration is cleared an a ne configuration sequence is initiated.(Flanco desendente:Reset y en flanco ascendente: la nueva configuracion)
CFGBVS:Configuration Banks Voltage Select.Determines the I/O voltage operating range.High =Range 2.5V to 3.3v, Low= Range 1.8V or less.
PUDC_B:Pull-up during configuration.Low=internal pull-up enable, High: internal pull-up disable.

No uso
Temperature-sensing

Utilizo Slave serial mode para poder configurar la FPGA a través del USB 3.0.

Conector para Platform Cable USB II

Headers para alimentar por etapas

TDI: JTAG Test Data Input. JTAG chain serialized data input
TDO: JTAG Test Data Output. JTAG serealized data output
TCK: JTAG Test Clock. Clock for all devices on a JTAG chain.
TMS: JTAG Test Mode Select.Mode select for all devices on the Jtag chain

Configuring an FPGA Over USB Using Cypress AN84868

Multi-region Clock Capable pin (MRCC):these pins can route the clock input to multiple clock regions.

Conexiones utilizando "Design Guidelines" pag 102 de "UG586 :7 Series FPGAs Memory Interface Solutions".

PCB!!!!!
(INFO sacada de: UG483)

PCB decoupling:
•Bulk capacitors (1210): the low-frequency energy covered by bulk capacitors is not sensitive to capacitor location.Bulk capacitors can be placed almost anywhere on the PCB, but
the best placement is as close as possible to the FPGA.
•0805 and 0603 Ceramic Capacitors: cover the middle frequency range. Placement has some impact on their performance. The capacitors should be placed as close as possible to the FPGA.
Power:
• High-priority supplies should be placed closer to the FPGA (in the PCB stackup's top half)
• Low-priority supplies should be placed farther from the FPGA (in the PCB stackup's bottom
half)

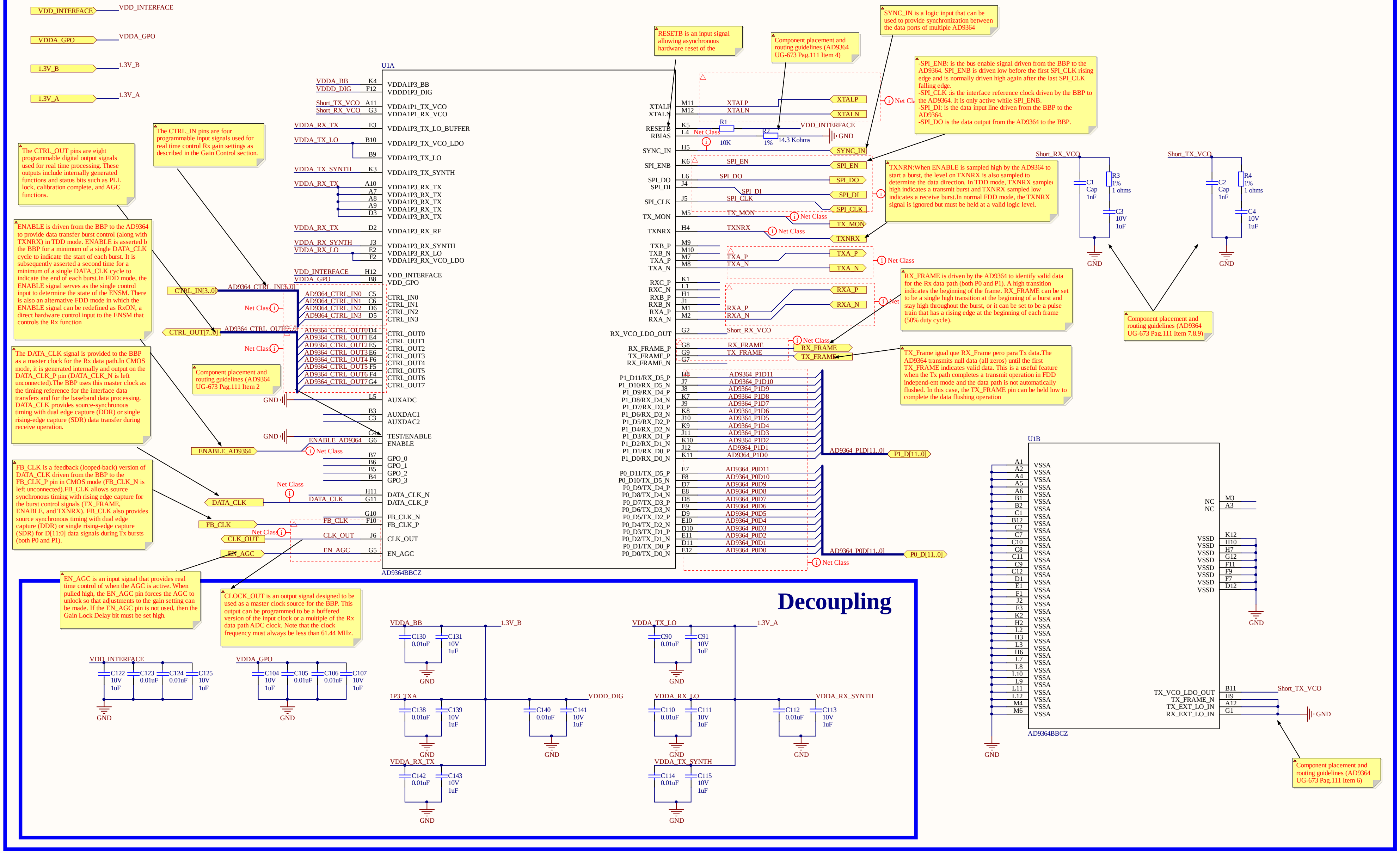
Routing:
•Usar impedancia de 50 ohms (Single-Ended).
•Usar impedancia de 100 ohms (Differential).
•No usar codos a 90 grados

BGA FanOut :
•UG1099 Recommended Design Rules and Strategies for BGA Devices

Title **FPGA ARTIX-7**
Size C
Number **2**
Revision
Date: 21/03/2019
Sheet of **7**
File: D:\Tesis\..\FPGA.SchDoc
Drawn By: **Omar Lopez**

AD9364 Interface

CMOS MODE DATA PATH AND CLOCK SIGNALS



The CTRL_OUT pins are eight programmable digital output signals used for real time processing. These outputs include internally generated functions and status bits such as PLL lock, calibration complete, and AGC functions.

The CTRL_IN pins are four programmable input signals used for real time control Rx gain settings as described in the Gain Control section.

ENABLE is driven from the BBP to the AD9364 to provide data transfer burst control (along with TXNRX) in TDD mode. ENABLE is asserted b the BBP for a minimum of a single DATA_CLK cycle to indicate the start of each burst. It is subsequently asserted a second time for a minimum of a single DATA_CLK cycle to indicate the end of each burst.In FDD mode, the ENABLE signal serves as the single control input to determine the state of the ENSM. There is also an alternative FDD mode in which the ENABLE signal can be redefined as RxON, a direct hardware control input to the ENSM that controls the Rx function

The DATA_CLK signal is provided to the BBP as a master clock for the Rx data path.In CMOS mode, it is generated internally and output on the DATA_CLK_P pin (DATA_CLK_N is left unconnected).The BBP uses this master clock as the timing reference for the interface data transfers and for the baseband data processing. DATA_CLK provides source-synchronous timing with dual edge capture (DDR) or single rising-edge capture (SDR) data transfer during receive operation.

Component placement and routing guidelines (AD9364 UG-673 Pag.111 Item 2)

FB_CLK is a feedback (looped-back) version of DATA_CLK driven from the BBP to the FB_CLK_P pin in CMOS mode (FB_CLK_N is left unconnected).FB_CLK allows source synchronous timing with rising edge capture for the burst control signals (TX_FRAME, ENABLE, and TXNRX). FB_CLK also provides source synchronous timing with dual edge capture (DDR) or single rising-edge capture (SDR) for D[11:0] data signals during Tx bursts (both P0 and P1).

EN_AGC is an input signal that provides real time control of when the AGC is active. When pulled high, the EN_AGC pin forces the AGC to unlock so that adjustments to the gain setting can be made. If the EN_AGC pin is not used, then the Gain Lock Delay bit must be set high.

CLOCK_OUT is an output signal designed to be used as a master clock source for the BBP. This output can be programmed to be a buffered version of the input clock or a multiple of the Rx data path ADC clock. Note that the clock frequency must always be less than 61.44 MHz.

RESETB is an input signal allowing asynchronous hardware reset of the

Component placement and routing guidelines (AD9364 UG-673 Pag.111 Item 4)

SYNC_IN is a logic input that can be used to provide synchronization between the data ports of multiple AD9364

-SPI_ENB: is the bus enable signal driven from the BBP to the AD9364. SPI_ENB is driven low before the first SPI_CLK rising edge and is normally driven high again after the last SPI_CLK falling edge.
-SPI_CLK :is the interface reference clock driven by the BBP to the AD9364. It is only active while SPI_ENB.
-SPI_DI: is the data input line driven from the BBP to the AD9364.
-SPI_DO is the data output from the AD9364 to the BBP.

TXNRN:When ENABLE is sampled high by the AD9364 to start a burst, the level on TXNRX is also sampled to determine the data direction. In TDD mode, TXNRX sampled high indicates a transmit burst and TXNRX sampled low indicates a receive burst.In normal FDD mode, the TXNRX signal is ignored but must be held at a valid logic level.

RX_FRAME is driven by the AD9364 to identify valid data for the Rx data path (both P0 and P1). A high transition indicates the beginning of the frame. RX_FRAME can be set to be a single high transition at the beginning of a burst and stay high throughout the burst, or it can be set to be a pulse train that has a rising edge at the beginning of each frame (50% duty cycle).

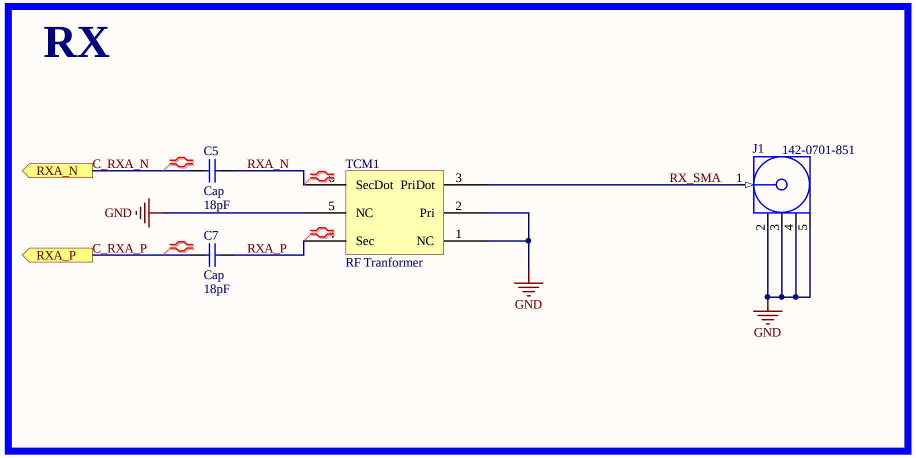
Component placement and routing guidelines (AD9364 UG-673 Pag.111 Item 7,8,9)

TX_Frame igual que RX_Frame pero para Tx data.The AD9364 transmits null data (all zeros) until the first TX_FRAME indicates valid data. This is a useful feature when the Tx path completes a transmit operation in FDD independ-ent mode and the data path is not automatically flushed. In this case, the TX_FRAME pin can be held low to complete the data flushing operation

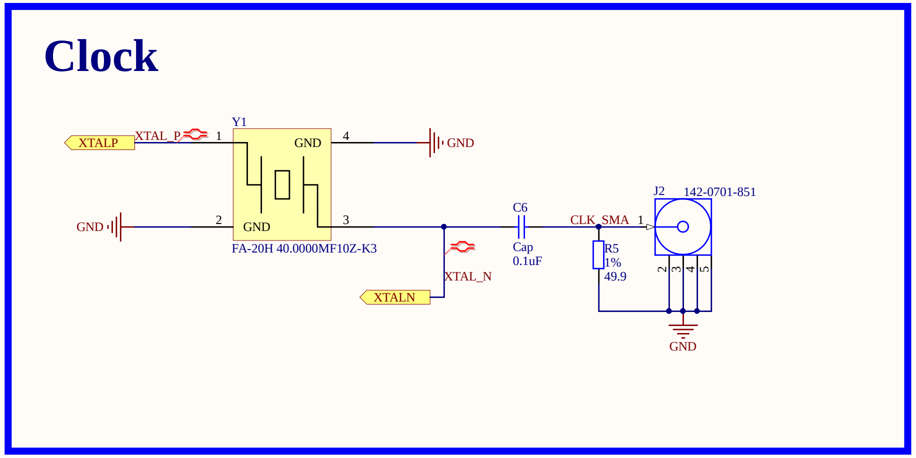
Component placement and routing guidelines (AD9364 UG-673 Pag.111 Item 6)

Title	AD9364 Interface	
Size C	Number 3	Revision
Date: 21/03/2019	Sheet 7 of	
File: D:\Tesis\..\AD9364_Interface.SchDoc	Drawn By: Omar Lopez	

RX



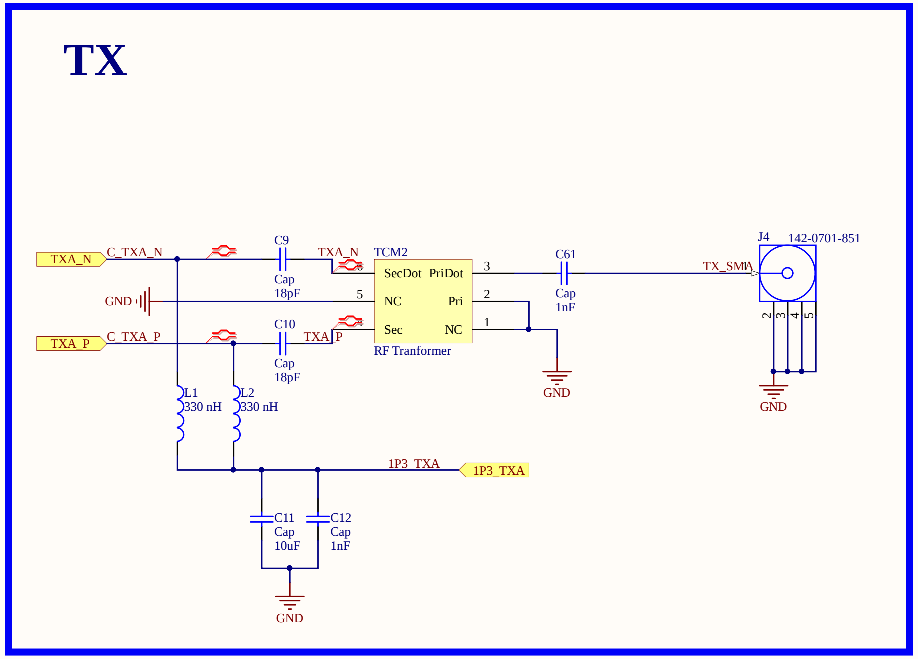
Clock



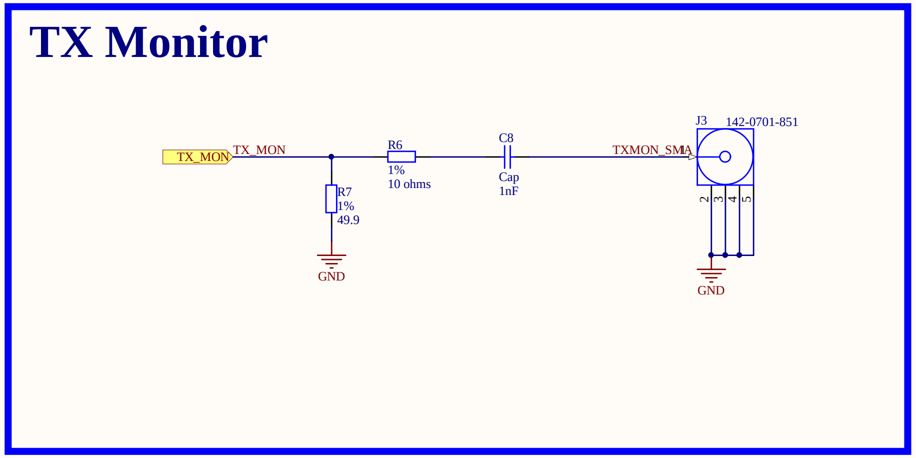
Posible mejoras:
1.utilizar Balum para cada diferentes rangos de frequencia y un selector de RF.
2.Amplificador PGA-102 a la salida de TX

Balum Link

TX



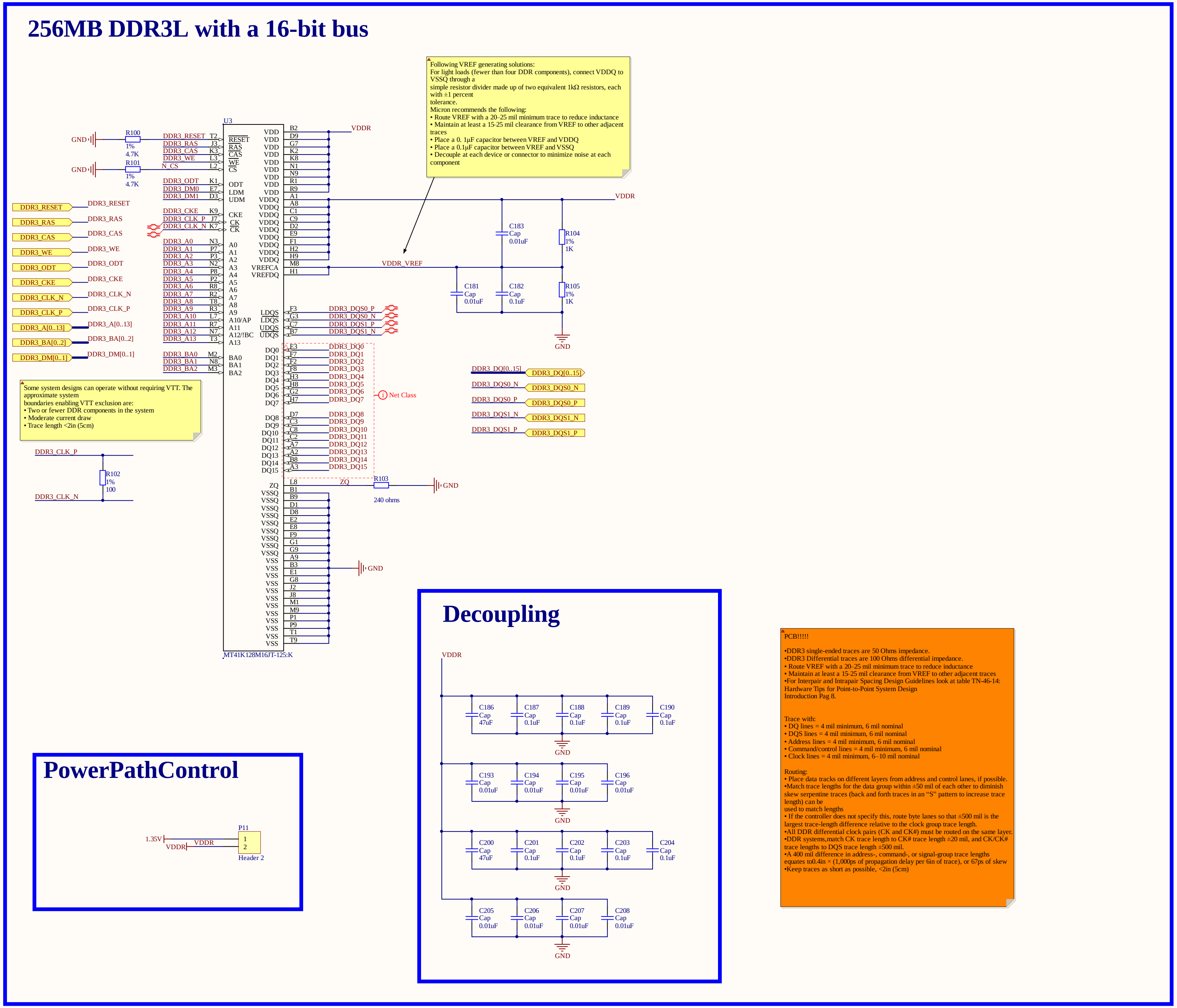
TX Monitor



Title **AD9364 RF**

Size A3
Number **4**
Revision

Date: 21/03/2019
Sheet of 7
File: D:\Tesis\..\AD9364_RF.SchDoc
Drawn By: **Omar Lopez**



256MB DDR3L with a 16-bit bus

Following VREF generating solutions:
For light loads (fewer than four DDR components), connect VDDQ to VSSQ through a
simple resistor divider made up of two equivalent 1kΩ resistors, each with ±1 percent
tolerance.
Micron recommends the following:
- Route VREF with a 20–25 mil minimum trace to reduce inductance
- Maintain at least a 15-25 mil clearance from VREF to other adjacent traces
- Place a 0. 1µF capacitor between VREF and VDDQ
- Place a 0.1µF capacitor between VREF and VSSQ
- Decouple at each device or connector to minimize noise at each component

Some system designs can operate without requiring VTT. The approximate system
boundaries enabling VTT exclusion are:
- Two or fewer DDR components in the system
- Moderate current draw
- Trace length <2in (5cm)

Decoupling

PowerPathControl

PCB!!!!!

- •DDR3 single-ended traces are 50 Ohms impedance.
- •DDR3 Differential traces are 100 Ohms differential impedance.
- Route VREF with a 20–25 mil minimum trace to reduce inductance
- Maintain at least a 15-25 mil clearance from VREF to other adjacent traces
- •For Interpair and Intrapair Spacing Design Guidelines look at table TN-46-14: Hardware Tips for Point-to-Point System Design
Introduction Pag 8.

Trace with:
- DQ lines = 4 mil minimum, 6 mil nominal
- DQS lines = 4 mil minimum, 6 mil nominal
- Address lines = 4 mil minimum, 6 mil nominal
- Command/control lines = 4 mil minimum, 6 mil nominal
- Clock lines = 4 mil minimum, 6–10 mil nominal

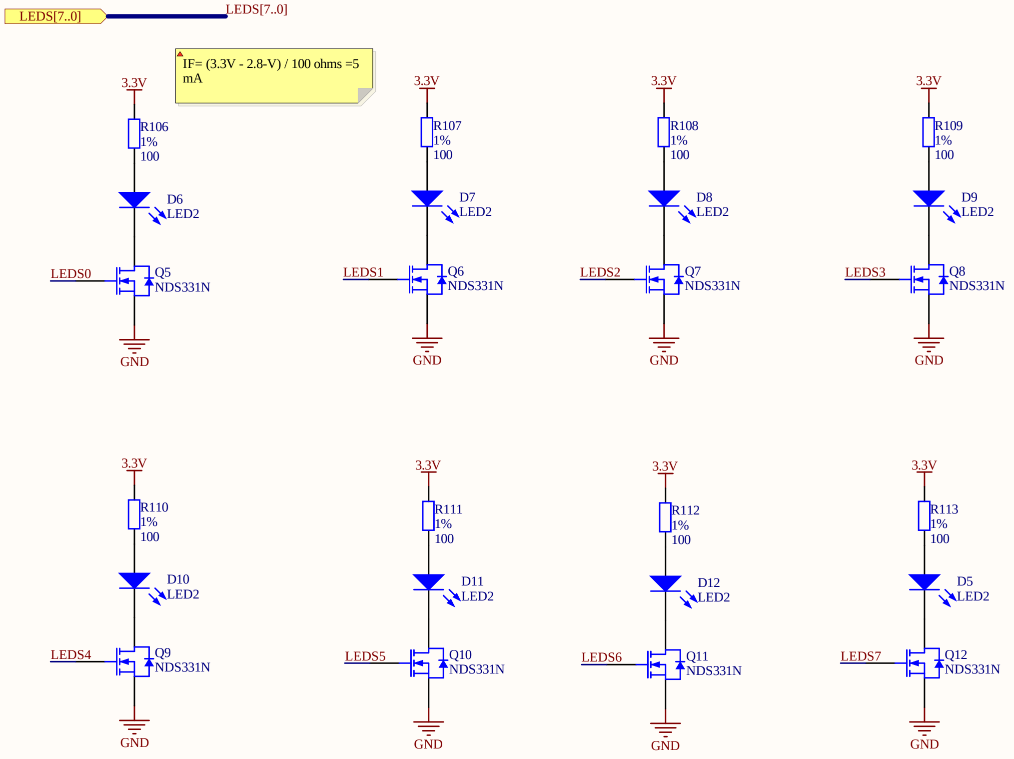
Routing:
- Place data tracks on different layers from address and control lanes, if possible.
- •Match trace lengths for the data group within ±50 mil of each other to diminish skew serpentine traces (back and forth traces in an “S” pattern to increase trace length) can be
used to match lengths
- If the controller does not specify this, route byte lanes so that ±500 mil is the largest trace-length difference relative to the clock group trace length.
- •All DDR differential clock pairs (CK and CK#) must be routed on the same layer.
- •DDR systems,match CK trace length to CK# trace length ±20 mil, and CK/CK# trace lengths to DQS trace length ±500 mil.
- •A 400 mil difference in address-, command-, or signal-group trace lengths equates to0.4in × (1,000ps of propagation delay per 6in of trace), or 67ps of skew
- •Keep traces as short as possible, <2in (5cm)

Title **Memory**

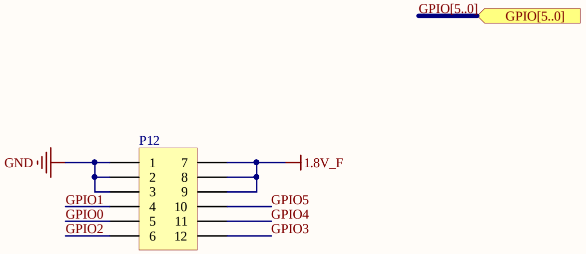
Size C
Number **6**
Revision

Date: 21/03/2019
Sheet of **7**
File: D:\Tesis\..\Memory.SchDoc
Drawn By: **Omar Lopez**

Leds



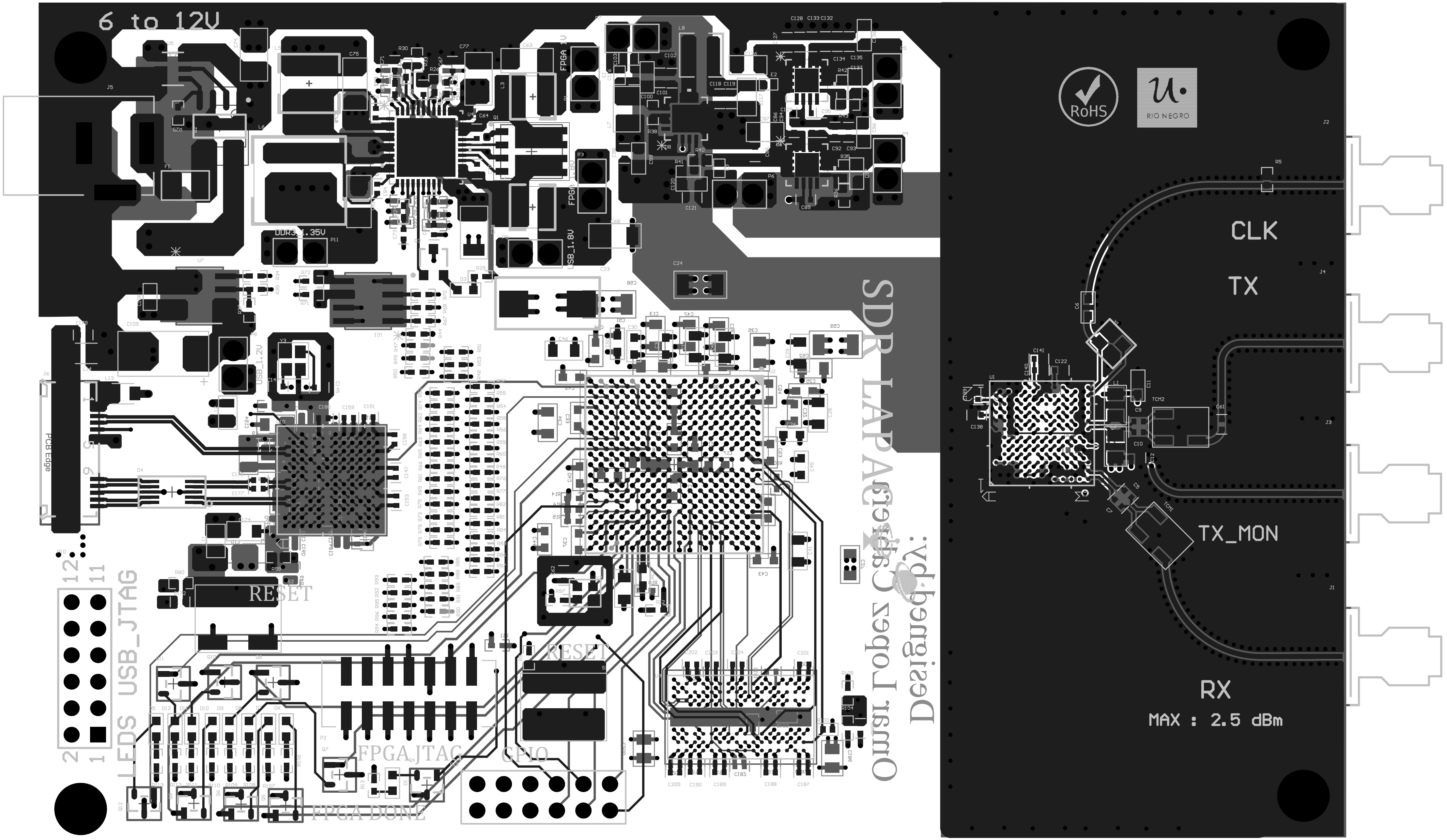
GPIO



Title **GPIO**

Size B
Number 7
Revision

Date: 21/03/2019
Sheet of 7
File: D:\Tesis\..\GPIO.SchDoc
Drawn By: **Omar Lopez**


6 to 12V
PCB Edge
DDR3L 1.35V
FPGA 1V
FPGA
USB_1.2V
USB_1.8V
SDR LAPAG
Designed by:
Omar Lopez
RESET
RESET
LEDS USB_JTAG
FPGA JTAG
GPIO
FPGA DONE
RoHS
RIO NEGRO
CLK
TX
TX_MON
RX
MAX : 2.5 dBm