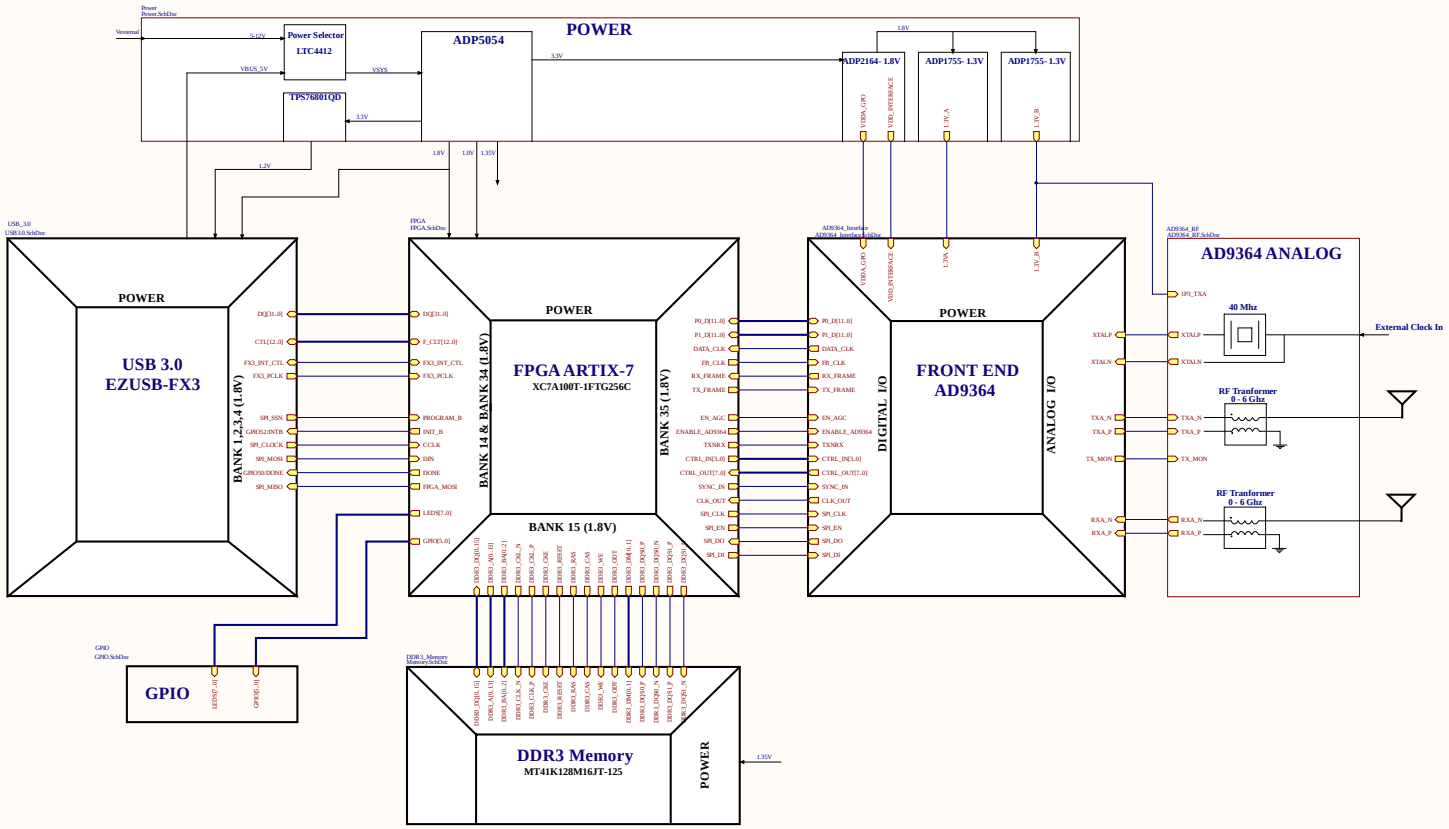
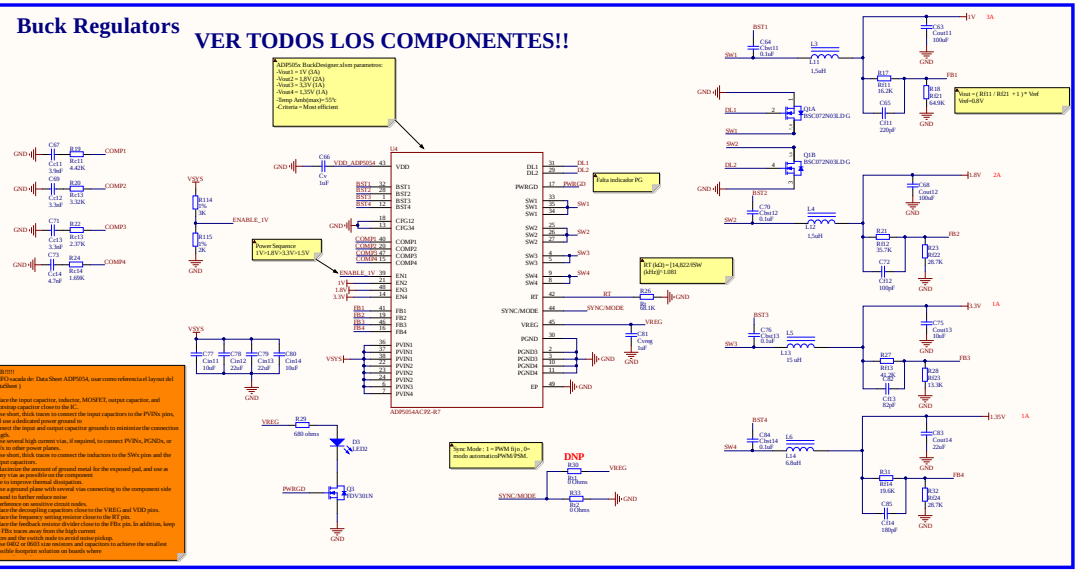


Title: Block Diagram			
Size: D	Number: 0	Revision:	
Date: 04/07/2013	Sheet of: 7		
File: D:\Tesis\...\intro.SchDoc	Drawn By: Omar Lopez		

Buck Regulators

VER TODOS LOS COMPONENTES!!



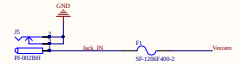
Power Path Selector

Funcionamiento:
-Si solo the primary supply is present,the Power Source Selector will power the LTC4412 from the VIN pin.

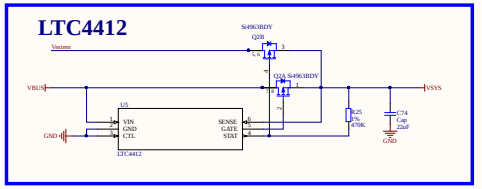
GATE (Pin 5): Primary P-Channel MOSFET Power Switch Gate Drive Pin. This pin is directed by the power controller to maintain a forward regulation voltage (VFR) of 20mV between the VIN and SENSE pins when an auxiliary power source is not present. When an auxiliary power source is connected, the GATE pin will pull up to the SENSE pin voltage, turning off the primary P-channel power switch.

SENSE (Pin 6): Power Sense Input Pin. Supplies power to the internal circuitry and is a voltage sense input to the internal analog controller.The other input to the controller is the VIN pin). This input is usually supplied power from an auxiliary source such as an AC adapter or back-up battery which also supplies current to the load.

External Voltage



LTC4412

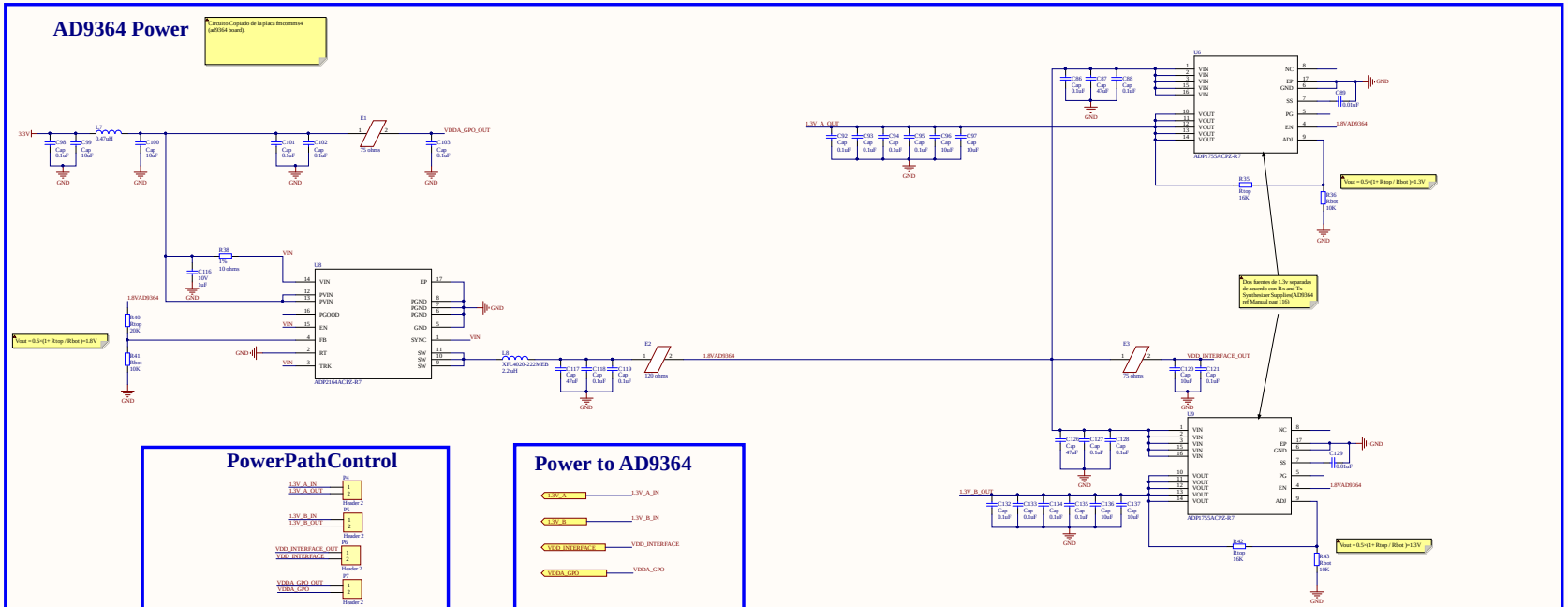


VIN (Pin 1): Primary Input Supply Voltage. Supplies power to the internal circuitry and is one of two voltage sense inputs to the internal analog controller (The other input to the controller is the SENSE pin). This input is usually supplied power from a battery or other power source which supplies current to the load. This pin can be bypassed to ground with a capacitor in the range of 0.1µF to 10µF if needed to suppress load transients.

STAT (Pin 4): Open-Drain Output Status Pin. When the SENSE pin is pulled above the VIN pin with an auxiliary power source by about 20mV or more, the reverse turnoff threshold (VRTO) is reached. The STAT pin sold then go from an open state to a 10µA current sink (IS)(SINK). The STAT pin can be used to turn off a DC dump with an external resistor, to turn on an auxiliary secondary power switch and/or signal the presence of an auxiliary power source to a microcontroller.

AD9364 Power

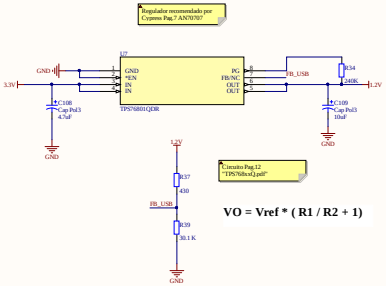
Circuito Copiado de la placa fmcomms4 (ad9364 board).



PowerPathControl

Power to AD9364

TPS76801QD USB Power



Title: Power			
Size: D	Number: 5	Revision:	
Date: 04/07/2013	Sheet of: 7		
File: D:\Tesis\...\Power.SchDoc	Drawn By: Osmar Lapaz		

Powe&Decoupling

PowerPathControl

Clock&Boot

Data&Control

JTAG

Interface

Title	USB 3.0		
Size	Number		Revision
D	1		
Date:	04/07/2013	Sheet of	7
File:	D:\Trabajo\...\USB3.0\Sch.Dsc	Drawn By:	Omar Lopez

Powe&Decoupling

Los datos para las conexiones fueron sacados de UG483 Xilinx(Table 2-2 y Table 2-5) y "7 Series Schematic Review Recommendations"

The Xilinx Power Estimator (XPE) tool is used to estimate the current on each power rail.

PCB decoupling guidelines are provided on a per-device basis based on very high utilization so as to cover a majority of use cases. Resource usage consists (in part) of:
- 80% of LUTs and registers at 245 MHz
- 80% block RAM and DSP at 491 MHz
- 50% MMCM and 25% PLL at 500 MHz
- 100% I/O at SSTL 1.2/1.35 at 1,200/800 MHz

U2G — XC7A100T-1FTG256C
U2H — XC7A100T-1FTG256C
U2F — XC7A100T-1FTG256C

VCCINT, VCCBRAM, VCCAUX, VCCO_14, VCCO_15, VCCO_34, VCCO_35, VCCO_Banks, VCCO_0

Config&Boot

M[2:0]: Configuration Mode 111=Slave Serial configuration.
CCLK: Configuration Clock, in Slave Serial configuration:CCLK must be driven from an external clock source, which also provides data.

IF= (3.3V - 2.8-V) / 100 ohms =5 mA

INIT_B: FPGA drives this pin low when is in a configuration reset state,when is initializing its configuration memory or when detected a configuration error.
DONE: High indicates completion of the configuration sequence.The DONE output is a open-drain by default.
PROGRAM_B: when is pulsed Low, FPGA configuration is cleared an a new configuration sequence is initiated.(Flanco desendente:Reset y en flanco ascendente: la nueva configuracion)
CFGBVS:Configuration Banks Voltage Select.Determines the I/O voltage operating range.High =Range 2.5V to 3.3v, Low= Range 1.8V or less.
PUDC_B:Pull-up during configuration.Low=internal pull-up enable, High: internal pull-up disable.

No uso Temperature-sensing

Clock

Y2 — SIT8008AI-72-18E-100.000000G

JTAG

Conector para Platform Cable USB II

TDI: JTAG Test Data Input. JTAG chain serialized data input
TDO: JTAG Test Data Output. JTAG serealized data output
TCK: JTAG Test Clock. Clock for all devices on a JTAG chain.
TMS: JTAG Test Mode Select.Mode select for all devices on the Jtag chain

PowerPathControl

Headers para alimentar por etapas

Slave Serial Mode

Utilizo Slave serial mode para poder configurar la FPGA a traves del USB 3.0.

USB-FPGA

U2C — XC7A100T-1FTG256C

PCB!!!!
(INFO sacada de: UG483)

PCB decoupling:
•Bulk capacitors (1210): the low-frequency energy covered by bulk capacitors is not sensitive to capacitor location.Bulk capacitors can be placed almost anywhere on the PCB, but the best placement is as close as possible to the FPGA.
•0805 and 0603 Ceramic Capacitors: cover the middle frequency range. Placement has some impact on their performance. The capacitors should be placed as close as possible to the FPGA.
Power:
• High-priority supplies should be placed closer to the FPGA (in the PCB stackup's top half)
• Low-priority supplies should be placed farther from the FPGA (in the PCB stackup's bottom half)

Routing:
•Usar impedancia de 50 ohms (Single-Ended).
•Usar impedancia de 100 ohms (Differential).
•No usar codos a 90 grados

BGA FanOut :
•UG1099 Recommended Design Rules and Strategies for BGA Devices

U2A — XC7A100T-1FTG256C

Configuring an FPGA Over USB Using Cypress AN84868

Multi-region Clock Capable pin (MRCC):these pins can route the clock input to multiple clock regions.

FPGA-AD9364

U2D — XC7A100T-1FTG256C

FPGA-DDR3

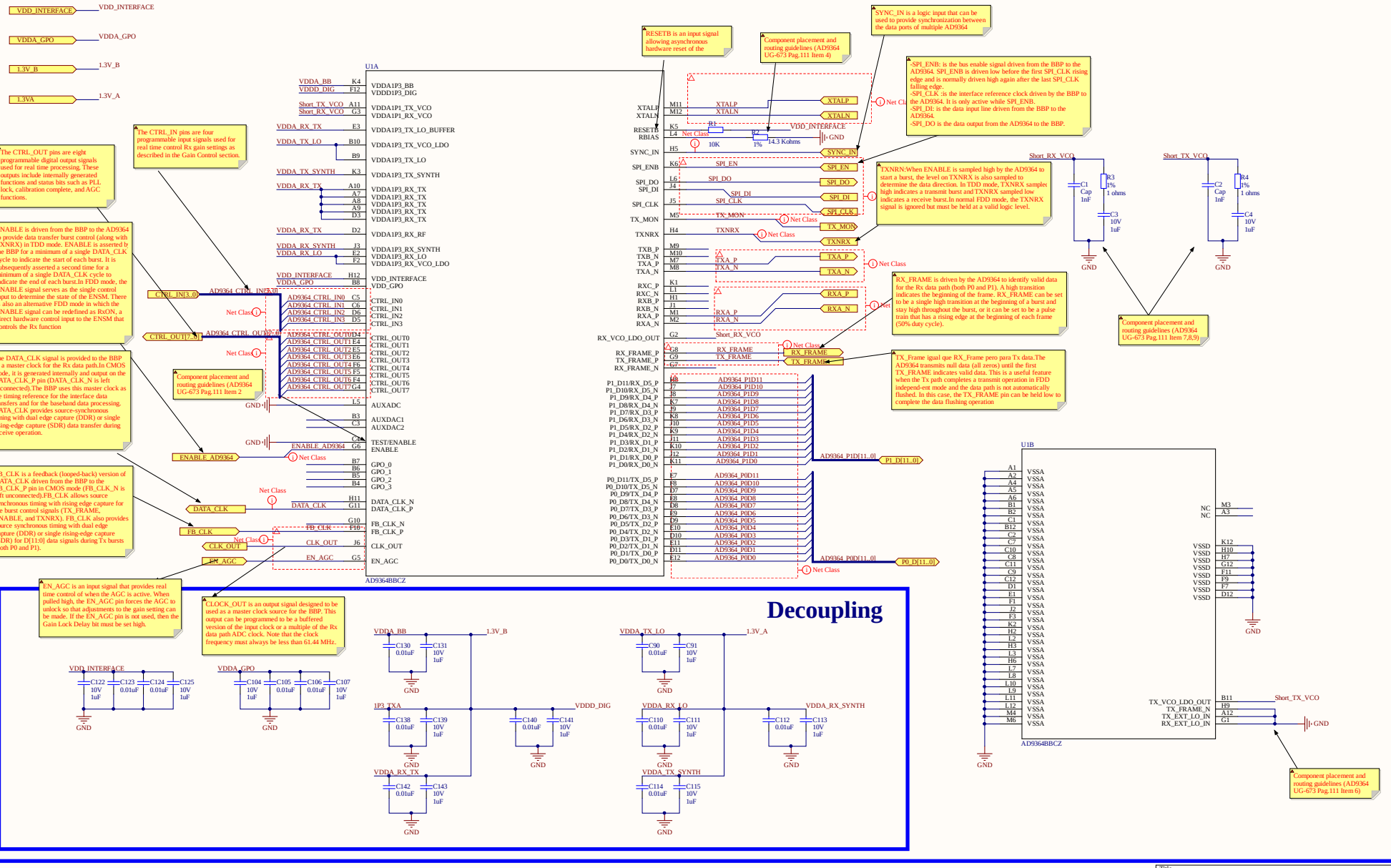
U2B — XC7A100T-1FTG256C

Conexiones utilizando "Design Guidelines" pag 102 de "UG586 :7 Series FPGAs Memory Interface Solutions".

Title	FPGA ARTIX-7
Size	C
Number	2
Revision	
Date:	04/07/2019
Sheet of	7
File:	D:\Tesis\..\FPGA.SchDoc
Drawn By:	Omar Lopez

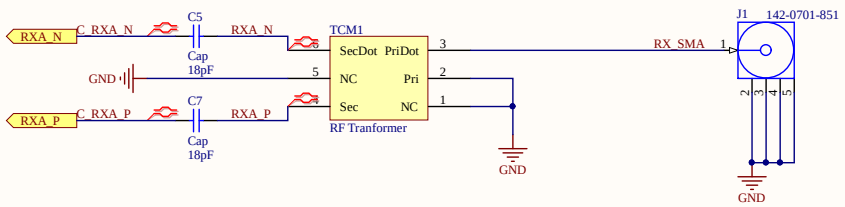
AD9364 Interface

CMOS MODE DATA PATH AND CLOCK SIGNALS

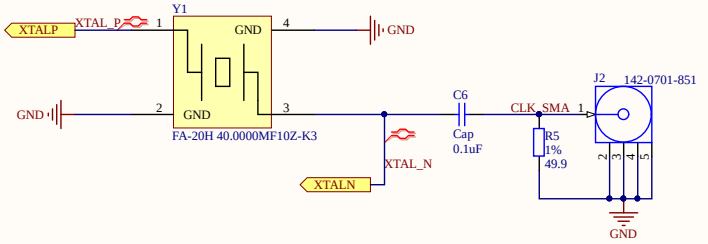


Title	AD9364 Interface		
Size C	Number 3		Revision
Date: 04/07/2019		Sheet of 7	
File: D:\Tesis\..\AD9364_Interface.SchDoc		Drawn By: Omar Lopez	

RX



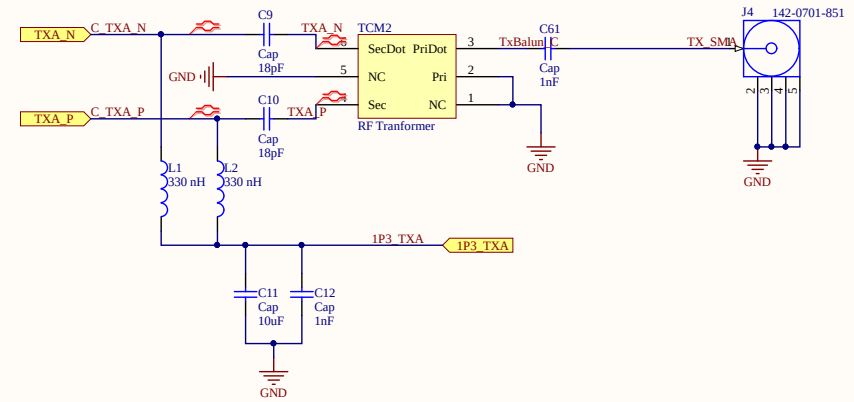
Clock



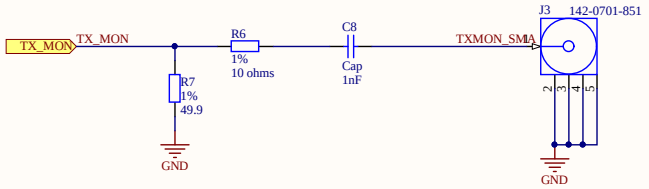
Posible mejoras:
1.utilizar Balum para cada diferentes rangos de frequencia y un selector de RF.
2.Amplificador PGA-102 a la salida de TX

Balum Link

TX

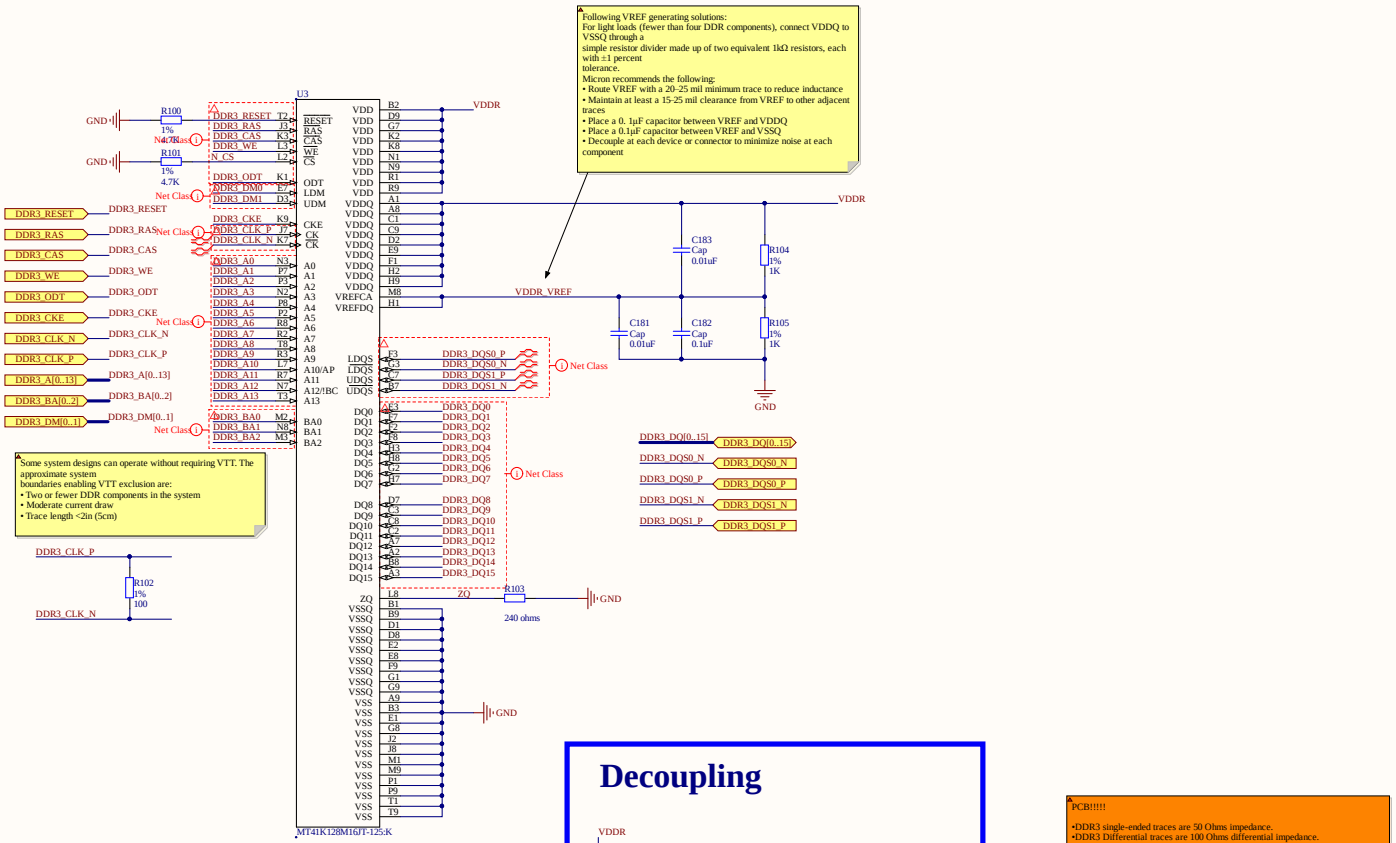


TX Monitor

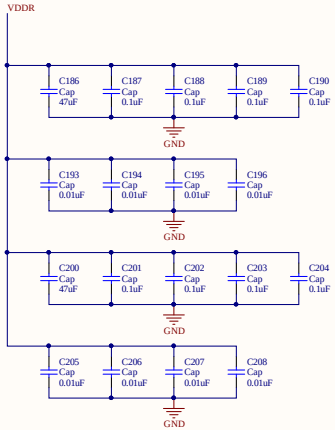


Title	**AD9364 RF**	
Size: A3	Number: **4**	Revision:
Date: 04/07/2019		Sheet of **7**
File: D:\Tesis\..\AD9364_RF.SchDoc		Drawn By: **Omar Lopez**

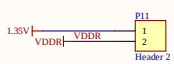
256MB DDR3L with a 16-bit bus



Decoupling



PowerPathControl



PCB!!!!!

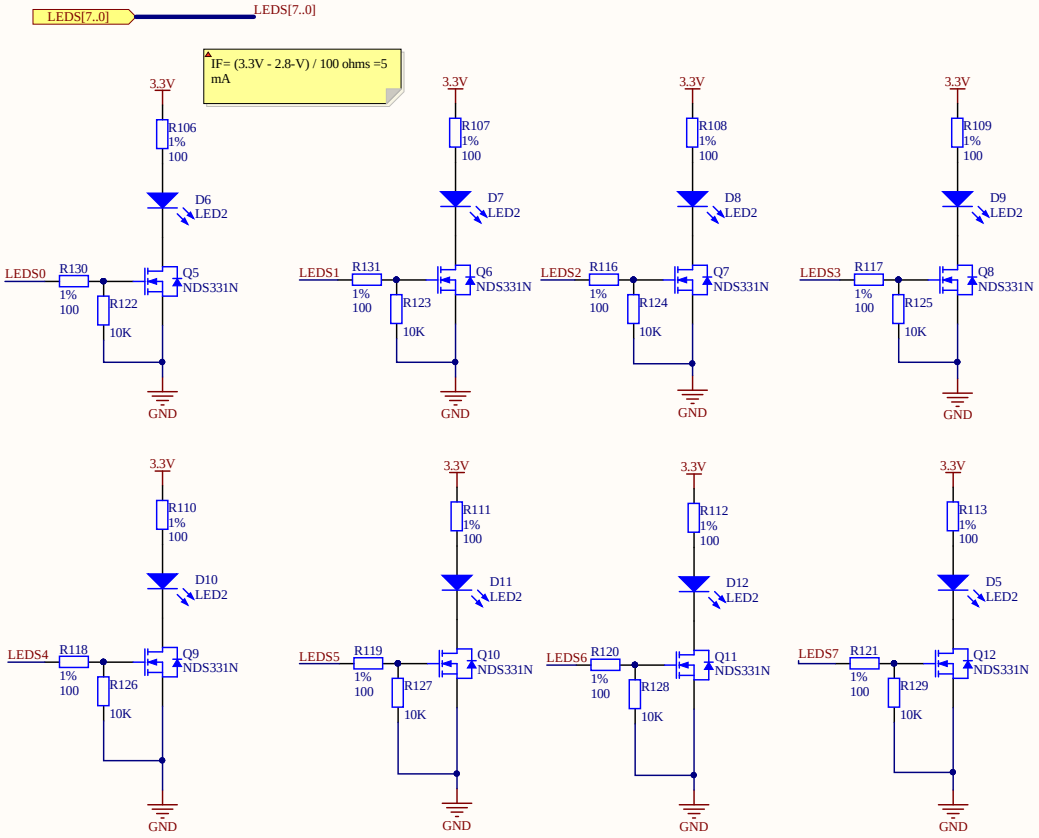
•DDR3 single-ended traces are 50 Ohms impedance.
•DDR3 Differential traces are 100 Ohms differential impedance.
• Route VREF with a 20-25 mil minimum trace to reduce inductance
• Maintain at least a 15-25 mil clearance from VREF to other adjacent traces
•For Interpair and Intrapair Spacing Design Guidelines look at table TN-46-14: Hardware Tips for Point-to-Point System Design
Introduction Pag 8.

Trace with:
• DQ lines = 4 mil minimum, 6 mil nominal
• DQS lines = 4 mil minimum, 6 mil nominal
• Address lines = 4 mil minimum, 6 mil nominal
• Command/control lines = 4 mil minimum, 6 mil nominal
• Clock lines = 4 mil minimum, 6–10 mil nominal

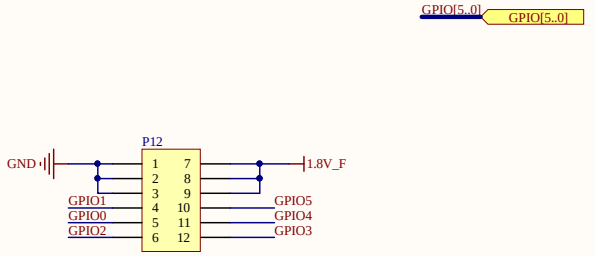
Routing:
• Place data tracks on different layers from address and control lanes, if possible.
•Match trace lengths for the data group within ±50 mil of each other to diminish skew serpentine traces (back and forth traces in an "S" pattern to increase trace length) can be
used to match lengths
• If the controller does not specify this, route byte lanes so that ±500 mil is the largest trace-length difference relative to the clock group trace length.
•All DDR differential clock pairs (CK and CK#) must be routed on the same layer.
•DDR systems,match CK trace length to CK# trace length ±20 mil, and CK/CK# trace lengths to DQS trace length ±500 mil.
•A 400 mil difference in address-, command-, or signal-group trace lengths equates to0.4in × (1,000ps of propagation delay per 6in of trace), or 67ps of skew
•Keep traces as short as possible, <2in (5cm)

Title: **Memory**		
Size: C	Number: **6**	Revision:
Date: 04/07/2019	Sheet of: 7	
File: D:\Tesis\..\Memory.SchDoc	Drawn By: **Omar Lopez**	

Leds



GPIO



Title: **GPIO**		
Size: B	Number: **7**	Revision:
Date: 04/07/2019	Sheet of **7**	
File: D:\Tesis\..\GPIO.SchDoc	Drawn By: **Omar Lopez**	

6 to 12V
DDR3_1.35V
USB_1.2V
FPGA_1V
USB_1.8V
LEDS USB_JTAG
RESET
FPGA_JTAG
GPIO
FPGA DONE
SDRIAPHY
CLK
TX
TX_MON
RX
MAX : 2.5 dBm
RoHS