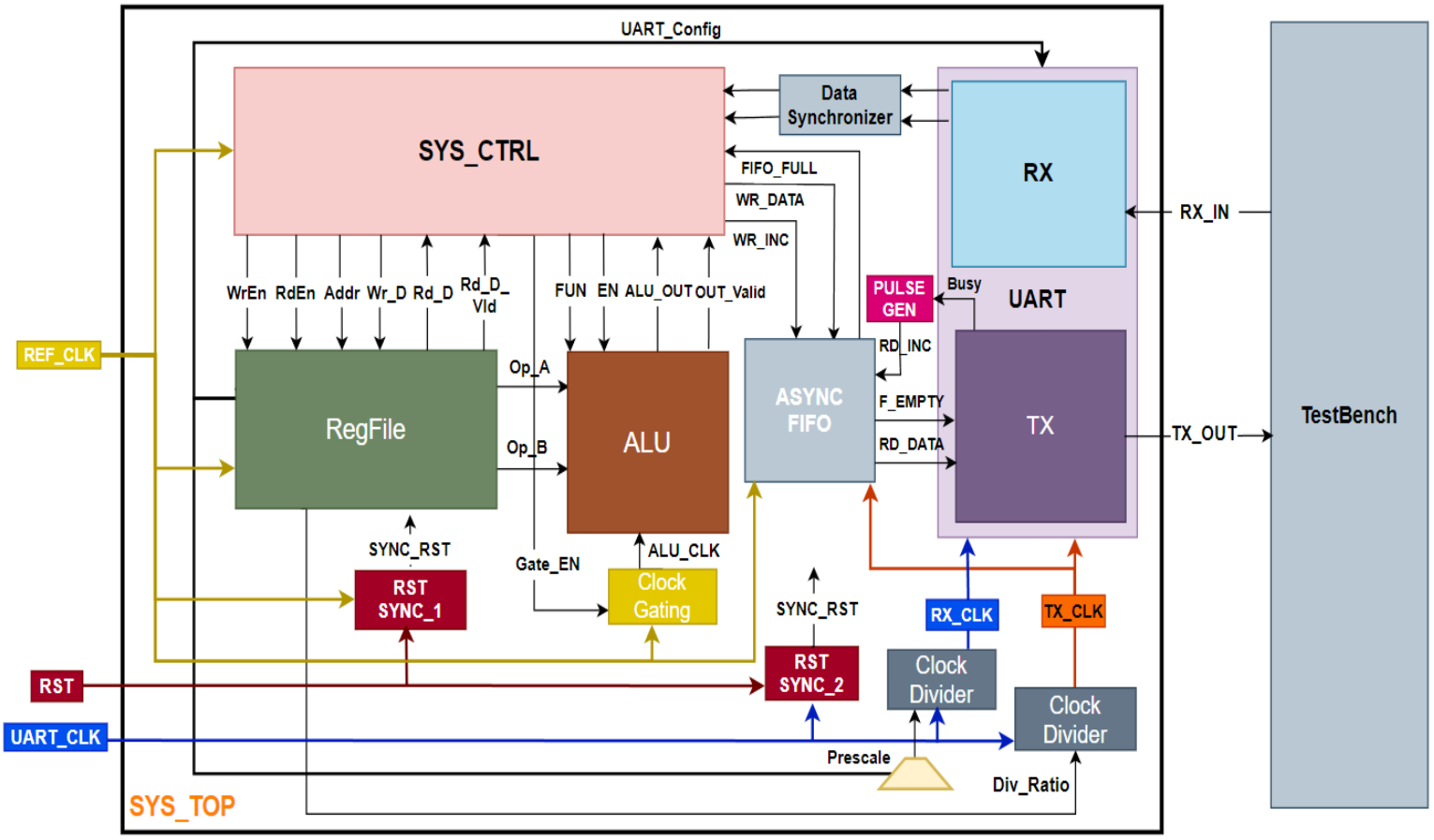
Final System



- **Description: -**

1 . This system contains 10 blocks: -

1) Clock Domain 1 (REF_CLK)

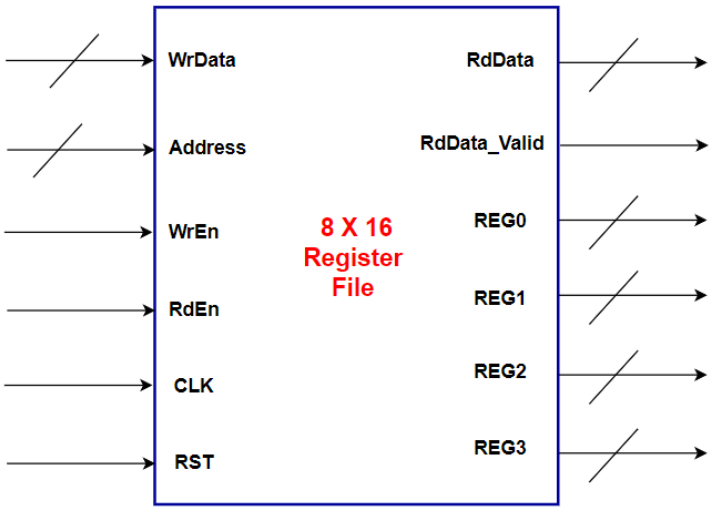
- **RegFile**
- **ALU**
- **Clock Gating**
- **SYS_CTRL**

- **Clock Domain 2 (UART_CLK)**
  - **UART_TX**
  - **UART_RX**
  - **PULSE_GEN**
  - **Clock Dividers**
- **Data Synchronizers**
  - **RST Synchronizer**
  - **Data Synchronizer**
  - **ASYNC FIFO**

CLOCK Domain 1

1) RegFile: -

- **Block Interface: -**



- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	TOP Input Port (REF_CLK)
RST	IN	1	Active Low Reset	RST_SYNC
Address	IN	Parameterized (default : 4 bits)	Address bus	SYS_CTRL
WrEn	IN	1	Write Enable	SYS_CTRL
RdEn	IN	1	Read Enable	SYS_CTRL
WrData	IN	Parameterized (default : 8 bits)	Write Data Bus	SYS_CTRL
RdData	OUT	Parameterized (default : 8 bits)	Read Data Bus	SYS_CTRL
RdData_Valid	OUT	1	Read Data Valid	SYS_CTRL
REG0	OUT	Parameterized (default : 8 bits)	Register at Address 0x0	ALU
REG1	OUT	Parameterized (default : 8 bits)	Register at Address 0x1	ALU
REG2	OUT	Parameterized (default : 8 bits)	Register at Address 0x2	UART
REG3	OUT	Parameterized (default : 8 bits)	Register at Address 0x3	Clock Divider

- **Reserved Registers Description: -**

1) **REG0 (Address: 0x0)**

ALU Operand A

2) **REG1 (Address: 0x1)**

ALU Operand B

3) **REG2 (Address: 0x2)**

UART Config

REG2[0]: Parity Enable
(Default = 1)
REG2[1]: Parity Type
(Default = 0)
REG2[7:2]: Prescale
(Default = 32)

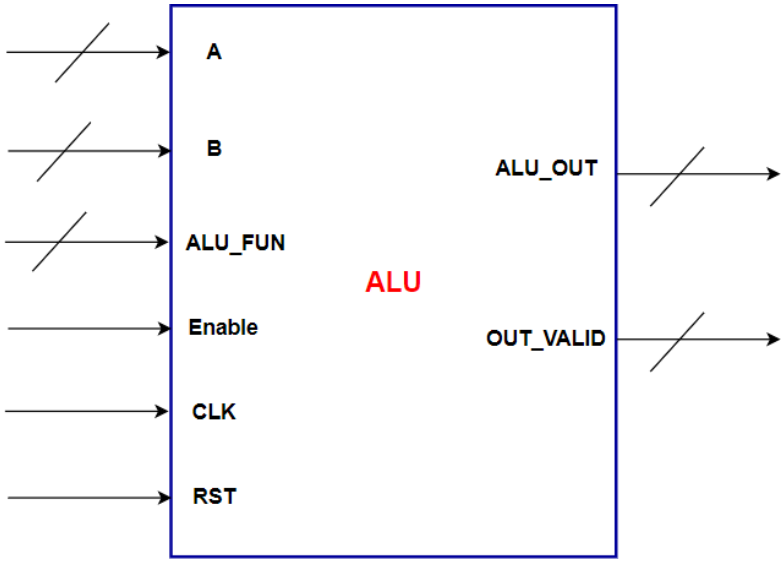
4) **REG3 (Address: 0x3)**

Div Ratio

REG3[7:0]: Division ratio
(Default = 32)

2) ALU:

- **Block Interface: -**

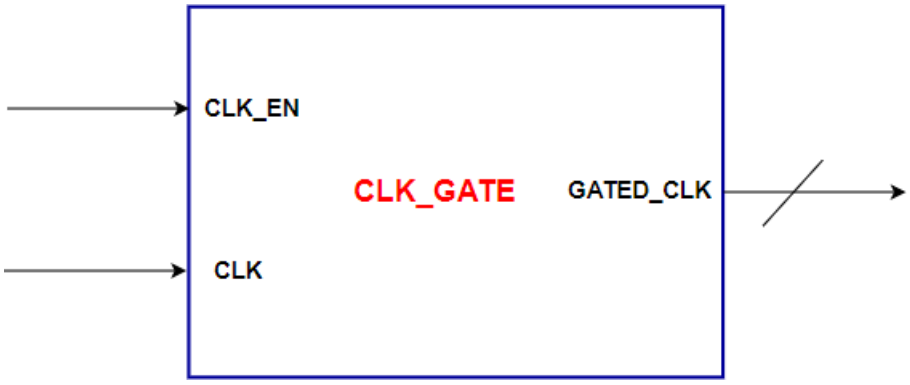


- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	CLK_GATE
RST	IN	1	Active Low Reset	RST_SYNC
A	IN	Parameterized (default : 8 bits)	Operand A	RegFile (REG0)
B	IN	Parameterized (default : 8 bits)	Operand B	RegFile (REG1)
ALU_FUN	IN	Parameterized (default : 4 bits)	ALU Function	SYS_CTRL
Enable	IN	1	ALU Enable	SYS_CTRL
ALU_OUT	OUT	Parameterized (default : 8 bits)	ALU Result	SYS_CTRL
OUT_VALID	OUT	1	Result Valid	SYS_CTRL

3) Clock Gating: -

- **Block Interface: -**

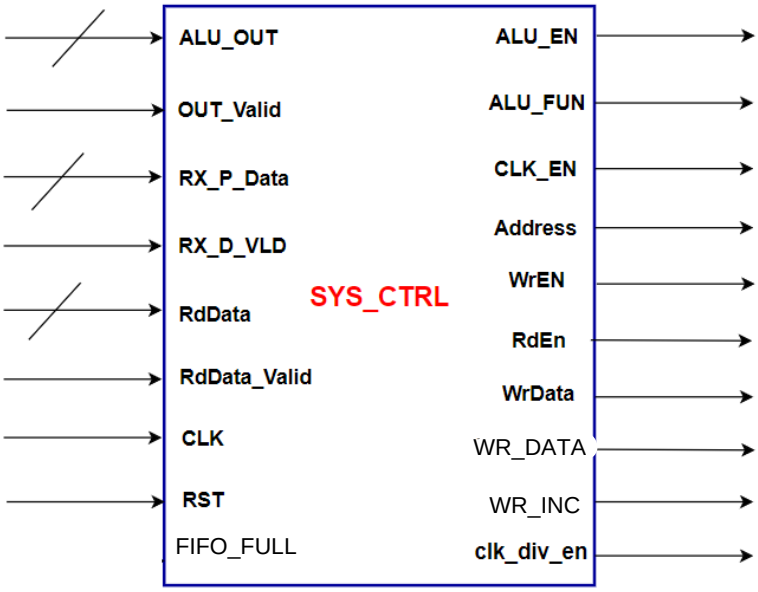


- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	TOP Input Port (REF_CLK)
CLK_EN	IN	1	Clock Enable	SYS_CTRL
GATED_CLK	out	1	Gated Clock signal	ALU

4) SYS_CTRL:

- **Block Interface: -**



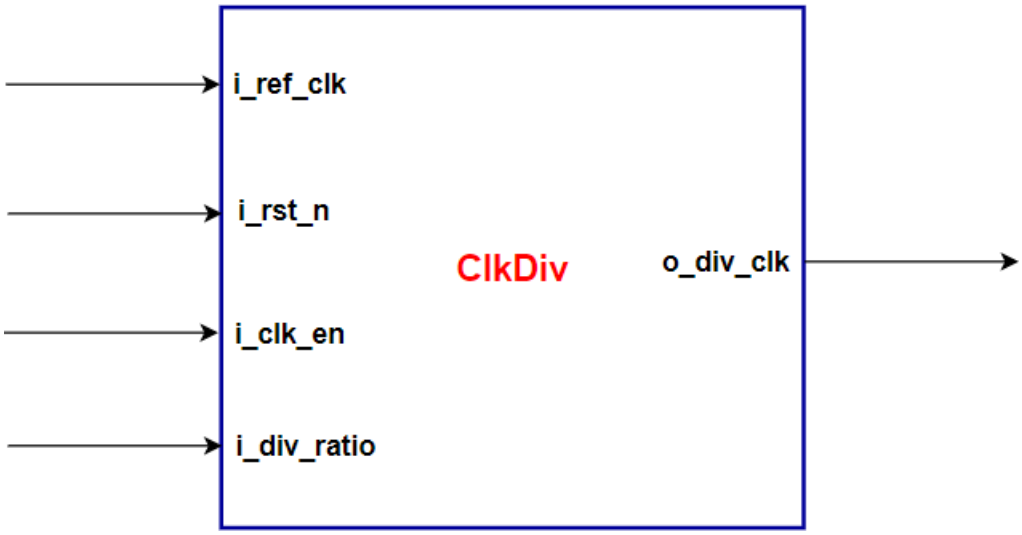
- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	TOP Input Port (REF_CLK)
RST	IN	1	Active Low Reset	RST_SYNC
ALU_OUT	IN	16	ALU Result	ALU
OUT_Valid	IN	1	ALU Result Valid	ALU
ALU_FUN	OUT	4	ALU Function signal	ALU
ALU_**EN**	OUT	1	ALU Enable signal	ALU
CLK_EN	OUT	1	Clock gate enable	CLK_GATE
Address	OUT	4	Address bus	RegFile
WrEn	OUT	1	Write Enable	RegFile
RdEn	OUT	1	Read Enable	RegFile
WrData	OUT	8	Write Data Bus	RegFile
RdData	IN	8	Read Data Bus	RegFile
RdData_Valid	IN	1	Read Data Valid	RegFile
RX_P_DATA	IN	8	UART _RX Data	UART_RX
RX_D_VLD	IN	1	RX Data Valid	UART_RX
WR_DATA	OUT	8	FIFO Input Data	ASYNC_FIFO
WR_INC	OUT	1	FIFO Write increment	ASYNC_FIFO
clk_div_en	OUT	1	Clock divider enable	CLKDiv
FIFO_FULL	IN	1	FIFO Full Flag	ASYNC_FIFO

CLOCK Domain 2

1) Clock Divider: -

- **Block Interface: -**

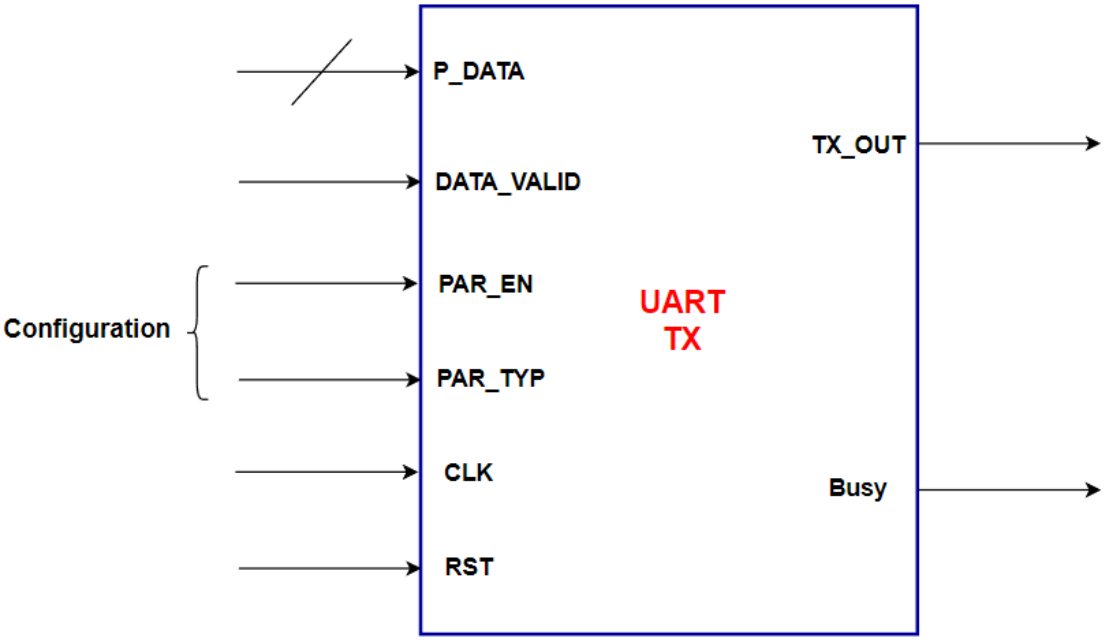


- **Signal Description: -**

Port	Direction	Width	Description	Connected to
I_ref_clk	IN	1	Clock Signal	TOP Input Port (UART_CLK)
I_rst_n	IN	1	Active Low Async Reset	RST_SYNC_2
I_clk_en	IN	1	Clock divider enable	1'b1 (Supply)
I_div_ratio	IN	Parameterized (default : 8 bits)	Division ratio	RegFile
O_div_clk	out	1	Divided clock	UART_TX UART_RX

2) UART_TX: -

- **Block Interface: -**

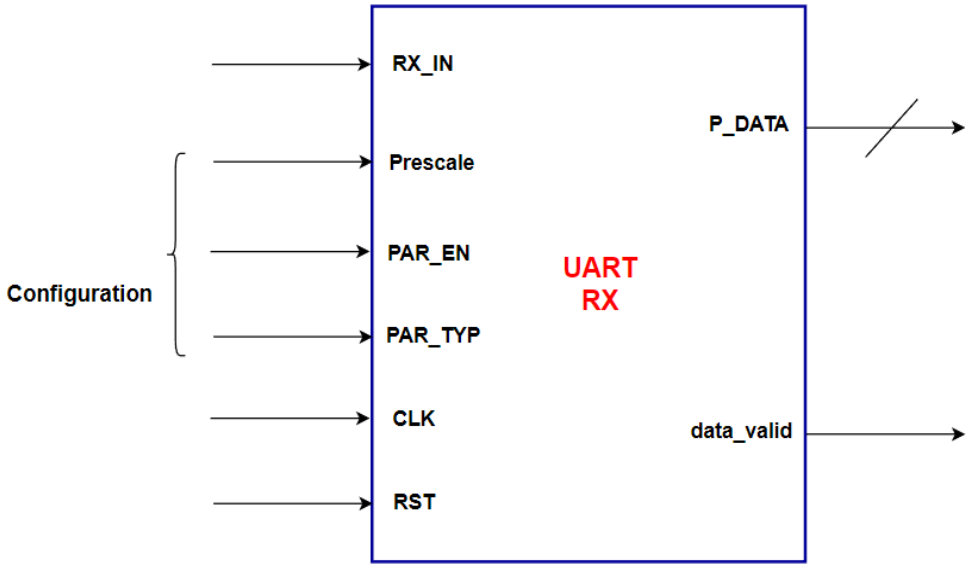


- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	CLKDiv
RST	IN	1	Active Low Reset	RST_SYNC_2
PAR_EN	IN	1	Parity Enable	RegFile
PAR_TYP	IN	1	Parity Type	RegFile
P_DATA	IN	Parameterized (default : 8 bits)	Parallel IN Data	ASYNC_FIFO
DATA_VALID	IN	1	IN Data Valid	ASYNC_FIFO
S_DATA	OUT	1	frame serial bits	TOP Output Port (TX_OUT)
Busy	OUT	1	Uart status signal	PULSE_GEN

3) UART_RX: -

- **Block Interface: -**

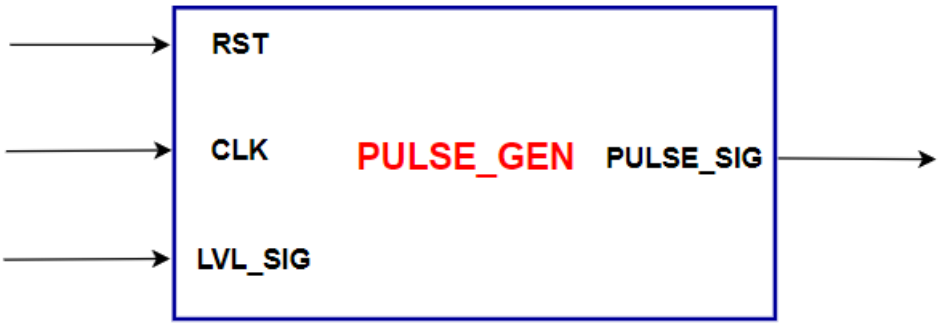


- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	TOP Input Port (UART_CLK)
RST	IN	1	Active Low Reset	RST_SYNC_2
Prescale	IN	6	Prescale	RegFile
PAR_EN	IN	1	Parity Enable	RegFile
PAR_TYP	IN	1	Parity Type	RegFile
RX_IN	IN	1	frame serial bits	TOP Input Port (RX_IN)
P_DATA	OUT	Parameterized (default : 8 bits)	Parallel Out Data	DATA_SYNC
DATA_VLD	OUT	1	Out Data Valid	DATA_SYNC
PAR_ERR	OUT	1	Frame parity error	TOP Output Port
STP_ERR	OUT	1	Frame stop error	TOP Output Port

4) PULSE_GEN: -

- **Block Interface: -**



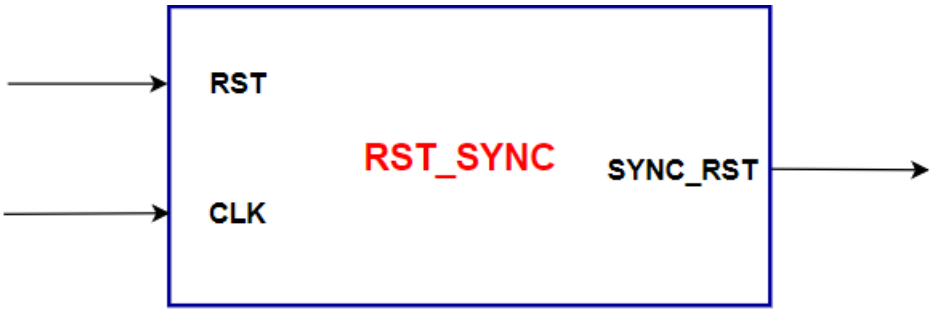
- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	TOP Input Port (UART_TX)
RST	IN	1	Active Low Reset	RST_SYNC_2
LVL_SIG	IN	1	Level signal	UART_TX
PULSE_SIG	OUT	1	Pulse signal	ASYNC_FIFO

Synchronizers

1) RST_Sync: -

- **Block Interface: -**

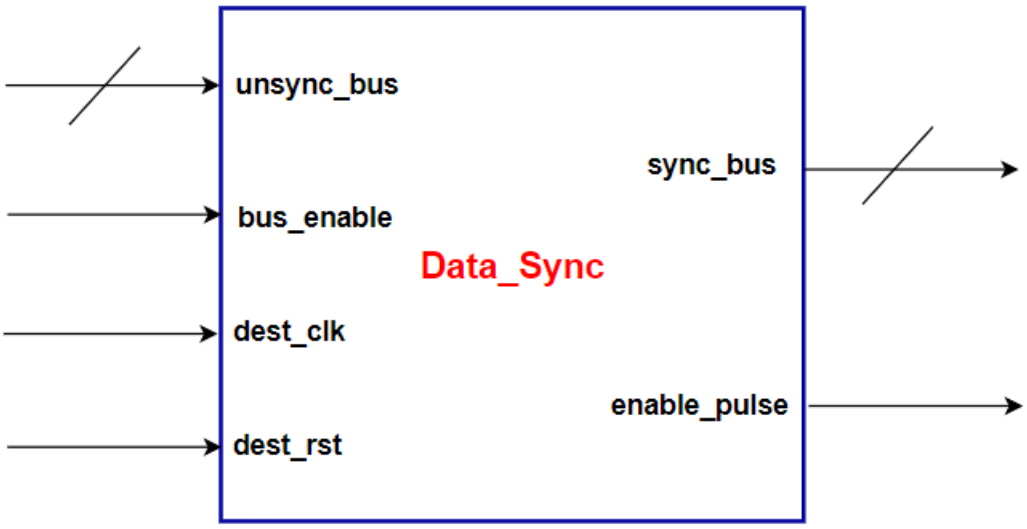


- **Signal Description: -**

Port	Direction	Width	Description
RST	IN	1	Clock Signal
CLK	IN	1	Active Low Async Reset
SYNC_RST	OUT	1	Active Low synchronized Reset

2) Data_Sync: -

- **Block Interface: -**

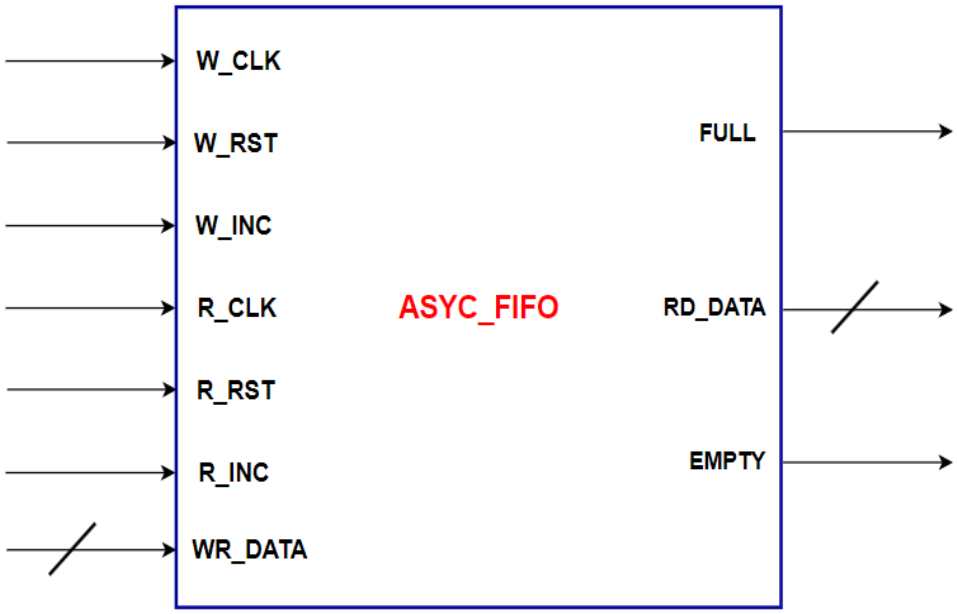


- **Signal Description: -**

Port	Direction	Width	Description
unsync_bus	IN	8	Unsynchronized bus
bus_enable	IN	1	Bus enable signal
dest_clk	IN	1	Destination Clock Signal
dest_rst	IN	1	Destination Active Low Reset
sync_bus	OUT	8	synchronized bus
enable_pulse_d	OUT	1	enable pulse signal

3) ASYNC_FIFO: -

- **Block Interface: -**



- **Signal Description: -**

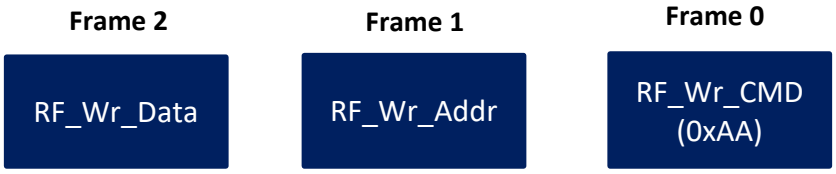
Port	Width	Description	Connected to
W_CLK	1	Source domain clock	TOP Input Port (REF_CLK)
W_RST	1	Source domain Async reset	RST_SYNC_1
W_INC	1	Write operation enable	SYS_CTRL
R_CLK	1	Destination domain clock	RST_SYNC_2
R_RST	1	Destination domain Async reset	RST_SYNC_2
R_INC	1	Read operation enable	PULSE_GEN
WR_DATA	Parameterized default (8-bits)	Write Data Bus	SYS_CTRL
RD_DATA	Parameterized default (8-bits)	Read Data Bus	UART_TX
FULL	1	FIFO Buffer full flag	SYS_CTRL
EMPTY	1	FIFO Buffer empty flag	UART_TX

Introduction

- The system is responsible to do some operation based on the received commands from the master through UART_RX interface, once the operation is done, the system is responsible to send the result to the master through UART_TX interface.

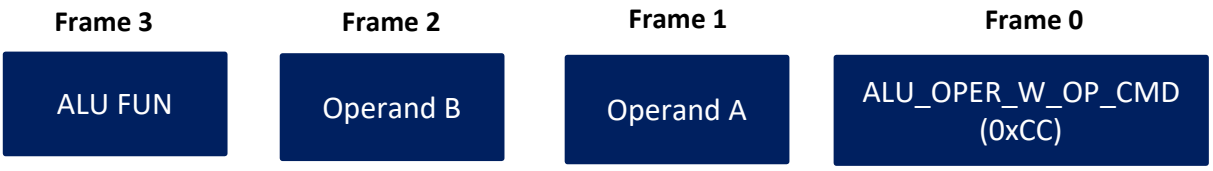
- Supported Operations: -
    1. **ALU Operations: -**
        - **Addition**
        - **Subtraction**
        - **Multiplication**
        - **Division**
        - **AND**
        - **OR**
        - **NAND**
        - **NOR**
        - **XOR**
        - **XNOR**
        - **CMP: A = B**
        - **CMP: A > B**
        - **SHIFT: A >> 1**
        - **SHIFT: A << 1**
    2. **Register File Operations**
        - **Register File Write**
        - **Register File read**

- Supported Commands: -
    1. **Register File Write command (3 frames)**



2. **Register File Read command (2 frames)**

3. **ALU Operation command with operand (4 frames)**



4. **ALU Operation command with No operand (2 frames)**

System Specifications: -

- Reference clock (REF_CLK) is 100 MHz
- UART clock (UART_CLK) is 3.6864 MHz uart_TX = 115.2 khz == uart_clk/32
- Clock Divider is always on (clock divider enable = 1)

Sequence of Operation (Must include in the testbench): -

- Initially configuration operations are performed through Register file write operations in addresses (0x2, 0x3).
- The Master (Testbench) start to send different commands (RegFile Operations, ALU operations)
- Our system will receive the command frames through UART_RX, it sent to the SYS_CTRL block to be processed
- Once the operation of the command is performed using ALU/RegFile, SYS_CTRL sends the result to the master through UART_TX
- Register File Address Range for normal write/read operations (From 0x4 to 0x15)
- Register File Addresses reserved for configurations and ALU operands (From 0x0 to 0x3)