System Lab

You have to go through the digital backend flow including: -

- Synthesis
- Formality post-synthesis

Steps: -

- Synthesis Stage: -
  i. Add the following constraints in cons.tcl file.
    - Create your master clocks
      - REF_CLK (100 MHz)
      - UART_CLK (3.686 MHz)
    - Create your generated clocks
      - ALU_CLK (master_clk = REF_CLK , div_ratio = 1)
      - RX_CLK (master_clk = UART_CLK , div_ratio = 1)
      - TX_CLK (master_clk = UART_CLK , div_ratio = 32)
    - Create a clock uncertainty with 0.2 ns for setup (all master & generated clocks)
    - Create a clock uncertainty with 0.1 ns for hold (all master & generated clocks)
    - Clock Grouping
    - Input delays on all input ports except (CLK & RST) with 20% clock period
    - output delays on all output ports with 20% clock period
    - Add Buffer driving cell for all input ports except all clocks & resets
    - Add load of 0.5 pf on all output ports
    - Set operation condition using slow and fast libraries

  ii. Run synthesis and check the followings
    - No Errors, loops and latches in syn.log file
    - Check Setup timing analysis report for Violating paths
    - Check Hold timing analysis report for Violating paths
- Formality post-synthesis Stage: -
  i. Run Formality and check it is succeeded with no failing points