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Research Article

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Course name	Digital Circuit Design
Course code	ECO354

Title: -

Design 2-bit Adder/Subtractor unit using CMOS

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Examiners committee	Signature

Research objectives

The Objective of this research is discussing Full adder working principle as well as Full subtractor working principle and using what discussed to design 2 bit parallel adder/subtractor then explaining its working principle, getting its truth table, simplified input equations, designing its sequential circuit and its CMOS implementation using Proteus simulation software.

Abstract

In this research we will first go through Full adder design, Truth table and operation.

Then we will go through parallel Full adders, then we will discuss how to add a full subtractor to a parallel Full adder.

Then we will discuss sequential circuit of Full adder and block diagram of parallel full adder and what changes do we need to add Full subtractor feature to a parallel Full adder.

Finally we will implement 2bit parallel full adder/subtractor in CMOS using Proteus simulation software.

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Introduction

Binary Addition Circuits:

Any Digital Computer must execute two basic Arithmetic Operations: addition and subtraction. Multiplication and Division operations become simple if both of these procedures are effectively implemented (as multiplication is repeated addition and division is repeated subtraction).

Consider the action of adding two binary digits, which is one of a digital computer's most basic functions. The two single bit binary integers are the four basic addition operations:

- 0 + 0 = 0
- 1 + 0 = 1
- 0 + 1 = 1
- 1 + 1 = (Carry)1 0

Each binary addition in the first three operations returns a sum of one bit, i.e., either 0 or 1. The output of the fourth addition operation (with inputs of 1 and 1), is two binary numbers. The lower significant bit is referred to as the 'Sum Bit,' and the higher significant bit is referred to as the ’Carry Bit’.

There may not be a problem with single-bit additions. When we try to add binary numbers with more than one bit, we may run into a problem.

Binary Adder Circuits are logic circuits that are designed to do the addition of two binary numbers, they are divided into:

- Half Adder
- Full Adder

Binary Subtraction Circuits:

Subtraction is another basic mathematical operation that Digital Computers can execute. Subtraction is a mathematical operation that involves subtracting one integer number from another to get the equal value. The ‘Minuend' is the number from which the other number is to be subtracted, and the ‘Subtrahend' is the number subtracted from the minuend.

Similar to the binary addition, binary subtraction is also has four possible basic operations. They are:

- 0 – 0 = 0
- 0 – 1 = (Borrow)1 1
- 1 – 0 = 1
- 1 – 1 = 0

Similar to adder circuits, basic subtraction circuits are classified into:

- Half Subtractor
- Full Subtractor

Review

Full Adder:

A Full Adder is a combinational logic circuit that performs three-bit addition and generates two outputs: a Sum and a Carry. Because the Half Adder is unable to respond to three inputs, the Full Adder is utilized to add three numbers at once.

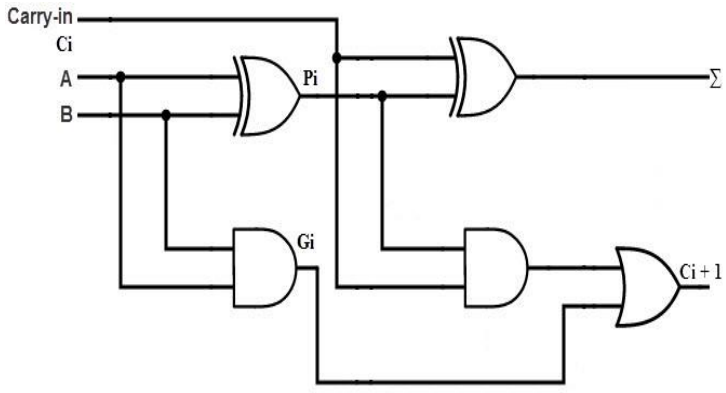
It has three inputs: two input variables that represent the two significant bits to be added, and a third input terminal that represents the carry from the preceding addition. A Sum and a Carry output are the two outputs.

Block Diagram of Full Adder

C_{in}	B	A	∑	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table

Full adder Sequential circuit & equations of Sum and carry:



$$S = A \oplus B \oplus C_{in}$$

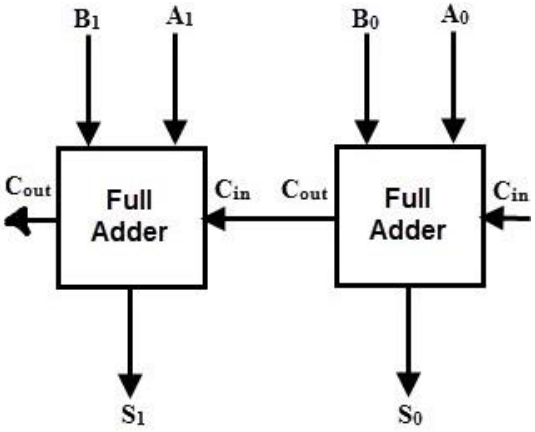
$$C_{out} = AB + BC_{in} + C_{in}A$$

Parallel Binary Adders:

As previously stated, a single Full Adder adds two one-bit values as well as the carry input. More than one complete adder is necessary to add binary values with more than one bit, and the number of Full Adders required depends on the number of bits.

As a result, a Parallel Adder is made up of many Full Adders and is used to add all bits of two numbers at the same time.

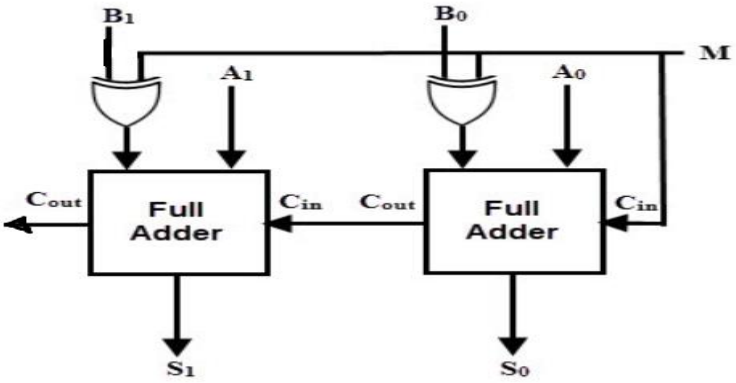
Since we only need 2 bit adder then Parallel binary adders of two two-bit values block diagram should be:



Parallel Adder / Subtractor:

A single common binary adder can perform both addition and subtraction operations.

Such binary circuit can be designed by adding an Ex-OR gate with each full adder.



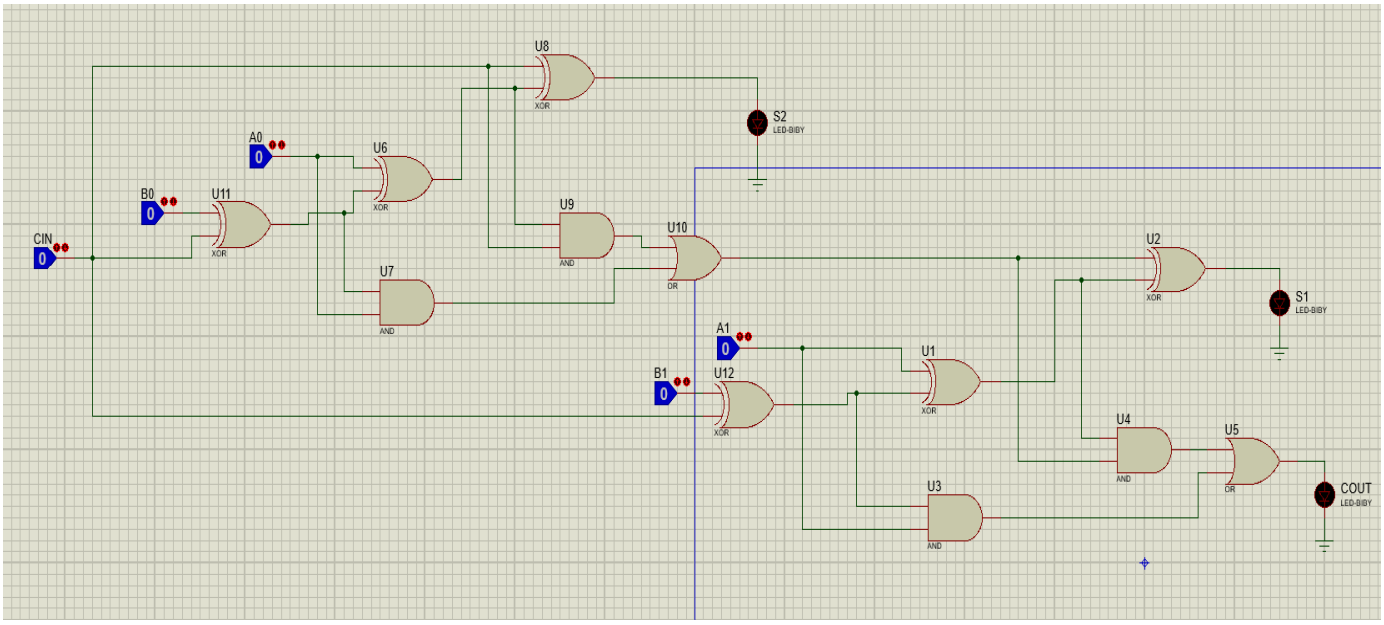
The mode input control line M is connected with carry input of the least significant bit of the full adder. This control line decides the type of operation, whether addition or subtraction.

When M= 1, the circuit is a subtractor and when M=0, the circuit becomes adder. The Ex-OR gate consists of two inputs to which one is connected to the B and other to input M. When M = 0, B Ex-OR of 0 produce B. Then, full adders add the B with A with carry input zero and hence an addition operation is performed.

When M = 1, B Ex-OR of 0 produce B complement and also carry input is 1. Hence the complemented B inputs are added to A and 1 is added through the input carry, nothing but a 2's complement operation. Therefore, the subtraction operation is performed.

Design & Simulation

Sequential circuit of 2bit Adder/Subtractor:



Truth Table:

CIN	A1	A0	B1	B0	S1	S0	COUT
0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0
0	0	0	1	0	1	0	0
0	0	0	1	1	1	1	0
0	0	1	0	0	0	1	0
0	0	1	0	1	1	0	0
0	0	1	1	0	1	1	0
0	0	1	1	1	0	0	1
0	1	0	0	0	1	0	0
0	1	0	0	1	1	1	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	1	1
0	1	1	0	0	1	1	0
0	1	1	0	1	0	0	1
0	1	1	1	0	0	1	1
0	1	1	1	1	1	0	1
1	0	0	0	0	0	0	1
1	0	0	0	1	1	1	0
1	0	0	1	0	1	0	0

1	0	0	1	1	0	1	0
1	0	1	0	0	0	1	1
1	0	1	0	1	0	0	1
1	0	1	1	0	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	0	1	0	1
1	1	0	0	1	0	1	1
1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	1	1	1
1	1	1	0	1	1	0	1
1	1	1	1	0	0	1	1
1	1	1	1	1	0	0	1

Equation of Sum and carry:

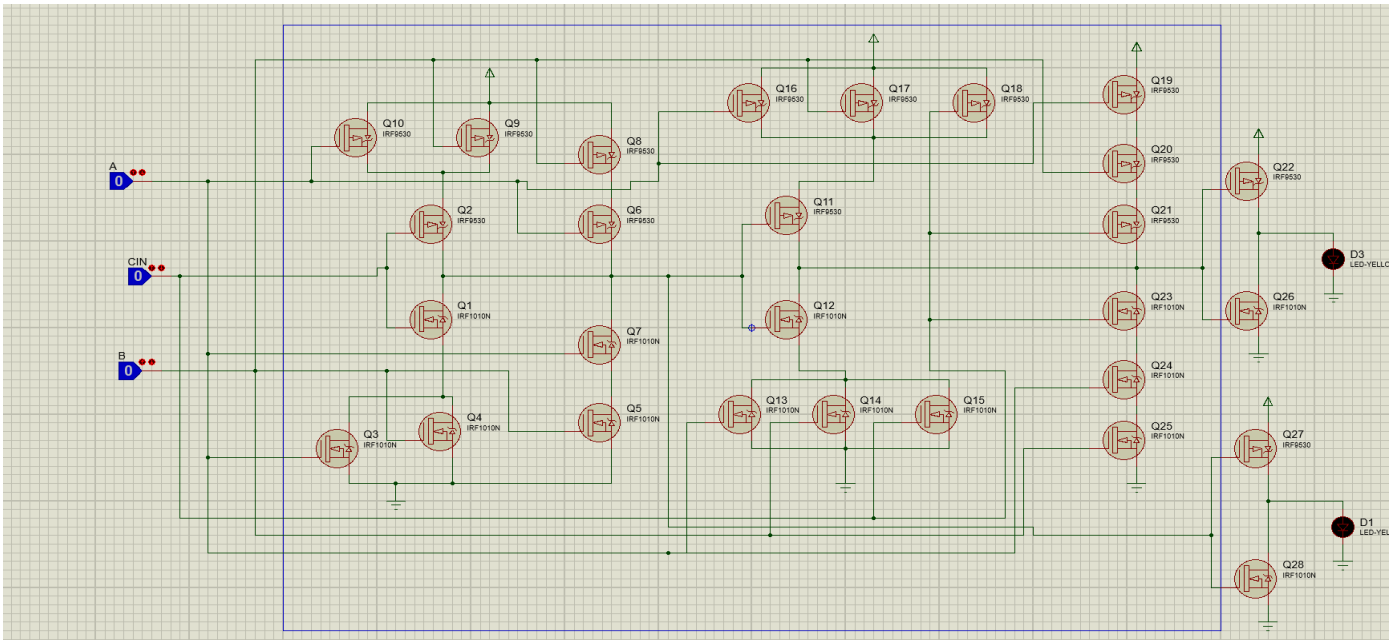
S1 = A1'B1B0' + A1B1'B0' + CIN'A1'A0'B1 + CIN'A1A0'B1' + CINA1'A0B1 + CINA1A0B1' + CIN'A1'A0B1'B0 + CIN'A1A0B1B0 + CINA1'A0'B1'B0 + CINA1A0'B1B0

S0 = A0'B0 + A0B0'

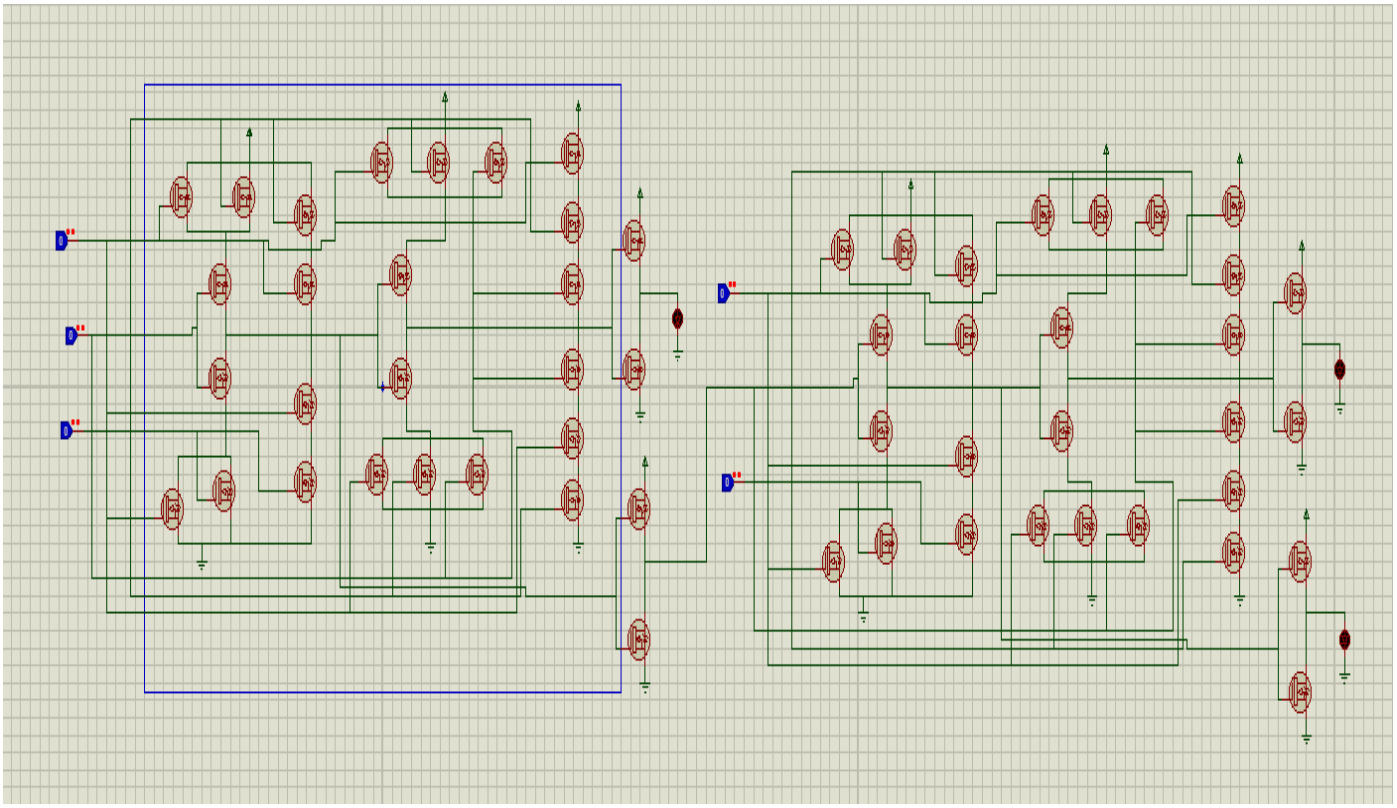
COUT = A0B1B0 + CIN'A1B1 + A1B1B0' + A1A0B0 + CINB1'B0' + CINA0B1' + CINA1B1'

Implementation on CMOS:

First designing a 1-bit Full adder

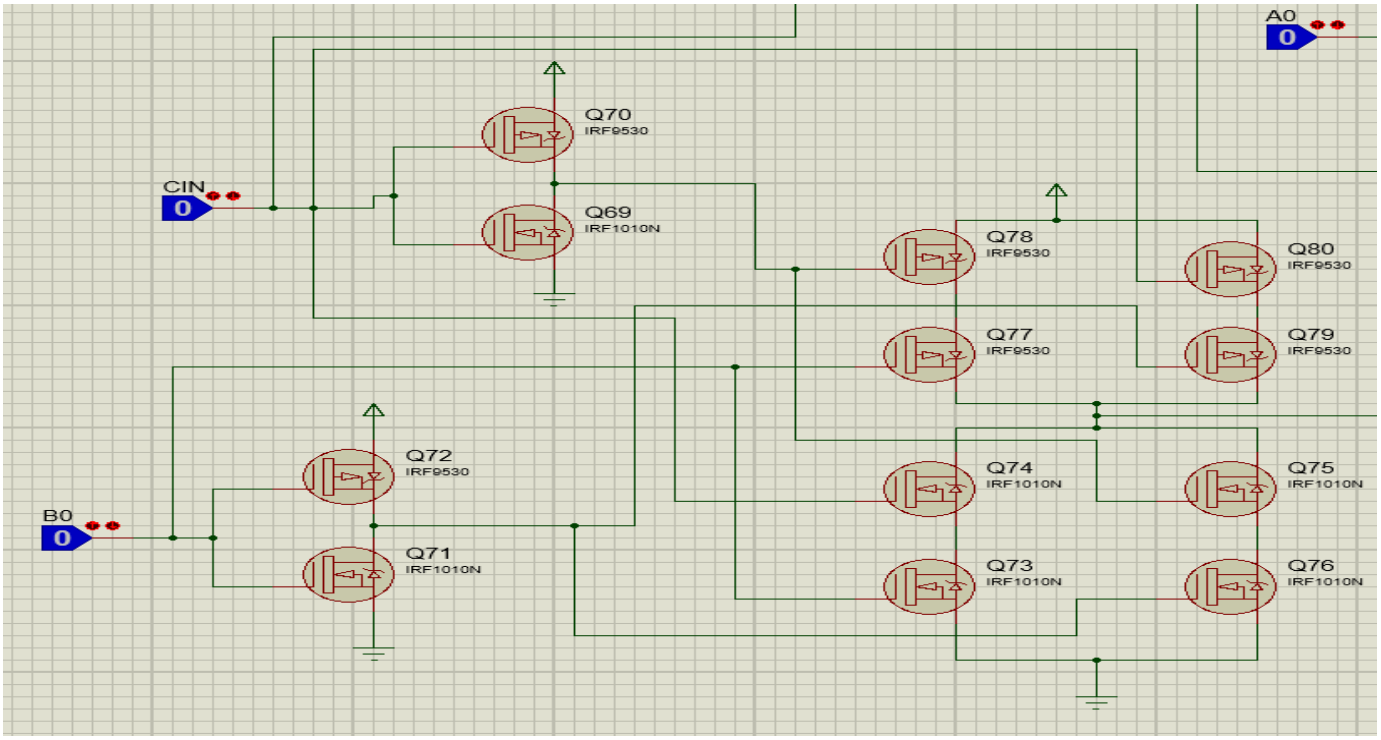


Then adding another 1-bit Full adder using Parallel full adder technique discussed above.

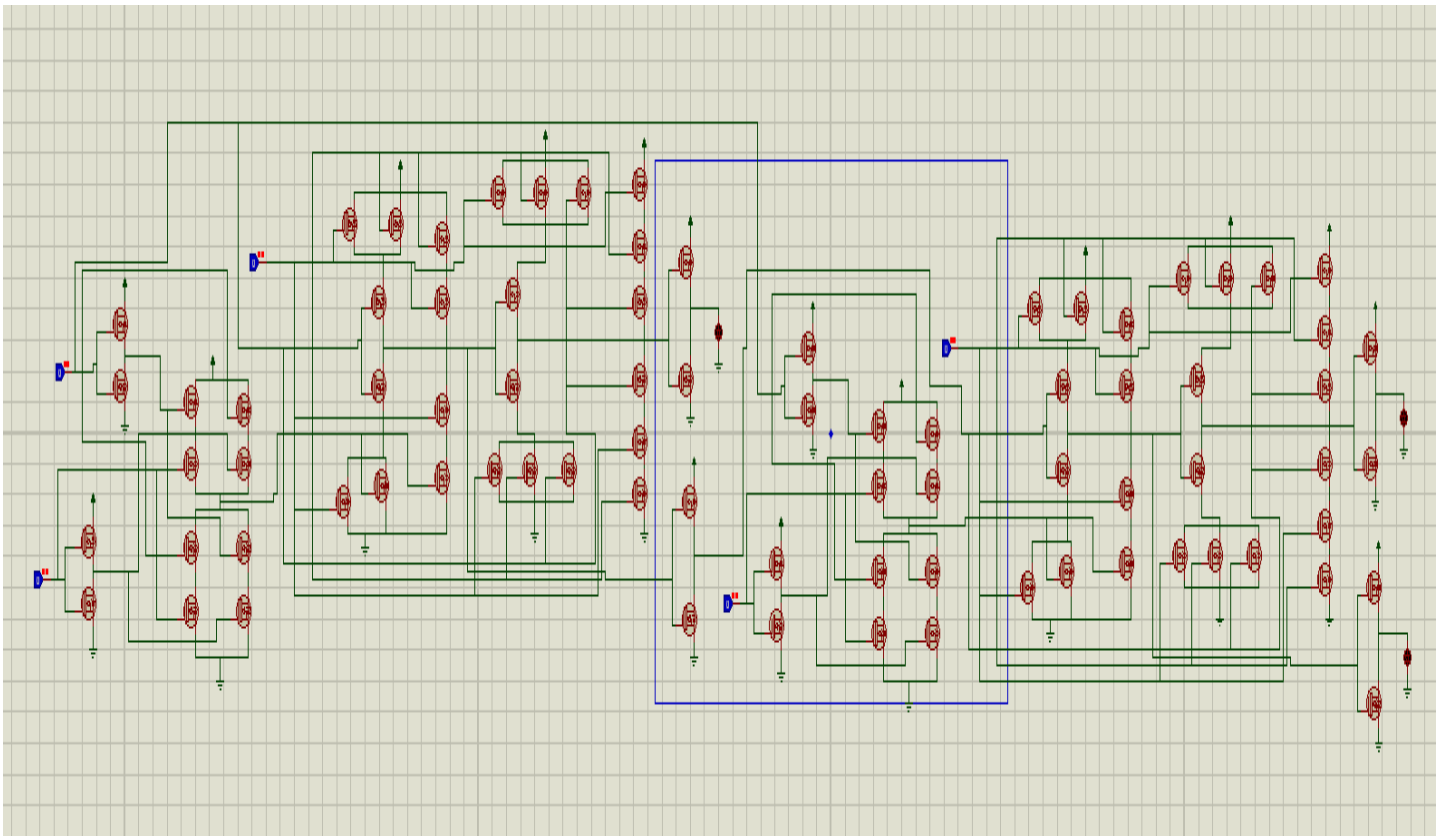


Finally adding x-or gate connecting M Control point with B inputs and CIN.

x-or circuit:



2-Bit Full Adder/Subtractor:

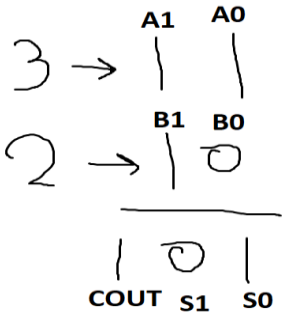


Results and Discussion

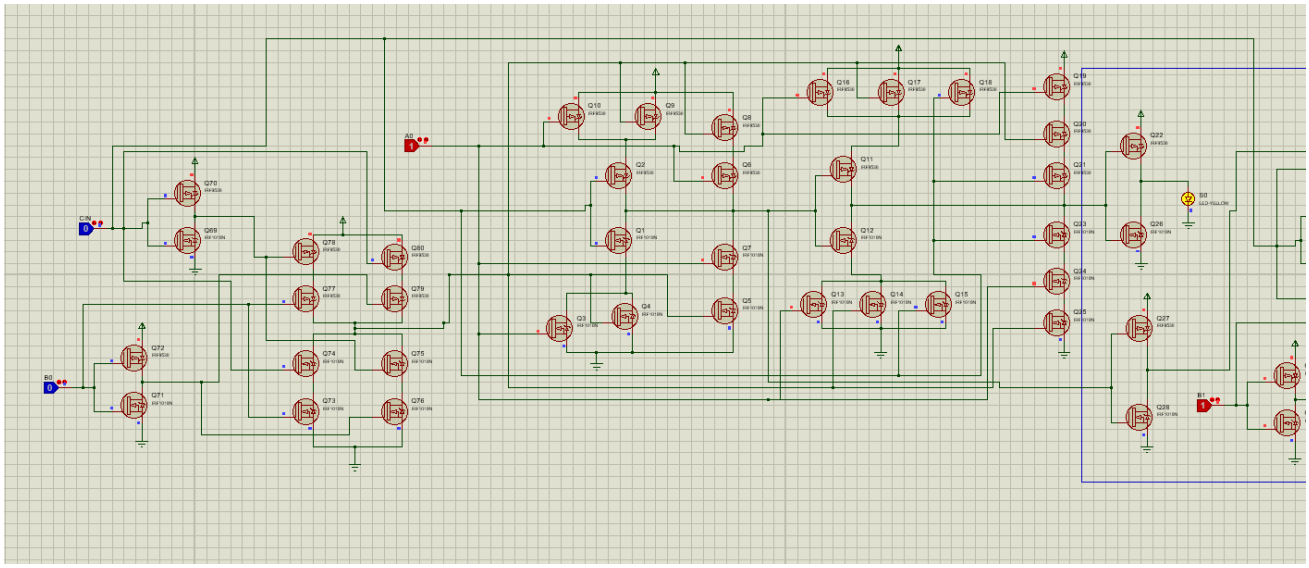
Analyzing 2 example 1 for addition mode and other for subtracting:

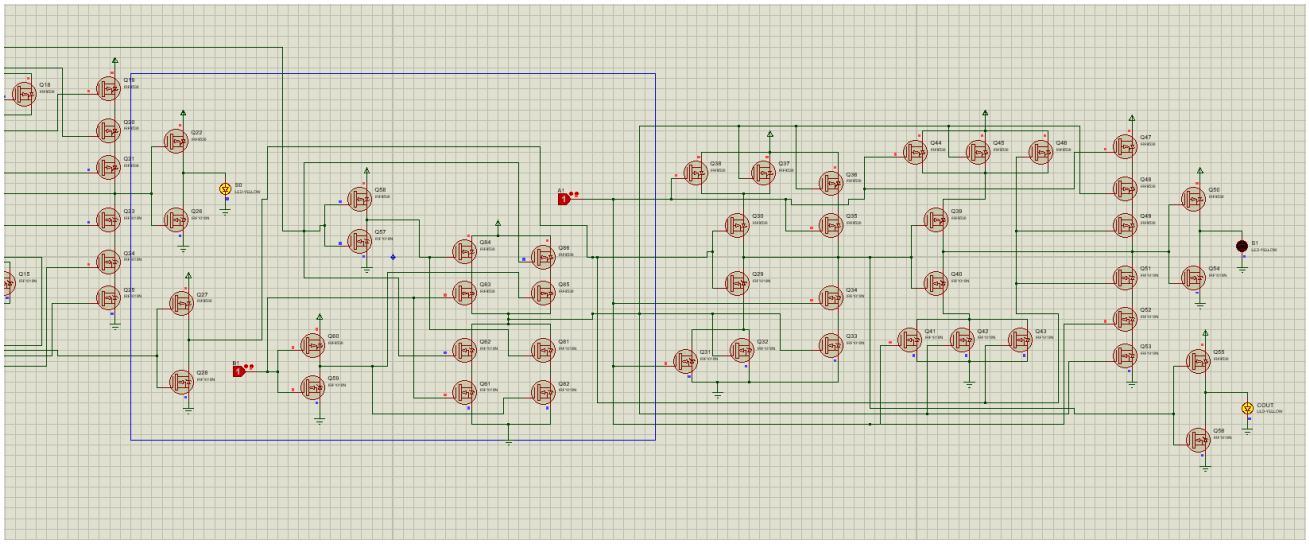
Ex1: addition of 3 ’11’ and 2 ‘10’

Cin =0, M = 0 meaning that Circuit is in addition mode.

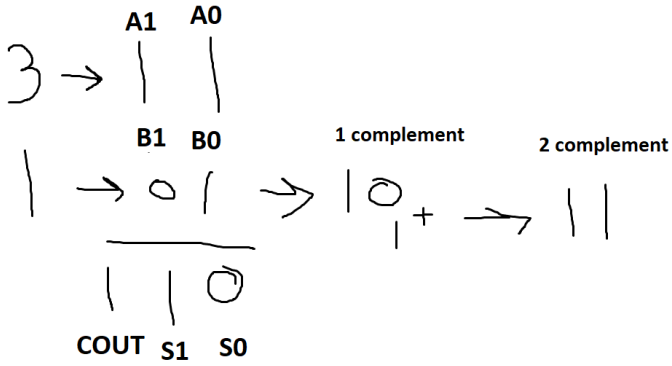


Using CMOS:





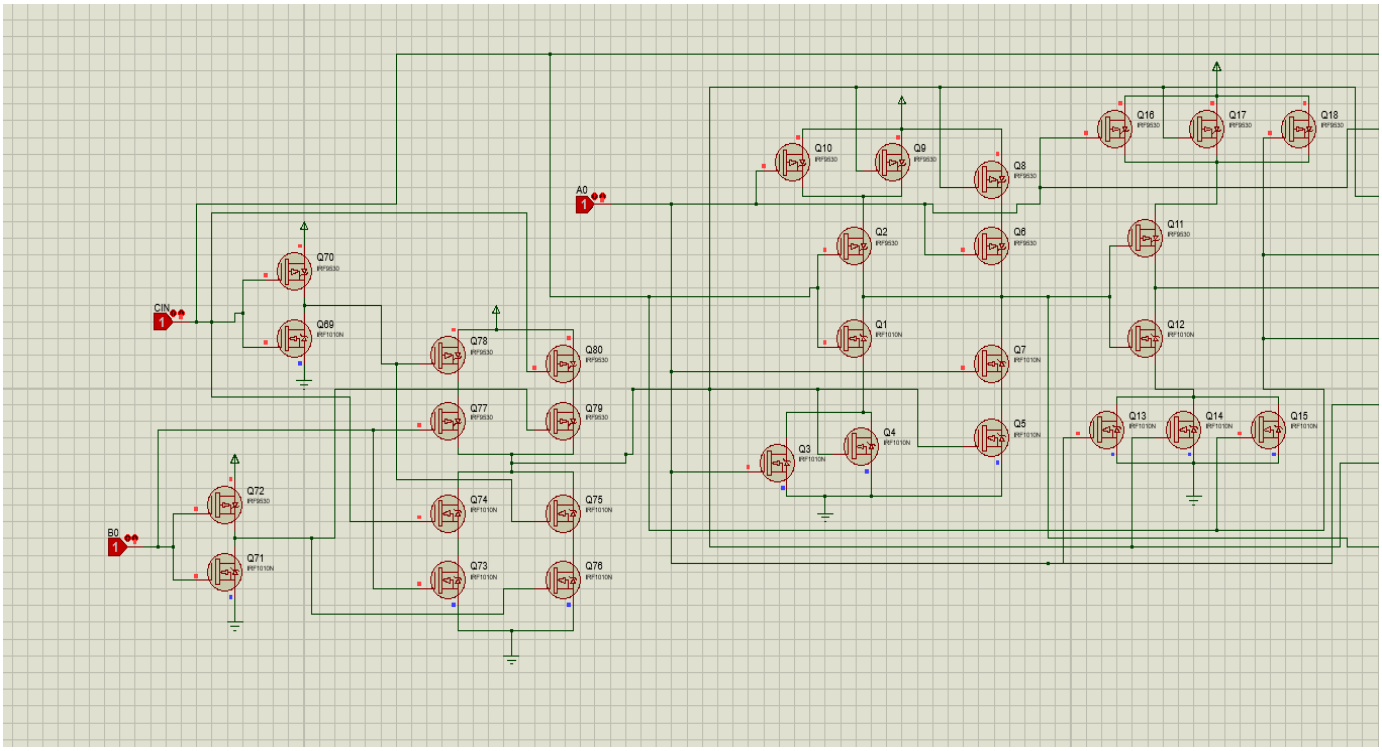
Ex2: Subtracting 3 ’11’ and 1 ‘01’:

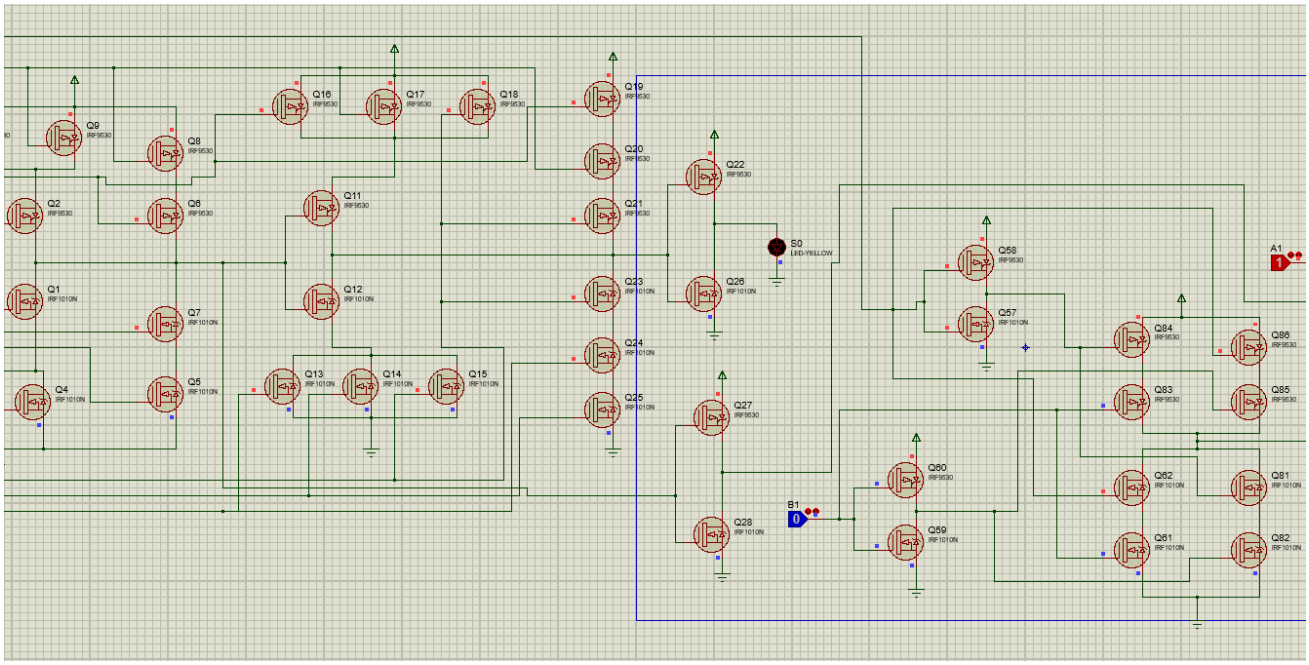


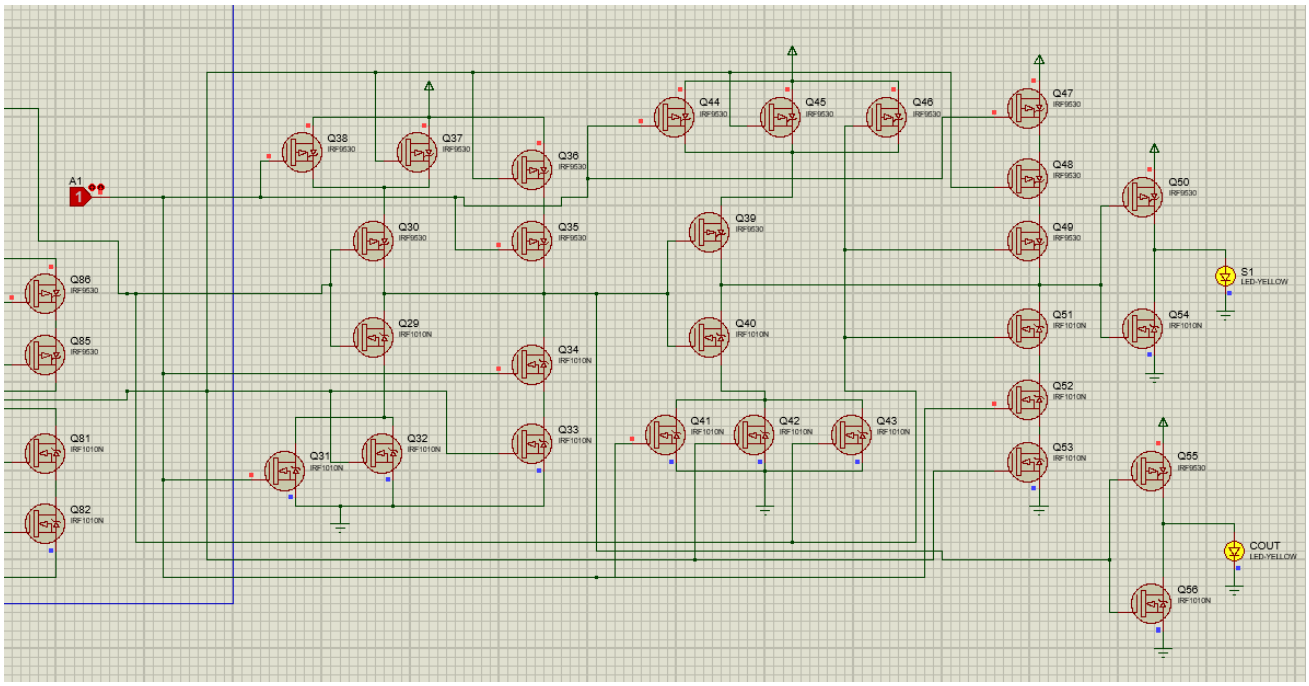
In Subtractor mode M is set to 1 which as discussed above produce the B complement while also carrying the input is 1. As a result, the complemented B inputs are added to A, and 1 is added via the input carry, which is nothing more than a 2's complement operation. As a result, the subtraction operation is carried out.

In subtraction we convert the number to its 1 complement so 1 ‘01’ to ‘10’ then adding 1 to it to get 2 complement so it becomes ‘11’ then adding 3 to that number resulting in ‘110’

Using CMOS:




Q9
Q8
Q16
Q17
Q18
Q19
Q20
Q22
Q2
Q6
Q11
Q21
S0
LED-YELLOW
Q58
A1
Q1
Q12
Q23
Q26
Q57
Q84
Q86
Q7
Q24
Q4
Q5
Q13
Q14
Q15
Q25
Q27
Q83
Q85
Q60
Q62
Q81
B1
Q28
Q59
Q61
Q82


A1
Q38
Q37
Q36
Q44
Q45
Q46
Q47
Q48
Q50
Q30
Q35
Q39
Q49
S1
LED-YELLOW
Q86
Q29
Q40
Q51
Q54
Q85
Q34
Q52
Q81
Q31
Q32
Q33
Q41
Q42
Q43
Q53
Q55
COUT
LED-YELLOW
Q82
Q56

Conclusions

As a summary we were able to design a 2-bit adder/subtractor after going through its working principle, block diagram and the procedures required to implement a subtractor to parallel Full adders, then we discuss how to implement such a circuit first using sequential circuit obtain both its truth table and Output equations then implementing the sequential circuit using CMOS in Proteus Simulation software discussing few live examples to check if it's working.

References

1 – ELECTRONICS HUB, [online], viewed in June 5, 2021, URL =

https://www.electronicshub.org/binary-adder-and-subtractor