Omar Naffaa, EIT

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Education

California State Polytechnic University, Pomona Pomona, CA
Bachelor of Science in Computer Engineering (GPA: 3.81/4.0)

Experience

Systems Engineering Intern May 2020 – October 2020
Niagara Bottling, LLC *Diamond Bar, CA*

- Designed a secure user management interface to add users to Niagara's Ignition Gateway, reducing employee downtime to access Ignition projects
- Developed scripts to pull data from Husky injection machines, reducing QA technician review time from 15 minutes to 5 minutes
- Automated Ignition setup to generate a standardized gateway setup with minimal user input

5G Self-Healing Network Simulator Researcher September 2018 – May 2020
California State Polytechnic University, Pomona *Pomona, CA*

- Applied C++ object-oriented design in the implementation of a cross-platform Self-Healing 5G network simulator
- Designed a heuristic self-healing algorithm that will be used to heal towers within the simulated network
- Developed a graphical user interface (GUI) with GTK+3 to collect input parameters needed from the end user

Warehouse Management Systems Intern June 2019 – August 2019
Niagara Bottling, LLC *Diamond Bar, CA*

- Developed a low-cost self-checkout embedded system using a Raspberry Pi and USB webcam
- Programmed a responsive UI that uses REST API to open a warehouse gate without human intervention
- Implemented Modbus TCP client to interface with Modbus server of an INTEG JNIOR

Decentralized Wastewater Treatment System Research Assistant June 2018 – June 2019
California State Polytechnic University, Pomona *Pomona, CA*

- Implemented an Android Application to control the treatment system over the cloud
- Created a graphical user interface (GUI) using standard material design principles
- Performed JSON requests to push and pull data from the cloud using Internet of Things (IOT) platform ThingSpeak
- Published conference paper in IEEE 43rd Annual Computer Software and Applications Conference (COMPSAC)

Projects

Reconfigurable SoC | *System Verilog, C, C++, Xilinx Nexys A7*

- Developing hardware cores in System Verilog for the Nexys A7 FPGA
- Wrote drivers in C++ to allow applications to easily interface with designed SoC
- Created various applications that utilize written hardware cores and drivers
- Key components include the GPIO, UART, XADC, PWM, SPI, I2C, and PS2 cores

FPGA Based Frequency / Period Meter | *Verilog, Xilinx Nexys A7, Digilent DAC*

- Implemented sampler modules in Verilog to determine the frequency and period of a generated square wave
- Connected sampler modules to a binary to BCD seven segment display interface designed in Verilog

Big Data Analytics for 5G Self-Healing | *Python, Sklearn, AWS, S3, EMR, EC2*

- Created a simple decision tree model in Python to determine network basestation statuses using sklearn
- Created S3, EMR, and EC2 instances on our AWS Big Data Server

Technical Skills

Languages: C, C++, Python, Verilog/System Verilog, Java, C#, HTML, CSS, SQL, MATLAB, Bash
Developer Tools: Linux/UNIX, Git/GitHub, Visual Studio, Vivado / Vitis (Xilinx), Eclispe, Material-UI, Ignition, Wireshark
Protocols / Libraries: OpenCV, REST, HTTP, JSON, TCP/IP, UDP, OPC, SPI, I2C