Energy and power management in the computing continuum

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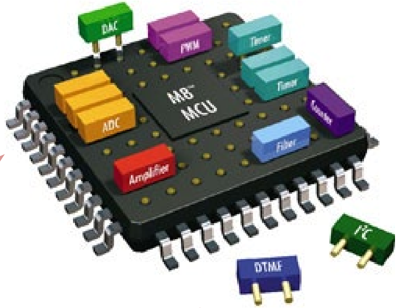
Organization of the Tutorial

- Introduction
- Basics on power consumption
- Power saving blocks and knobs
- Power states and ACPI
- Operating systems integration (the Linux use case)
- Thermal management
- Miscellanea + spots on EU projects
- Conclusions
- Lunch time

Modern applications

MOBILE



LIFE-CRITICAL

PROCESSING
POWER

Rationale: power management requirements

Needs for even more performance

- Plenty of raw computing power
- Multiple resource types

  (PEs, memories, communication channels)
- Complex resource organization

  (clustered. custom busses)

Applications

- Compete for resources
- QoS specification required
- Different Priority levels

Embedded Systems

- Limited resources
- Optimized power consumption
- Mobile Devices

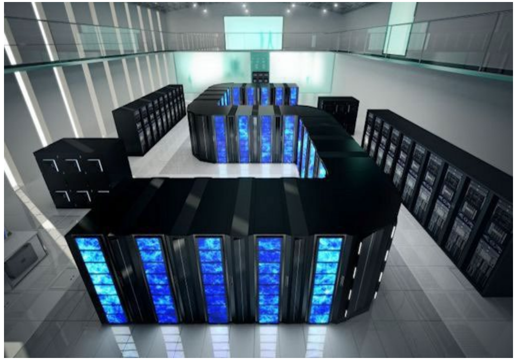
Moving across the computing continuum requirements

Power management goal

- To consume as little power as needed, given system state, configuration and use case

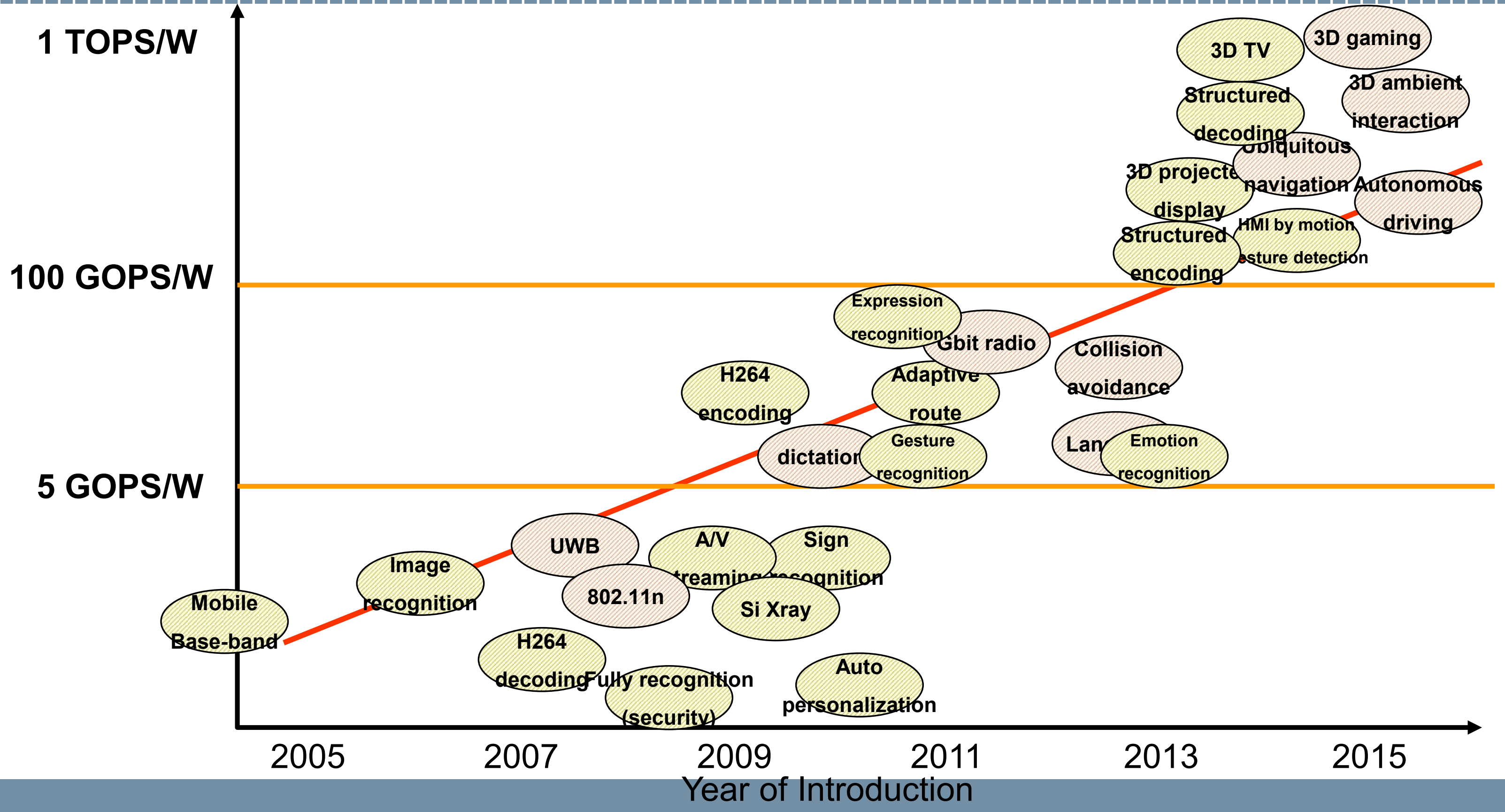
Impact

- Mobile and embedded devices
  - Battery life
  - Skin temperature
  - Regulatory compliance
- HPC and Data centres
  - Cooling effort and costs
  - Carbon footprint

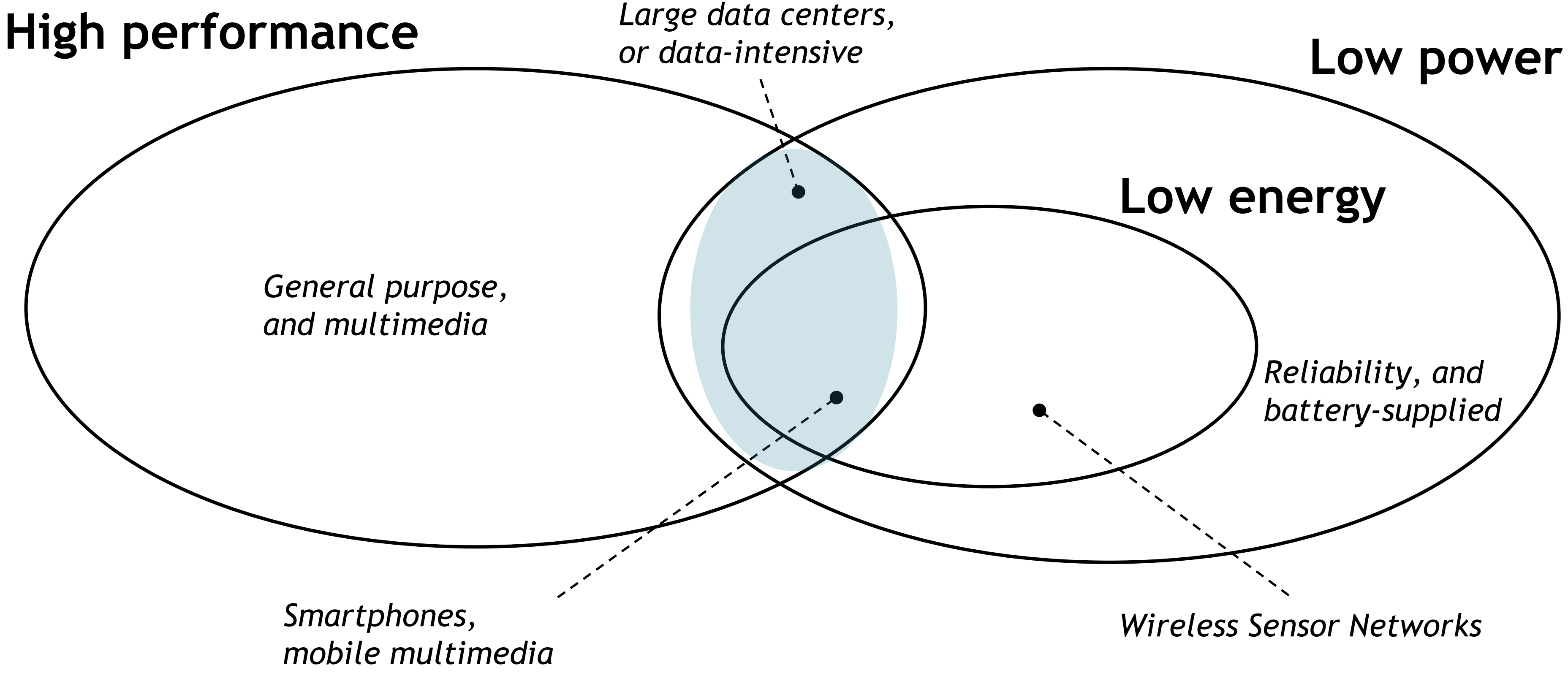


HPC CINECA “Marconi”

Market application rush, not just performance



Application scenarios



Energy, power & thermal

Cross correlation

- The main factors making the difference are the time scale and the constraints/requirements
- Knobs and sensors play also a crucial role

Energy

- Important for battery operated systems (but also peak power is relevant)
- Impact on the total cost of ownership (TCO) of data and HPC centers

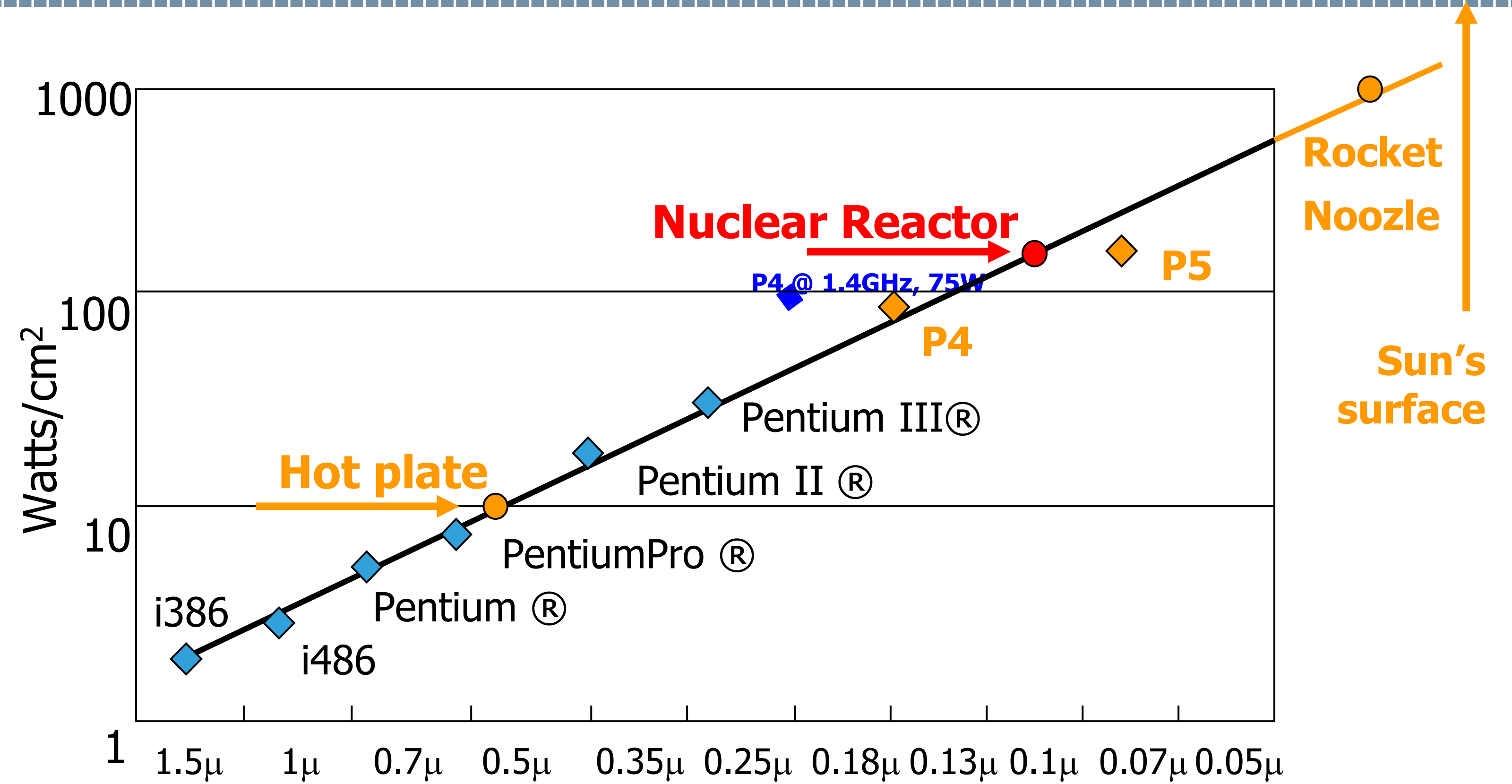
Power

- Import for the design of the power supply and selection of the package
- Impact on the overall power consumption and on the operating temperature
- Average and peak power are both relevant for energy and thermal optimization

Thermal

- Reliability is strongly affected by the operating temperature
- Impact on the cost of the cooling and sustainability (energy recovery?)

Power density trend of single node Intel CPUs



The challenge of a Power-performance tradeoff

Rationale

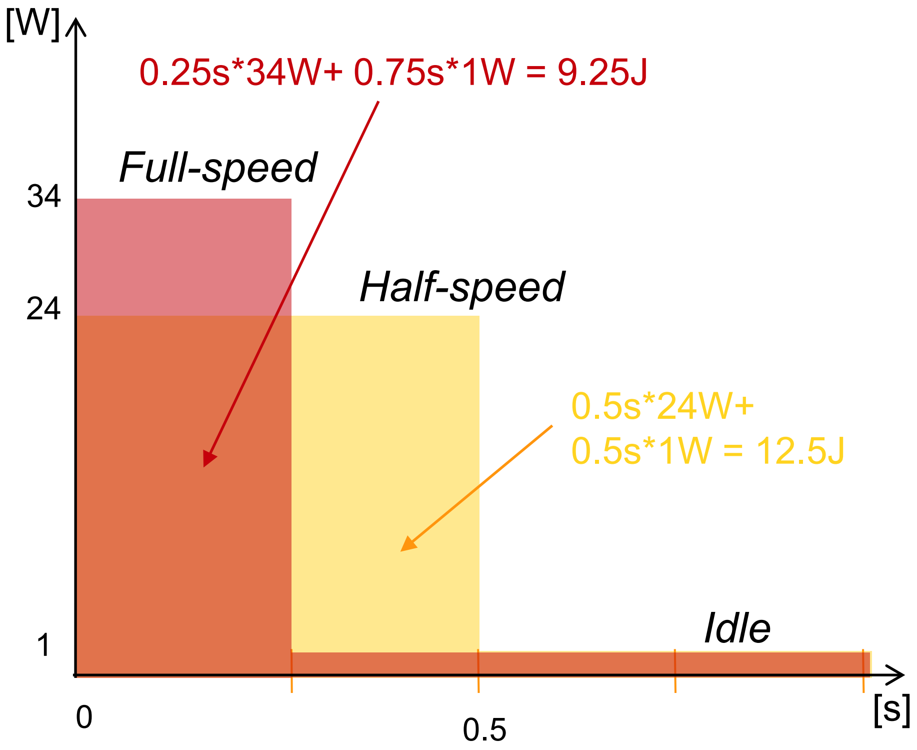
- The driving trade-off in future MPSoCs
- Highly application-dependent

Power optimization goals

- Peak-power
  - Minimize for device and system reliability, life-time
- Energy
  - Minimize for availability

User perceived performance

- Quality-of-Service, e.g., throughput, responsiveness



Tradeoff vs retargetable solutions

Application requirements are very different each other

- How to meet application requirements using “generalized” development?
- How to solve power/performance trade-off?
- How to efficiently tune on-chip resources to applications?

What about current Power Management support?

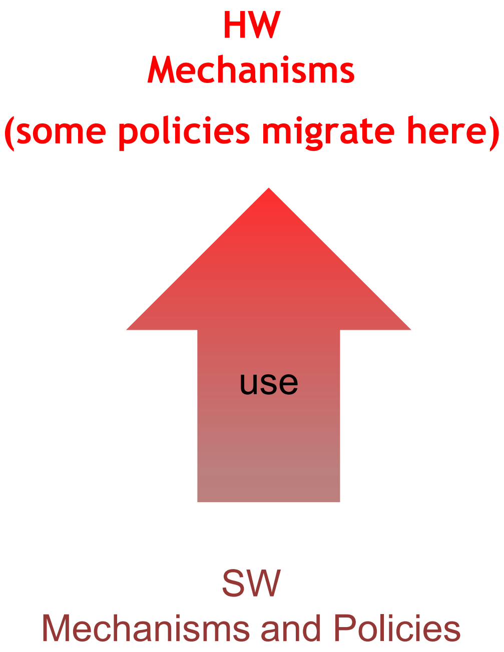
Methodologies vs management

Methodologies

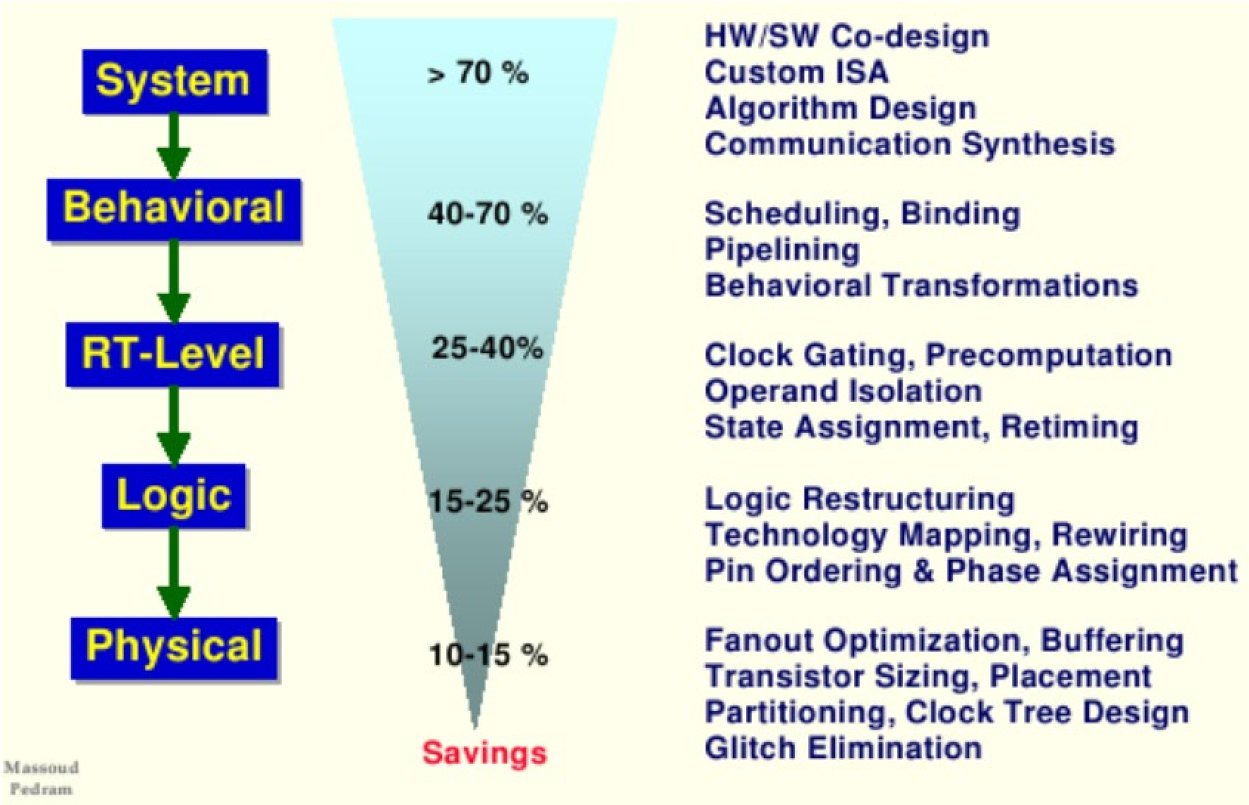
- The *static* view of the problem
- Define building blocks for Power Management
    - e.g., Silicon technology, design guidelines…
- Should properly support run-time management

Management

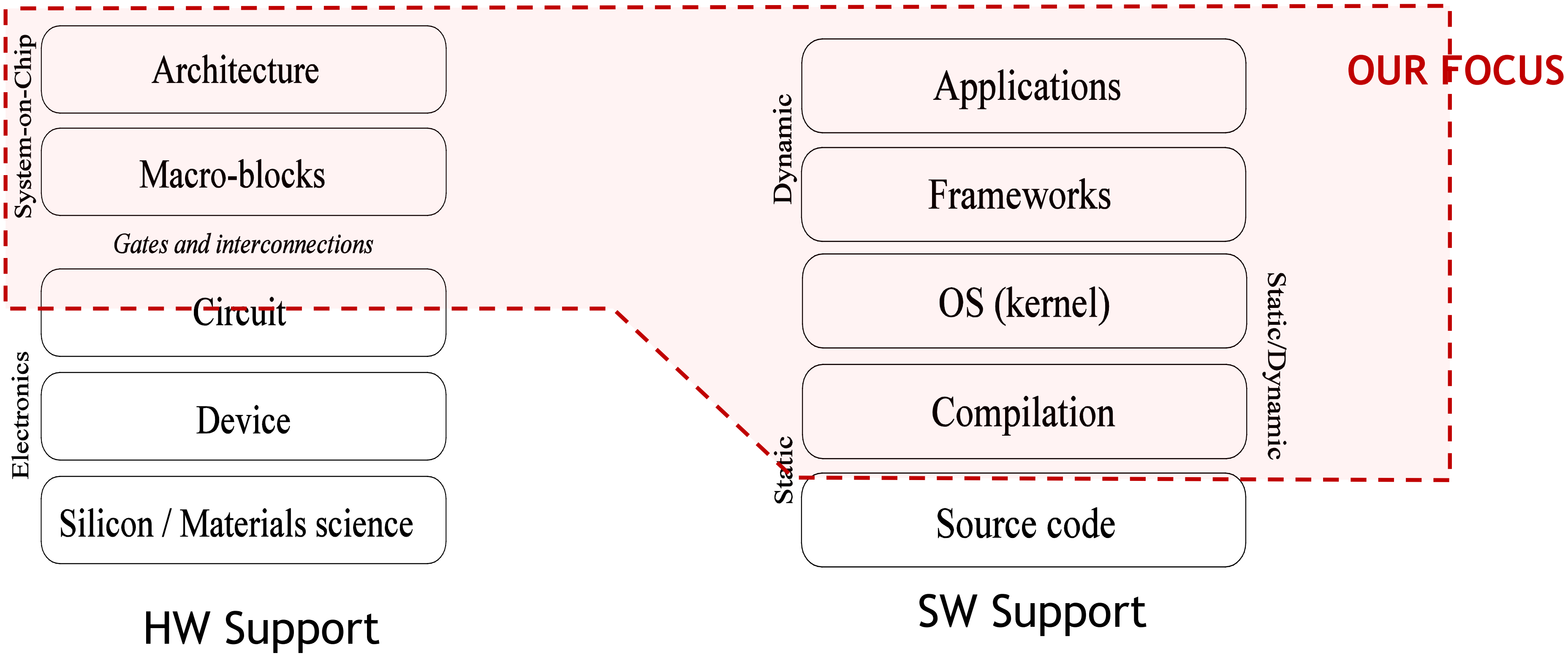
- The *dynamic* view of the problem
- Exploit building blocks to support system-wide optimization
    - Monitoring current application requirements
    - Accounting for resources availability
- Should be flexible and adaptable



Power saving opportunities



Hw and Sw abstraction layers



Monitoring is just a part of the management

Simplest solution

- Just estimate and size for the worst case
- Solution available at design time

Main criticalities

- Reliability of the estimates
- Change of scenario (e.g., workload, input data, operating conditions, components, …)
- Too conservative and costly solutions, especially for consumer electronics

Management … means implementing a control system

- Sensing of relevant parameters
- Availability of knobs
- Definition of management policies capable to adapt also at run-time (proactive vs reactive)
- Working possibly on the entire Hw-Sw stack
- For some thermal phenomena, the speed of the overall control loop is crucial

Suggested topics for reviews (others possible)

Goal

- Present the state of the art of a relevant topic/challenge
- Identification of weak points, missing technologies, possible investigations
- 10-20 minutes talk with slides
- Better working in groups

Not exhaustive list of topics (just a suggestion)

- Power monitoring of CPU, GPUs and FPGA hardware (one tech)
- Ageing and reliability related to thermal problems
- Run-time management for Power and Thermal
- Power management in microcontrollers
- Voltage regulators, battery modeling
- Impact of software structure on the power consumption, Security/DOS attacks,…
- Real-time scheduling vs power consumption

Some material where to start

- D. Zoni, L. Cremona and W. Fornaciari, "Design of Side-Channel-Resistant Power Monitors," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 41, no. 5, pp. 1249-1263, May 2022, doi: 10.1109/TCAD.2021.3088781
- D. Zoni, L. Cremona and W. Fornaciari, “Automatic identification and hardware implementation of a resource-constrained power model for embedded systems”, Sustainable Computing: Informatics and Systems, Volume 29, Part B, March 2021, 100467. https://doi.org/10.1016/j.suscom.2020.100467
- AAVV, Predictive Reliability and Fault Management in Exascale Systems: State of the Art and Perspective, ACM Computing Surveys, Vol. 53, No. 5, Article 95. Publication date: September 2020, https://doi.org/10.1145/3403956
- D.Zoni, A.Galimberti, W.Fornaciari, A survey on run-time power monitors at the edge, ACM Computing Surveys, 2023
- D. Zoni, L. Cremona and W. Fornaciari, "All-Digital Control-Theoretic Scheme to Optimize Energy Budget and Allocation in Multi-Cores," in *IEEE Transactions on Computers*, vol. 69, no. 5, pp. 706-721, 1 May 2020, doi:10.1109/TC.2019.2963859

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- A. Bhuiyan, F. Reghenzani, W. Fornaciari and Z. Guo, "Optimizing Energy in Non-Preemptive Mixed-Criticality Scheduling by Exploiting Probabilistic Information," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 39, no. 11, pp. 3906-3917, Nov. 2020, doi: 10.1109/TCAD.2020.3012231
- F. Terraneo, A. Leva, W. Fornaciari and D. Atienza, "Modeling and Simulation Challenges and Solutions in Cooling Systems for Nanoscale Integrated Circuits[Feature]," in *IEEE Circuits and Systems Magazine*, vol. 23, no. 1, pp. 36-56, Firstquarter 2023, doi: 10.1109/MCAS.2023.3234727
- F. Terraneo, A. Leva, W. Fornaciari, M. Zapater and D. Atienza, "3D-ICE 3.0: Efficient Nonlinear MPSoC Thermal Simulation With Pluggable Heat Sink Models," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 4, pp. 1062-1075, April 2022, doi: 10.1109/TCAD.2021.3074613.
- DATA sheets of microcontrollers