**A.A. 2021-2022**

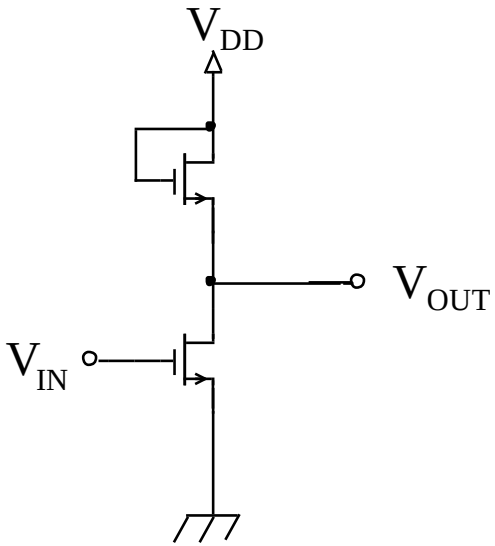
# Elementi di Elettronica (INF)

**Prof. Paolo Crippa**

# Circuiti Logici a MOSFET

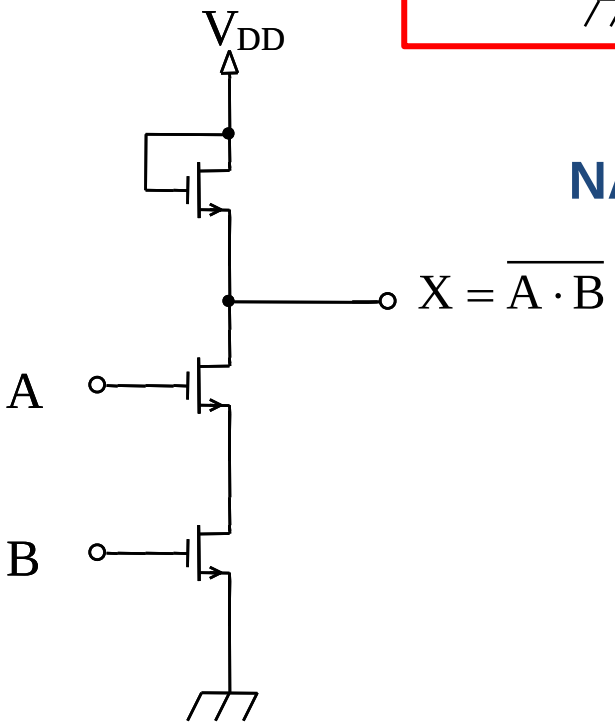
# Logica Random nMOS

## Inverter NMOS

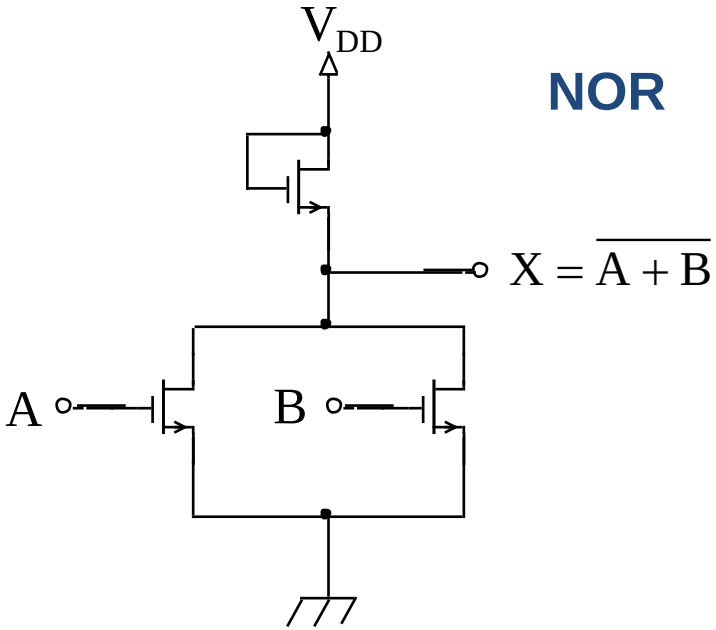



| $V_{IN}$ | $V_{OUT}$ |
|---|---|
| $V_0$ | $V_1$ |
| $V_1$ | $V_0$ |

## NAND

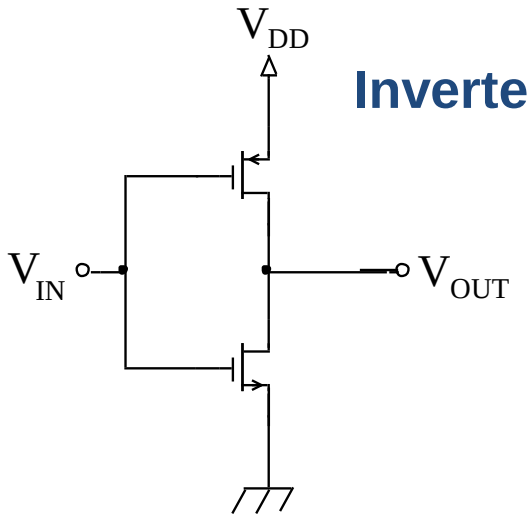



## NOR

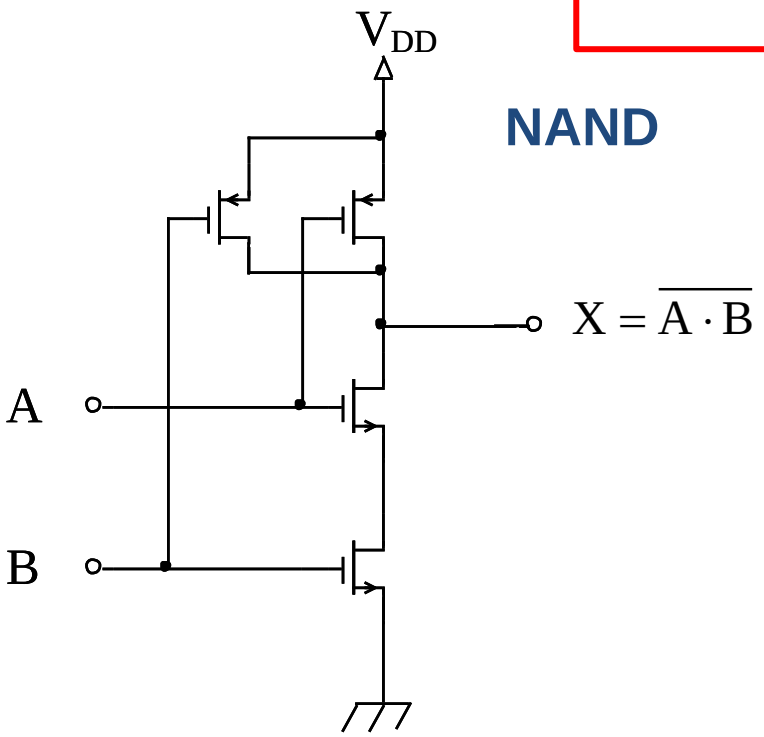


# Logica Random CMOS

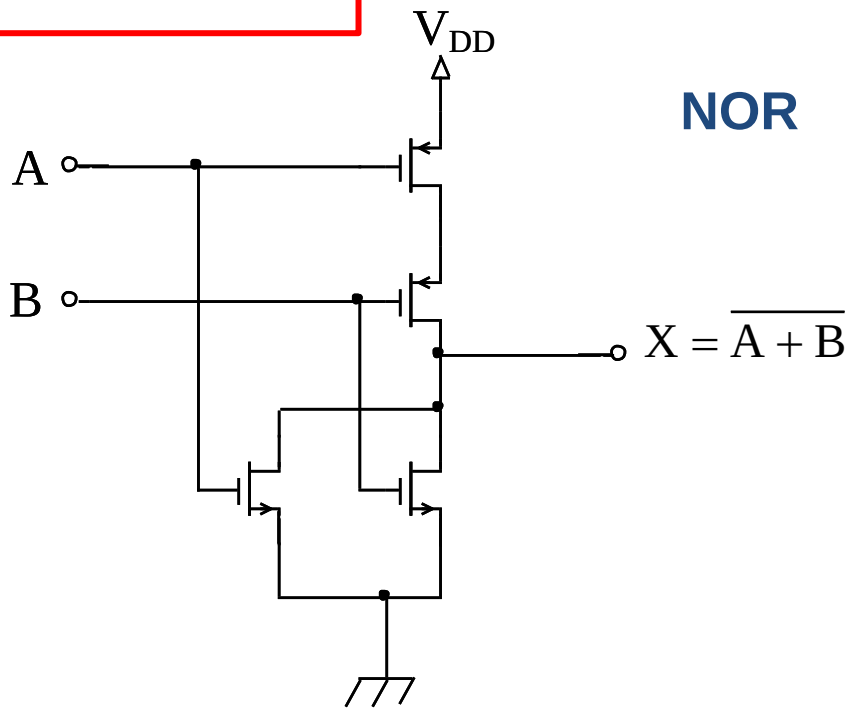
## Inverter CMOS




## NAND

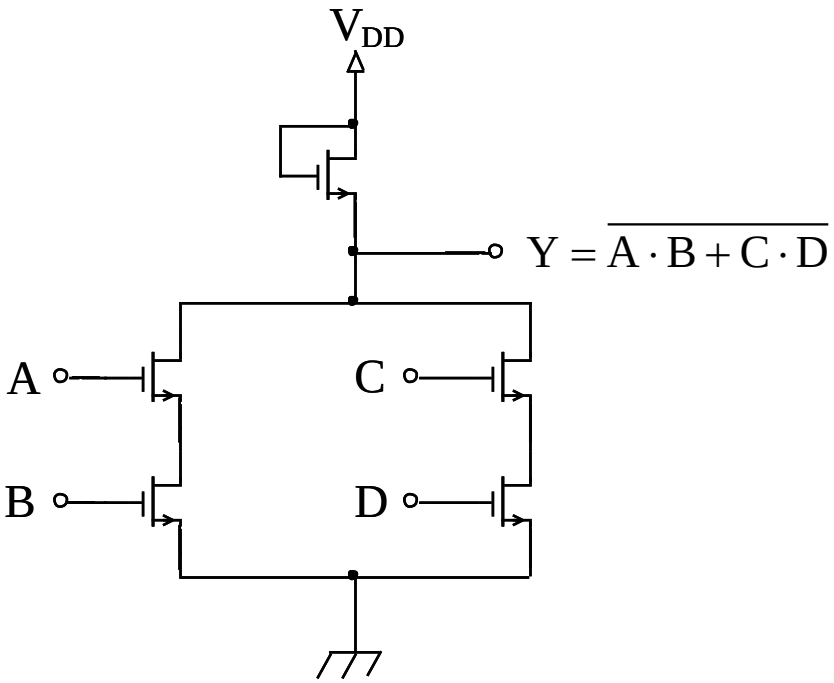


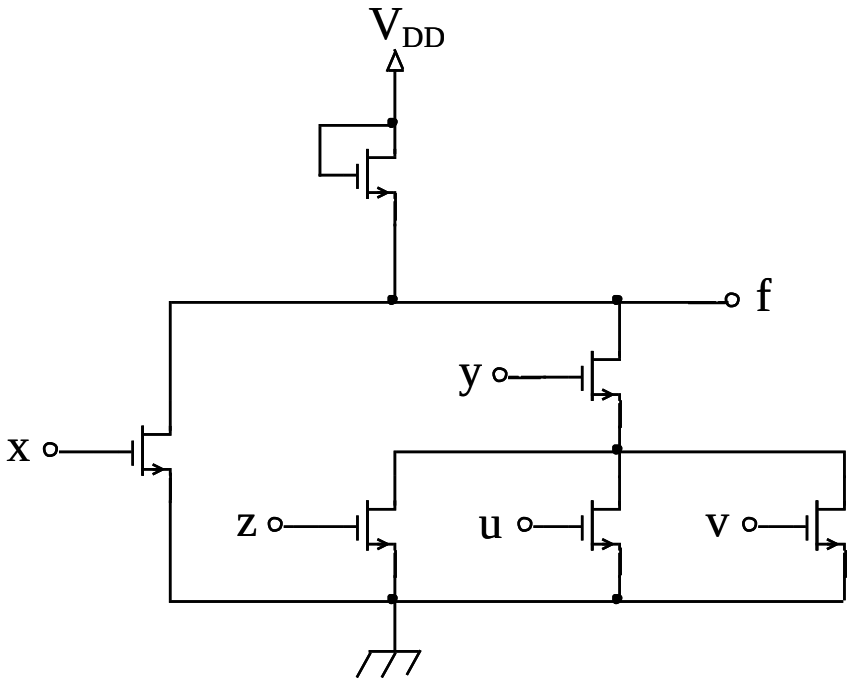

## NOR



# Strutture Complesse nMOS

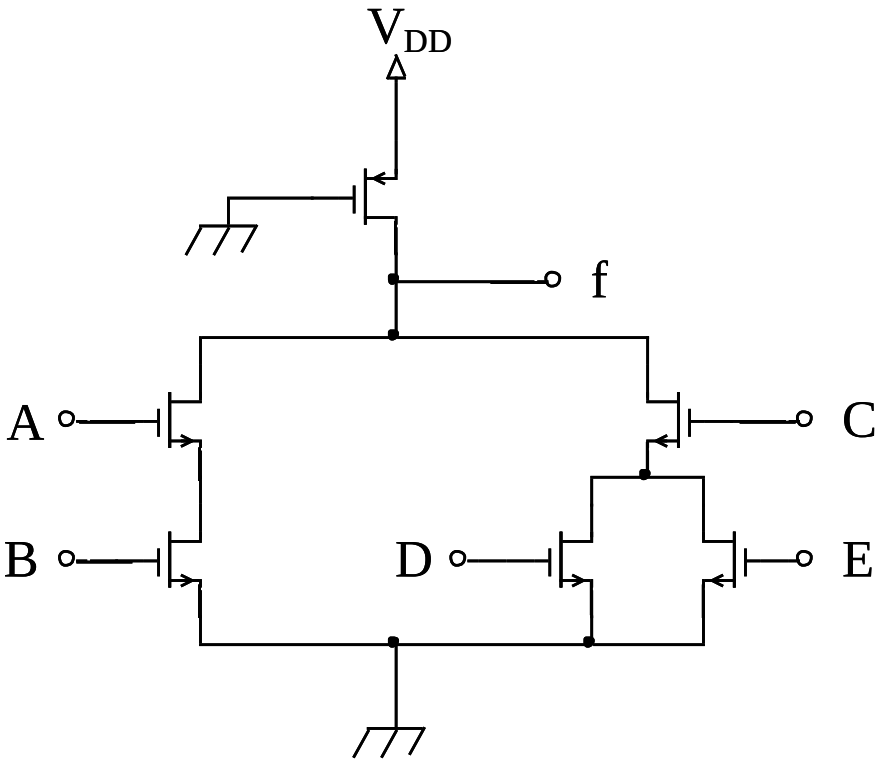





$$f = \overline{(u + v + z) \cdot y + x}$$

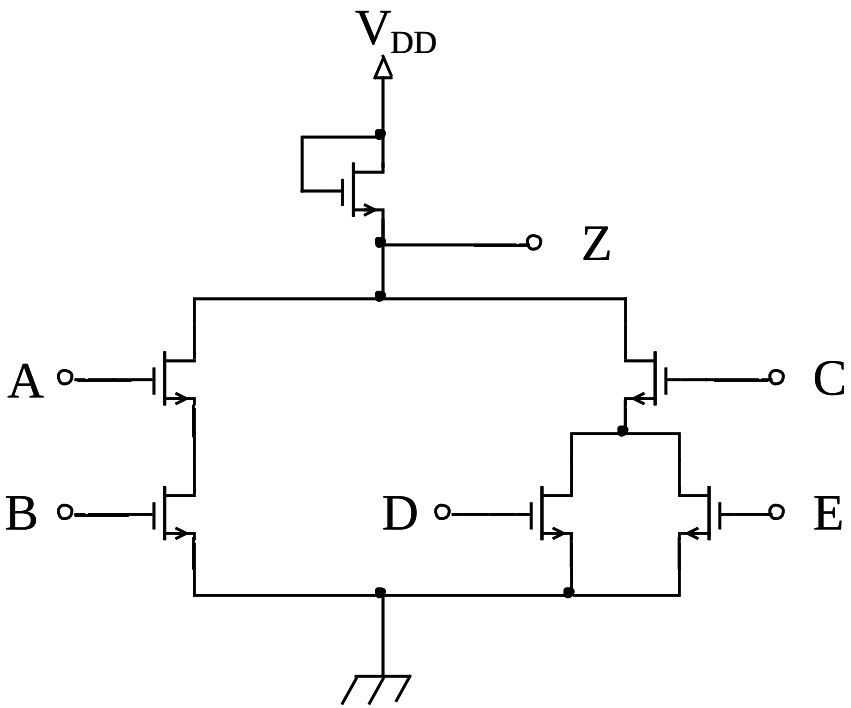
# Pseudo nMOS



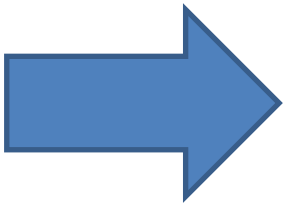

$$f = \overline{A \cdot B + C \cdot (D + E)}$$

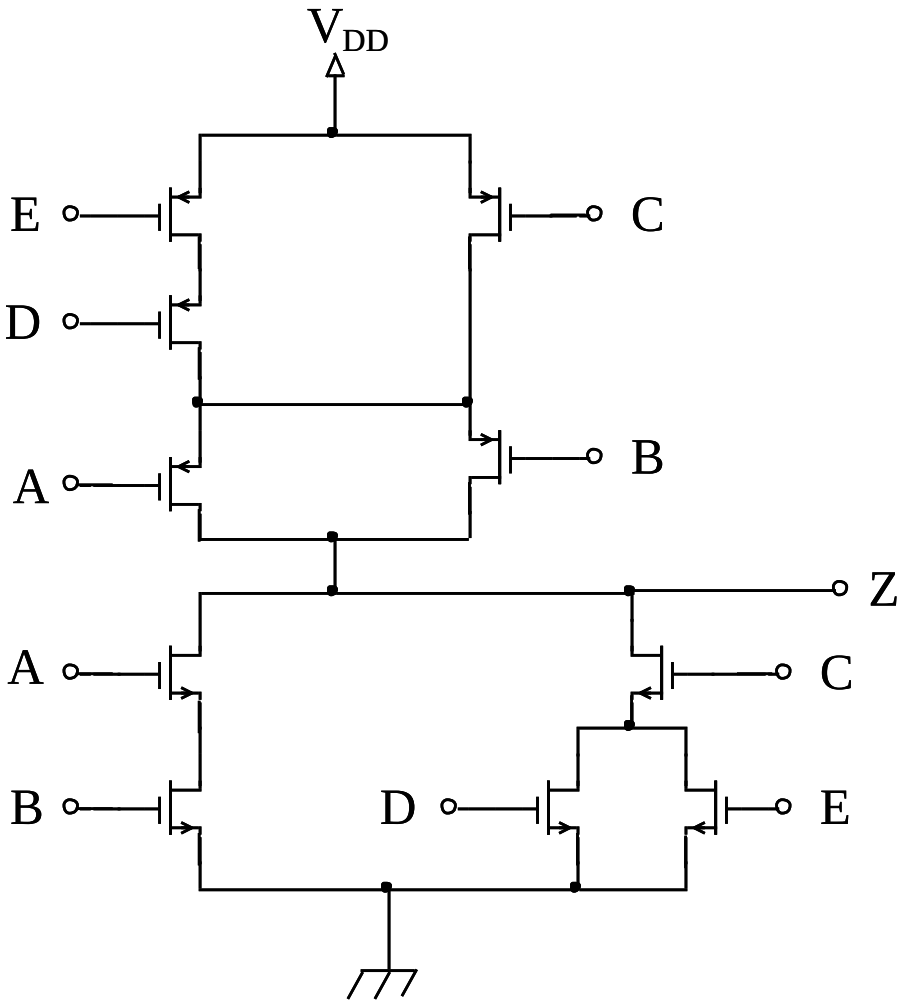
# Strutture Complesse CMOS

$$Z = \overline{A \cdot B + C \cdot (D + E)}$$




nMOS





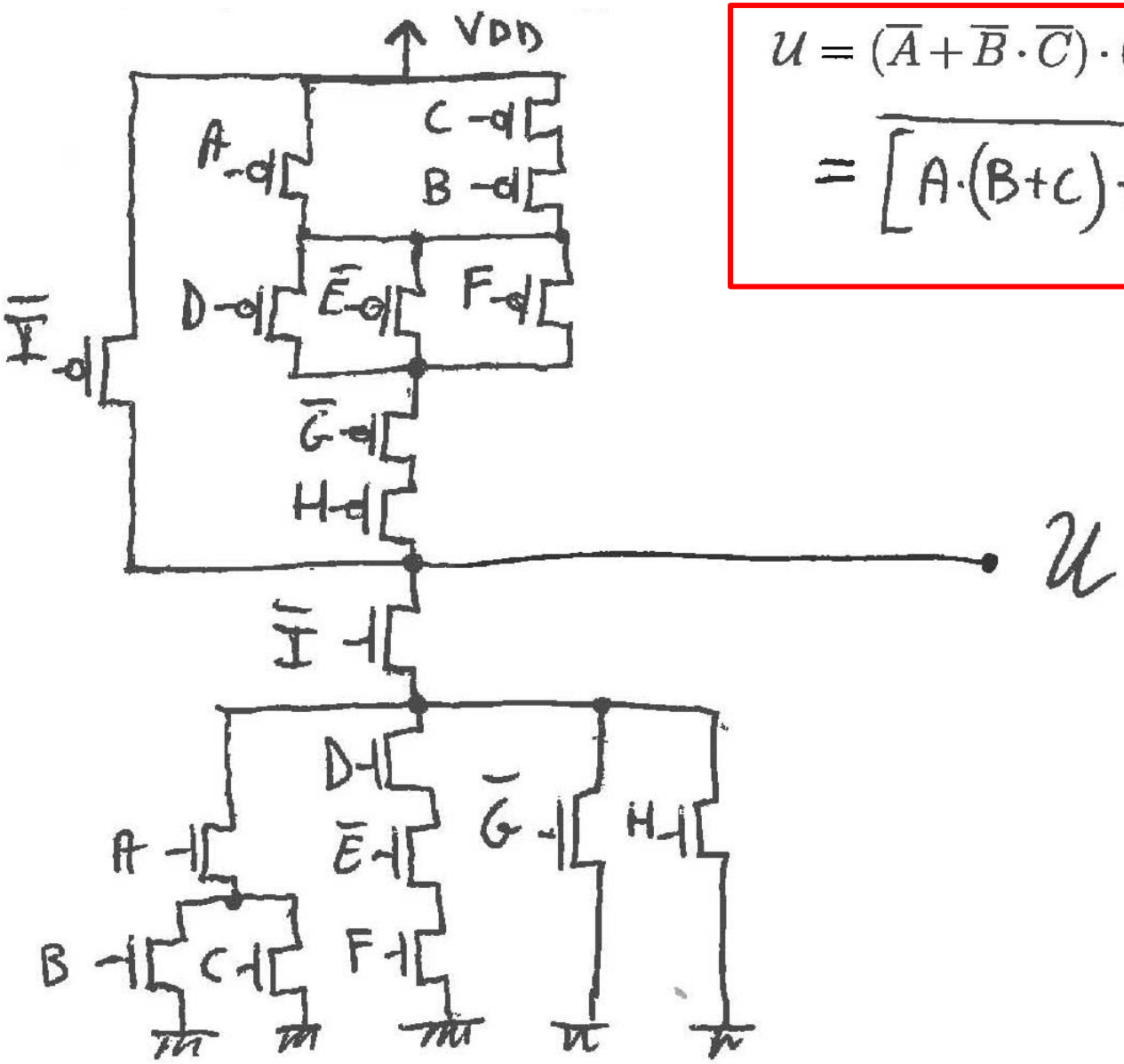

CMOS

# Strutture Complesse CMOS



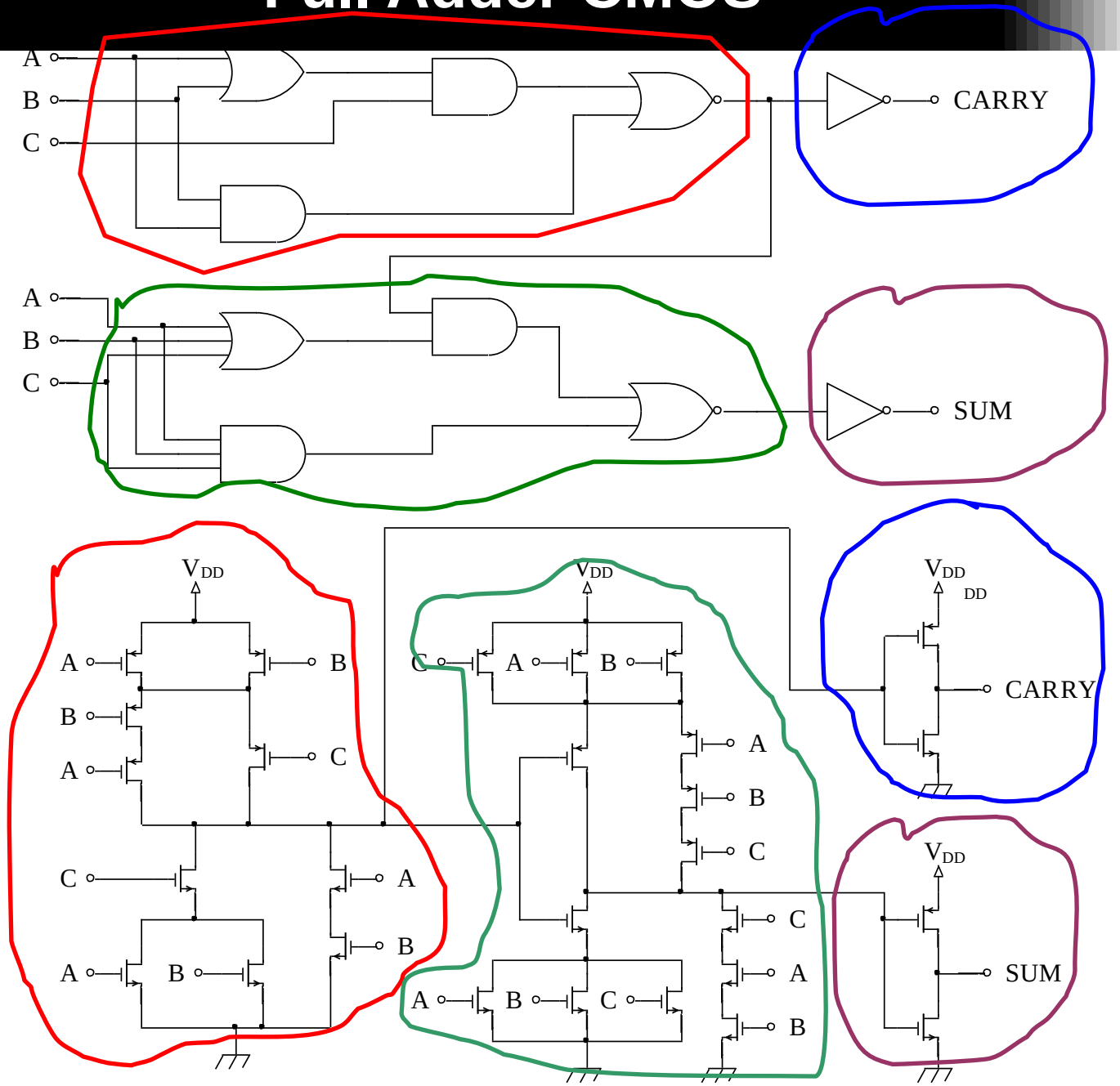
$$U = (\overline{A} + \overline{B} \cdot \overline{C}) \cdot (\overline{D} + E + \overline{F}) \cdot G \cdot \overline{H} + I$$

$$= \overline{\left[ A \cdot (B + C) + D \cdot \overline{E} \cdot F + \overline{G} + H \right] \cdot \overline{I}}$$



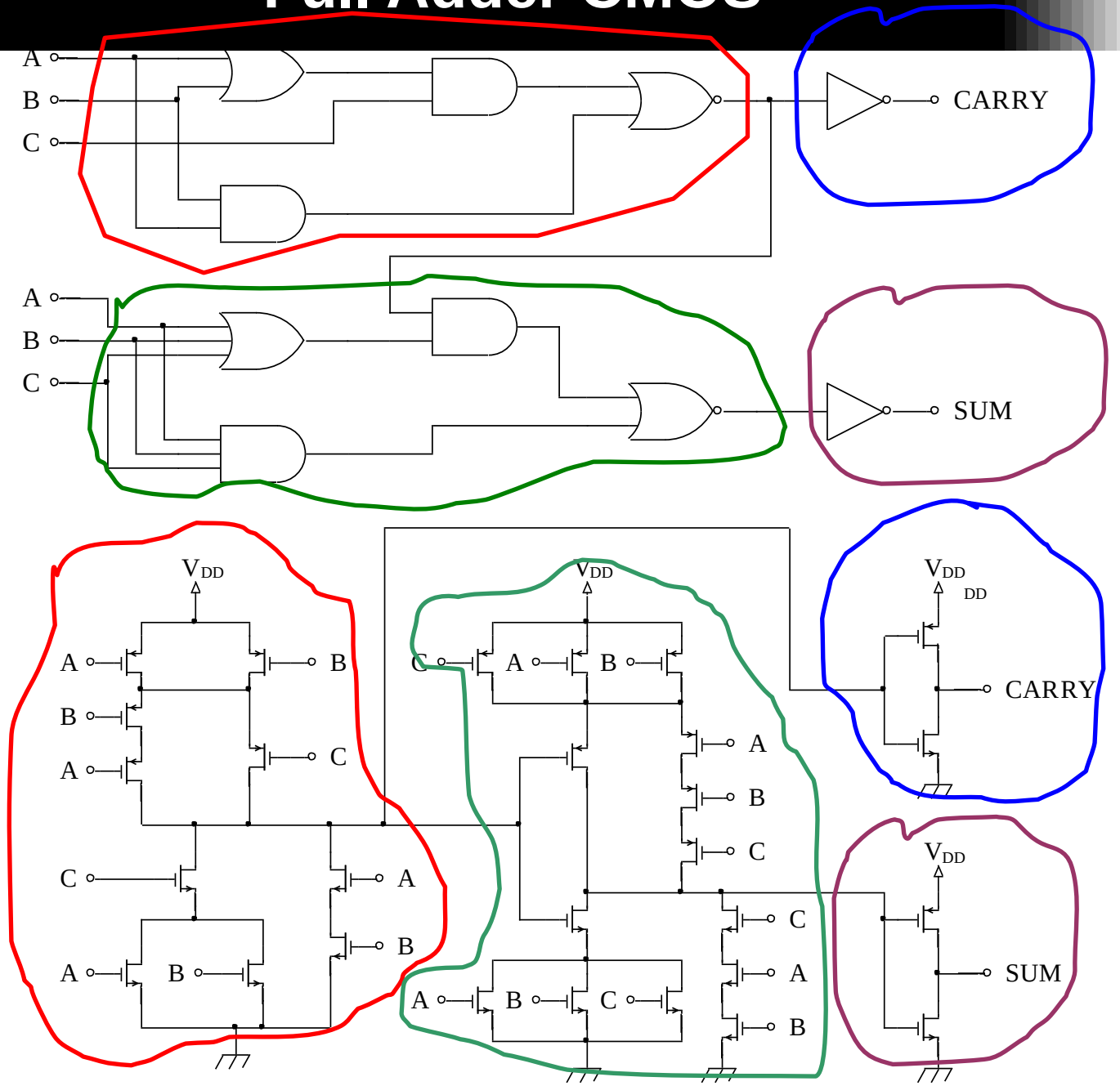
# Full Adder CMOS





# Full Adder CMOS



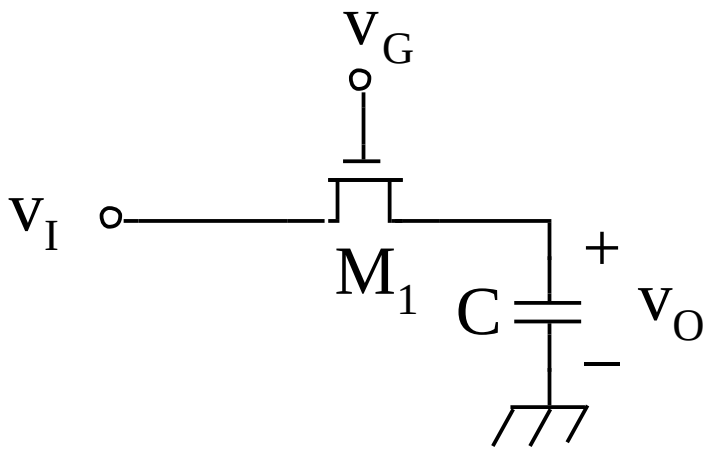


# Pass Transistor nMOS

$V_L = 0\ V$

$V_H = 5\ V$

$V_{TH} = 0.7\ V$

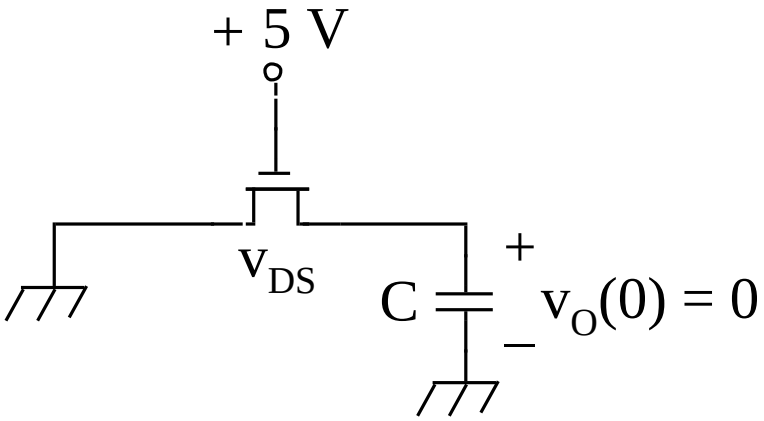


# Pass-Transistor nMOS

**Caso A)**

$V_{TH} = 0.7\ V$

$\mathbf{v_G = V_H = 5\ V}$




$v_{IN} = V_L = 0\ V$

$v_O(0) = V_L = 0\ V$

1) $v_{DS} = 0$ , $v_{GS} > v_{TH}$ , $M_1 = ON$

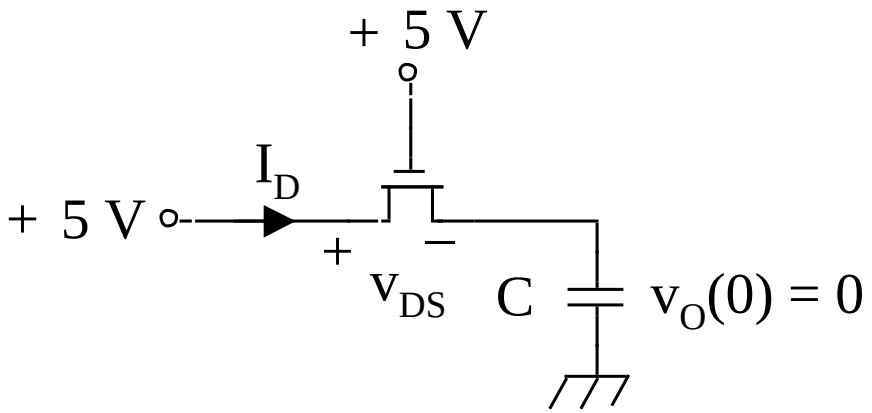
$v_O(t = \infty) = V_L = 0\ V$

# Pass-Transistor nMOS

$V_{TH} = 0.7\ V$

$v_{IN} = V_H = 5\ V$

$v_O(0) = V_L = 0\ V$




2) $v_{DS}(0) = V_H > v_{GS} - V_{TH} = V_H - V_{TH}$ $M_1$ in saturazione

$I_D = \frac{\beta}{2} \cdot (v_{GS} - V_{TH})^2 \rightarrow$ C si carica, C smette di caricarsi quando $I_D = 0$

$\Rightarrow v_G - v_{OM} - V_{TH} = 0 \Rightarrow \mathbf{v_{OM}} = v_G - V_{TH} = 5 - V_{TH}$ Valore massimo di $v_O$

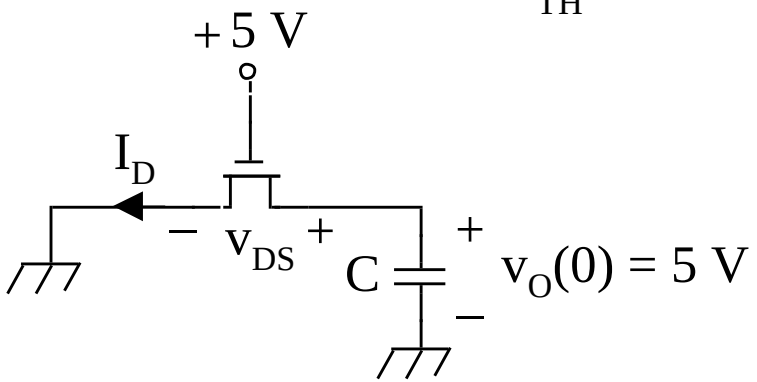
$v_O(t = \infty) = V_H - V_{TH} = 5\ V - 0.7\ V = 4.3\ V$

# Pass-Transistor nMOS

$V_{TH} = 0.7\ V$

$v_{IN} = V_L = 0\ V$

$v_O(0) = V_H = 5\ V$




3) C si scarica attraverso $M_1$

Inizialmente con $v_O \geq v_{GS} - V_{TH}$ $M_1$ è in saturazione

$$I_D = \frac{\beta}{2} \cdot (v_{GS} - V_{TH})^2 = -C \cdot \frac{dv_O}{dt}$$

poi con $v_O \leq v_{GS} - V_{TH}$ $M_1$ è in triodo

$$I_D = \beta \cdot \left[ (v_{GS} - V_{TH}) \cdot v_O - \frac{v_O^{\,2}}{2} \right] = -C \cdot \frac{dv_O}{dt}$$

al termine del triodo $v_O = 0$.

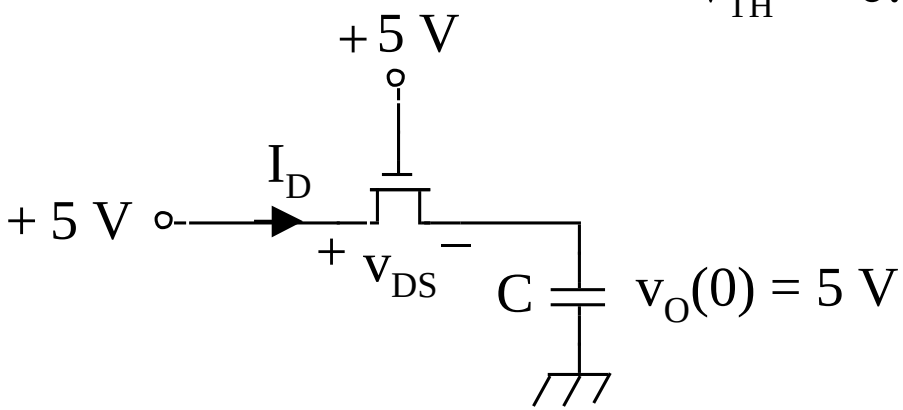
$v_O(t = \infty) = V_L = 0\ V$

# Pass-Transistor nMOS

$V_{TH} = 0.7\ V$

$v_{IN} = V_H = 5\ V$

$v_O(0) = V_H = 5\ V$




$v_{DS} = 0\ V \qquad v_{GS} = 0\ V < V_{TH}$

$v_O(t = \infty) = V_H = 5\ V$

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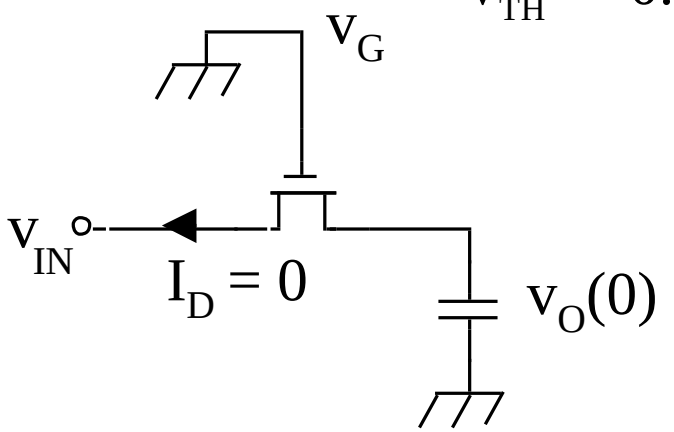
## Caso B)

$V_{TH} = 0.7\ V$

$\mathbf{v_G = V_L = 0\ V}$

$v_{GS} = v_G - v_S$ dove $v_S \geq 0 \Rightarrow v_{GS} \leq 0\ V$

quindi $v_{GS} < V_{TH} \rightarrow$ $M_1$ = OFF




Qualsiasi sia il valore di $V_{IN}$ $v_O = v_O(0)$

$v_O(t = \infty) = v_O(0)$

# Pass-Transistor nMOS

| $v_I$ | $v_G$ | $v_O(t=\infty)$ |
|---|---|---|
| 0 V | 5 V | 0 V |
| 5 V | 5 V | $\begin{cases} 5\,\text{V} \\ 4.3\,\text{V} \end{cases}$ |
| 0 V | 0 V | $v_O(0)$ |
| 5 V | 0 V | $v_O(0)$ |

| $v_I$ | $v_G$ | $v_O(t=\infty)$ |
|---|---|---|
| $V_L$ | $V_H$ | $V_L$ |
| $V_H$ | $V_H$ | $V_H$ $\begin{cases} V_H \\ V_H - V_{TH} \end{cases}$ |
| $V_L$ | $V_L$ | $v_O(0)$ |
| $V_H$ | $V_L$ | $v_O(0)$ |

**Circuito non rigenerativo !**

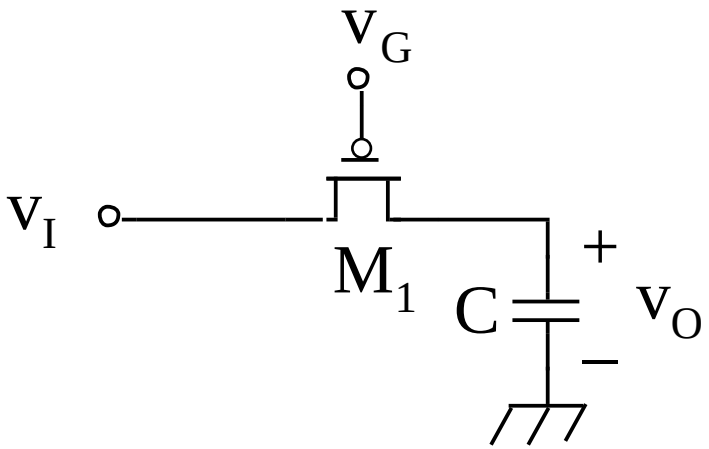
# Pass Transistor pMOS



$$V_L = 0\ V$$

$$V_H = 5\ V$$

$$V_{TH} = -0.7\ V$$



# Pass-Transistor pMOS

| $v_I$ | $v_G$ | $v_O(t=\infty)$ |
|---|---|---|
| 0 V | 5 V | $v_O(0)$ |
| 5 V | 5 V | $v_O(0)$ |
| 0 V | 0 V | $\begin{cases} 0\,\text{V} \\ 0.7\,\text{V} \end{cases}$ |
| 5 V | 0 V | 5 V |

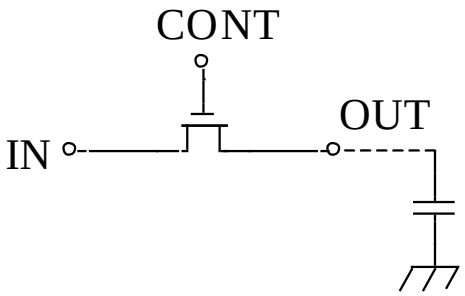
| $v_I$ | $v_G$ | $v_O(t=\infty)$ |
|---|---|---|
| $V_L$ | $V_H$ | $v_O(0)$ |
| $V_H$ | $V_H$ | $v_O(0)$ |
| $V_L$ | $V_L$ | $V_L$ $\begin{cases} V_L \\ V_L - V_{TH} \end{cases}$ |
| $V_H$ | $V_L$ | $V_H$ |

**Circuito non rigenerativo !**

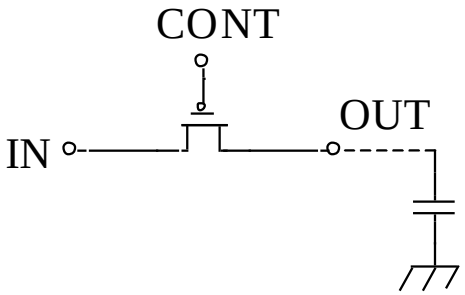
$|V_{TH}|$

# Logica a Pass-Transistor (Trasmission Gate) o Steering Logic






| IN | CONT | OUT |
|---|---|---|
| 0 | 0 | X |
| 1 | 0 | X |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

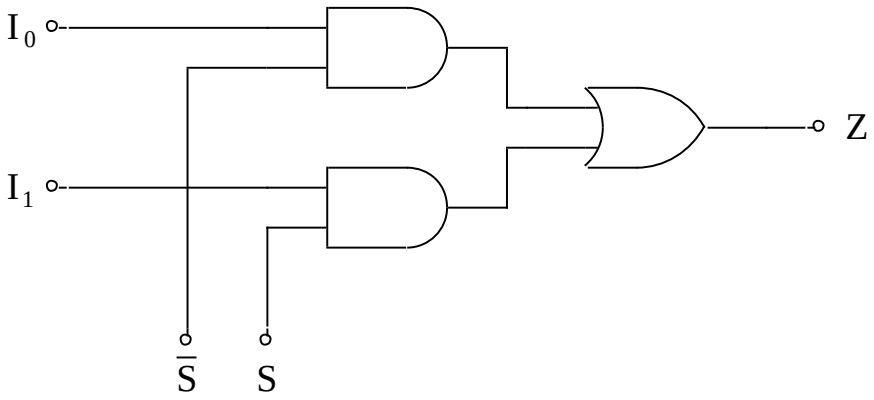


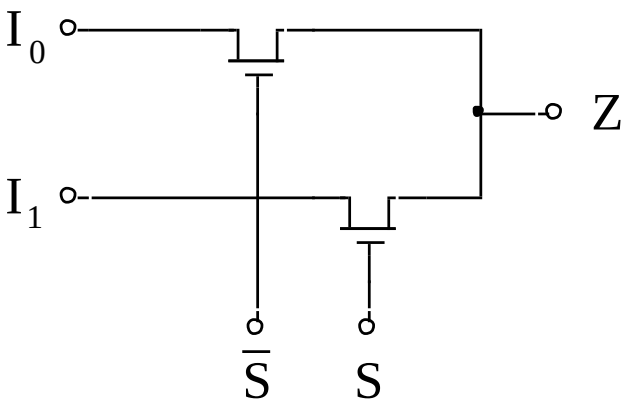

| IN | CONT | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | X |
| 1 | 1 | X |

**Circuiti non rigenerativi**

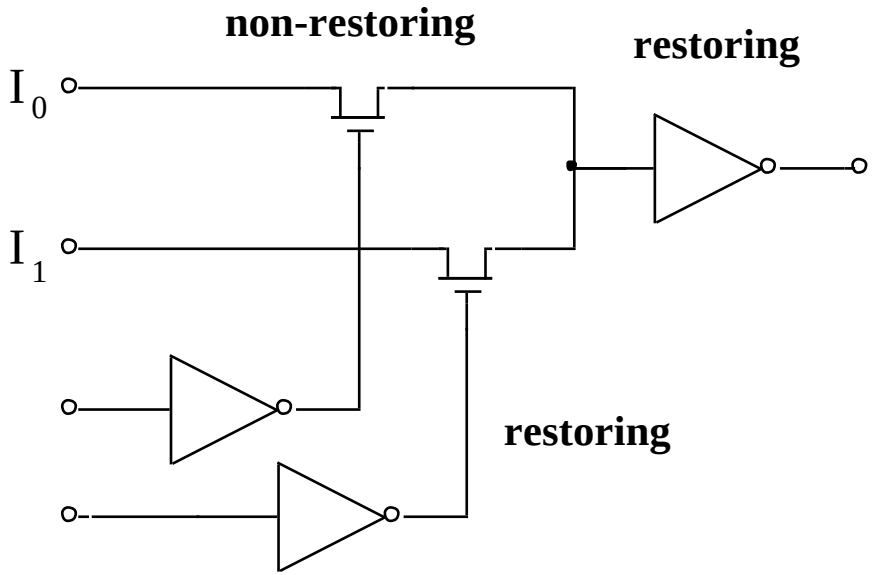
# Selettore con Pass-Transistor





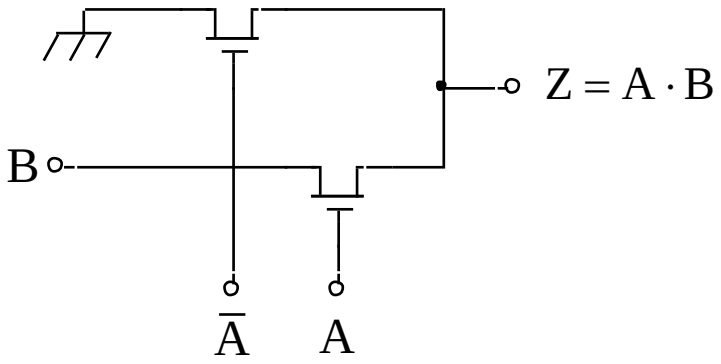

## circuito rigenerativo



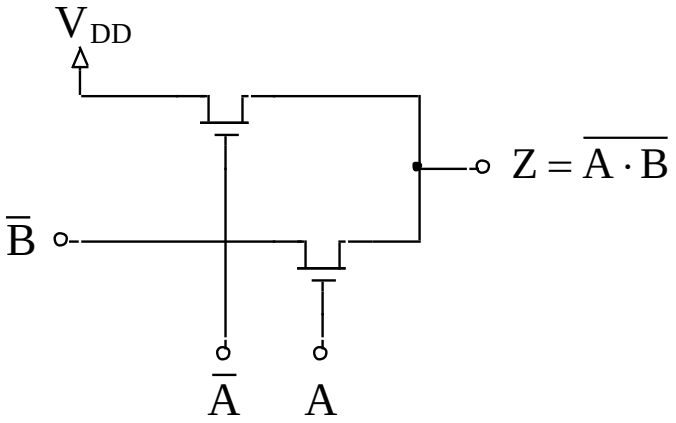
# AND, OR, NAND, NOR a Pass-Transistor



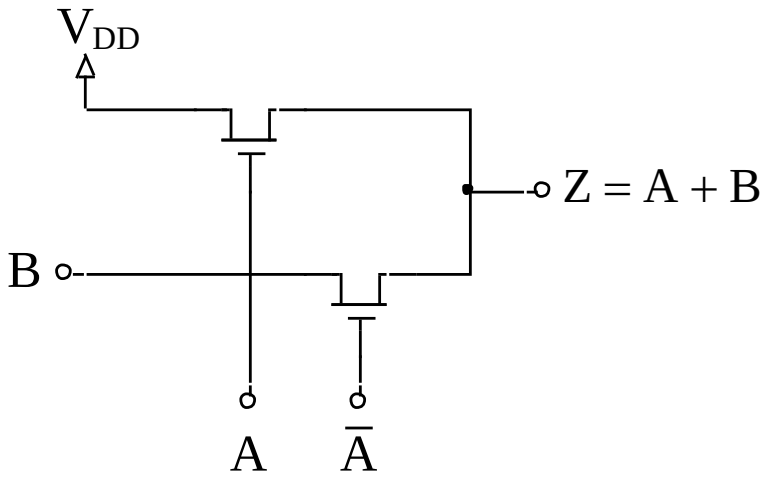
## AND



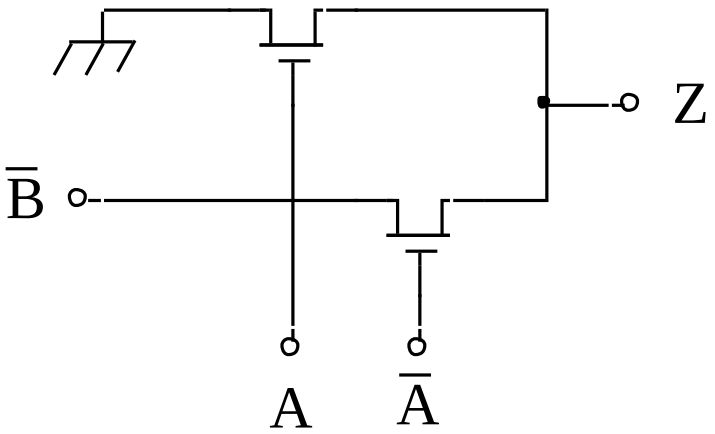

## NAND



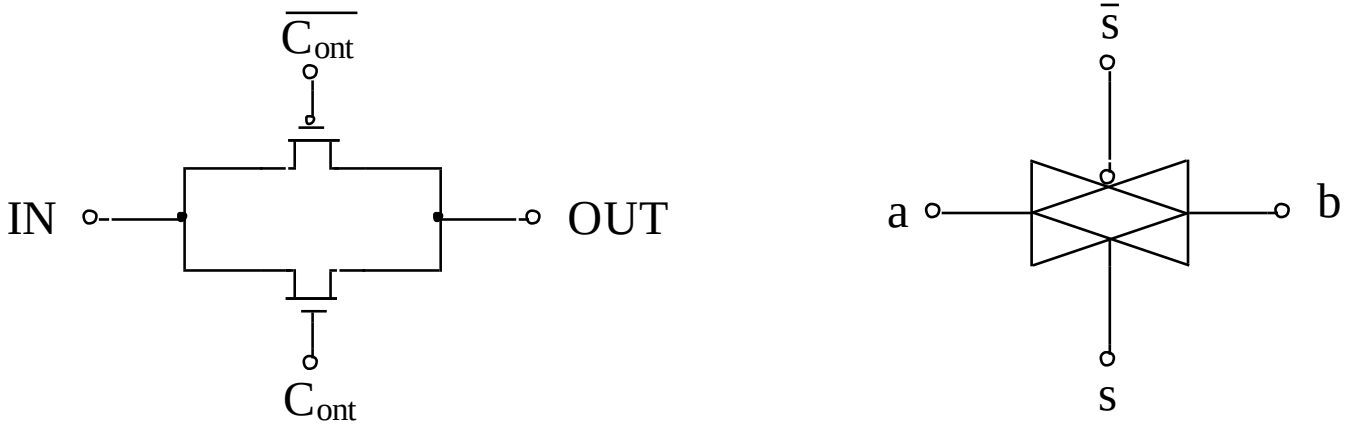

## OR



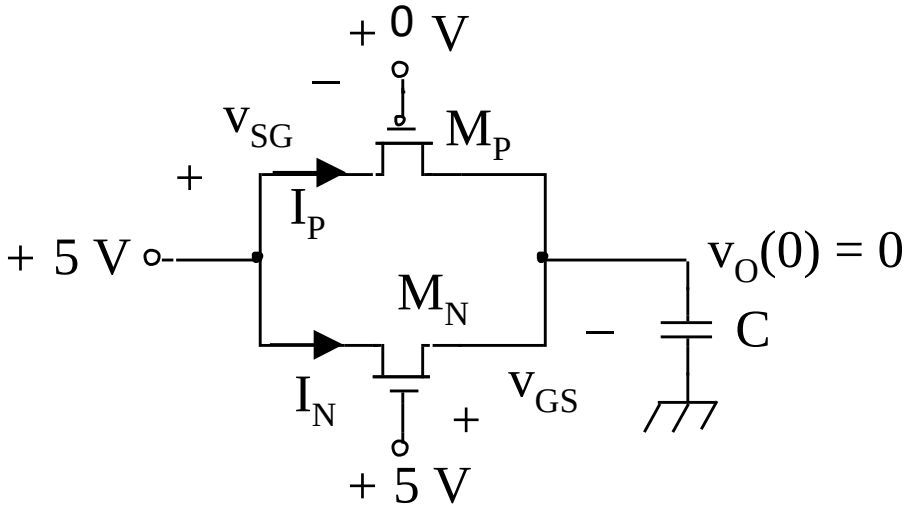

## NOR



# Pass-Transistor CMOS

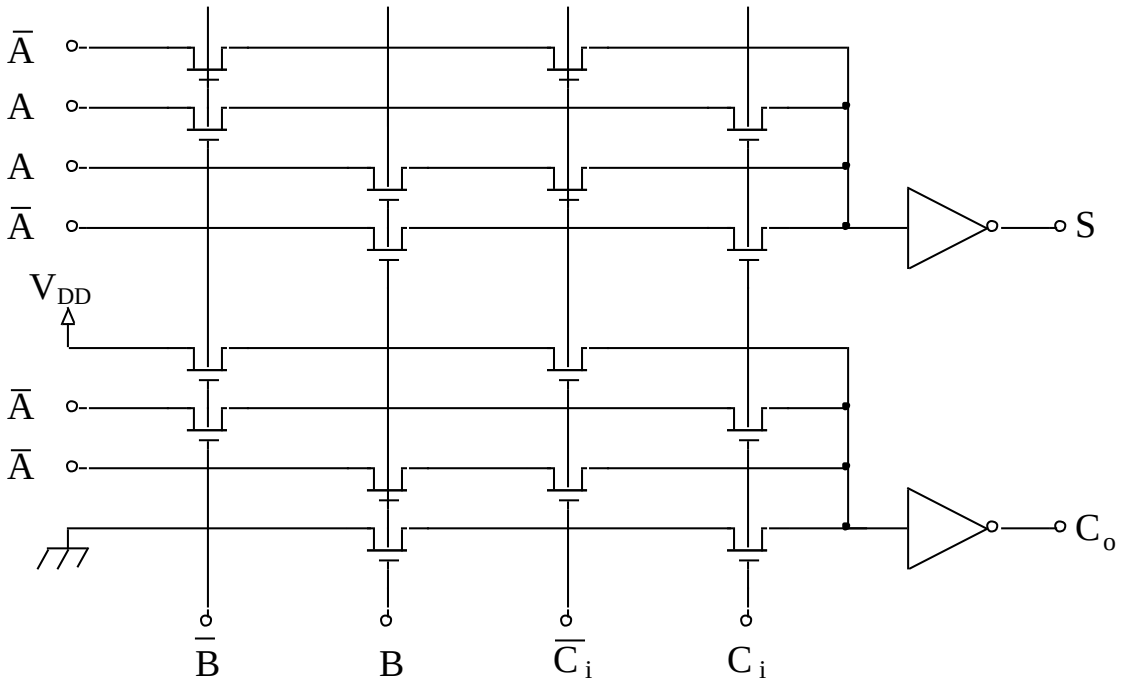



**è un circuito rigenerativo: es. trasferimento di un 1**

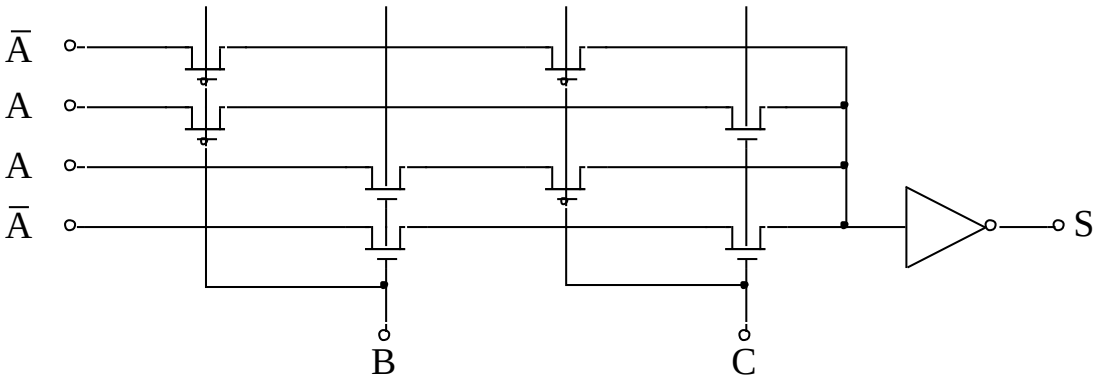


# Full Adder con Pass-Transistor

| Input | | Control | | |
|---|---|---|---|---|
| **A** | **B** | **$C_i$** | **$\overline{S}$** | **$\overline{C_o}$** |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |




con pass-transistor NMOS e PMOS



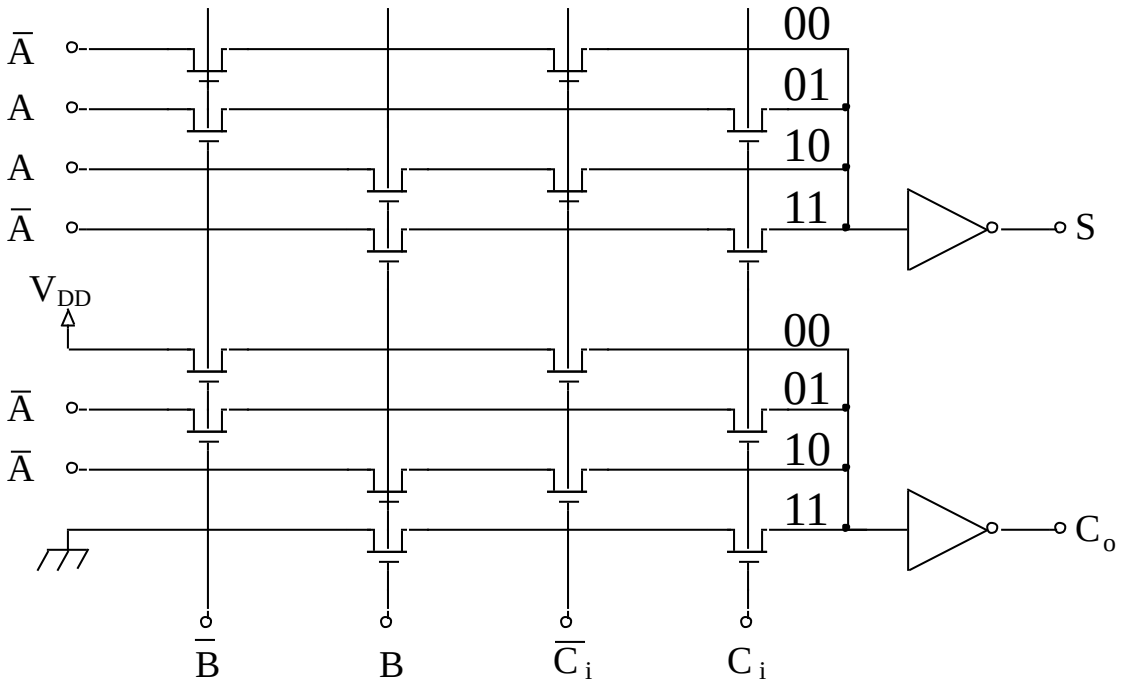
# Full Adder con Pass-Transistor

control input

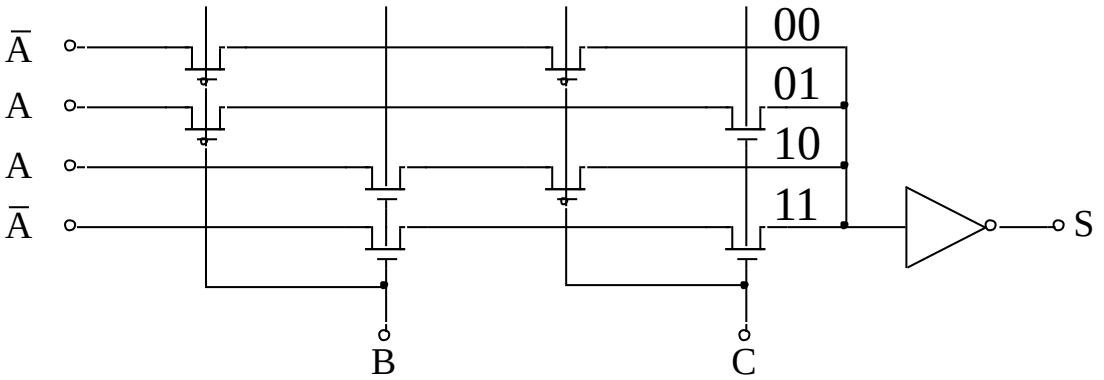
| B | Ci | A | S' | |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | A' |
| 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 0 | A |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | A |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 1 | A' |
| 1 | 1 | 1 | 0 | |

control input

| B | Ci | A | Co' | |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 1 | A' |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | A' |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | |



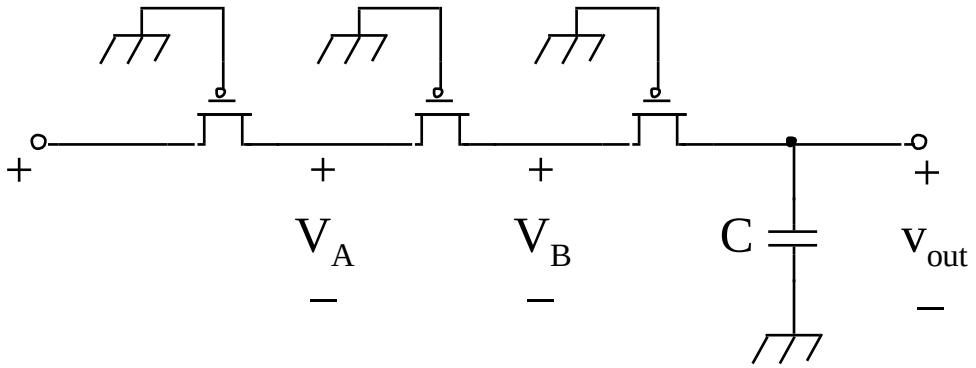

con pass-transistor NMOS e PMOS



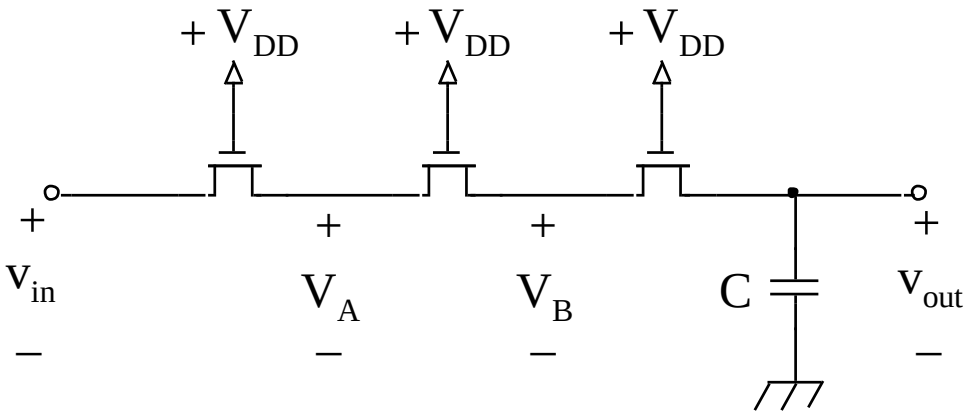
# Catene pMOS e nMOS



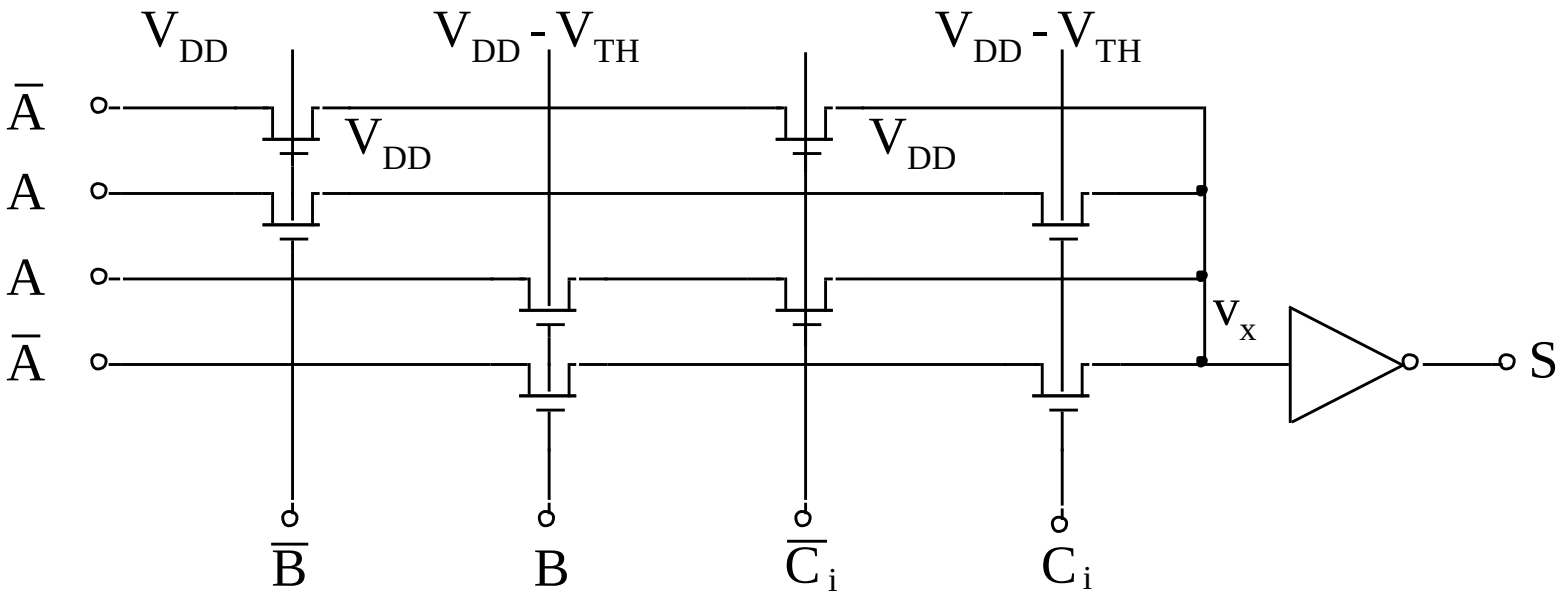
## catene di pMOS:
## 1 trasferito senza perdite, 0 perde una Vth




## catene di nMOS:
## 0 trasferito senza perdite, 1 perde una Vth

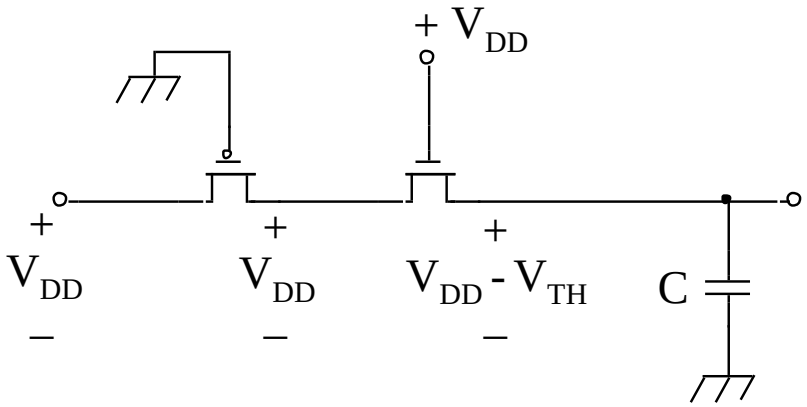


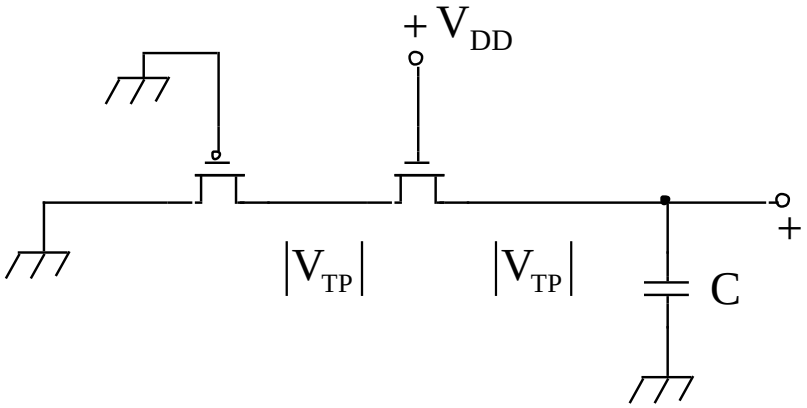
# Esempio

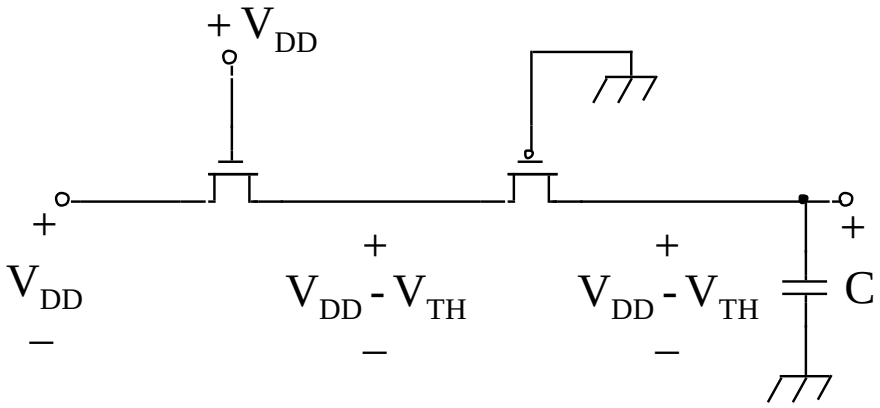

$V_{DD}$
$V_{DD} - V_{TH}$
$V_{DD} - V_{TH}$
$\overline{A}$
A
A
$\overline{A}$
$V_{DD}$
$V_{DD}$
$V_x$
S
$\overline{B}$
B
$\overline{C}_i$
$C_i$

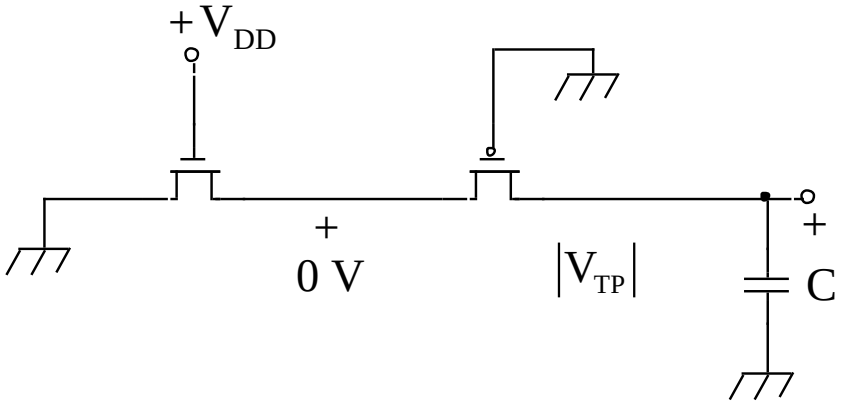
# Catene Miste pMOS e nMOS

## catene miste



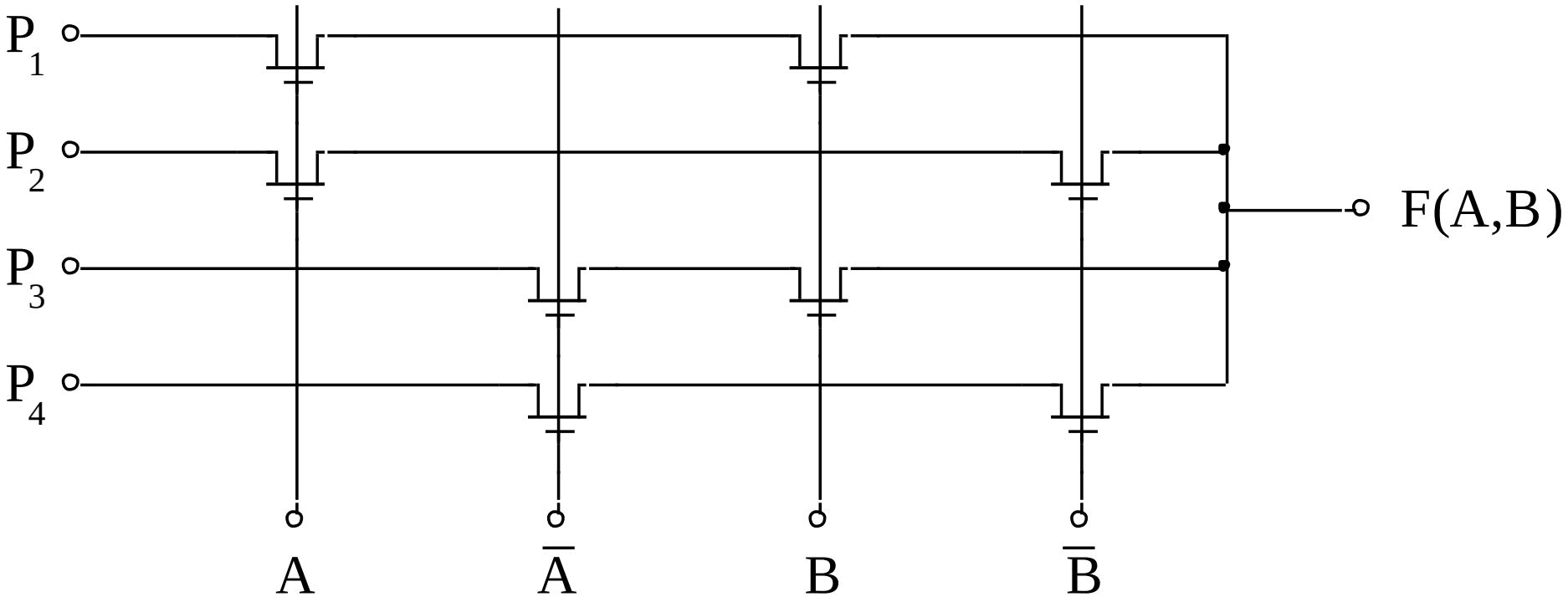



# Transistor Switch Array

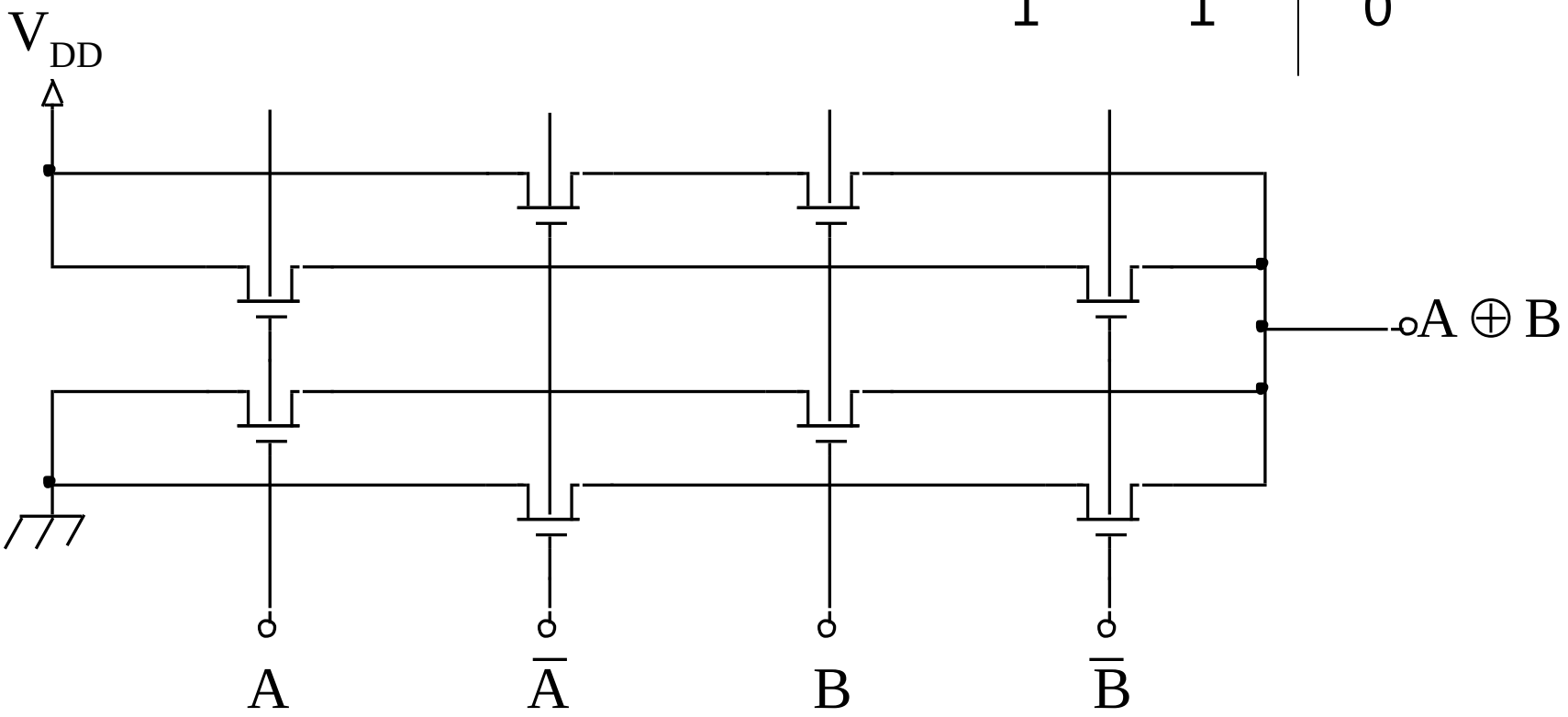




# Transistor Switch Array

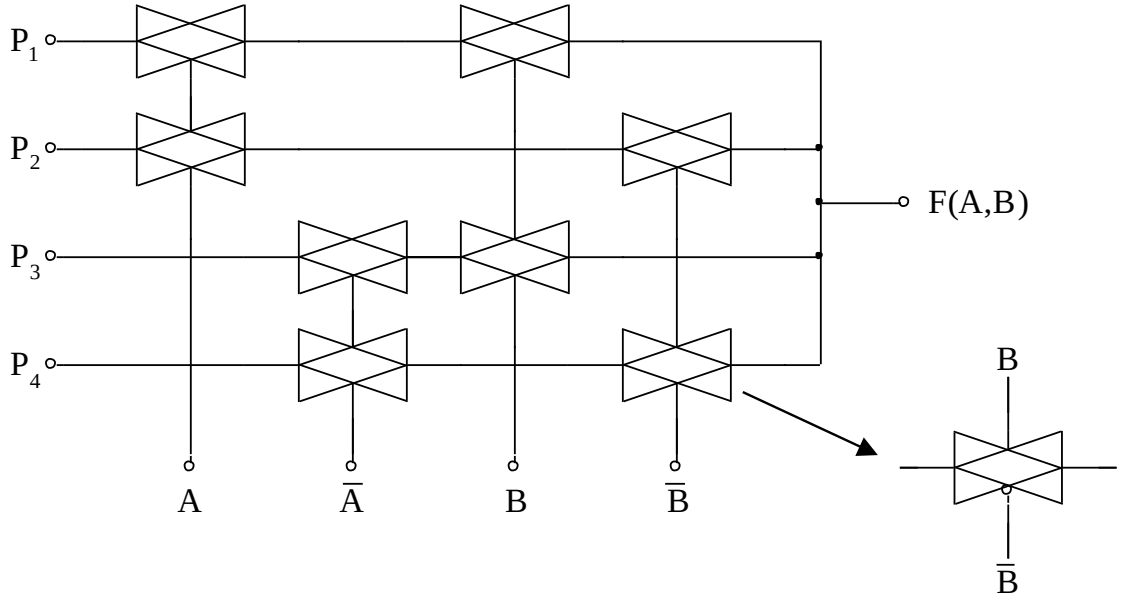
## Esempio: XOR o OR-esclusivo

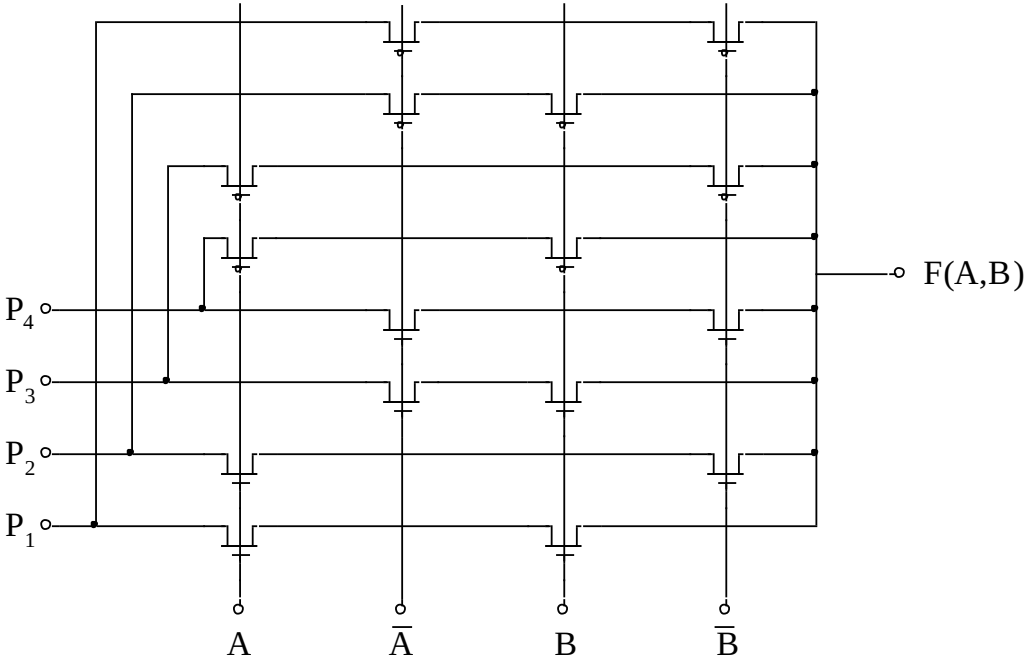
| A | B | Z = A ⊕ B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



# Realizzazione CMOS

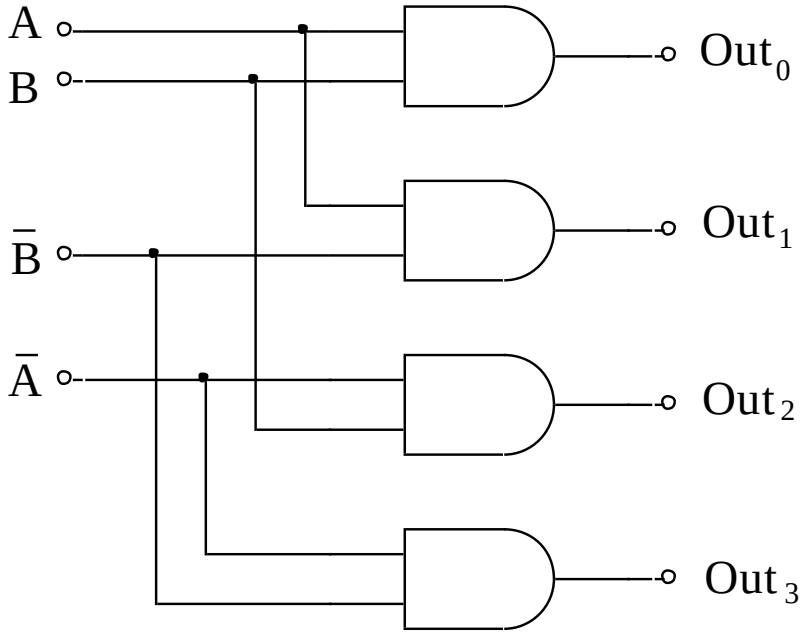




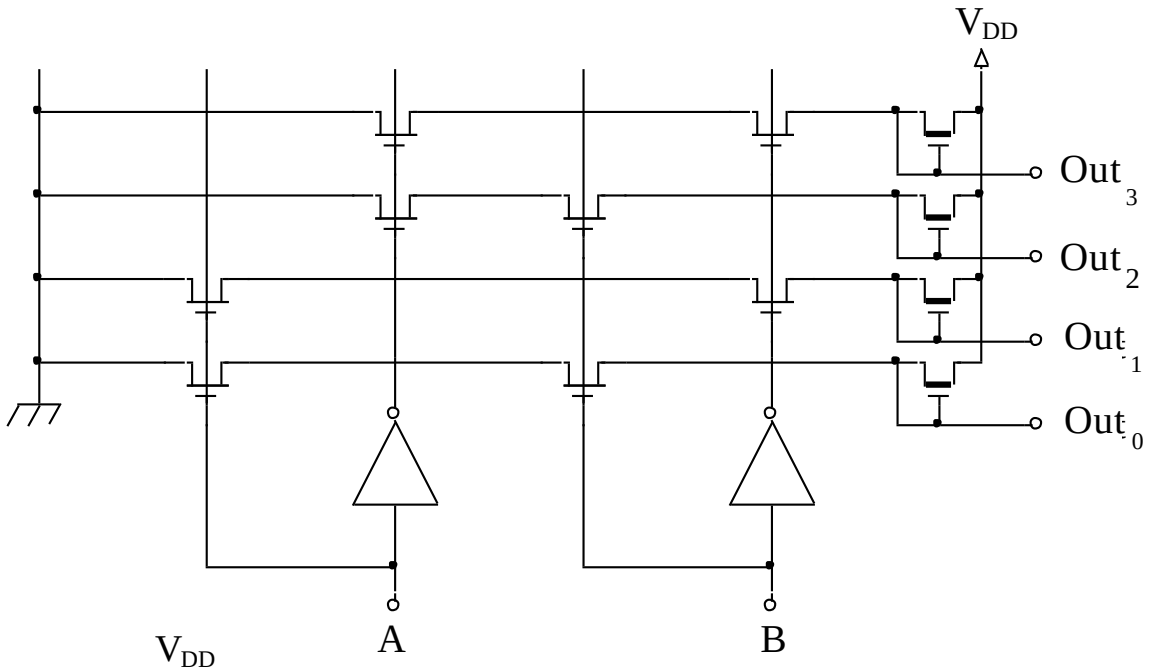
# Decoder

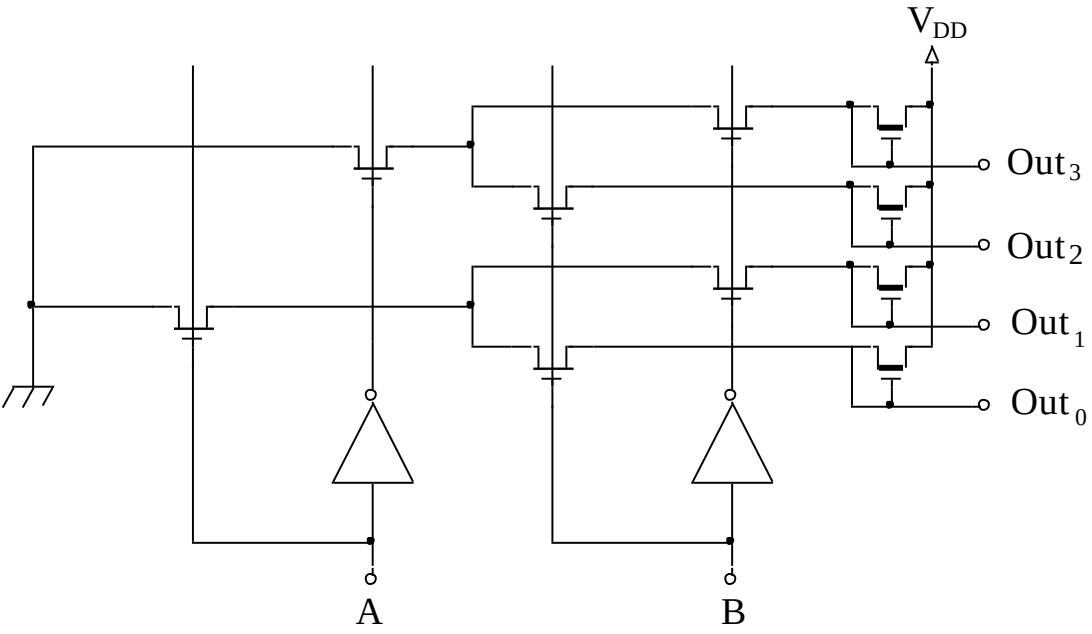
| **A** | **B** | |
|---|---|---|
| A | B | $Out_0$ |
| A | $\overline{B}$ | $Out_1$ |
| $\overline{A}$ | B | $Out_2$ |
| $\overline{A}$ | $\overline{B}$ | $Out_3$ |



# Decoder a NAND

## Realizzazione con NAND




## struttura ad albero

# Decoder a NOR

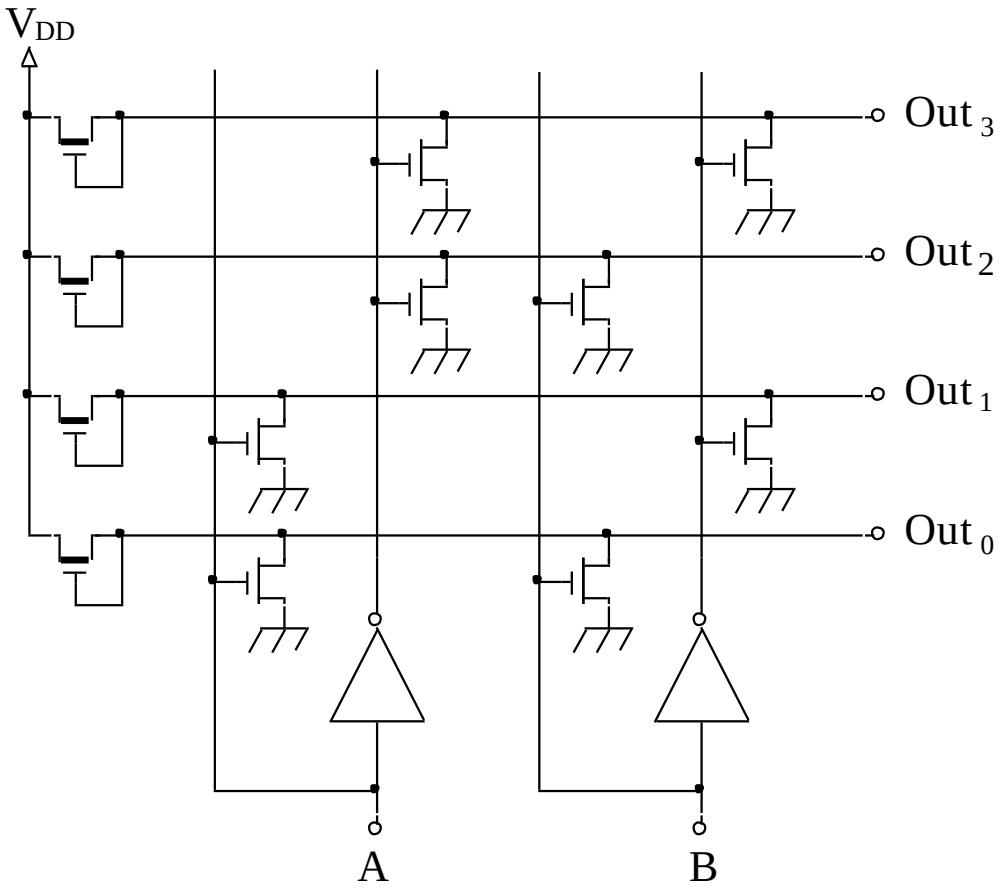
## Realizzazione con NOR

$$A + B \rightarrow Out_0$$

$$A + \overline{B} \rightarrow Out_1$$

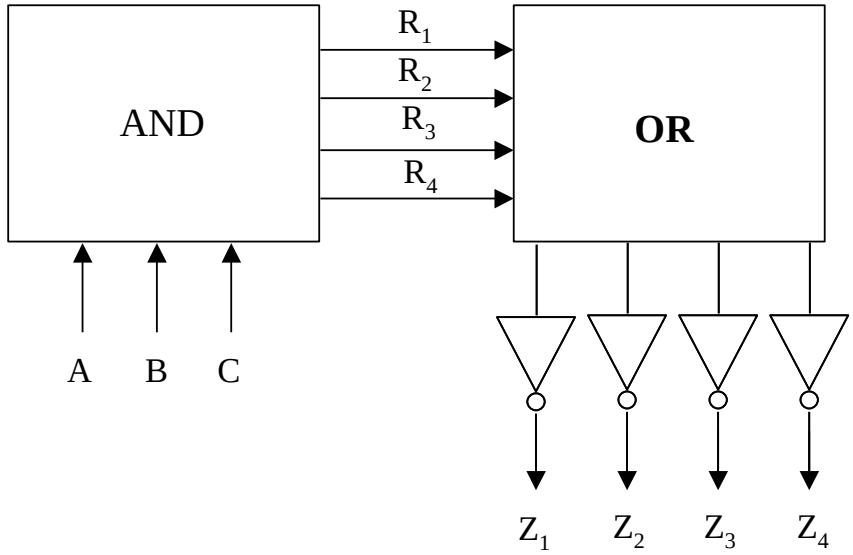
$$\overline{A} + B \rightarrow Out_2$$

$$\overline{A} + \overline{B} \rightarrow Out_3$$



# PLA in Logica nMOS

$$\begin{cases} Z_1 = A \\ Z_2 = A + \overline{A} \cdot \overline{B} \cdot C \\ Z_3 = \overline{B} \cdot \overline{C} \\ Z_4 = \overline{A} \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot \overline{C} \end{cases}$$




$$\begin{cases} R_1 = A = \overline{\overline{A}} \\ R_2 = \overline{A} \cdot \overline{B} \cdot C = \overline{A + B + \overline{C}} \\ R_3 = \overline{B} \cdot \overline{C} = \overline{B + C} \\ R_4 = \overline{A} \cdot B \cdot \overline{C} = \overline{A + \overline{B} + C} \end{cases}$$

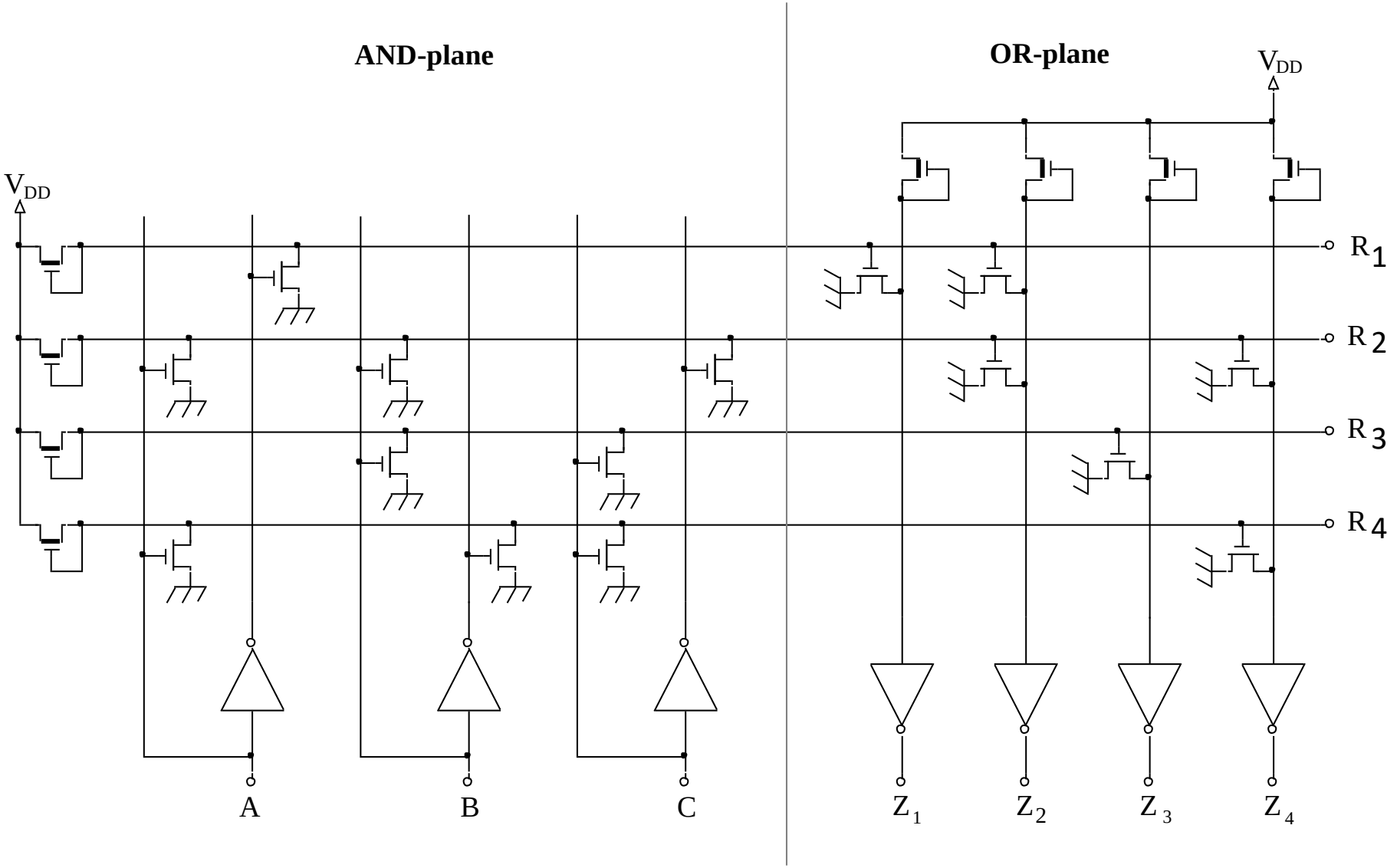
I singoli prodotti (minterm) possono essere realizzati con NOR.

$$\begin{cases} Z_1 = \overline{\overline{A}} = \overline{\overline{R_1}} \\ Z_2 = A + R_2 = \overline{\overline{R_1 + R_2}} \\ Z_3 = R_3 = \overline{\overline{R_3}} \\ Z_4 = R_2 + R_4 = \overline{\overline{R_2 + R_4}} \end{cases}$$

Le funzioni negate possono considerarsi come NOR dei prodotti.

# PLA in Logica nMOS





# Full Adder con PLA



$$\begin{cases} S = \bar{x} \cdot \bar{y} \cdot C_i + \bar{x} \cdot y \cdot \overline{C_i} + x \cdot \bar{y} \cdot \overline{C_i} + x \cdot y \cdot C_i \\ C_o = x \cdot C_i + x \cdot y + y \cdot \overline{C_i} \end{cases}$$

$$R_1 = \bar{x} \cdot \bar{y} \cdot C_i = \overline{x + y + \overline{C_i}}$$

$$R_2 = \bar{x} \cdot y \cdot \overline{C_i} = \overline{x + \bar{y} + C_i}$$

$$R_3 = x \cdot \bar{y} \cdot \overline{C_i} = \overline{\bar{x} + y + C_i}$$

$$S = R_1 + R_2 + R_3 + R_4$$

$$R_4 = x \cdot y \cdot C_i = \overline{\bar{x} + \bar{y} + \overline{C_i}}$$

$$R_5 = x \cdot C_i = \overline{\bar{x} + \overline{C_i}}$$

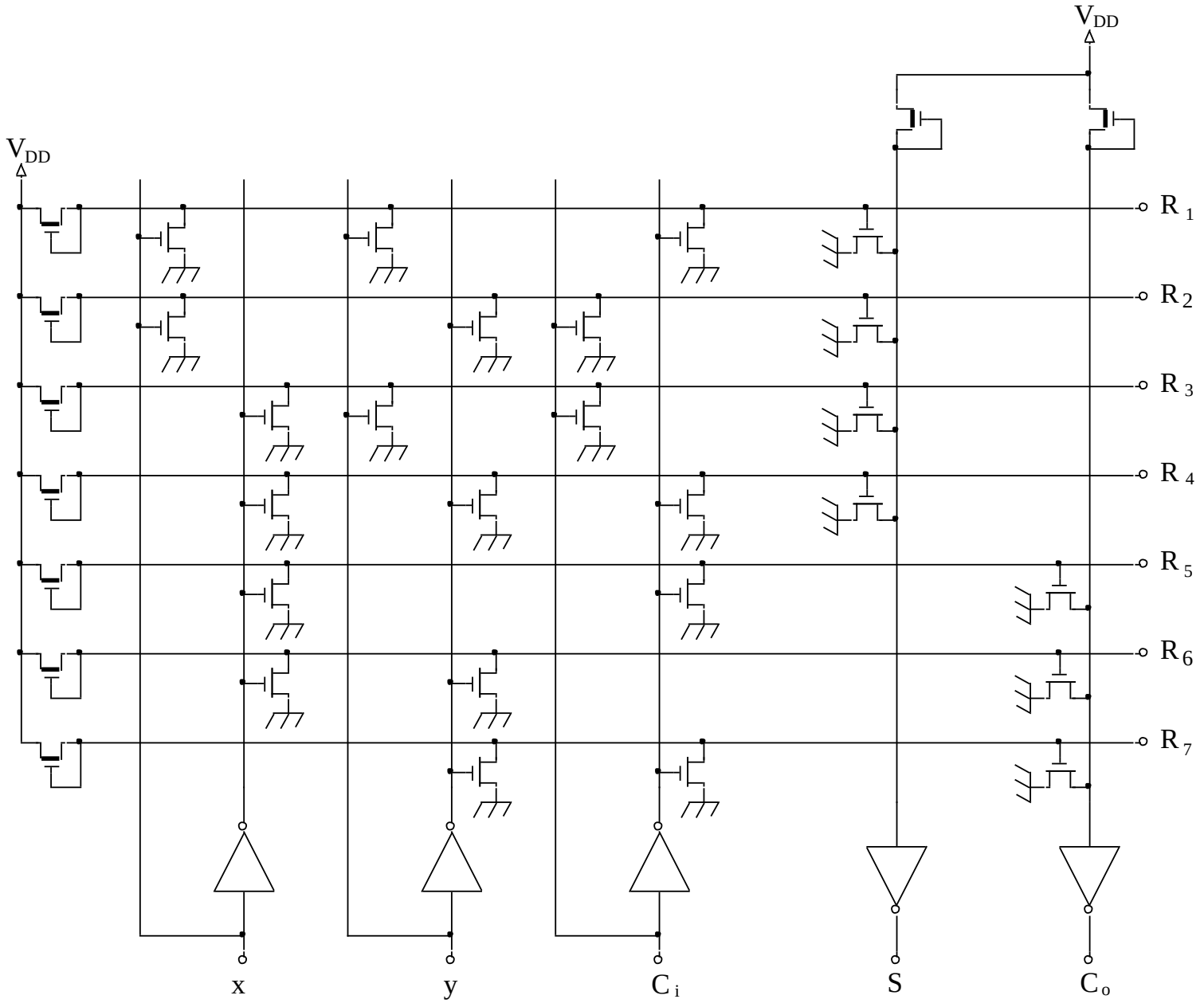
$$R_6 = x \cdot y = \overline{\bar{x} + \bar{y}}$$

$$C_o = R_5 + R_6 + R_7$$

$$R_7 = y \cdot C_i = \overline{\bar{y} + \overline{C_i}}$$

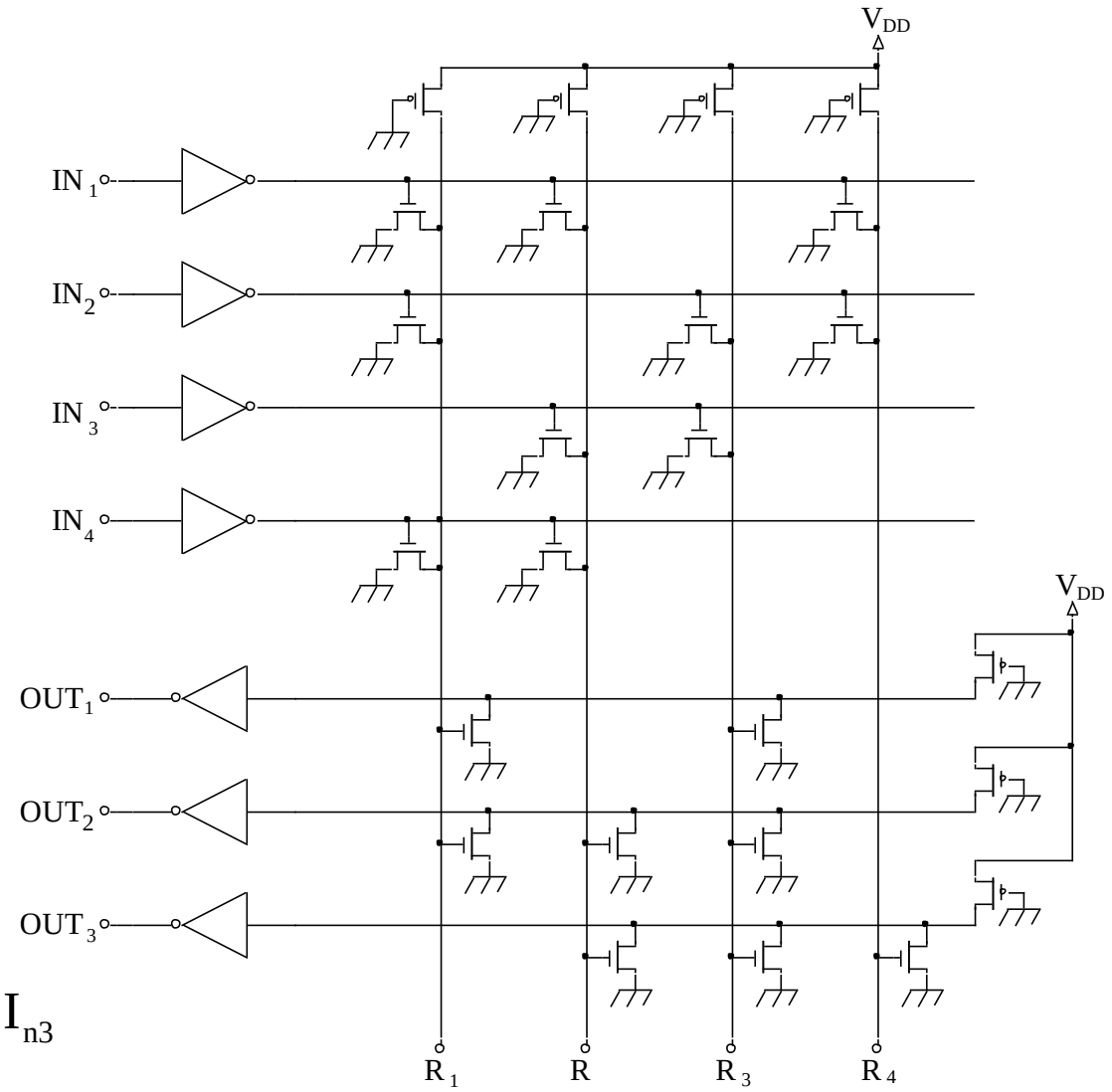
# Full Adder con PLA





# PLA in Logica Pseudo nMOS






$$R_1 = \overline{\overline{I_{n1}} + \overline{I_{n2}} + \overline{I_{n4}}} = I_{n1} \cdot I_{n2} \cdot I_{n4}$$

$$R_2 = \overline{\overline{I_{n1}} + \overline{I_{n3}} + \overline{I_{n4}}} = I_{n1} \cdot I_{n3} \cdot I_{n4}$$

$$R_3 = \overline{\overline{I_{n2}} + \overline{I_{n3}}} = I_{n2} \cdot I_{n3}$$

$$R_4 = \overline{\overline{I_{n1}} + \overline{I_{n2}}} = I_{n2} \cdot I_{n3}$$

$$OUT_1 = R_1 + R_3 = I_{n1} \cdot I_{n2} \cdot I_{n4} + I_{n2} \cdot I_{n3}$$

$$OUT_2 = R_1 + R_2 + R_3 = I_{n1} \cdot I_{n2} \cdot I_{n4} + I_{n1} \cdot I_{n3} \cdot I_{n4} + I_{n2} \cdot I_{n3}$$

$$OUT_3 = R_2 + R_3 + R_4 = I_{n1} \cdot I_{n3} \cdot I_{n4} + I_{n2} \cdot I_{n3} + I_{n1} \cdot I_{n2}$$