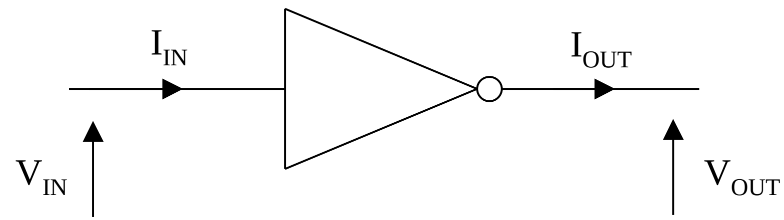
A.A. 2021-2022

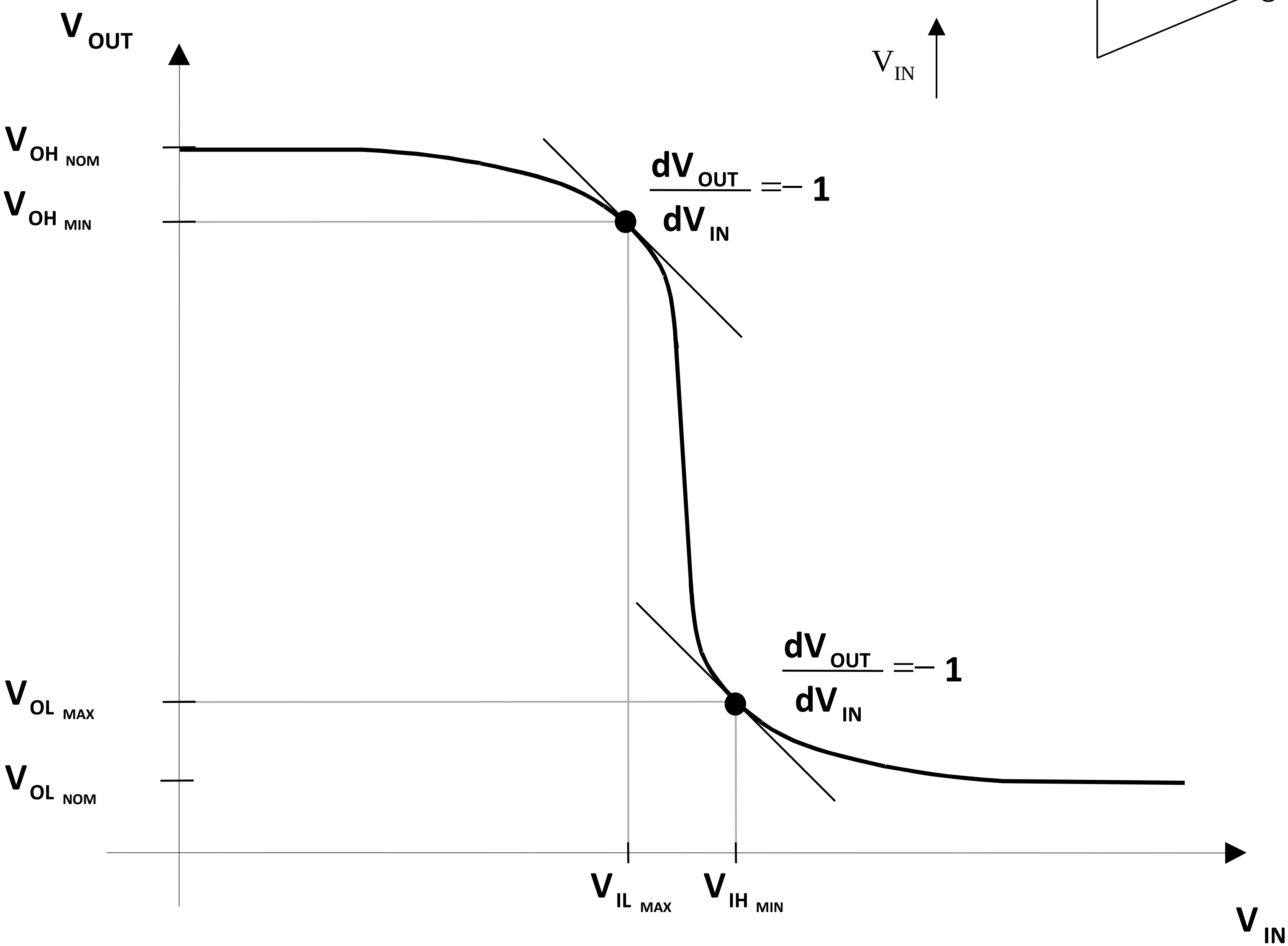
Elementi di Elettronica (INF)

Prof. Paolo Crippa

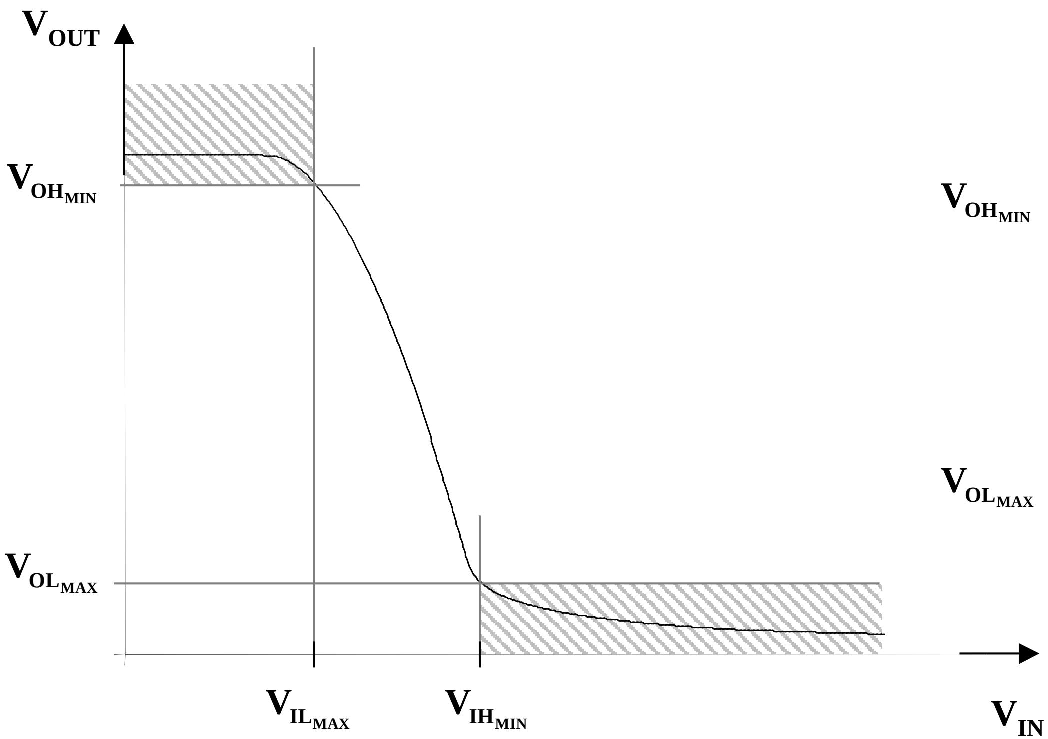
Inverter

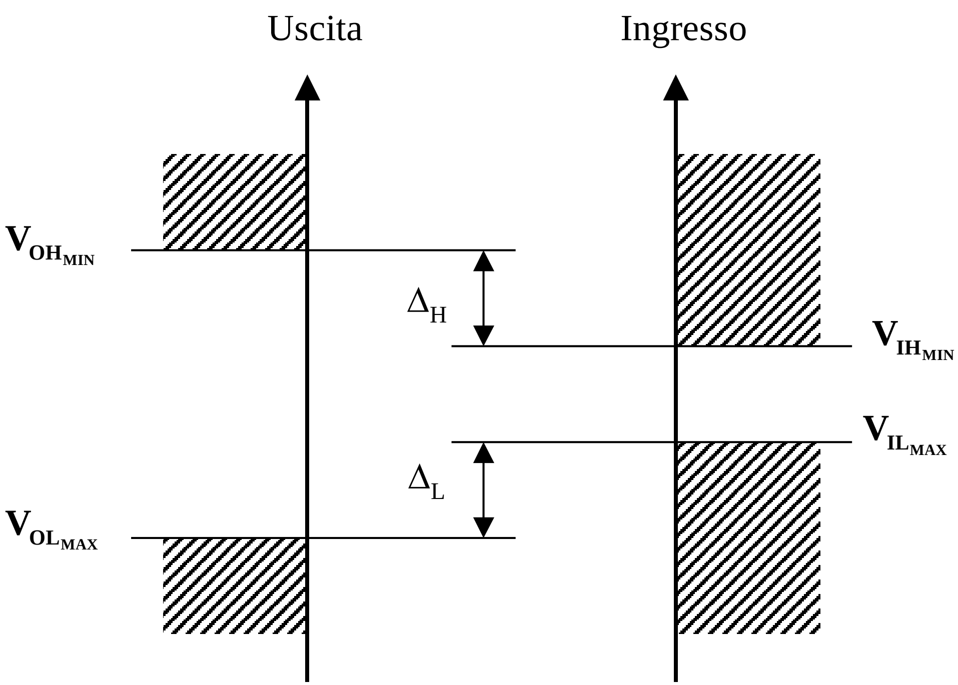
Caratteristiche dell'Inverter





Margini di Immunità ai Disturbi





In condizioni statiche la porta deve lavorare in una delle regioni con

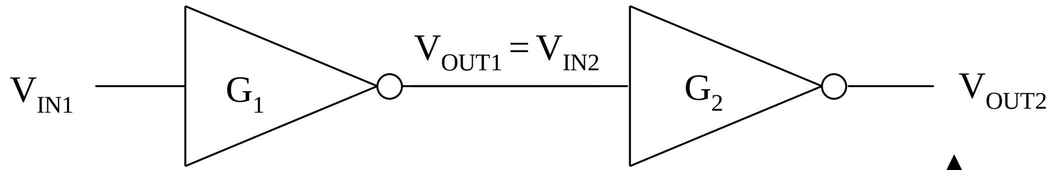
$$|A_v| < 1$$

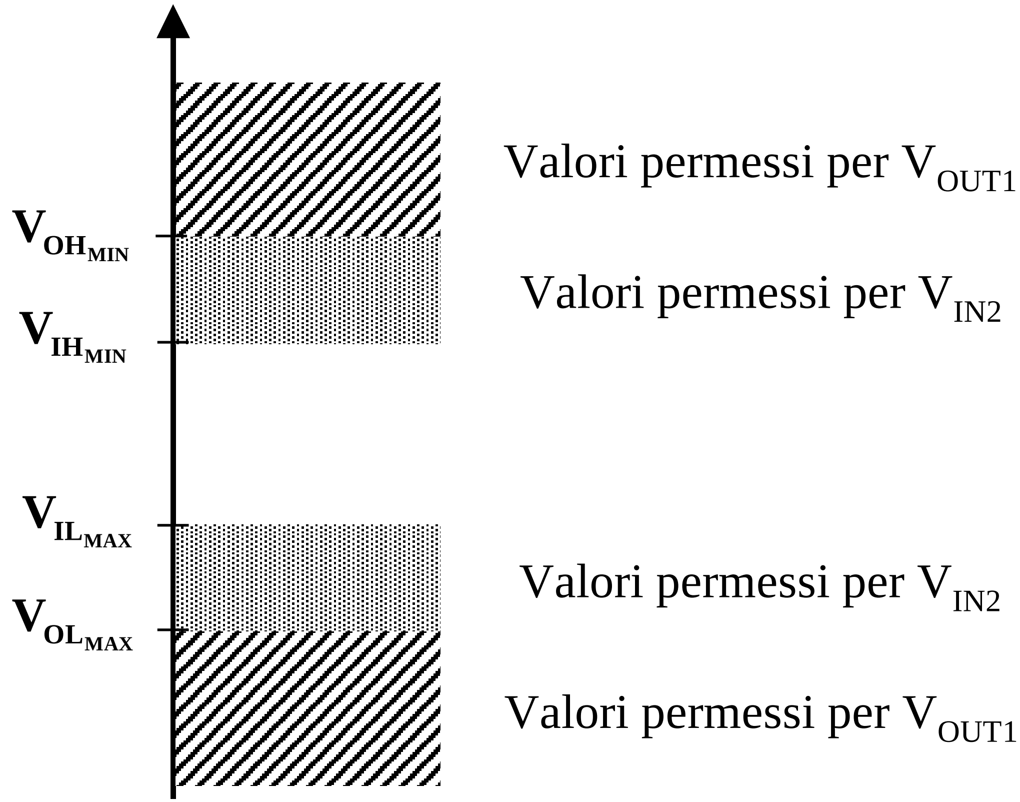
deve essere:

$$V_{IL_{MAX}} > V_{OL_{MAX}}$$

$$V_{OH_{MIN}} > V_{IH_{MIN}}$$

Margini di Immunità ai Disturbi





$$\Delta_H = V_{OH_{MIN}} - V_{IH_{MIN}}$$

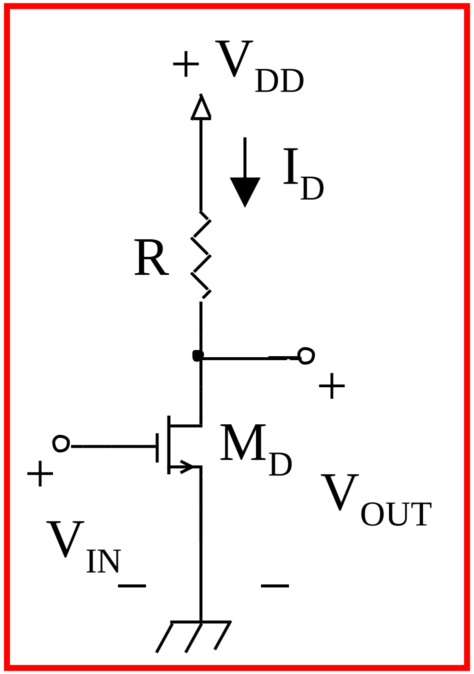
$$\Delta_L = V_{IL_{MAX}} - V_{OL_{MAX}}$$

$\Delta_H =$ margine di immunità ai disturbi sui valori alti

$\Delta_L =$ margine di immunità ai disturbi sui valori bassi

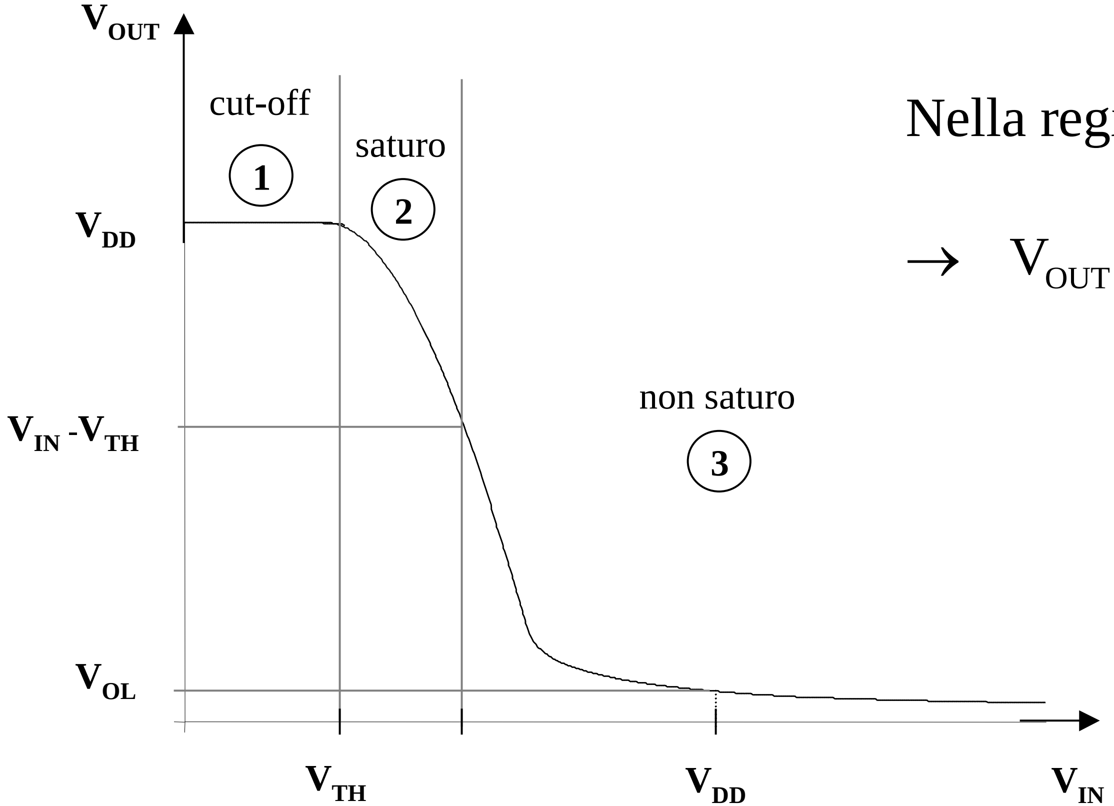
margine di immunità della porta $= \min\left(\Delta_H,\ \Delta_L\right)$ (caso peggiore)

Inverter NMOS con Carico Resistivo



$$
I_D = \frac{V_{DD} - V_{OUT}}{R} = \begin{cases} I_{sub} \;, \quad \text{per } V_{IN} \leq V_{TH} & \textbf{Cut - off} \quad (1) \\ \frac{\beta}{2} \cdot \left(V_{IN} - V_{TH}\right)^2 \;\; \text{per } V_{IN} \geq V_{TH} \;, \; \text{per } V_{OUT} \geq V_{IN} - V_{TH} & \textbf{Saturazione} \quad (2) \\ \beta \cdot \left[\left(V_{IN} - V_{TH}\right) \cdot V_{OUT} - \frac{V_{OUT}{}^2}{2}\right] \;\; \text{per } V_{IN} \geq V_{TH} \;, \; \text{per } V_{OUT} \leq V_{IN} - V_{TH} & \textbf{Triodo} \quad (3) \end{cases}
$$

Inverter NMOS con Carico Resistivo



Nella regione (1) $\dfrac{V_{DD}-V_{OUT}}{R} \cong 0$

$\rightarrow \quad V_{OUT} = V_{DD} = V_{OH}$

Nella regione (3) con $V_{IN} = V_{DD}$

$$\frac{V_{DD}-V_{OL}}{R} = \beta \cdot \left[\left(V_{DD}-V_{TH}\right) \cdot V_{OL} - \frac{1}{2} \cdot V_{OL}{}^{2} \right]$$

$$V_{OL} \cong \frac{V_{DD}}{1+\beta \cdot R \cdot \left(V_{DD}-V_{TH}\right)} \quad \rightarrow \quad 0\,V$$

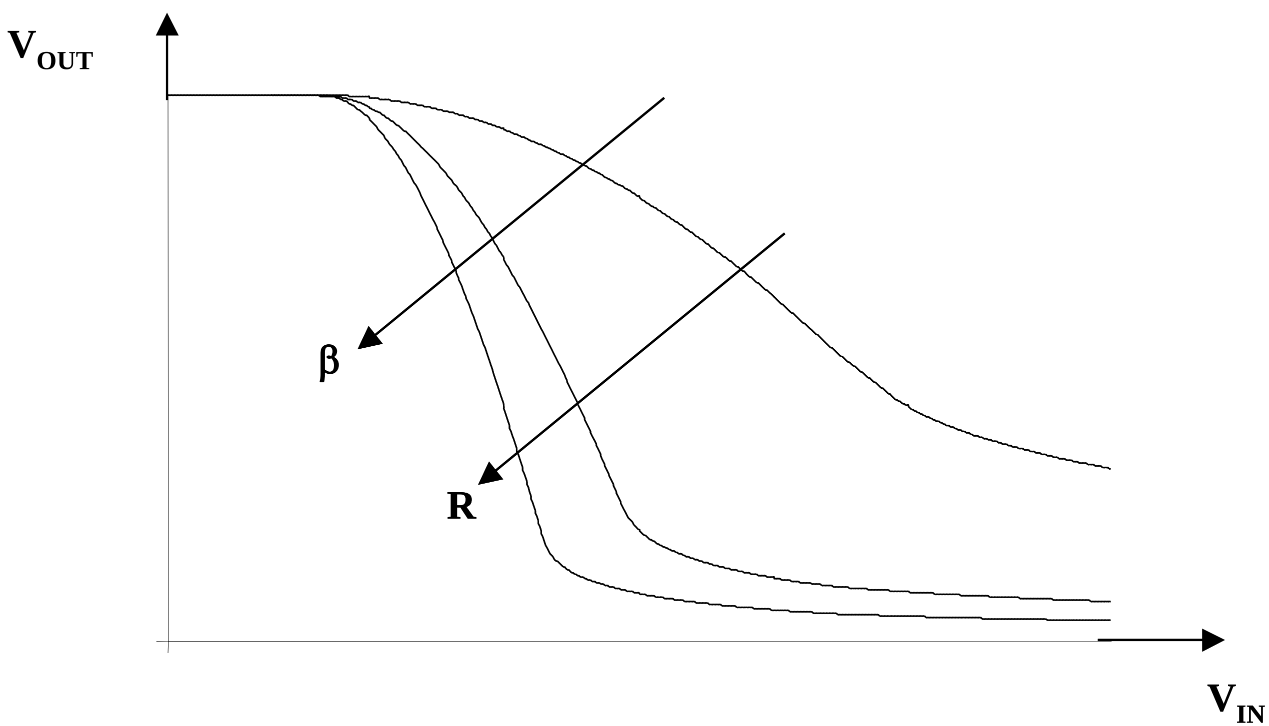
Inverter NMOS con Carico Resistivo

La pendenza nella regione (2) è

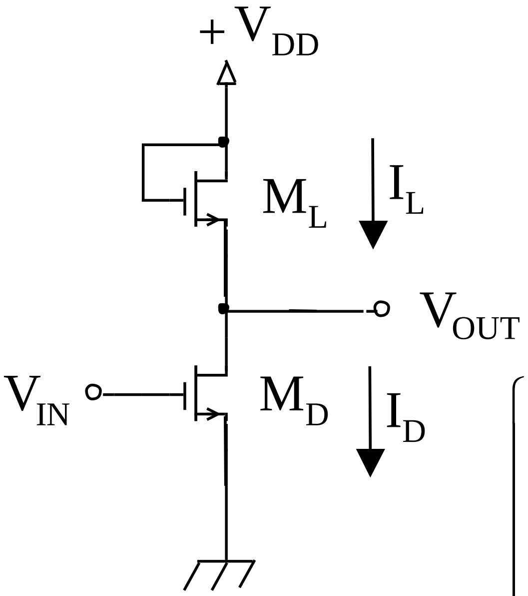
$$\frac{dV_{OUT}}{dV_{IN}} = A_v \quad \rightarrow \quad -\frac{1}{R}\cdot\frac{dV_{OUT}}{dV_{IN}} = \beta\cdot\left(V_{IN} - V_{TH}\right)$$

$$A_v = \frac{dV_{OUT}}{dV_{IN}} = -\beta\cdot\left(V_{IN} - V_{TH}\right)\cdot R$$

A_v aumenta in modulo all'aumentare di R e β.



Inverter NMOS con Carico Attivo



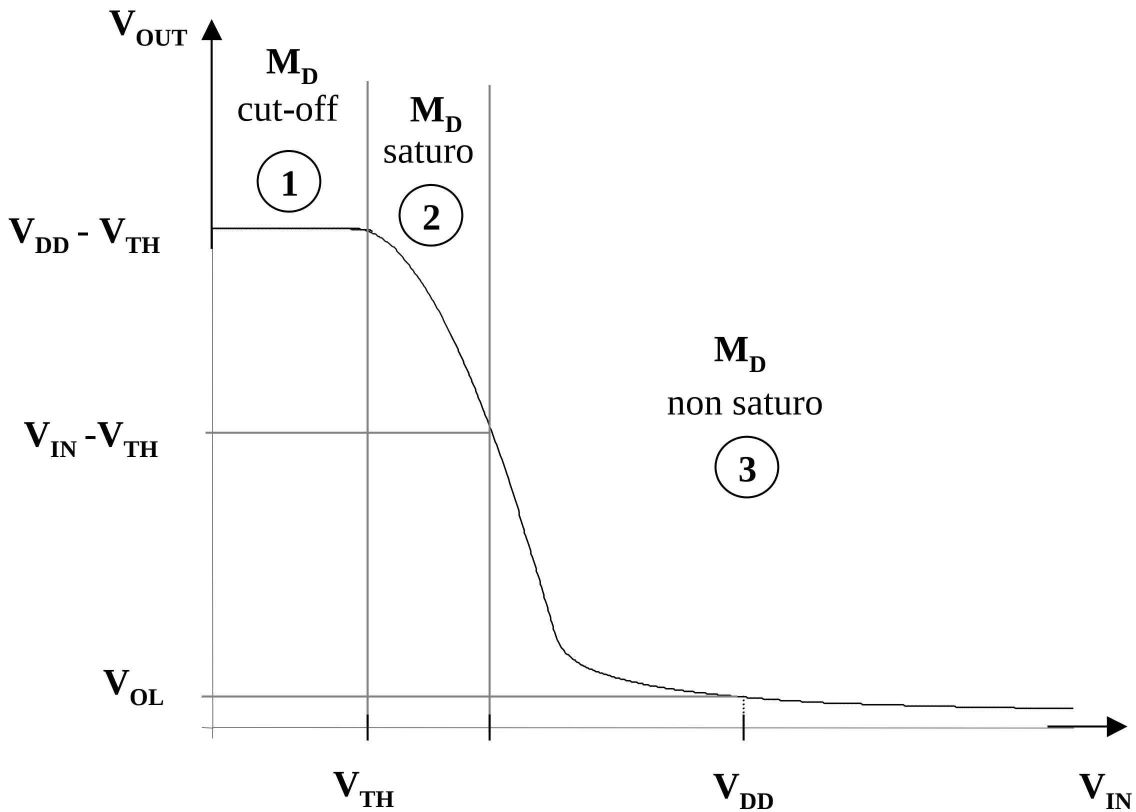
$$I_D = I_L$$

$$I_L = \frac{\beta_L}{2}\cdot\left(V_{GS} - V_{TH}\right)^2 = \frac{\beta_L}{2}\cdot\left(V_{DD} - V_{OUT} - V_{TH}\right)^2$$

$$I_D = \begin{cases} I_{sub}\ , & \text{per } V_{IN} \le V_{TH} \quad \textbf{Cut - off} \quad (1) \\ \frac{\beta_D}{2}\cdot\left(V_{IN} - V_{TH}\right)^2 & \text{per } V_{IN} \ge V_{TH}\ ,\ \textbf{Saturazione} \quad (2) \\ & \text{per } V_{OUT} \ge V_{IN} - V_{TH} \\ \beta_D \cdot\left[\left(V_{IN} - V_{TH}\right)\cdot V_{OUT} - \frac{V_{OUT}{}^2}{2}\right] & \text{per } V_{IN} \ge V_{TH}\ ,\ \textbf{Triodo} \quad (3) \\ & \text{per } V_{OUT} \le V_{IN} - V_{TH} \end{cases}$$

M_L è sempre in saturazione

Inverter NMOS con Carico Attivo

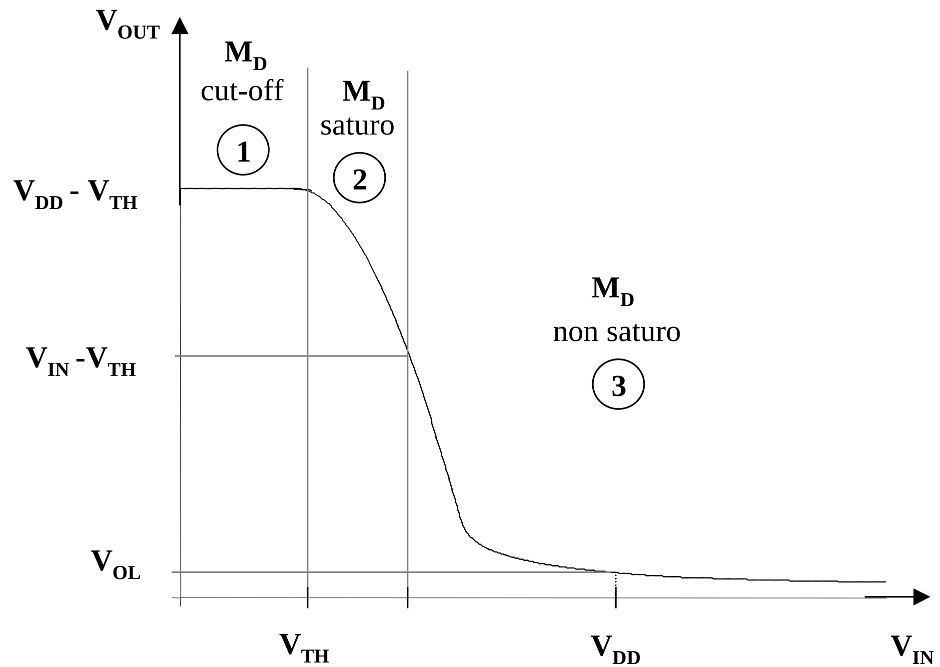


Nella regione (1) $\quad V_{IN} \leq V_{TH}\ ,\ I_D = I_{sub} \cong 0$

$$\text{ma } I_D = I_L = \frac{\beta_L}{2}\cdot\left(V_{GS} - V_{TH}\right)^2 = 0 \quad \Rightarrow \quad \left(V_{GS}\right)_L = V_{TH}$$

$$\left(V_{GS}\right)_L = V_{DD} - V_{OUT} = V_{TH} \;\rightarrow\; \mathbf{V_{OUT}} = \mathbf{V_{OH}} = V_{DD} - V_{TH} \quad \text{(max valore di } V_{OUT}\text{)}$$

Inverter NMOS con Carico Attivo



Nella regione (3)

$$\frac{\beta_L}{2}\cdot\left[\left(V_{DD}-\cancel{V_{OL}}\right)-V_{TH}\right]^2=\beta_D\cdot\left[\left(V_{DD}-V_{TH}\right)\cdot V_{OL}-\cancel{\frac{V_{OL}^2}{2}}\right]$$

$$\frac{\beta_L}{2}\cdot\left(V_{DD}-V_{TH}\right)^2\cong\beta_D\cdot\left(V_{DD}-V_{TH}\right)\cdot V_{OL}$$

$$\mathbf{V_{OL}}\cong\frac{\beta_L}{2\cdot\beta_D}\cdot V_{OH}$$ deve essere $$\frac{\beta_L}{\beta_D}\ll 1$$

Inverter NMOS con Carico Attivo

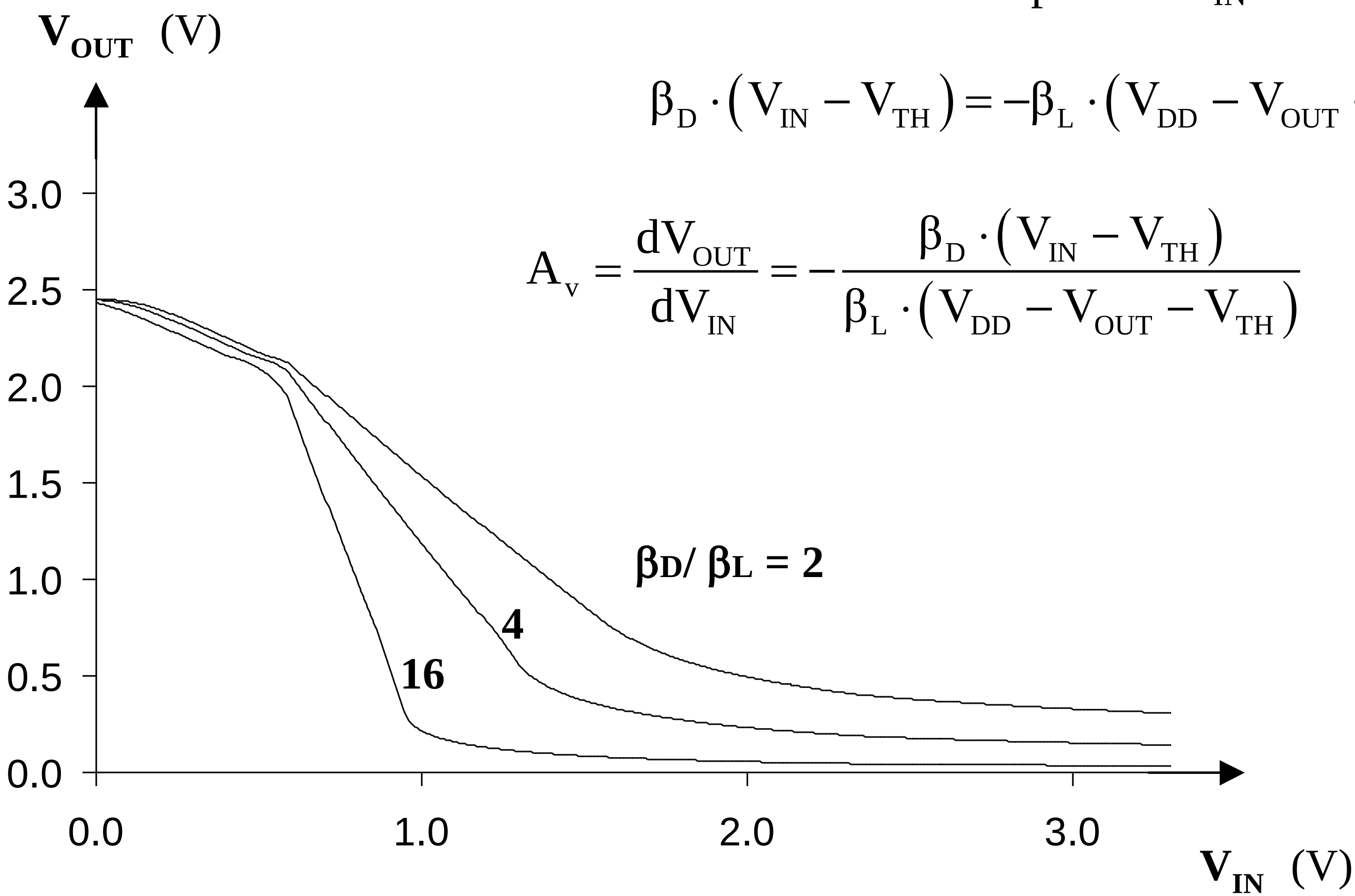
Nella regione (2)

$$\frac{\beta_D}{2}\cdot\left(V_{IN}-V_{TH}\right)^2=\frac{\beta_L}{2}\cdot\left(V_{DD}-V_{OUT}-V_{TH}\right)^2$$

Calcoliamo la derivata rispetto a V_{IN}

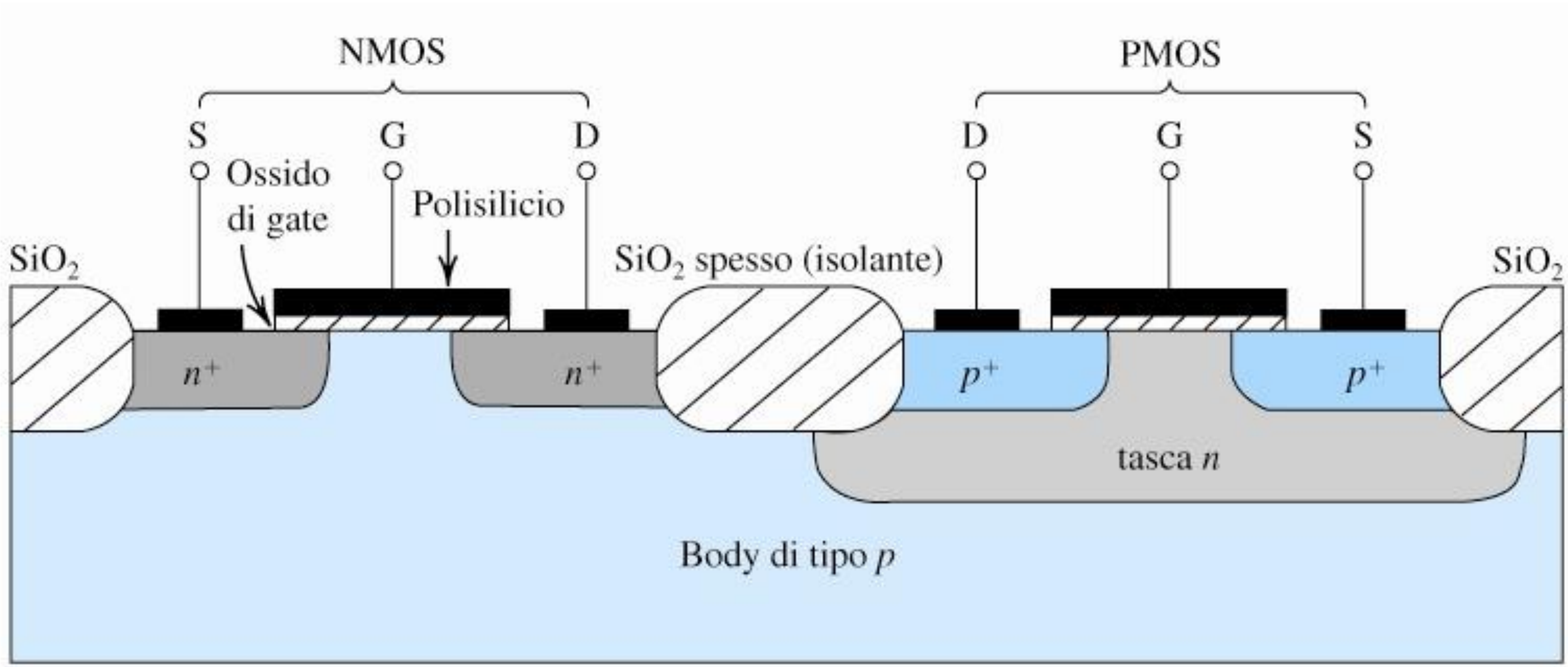
$$\beta_D\cdot\left(V_{IN}-V_{TH}\right)=-\beta_L\cdot\left(V_{DD}-V_{OUT}-V_{TH}\right)\cdot\frac{dV_{OUT}}{dV_{IN}}$$

$$A_v=\frac{dV_{OUT}}{dV_{IN}}=-\frac{\beta_D\cdot\left(V_{IN}-V_{TH}\right)}{\beta_L\cdot\left(V_{DD}-V_{OUT}-V_{TH}\right)}$$

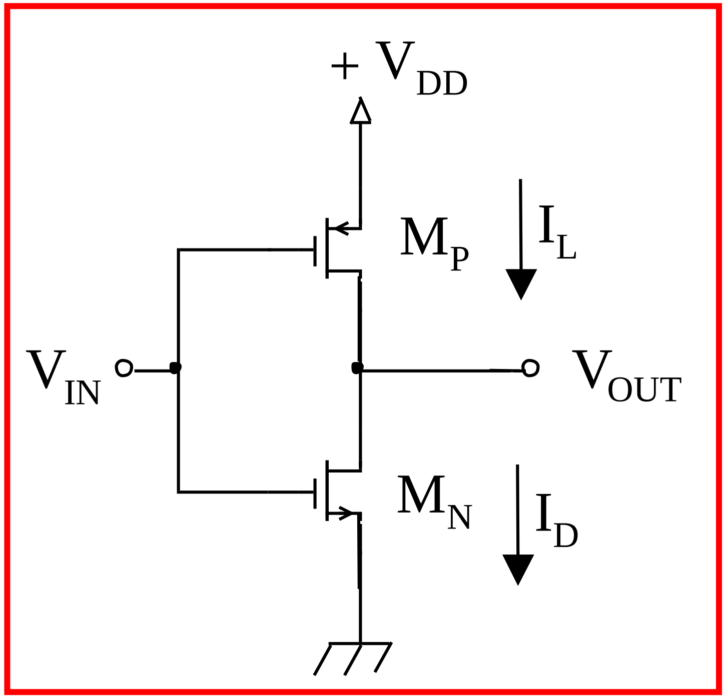


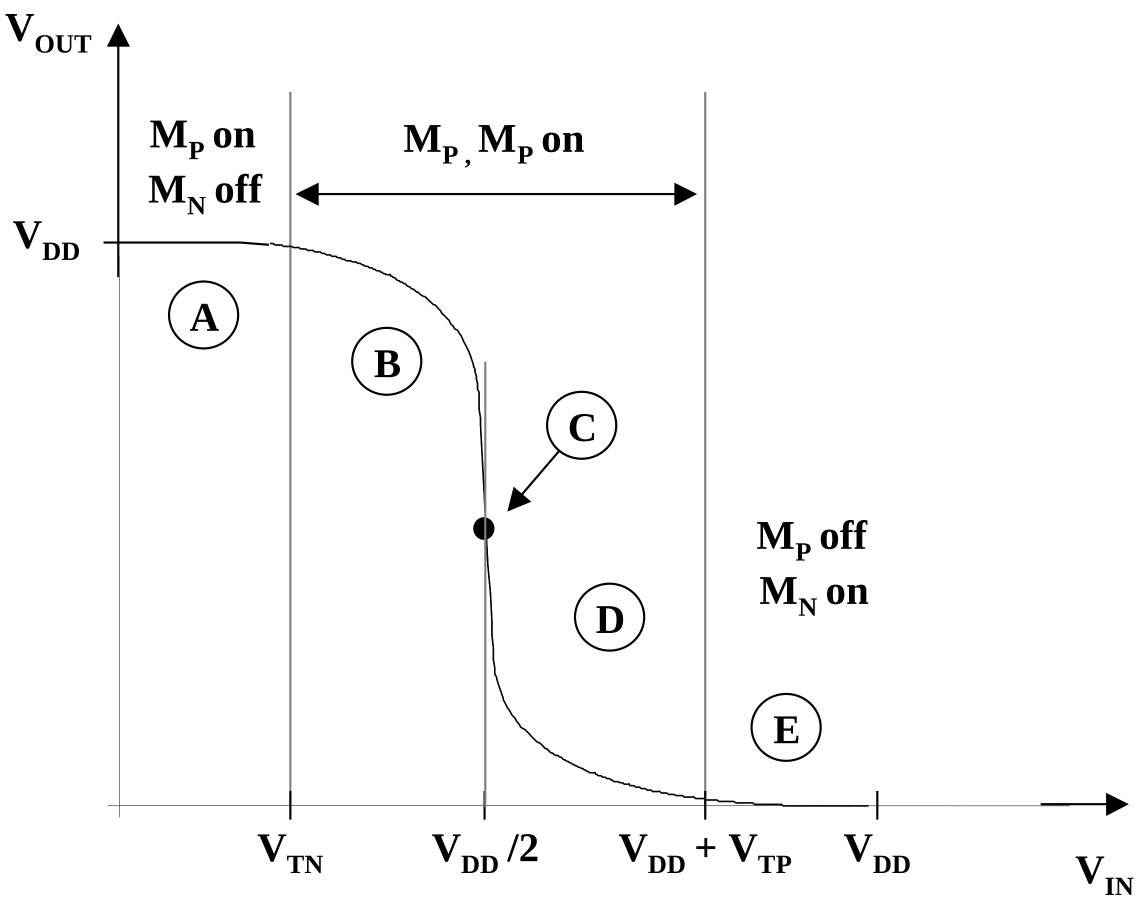
Tecnologia CMOS

Realizzazione in tecnologia planare CMOS di un nMOSFET e di un pMOSFET

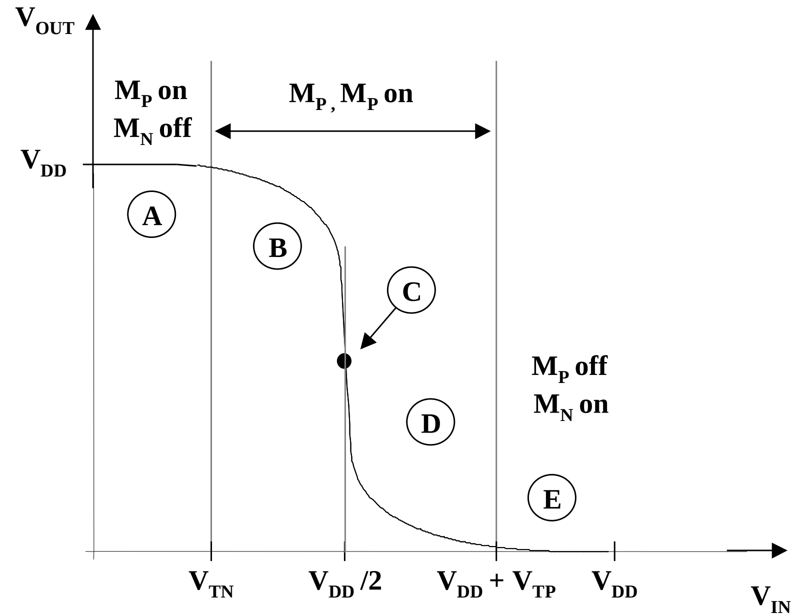


Inverter CMOS





Inverter CMOS



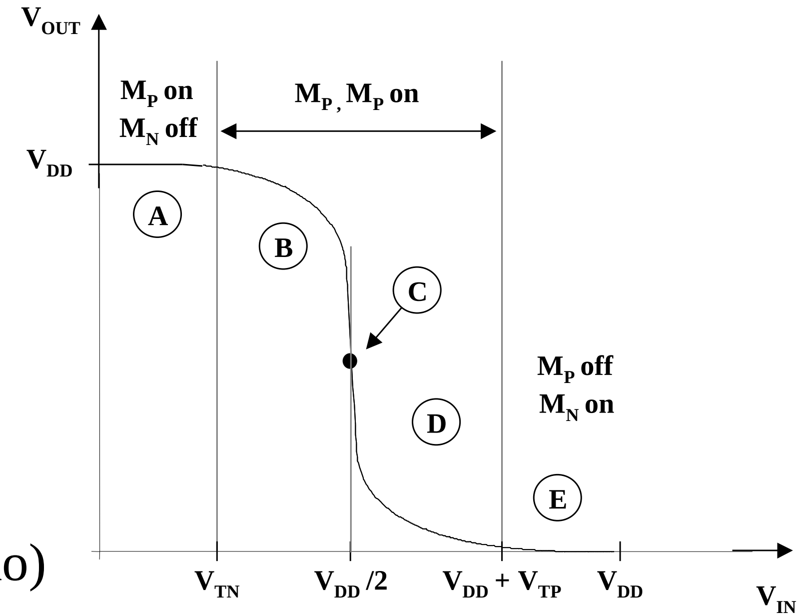
A) $0 \le V_{IN} \le V_{TN}$

$$\Rightarrow M_N = \text{OFF} \Rightarrow I_N = 0 \Rightarrow I_P = 0$$

$$\beta_P \cdot \left[(V_{SG} + V_{TP}) \cdot (V_{DD} - V_{OUT}) - \frac{(V_{DD} - V_{OUT})^2}{2} \right] = 0$$

$$\Rightarrow \quad \mathbf{V_{OUT}} = V_{DD} = V_{OH}$$

Inverter CMOS



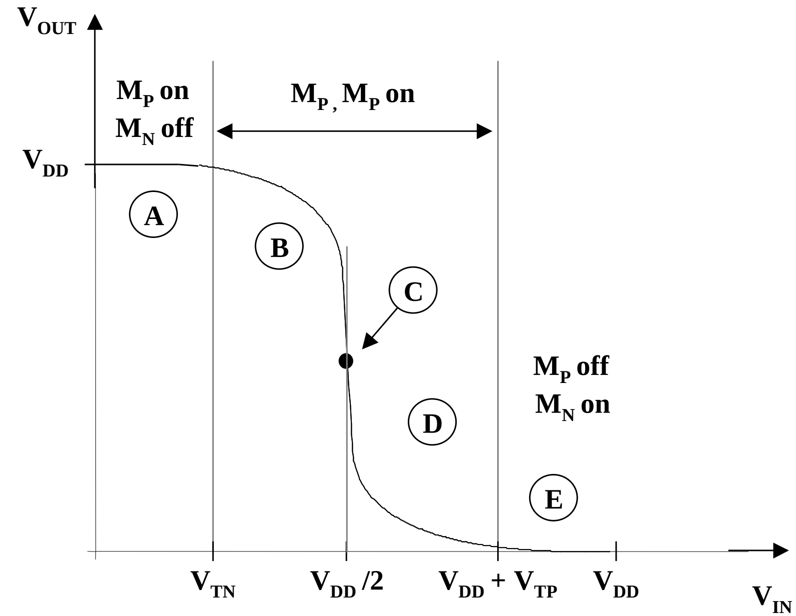
B) $V_{TN} < V_{IN} < V_{DD}/2$

M_N saturazione $\qquad$ M_P non saturazione (triodo)

$$\begin{cases} I_N = \beta_N \cdot \dfrac{\left(V_{IN} - V_{TN}\right)^2}{2} \\ \\ I_P = \beta_P \cdot \left[\left(V_{DD} - V_{IN} + V_{TP}\right) \cdot \left(V_{DD} - V_{OUT}\right) - \dfrac{\left(V_{DD} - V_{OUT}\right)^2}{2}\right] \end{cases}$$

$$I_N = I_P$$

Inverter CMOS



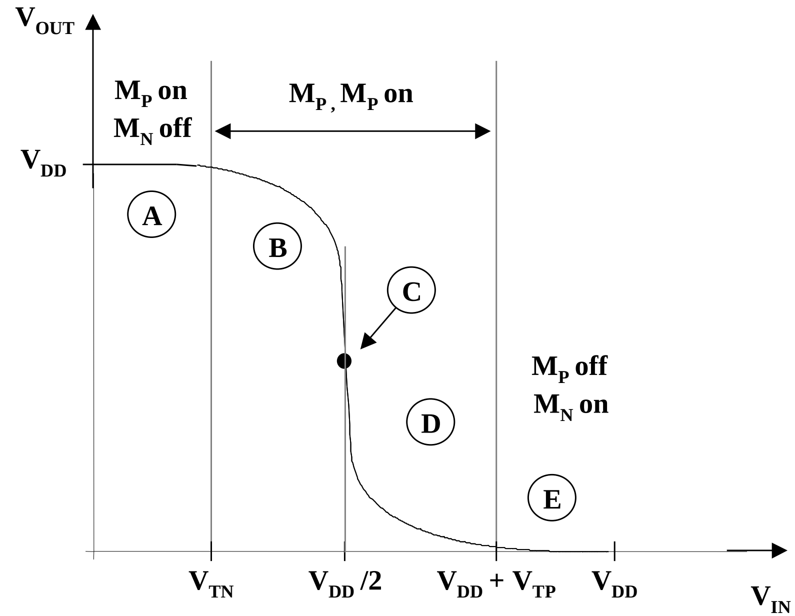
C) M_N saturazione M_P saturazione

$$I_N = I_P \quad \Rightarrow \quad \frac{\beta_N}{2}\cdot\left(V_{IN}-V_{TN}\right)^2 = \frac{\beta_P}{2}\cdot\left(V_{DD}-V_{IN}+V_{TP}\right)^2$$

- Se $\beta_N = \beta_P$, $V_{TP} = -V_{TN} = -V_{TH}$

$$\left(V_{IN}-V_{TH}\right)^2 = \left(V_{DD}-V_{IN}-V_{TH}\right)^2 \quad \Rightarrow \quad V_{IN} = \frac{V_{DD}}{2}$$

Inverter CMOS

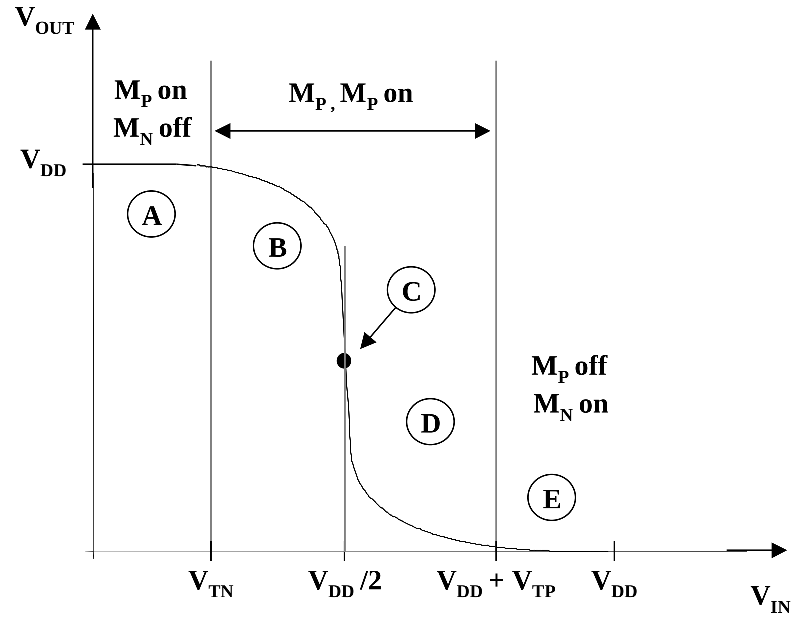


D) $V_{DD}/2 < V_{IN} < V_{DD} + V_{TP}$

M_N non saturazione $\qquad$ M_P saturazione

$$\begin{cases} I_N = \beta_N \cdot \left[\left(V_{IN} - V_{TN} \right) \cdot V_{OUT} - \dfrac{V_{OUT}^{\ 2}}{2} \right] \\ I_P = \dfrac{\beta_P}{2} \cdot \left(V_{DD} - V_{IN} + V_{TP} \right)^2 \end{cases}$$

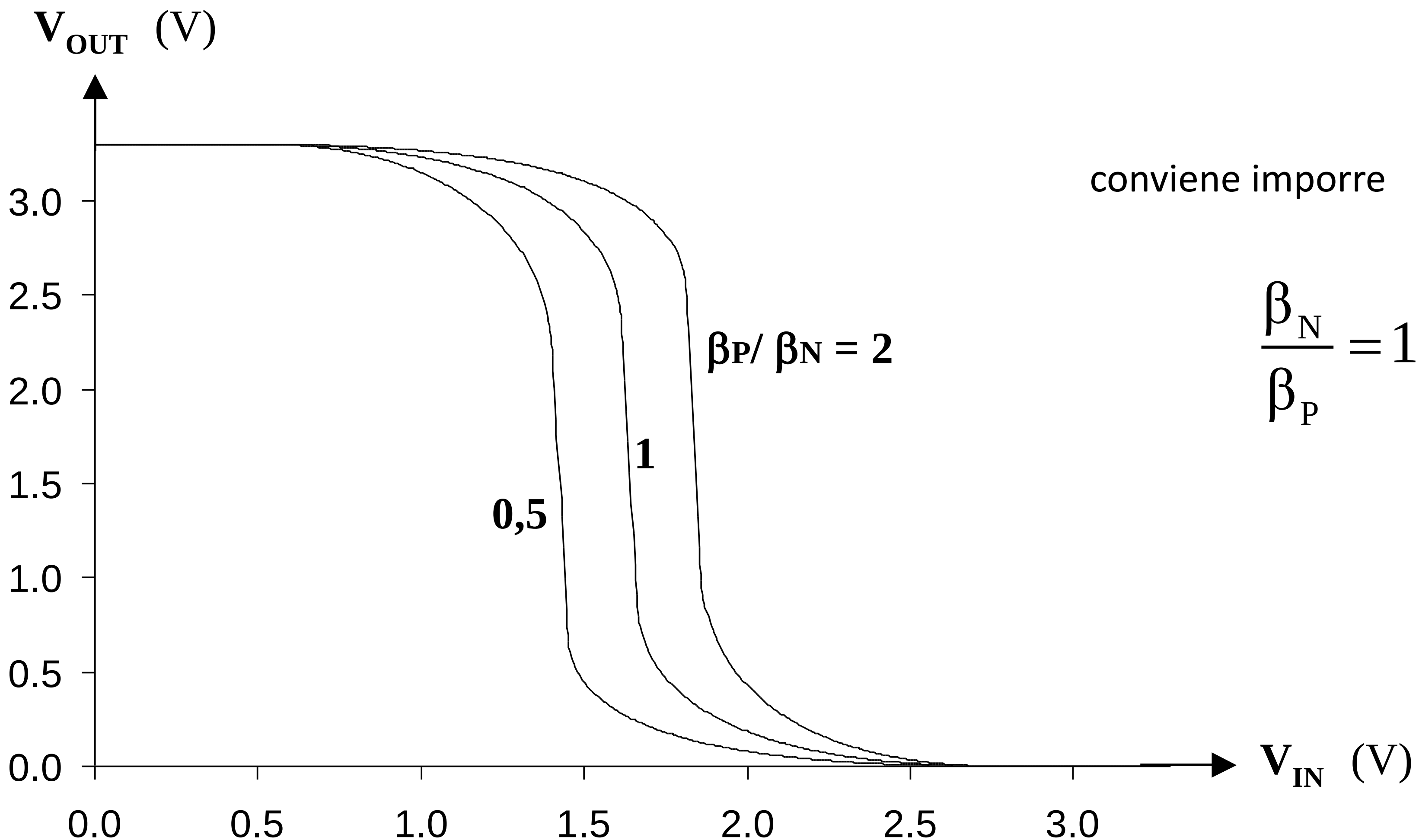
Inverter CMOS



E) $V_{IN} \geq V_{DD} + V_{TP} \;\Rightarrow\; V_{SG} \leq -V_{TP} \;\Rightarrow\; M_P = OFF \;\Rightarrow\; I_P = 0$

$$I_P = I_N = \beta_N \cdot \left[\left(V_{IN} - V_{TN} \right) \cdot V_{OUT} - \frac{V_{OUT}^{\;2}}{2} \right] = 0 \quad \text{deve essere} \quad \mathbf{V_{OUT}} = V_{OL} = 0$$

Inverter CMOS



conviene imporre

$$\frac{\beta_N}{\beta_P} = 1$$