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Energy and power management in the computing continuum

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Background on Electronics and Power consumption

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Basics on Power Management

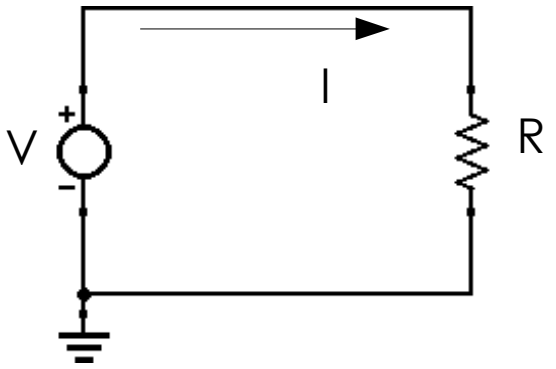
Outline

- **Basics on power consumption**
- Power saving blocks and knobs
- Power states and ACPI
- Operating systems integration (the Linux case)
- Thermal issues
- Miscellanea
- Presentation of the assignments
- Conclusions

Background: power

Power consumption in a simple V-R circuit

- Basic V-R circuit



- **Power**

Product between instantaneous values of current (I) and voltage (V)

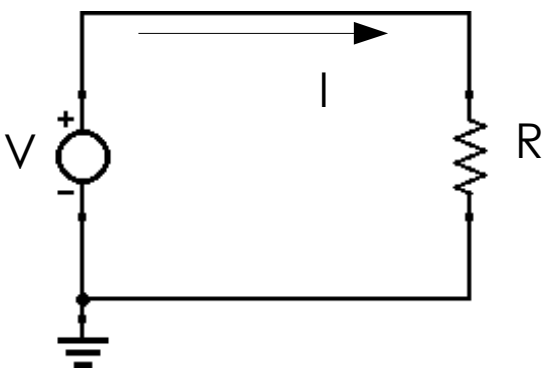
$$P = I * V = V^2/R$$

$$P(t) = I(t) * V(t) \ldots \text{it is } f(t)$$

Background: energy

Power consumption in a simple V-R circuit

- Basic V-R circuit



- **Energy**
  - ➔ Integration of the power over the time

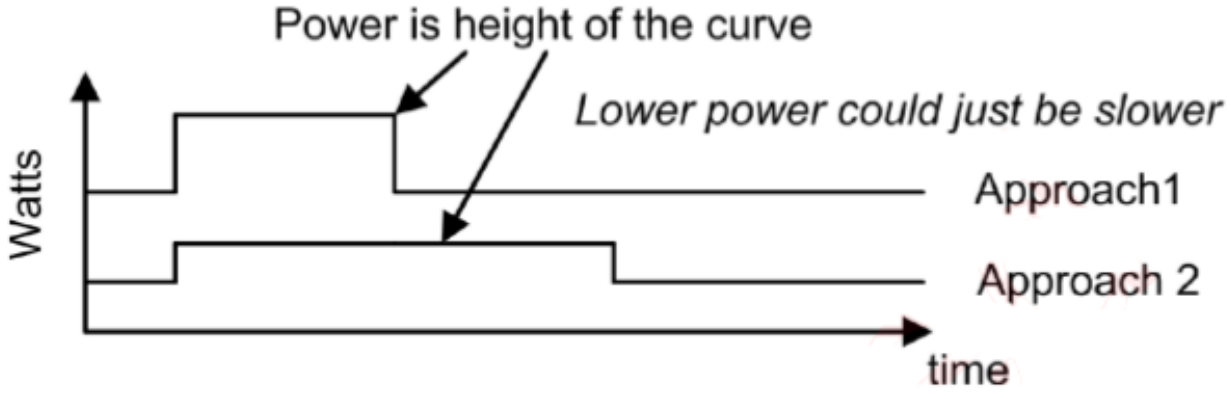
$$\int_{t} P\,dt \;\ldots\; it\ is\ still\ f(t)$$

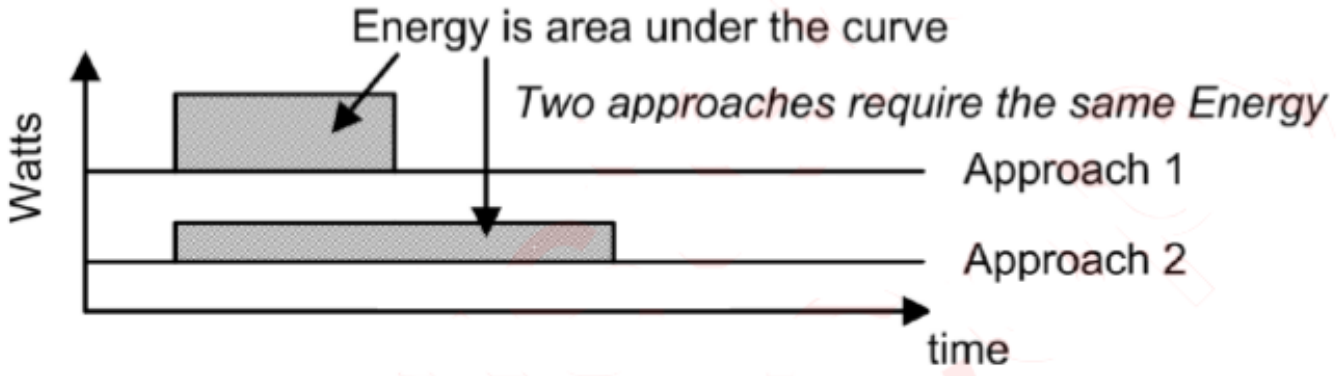
- **Power management affects also ENERGY management**

Background: power vs energy

Especially for battery operated devices, the distinction between power and energy is crucial:

- **Power** is the **instantaneous** power in the device
- **Energy** is the **integral** of the power over time





Low power it is not synonymous of low energy

Background: why heating

Power and temperature

- An electrical circuit dissipates part of the energy in form of heat

- **Joule's equation**: the amount of *heat* (***Q***) is due to...
  - The current fowing in the circuit (***I***)
  - The resistance of the circuit (***R***)
  - The operational time (**t**)

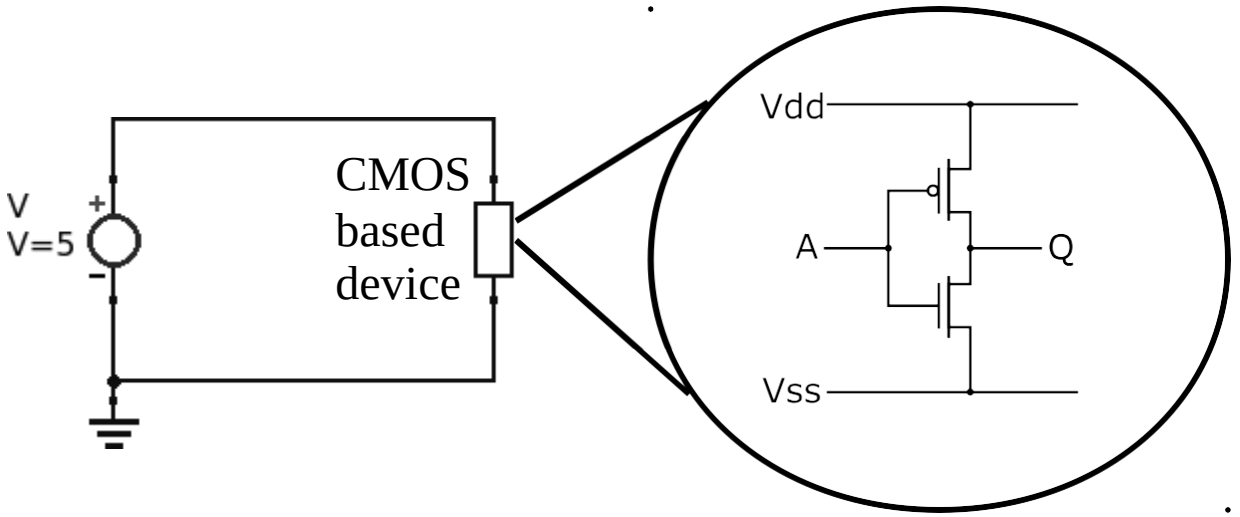
$$Q = I^2 R t$$

- **Power management affects also THERMAL management**

Sources of power dissipation

Power consumption in CMOS based circuits

- The power consumption is given by two contributions
  - The **dynamic** and the **static** power consumption



e.g., CMOS inverter

$$P_{total} = P_{dynamic} + P_{static}$$

Power Consumption in CMOS devices

Total Power = Dynamic Power + Static power

Dynamic Power: the power consumed when the device is active, that is when signals are changing values

- **Switching power:** the power required to charge and discharge the output capacitance on a gate
- **Internal Power:** short circuit currents that occur when both NMOS and PMOS transistors are on

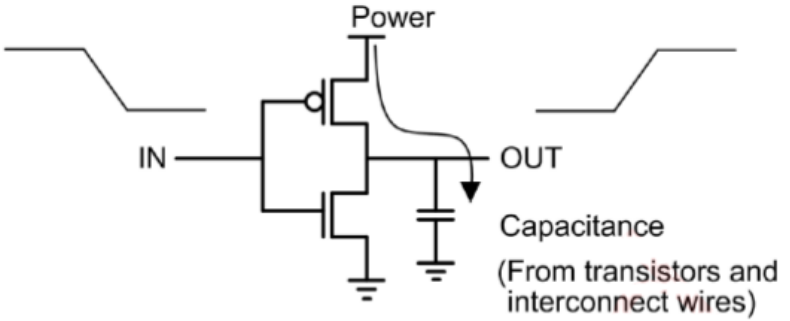
Static Power: the power consumed when the device is not switching values

- **Sub-threshold Leakage (Isub):** the current which flows from the drain o the source of the transistor operating in the weak inversion region
- **Gate Leakage** (**Igate**): the current which flows directly from gate through the oxide to the substrate due to gate oxide tunneling and hot carrier injection
- **Other leakage sources:** Gate Induced Drain, reverse bias Junction Leakage

Dynamic Power: Switching Power

Switching power is the primary source of dynamic power consumption

NOTE: Switching power is data dependent, since it is not a strong function of transistor size but rather a function of the switching activity and load capacitance



- The energy per transition is given by:

$$Energy/transition = C_L \bullet V_{dd}^2$$

- Where C_L is the load capacitance and Vdd is the power supply. We can describe the dynamic power as:

$$P_{dyn} = Energy/transition \bullet f = C_L \bullet V_{dd}^2 \bullet P_{trans} \bullet f_{clock}$$

- Where f is the frequency of transitions, P_{trans} is the probability of output transition, and fclock is the frequency of the system clock. If we define:

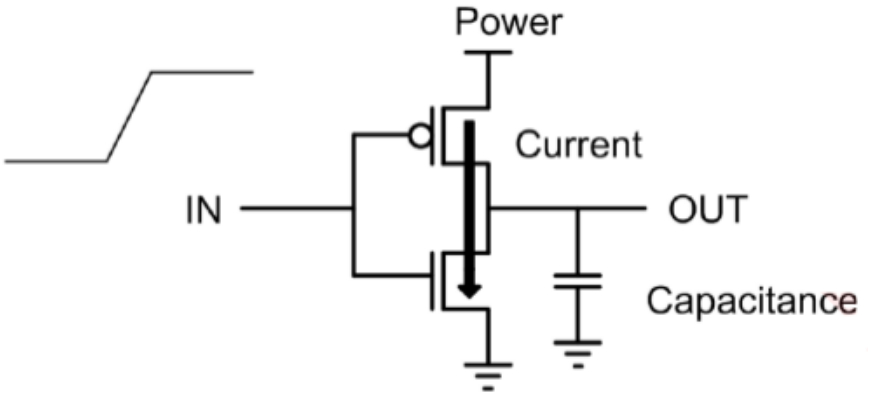
$$C_{eff} = P_{trans} \bullet C_L$$

- Now, we can define dynamic power with the following formulation

$$P_{dyn} = C_{eff} \bullet V_{dd}^2 \bullet f_{clock}$$

Dynamic Power: Internal Power

Internal power accounts for short circuits that happen when both NMOS and PMOS are ON



- The total dynamic power formula with internal power is:

$$P_{dyn} = \left(C_{eff} \bullet V_{dd}^2 \bullet f_{clock}\right) + \left(t_{sc} \bullet V_{dd} \bullet I_{peak} \bullet f_{clock}\right)$$

Where t_{SC} is the time duration of the short circuit current, and Ipeak is the total internal switching current.

- As long as the ramp time of the input signal is kept short, the overall dynamic power is dominated by the switching power:

$$P_{dyn} = C_{eff} \bullet V_{dd}^2 \bullet f_{clock}$$

Dynamic power in a nutshell

Dynamic power

- The device/component is active, i.e., the CMOS inverters are switching between logical states ("0" and "1")
- The power consumption is due to
  - Number of switching bits
  - Capacitance

    State transitions speed are upper-bounded by the capacitance
  - Clock frequency

    Affecting the switching rate
  - Voltage

$$P_{dyn} = N_b C f V^2$$

Static Power: Sub-threshold Leakage

Sub-threshold leakage occurs when the CMOS gate is not completely turned off

$$I_{SUB} = \mu C_{ox} V_{th}^2 \frac{W}{L} \cdot e^{\frac{V_{GS} - V_T}{nV_{th}}}$$

where **W** and **L** are the dimensions of the transistor, and $\mathbf{V_{th}}$ is the thermal voltage **kT/q** (25.9mV at room temperature). The parameter n is a function of the device fabrication process and ranges from 1.0 to 2.5.

- Sub-threshold leakage current **increase exponentially with temperature** allowing for great issues in low power system design. Moreover, the temperature increase with the power density, then it is possible to have a **positive feedback between temperature and leakage current**

- Sub-threshold leakage depends exponentially on the difference between $\mathbf{V_{GS}}$ and $\mathbf{V_T}$, thus **Vdd scaling must be carefully considered**

NOTE: we do not consider gate leakage here, while it can be nearly 1/3 of the sub-threshold leakage power @90nm, roughly equal to sub-threshold leakage @ 65nm. The common technological solution to face gate leakage is the introduction of the high-k dielectric material under 65nm

Leakage Power Reduction Techniques

- Detailed discussion
  - **Multi-VT**: using high V_T cells wherever performance goals allow and low V_T cells where necessary to meet timing
  - **Power Gating**: shutdown/cut-off power supply to a block of logic when it is not active

- Other approaches
  - **Variable Threshold CMOS (VTCMOS)**: applying a reverse bias voltage to the substrate, it is possible to reduce the value of the term (V_{GS}-V_T), effectively increasing V_T. It adds complexity to the technology library requiring additional power networks to separately control voltage, while the effectiveness of reverse body bias decreases with technology scaling
  - **Long Channel Devices**: using non-minimal length channels will reduce leakage. However, performance degrades, since lower dynamic current. Moreover, the greater gate capacitance increases the dynamic power consumption.

Dynamic Power Reduction Techniques

- There are a lot of techniques at architectural, logic design and circuit design than can reduce power, while all of them are focused on **voltage, frequency and switching activity** components of the dynamic power equation

- Switching activity:
  - Data dependent

- Frequency techniques (linear dependency of power on frequency)
  - **Clock gating**: driving the frequency to zero drives the power to zero also

- Voltage techniques (quadratic dependency of power on voltage)
  - **Multi-voltage:** assign different voltages to different blocks
  - **Variable supply voltage:** different voltage levels for the same block either dynamically or statically assigned

- Combined techniques, i.e. DVFS to mix advantages of different techniques

The Conflict between Dynamic and Static Power 1

The most effective way to reduce DYNAMIC POWER is to reduce the supply voltage, due to the quadratic relation between Vdd and dynamic power

(Vdd has lowered from 5V to 3.3V to 2.5V to 1.2, while ITRS road map predicted 1.0V @ 2009)

Lower Vdd means lower IDS (on or drive current in MOS), then slower speed, according to the following formula:

$$I_{DS} = \mu C_{ox} \frac{W}{L} \cdot \frac{(V_{GS} - V_T)^2}{2}$$

where \mu is the carrier mobility,C_{OX} is the gate capacitance, V_T is the threshold voltage and V_{GS} is the gate-source voltage.

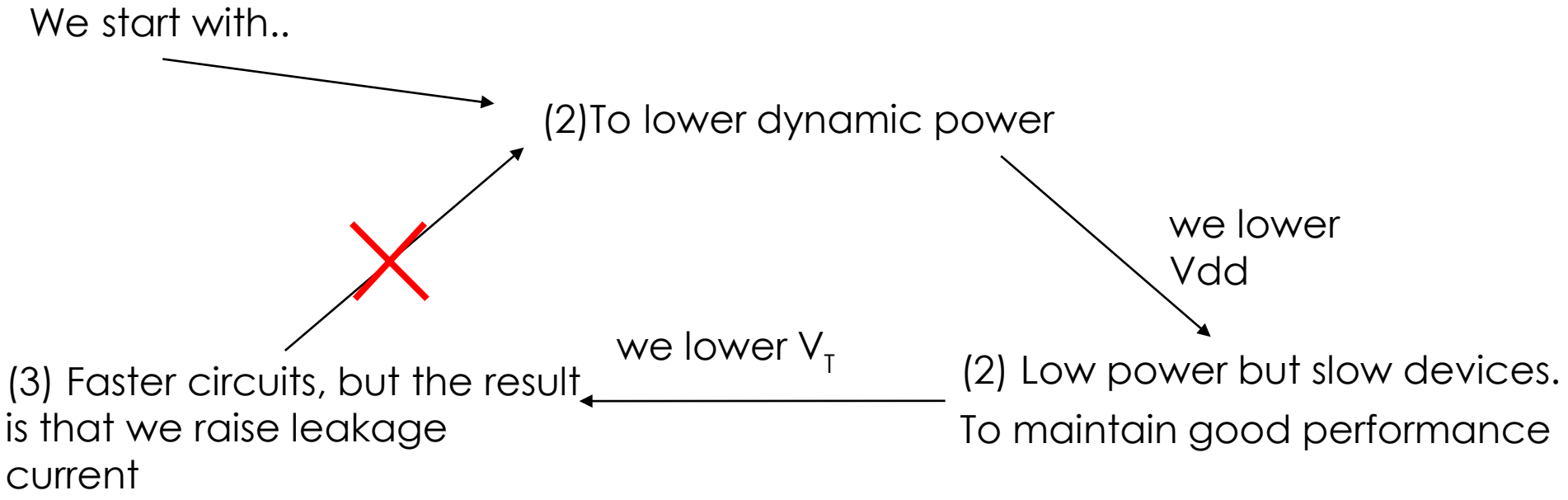
One viable solution to maintain good performance seems to be "setting a lower V_T value",

... but there is a problem...

The Conflict between Dynamic and Static Power 2

Lowering VT results in an exponential increase in the sub-threshold leakage current, thus leakage power, according to the following formulation:

Thus there is a conflict. To lower dynamic power we lower Vdd; to maintain good performance we lower VT; but the result is that we raise leakage current. While this process was reasonable until 90nm technology node, we are now experiencing the point where static power and dynamic one are comparable.



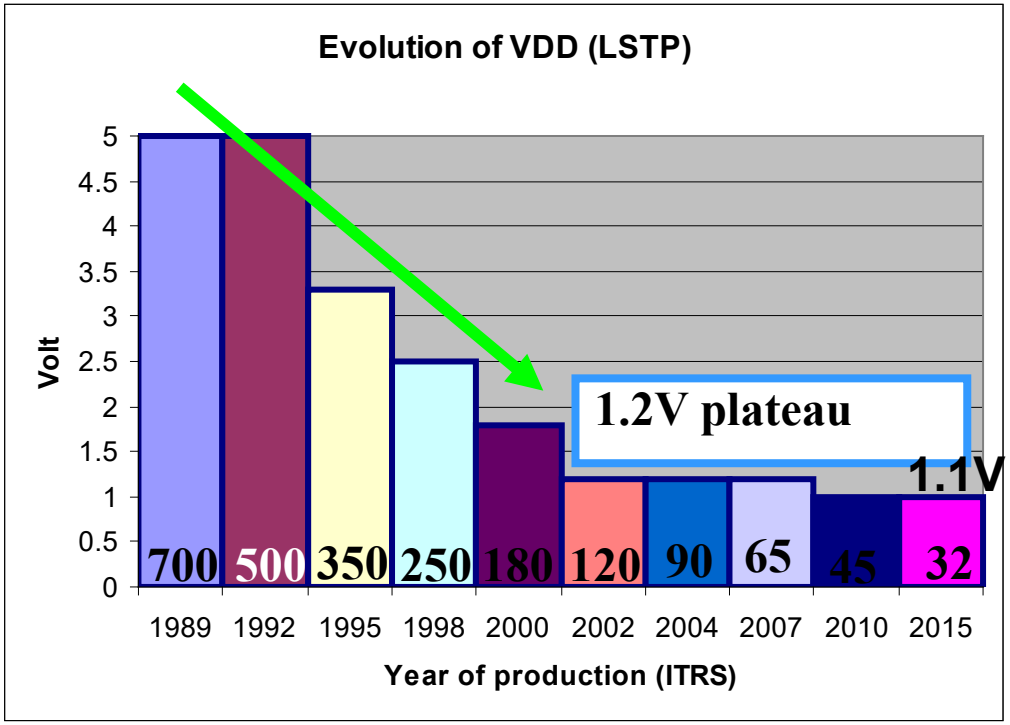
NOTE: Vdd reduction is no more a practical solution under 32nm

VDD is increasing the “power crisis”

VDD is no more scaling down

Regular decrease: 5V to 1.2V (0.7x per node)

5V plateau

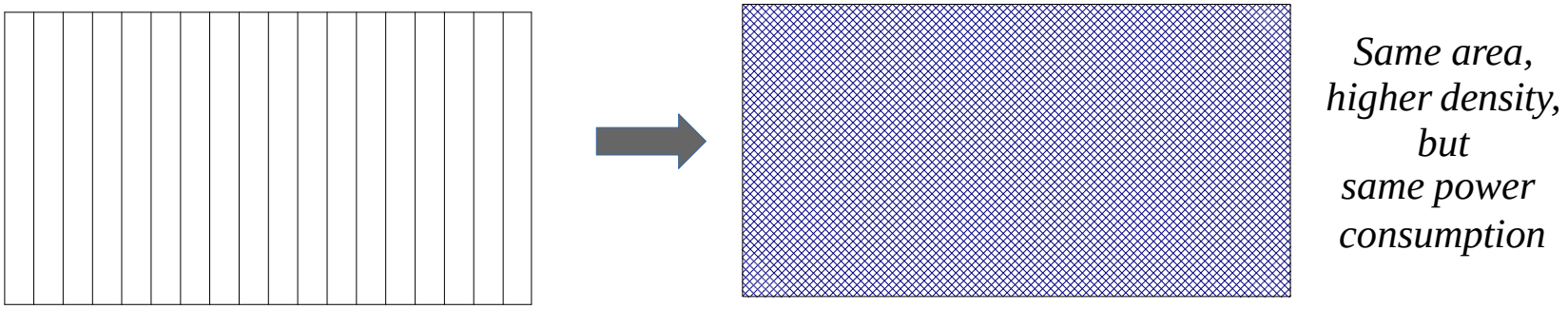


0,9-1V plateau

Towards a crisis

Dennard's scaling

- Consider the dynamic contribution to power consumption
- If silicon integration technology scales, the size of the CMOS transistors decreases and so...
  - The capacitance C decreases
  - The voltage V can be decreased as well
  - The frequency f can be increased to scale up the performance
  - The overall dynamic power consumption remains the same



130nm, f=1.50 GHz
P=25W

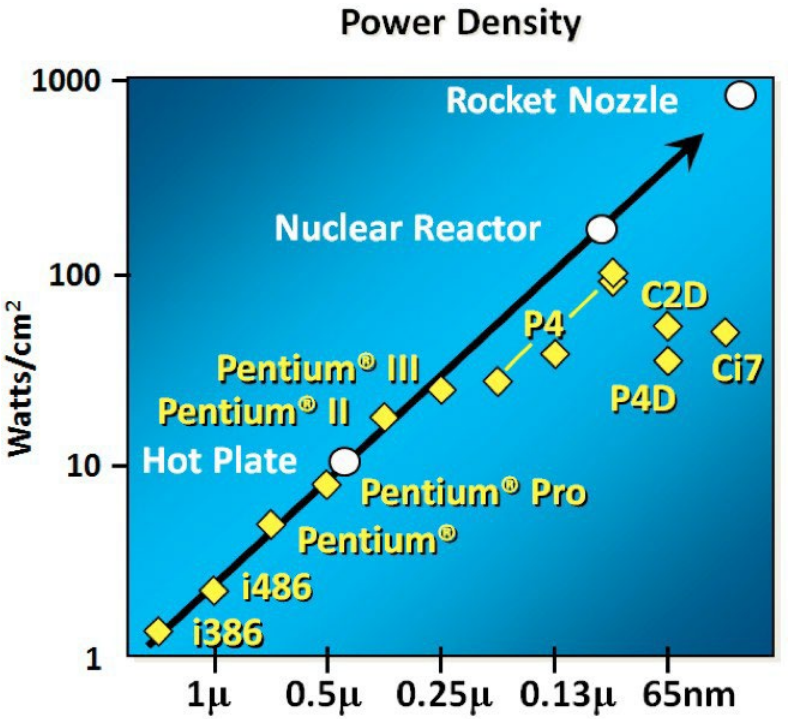
90nm, f=2 GHz
P=25W

Same area, higher density, but same power consumption

Towards a crisis

Dennard's scaling

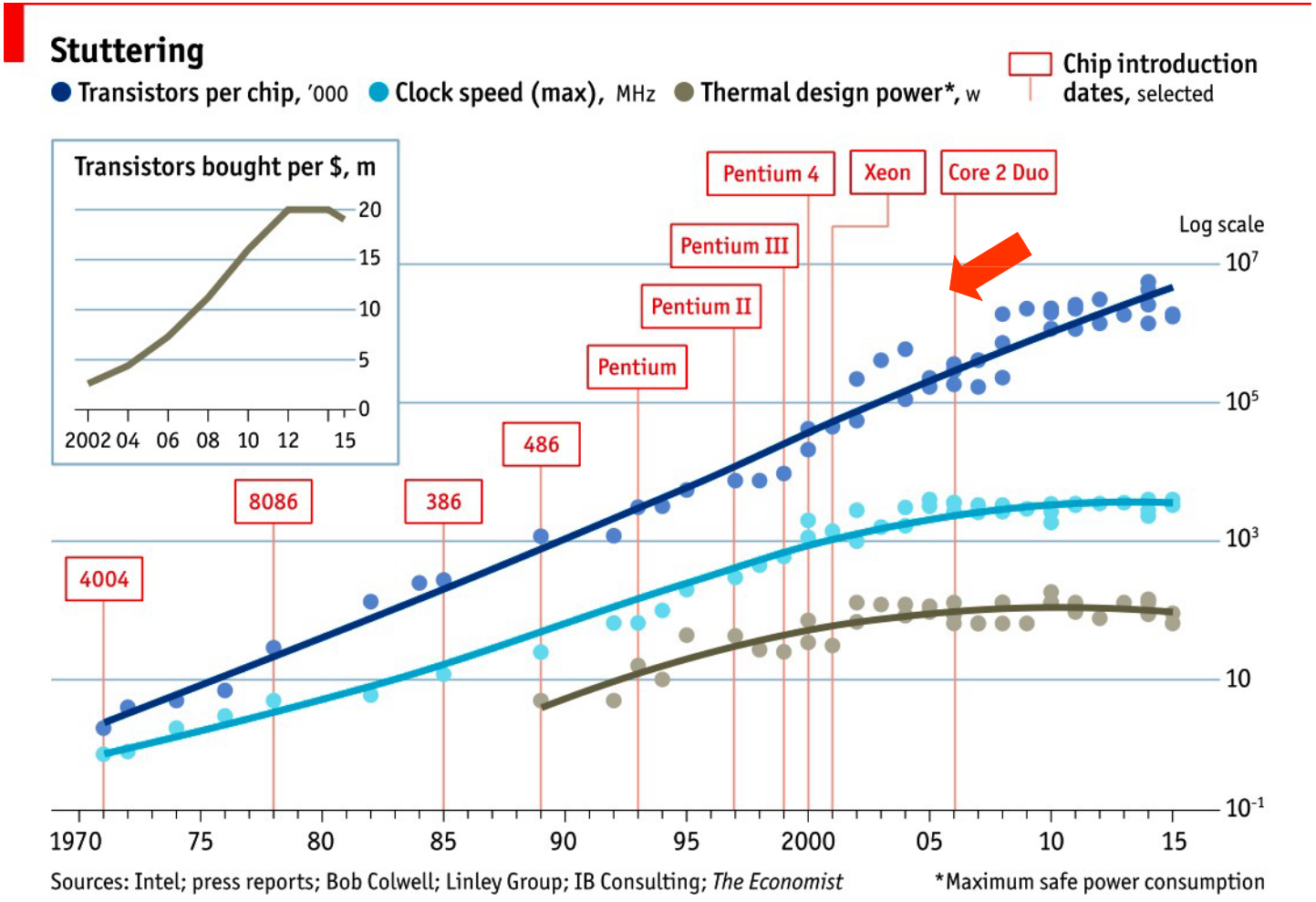
- Since 2005 (45nm) the Dennard's scaling law does not hold anymore
  - → Dark Silicon and the End of Multicore Scaling
- The static contribution to power consumption was ignored
- Smaller transistors means...
  - → Higher power density
  - → Higher leakage current
  - → Higher sensitivity of I_{leak} to the temperature
- We hit the *Power wall* → no more clock frequency scaling



Towards a crisis

Dennard's scaling

- End at 45nm



Towards a crisis – impact on Static Power

Static power

- The device/component is powered on but not operating (i.e., there is no switching activity
- The power consumption is dominated by
  - Voltage
  - Leakage current (typically in the order of 10-50 μA)

$$P_{sta} = I_{leak} V$$

- **Static power consumption contribution is growing due to the end of the Dennard's scaling**
  - The higher the integration scale of the CMOS technology the higher the amount of leakage current
  - The temperature has a further impact on the leakage current

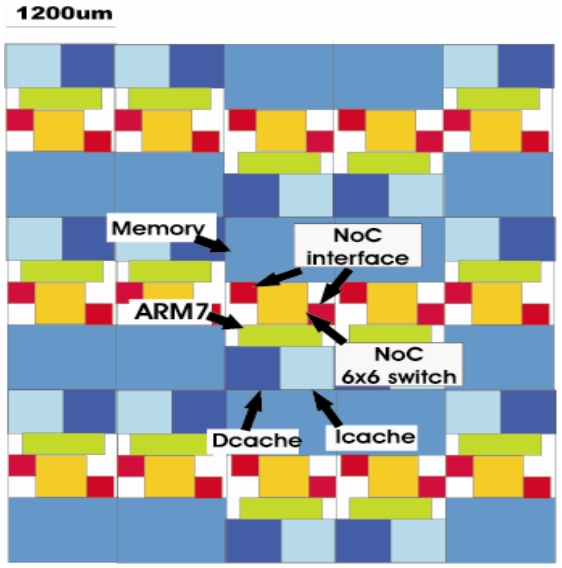
Thermal side of computing systems

Thermal Design Power (TDP)

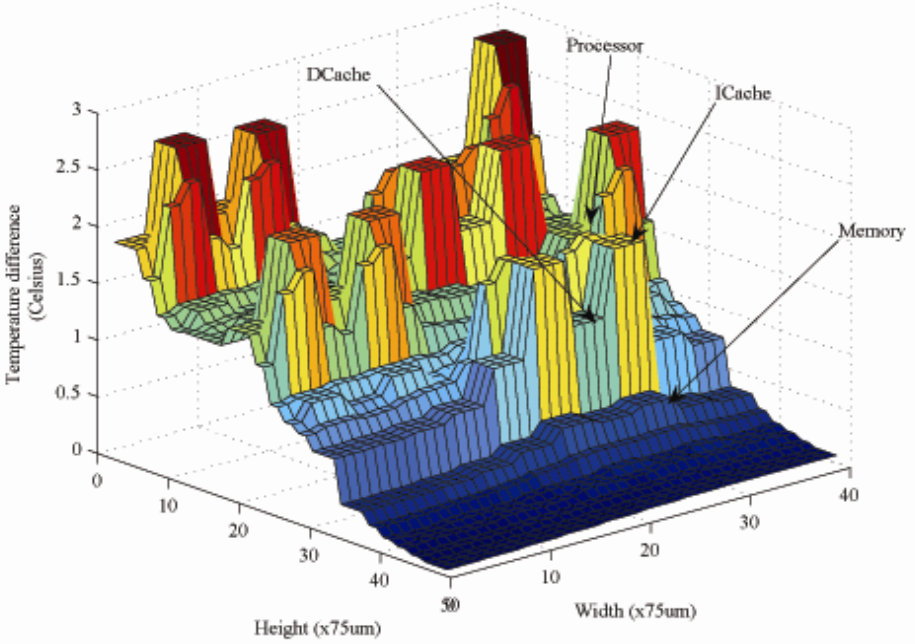
- It is the "power rating" of a computing system
- It represents the maximum amount of power that the cooling system is required to dissipate

System	TDP (W)	Cooling approach
Low-power embedded	< 5	Passive
Smartphone	4 - 5	Passive
Netbooks/Tablets	4 - 12	Mostly passive and possibly a fan
Low -power notebooks (e.g. Chromebook)	10 - 15	Passive and possibly a fan
Notebooks/Laptops	45 - 60	Heat-sink and a fan
Desktops	90 - 130	Heat-sink, multiple fans and (optionally) cooling tubes
Small servers	80 - 165	Heat-sink, multiple fans and (optionally) cooling tubes
Large servers and supercomputers	~ 300	Complex solutions in controlled rooms

Hot spots and thermal problems



Chip floorplan



Steady state temperature

Some hot spots in steady state:

- Silicon is a good thermal conductor (only 4x worse than Cu) and temperature gradients are likely to occur on large dies
- Lower power density than on a high performance CPU (lower frequency and less complex HW)