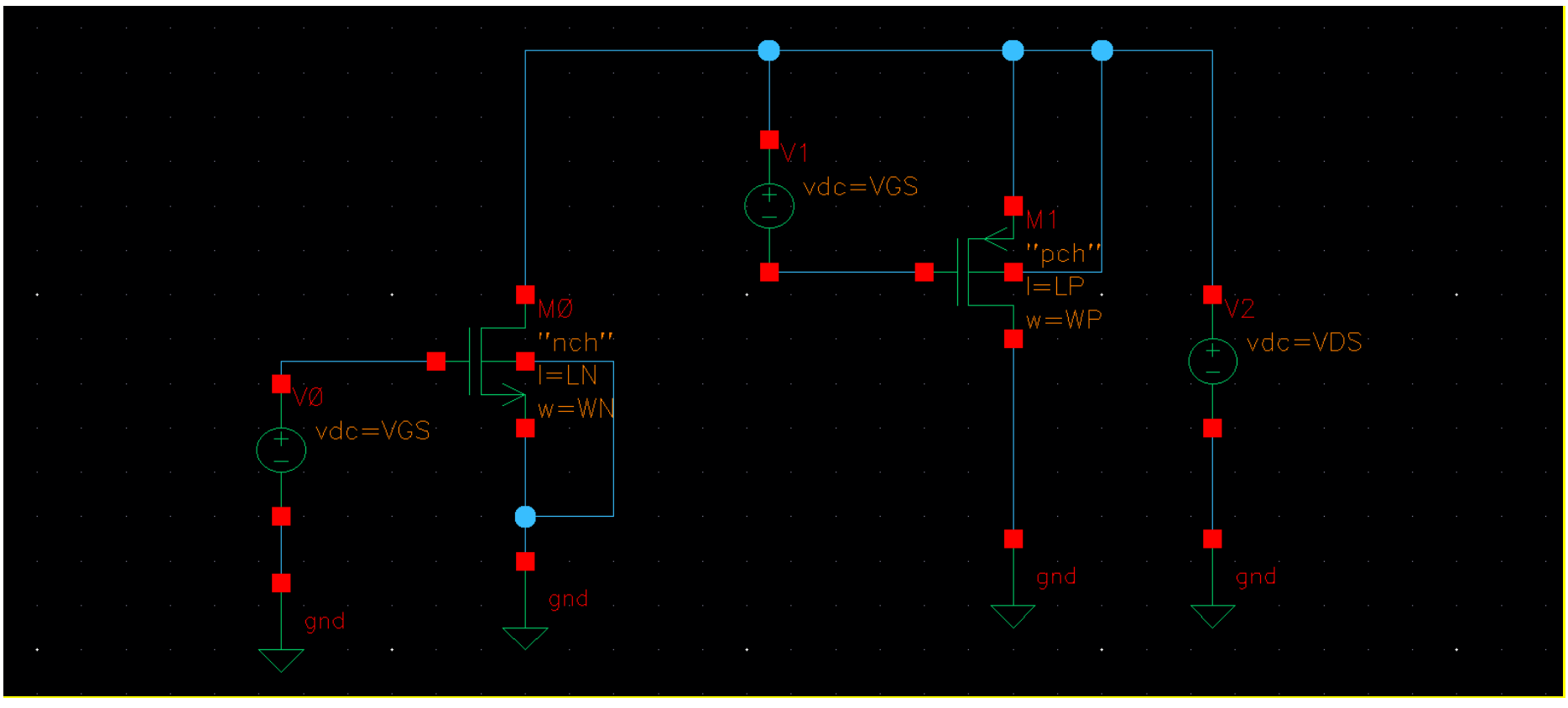
LAB 3

Part 1 (Sizing Chart):

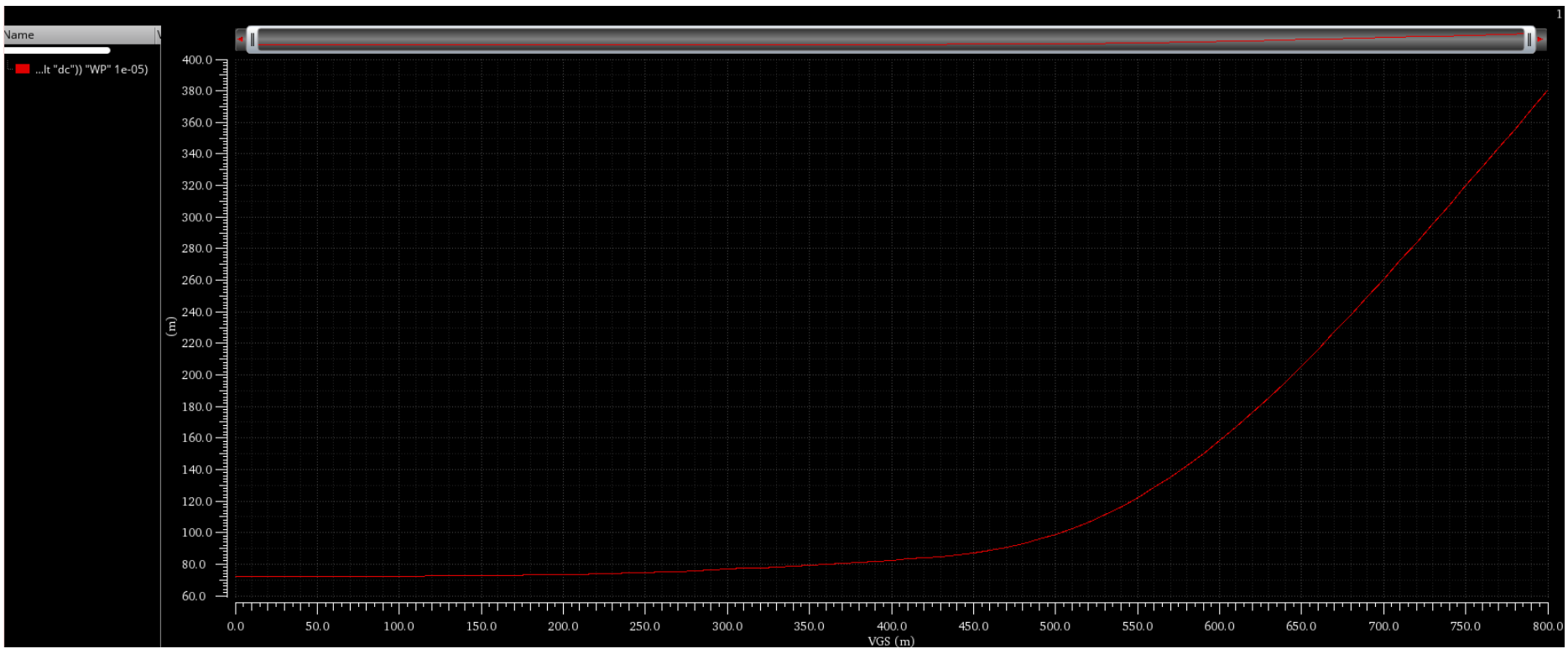
Circuit:



//comments:

- Intrinsic gain is related to (gm-id) ratio, this ration is sizing dependent as it is normalized figure so we can use in sizing process.
- (gm-id) ratio is considered an indicator to the inversion size in the channel of the transistor.
- If (gm-id) ratio is large then we have high gain, biasing move in the weak inversion direction, low power region, low speed, and large area.
- But if (gm-id) ratio is small then we have a large speed, low gain, and small size.
- V*Q is in moderate inversion region, So it is good starting point for any general purpose design.

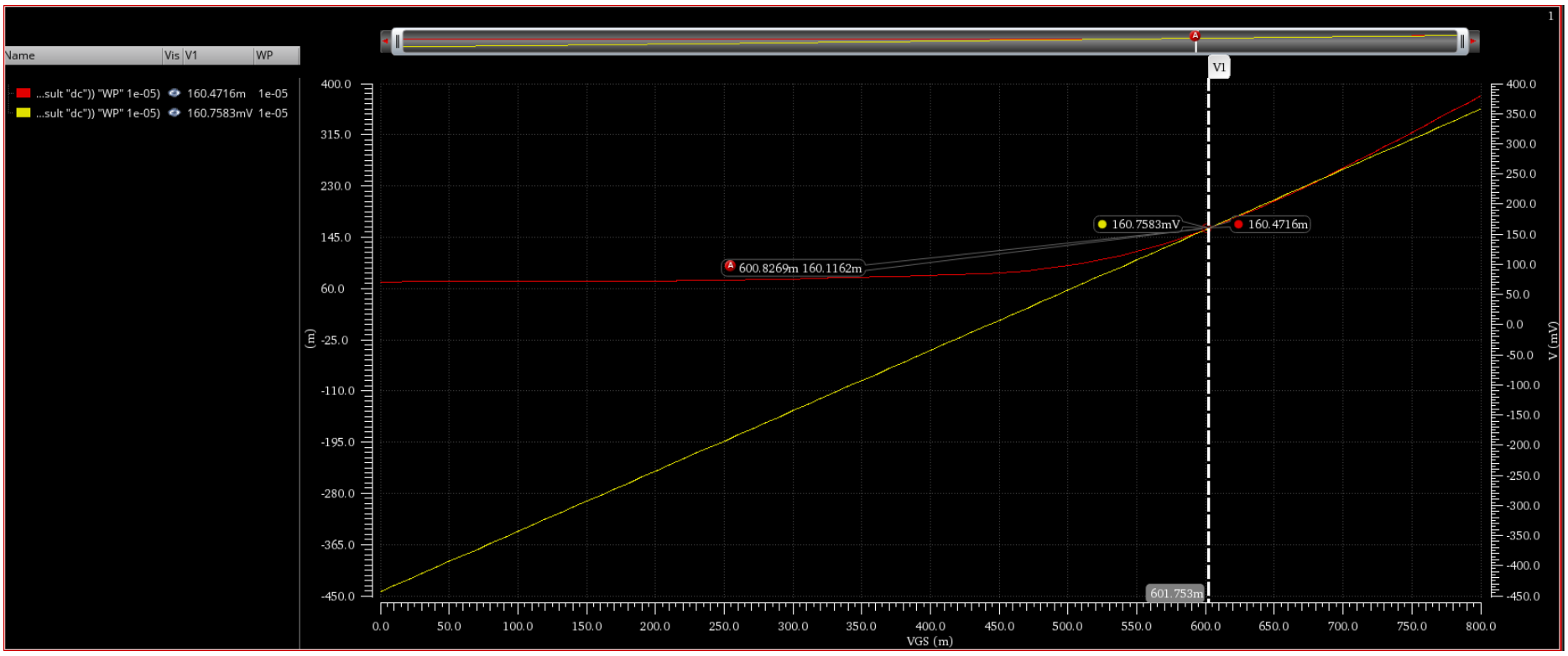
V* plot:



//comments:

- A Dc analysis is done to seep on VGS from 0 to (Vth+0.4) =0.8 V with a 10m V step size.
- V* = 2*ID/gm, so v* is plotted by sending the ID and gm to the calculator to get their expressions then v* equation is built.
- And for plotting Vov :
  - Vov = Vgs-Vth, so Vov is plotted by sending Vgs and Vth to that calculator to get their expressions, then Vov is plotted.

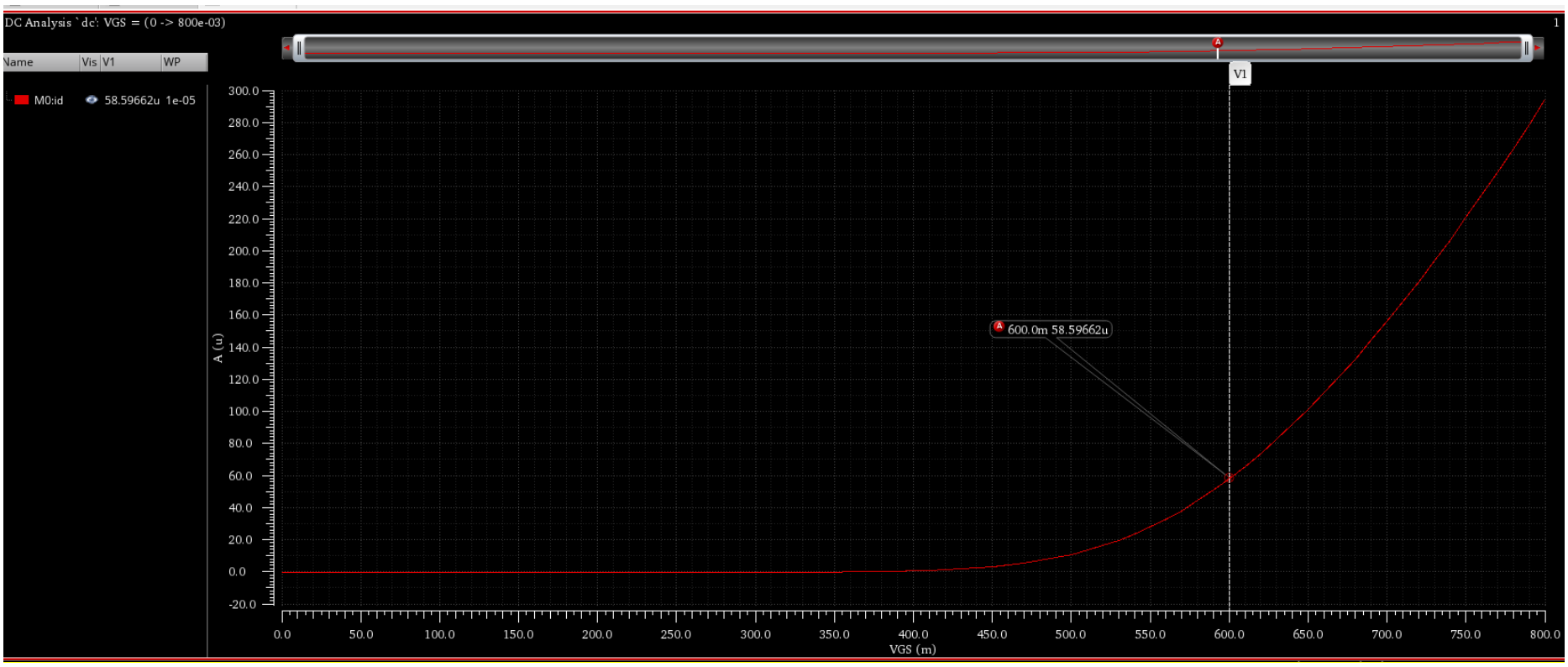
V* and Vov plot (after modifying the Y-axis):



//comments:

- The Y-axis constraints were modified to have the same range.
- From the plotting, it is clear that before the subthreshold operation as we go down the threshold value it is found that the deviation is large between the V* & Vov.
- And they are very close at the moderate values (moderate inversion) which is between subthreshold and under saturation.
- In saturation there is discrepancy as the device is still short channel, but this discrepancy is somehow acceptable.
- Generally, in real VDsat of a transistor the curve of V* and Vov will be closer than this.
- And you will notice that at the beginning of the strong inversion region, $V*$ and Vov are relatively close to each other (i.e., square-law is relatively valid). For deep strong inversion (large Vov: velocity saturation and mobility degradation) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law (although we are using L = 2μm).
- Since, V*Q = 160m V → then we get from the graph that VgsQ = 601m V and VovQ = 160.3m V.
- Then, we get the values of Id, gm and gds at the VgsQ (601m V) and will be named IDx, gmx, and gdsx respectively.

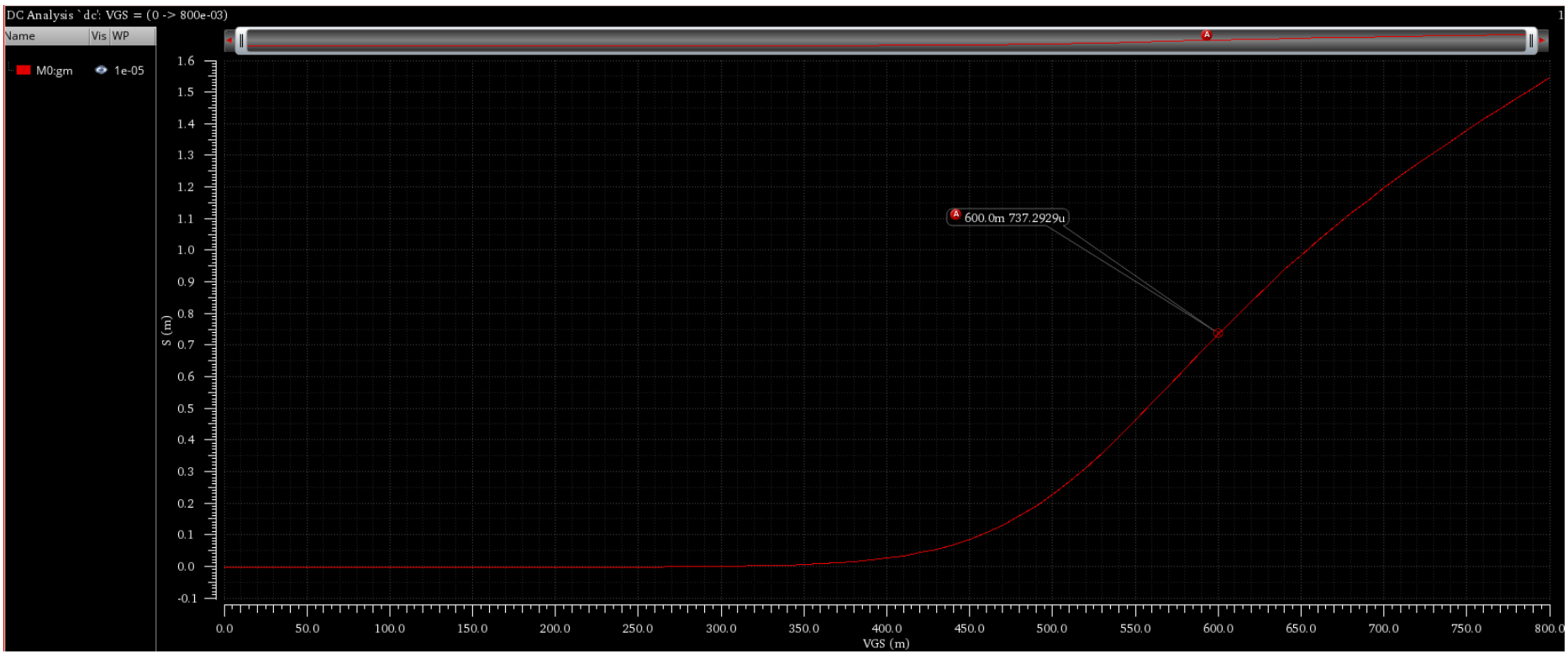
ID plot:



//comments:

- Then, IDx = 58.5u A
- There is difference between required Id and Idx due to linearity between device width and current, so a simple scaling is done to get the actual width _ *in the next pages*

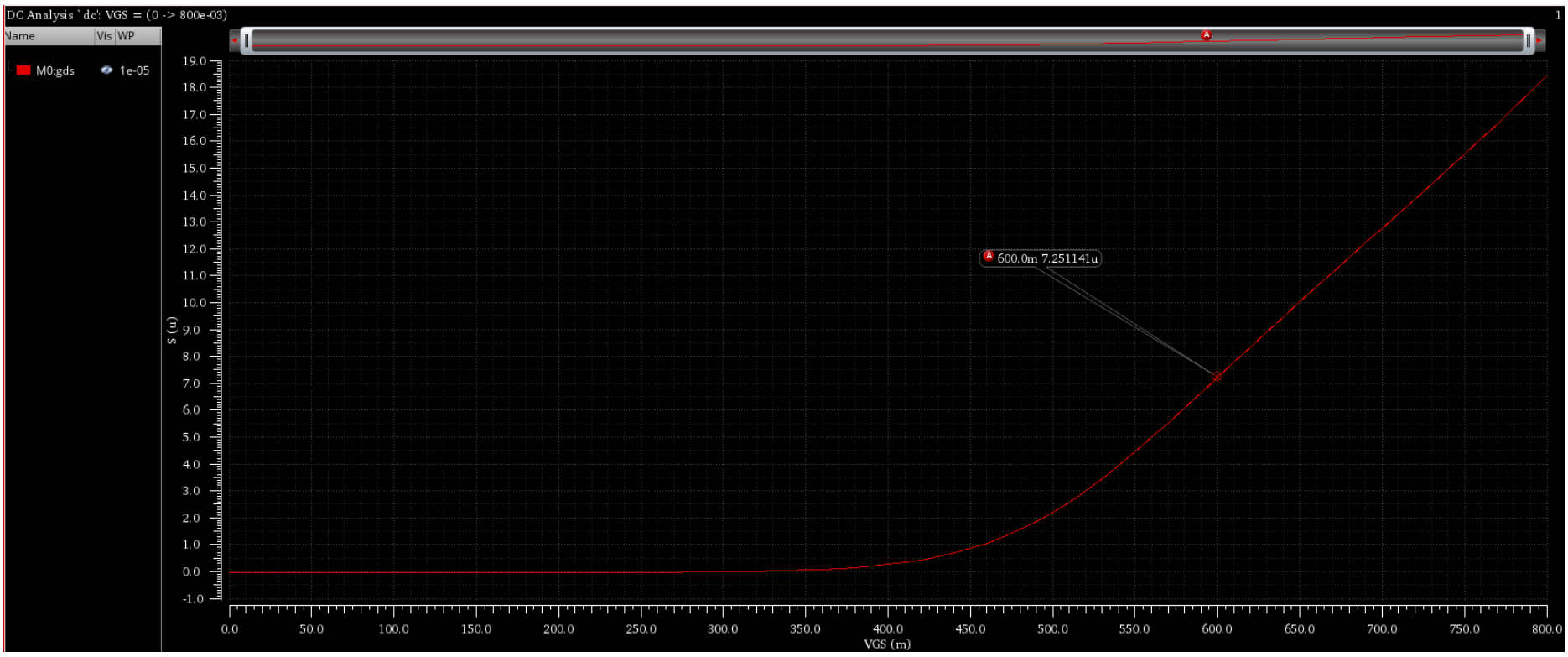
gm plot:



//comments:

- Then, gmx = 737.2929u

gds plot:



//comments:

- Then, gdsx = 7.251141u

//comments:

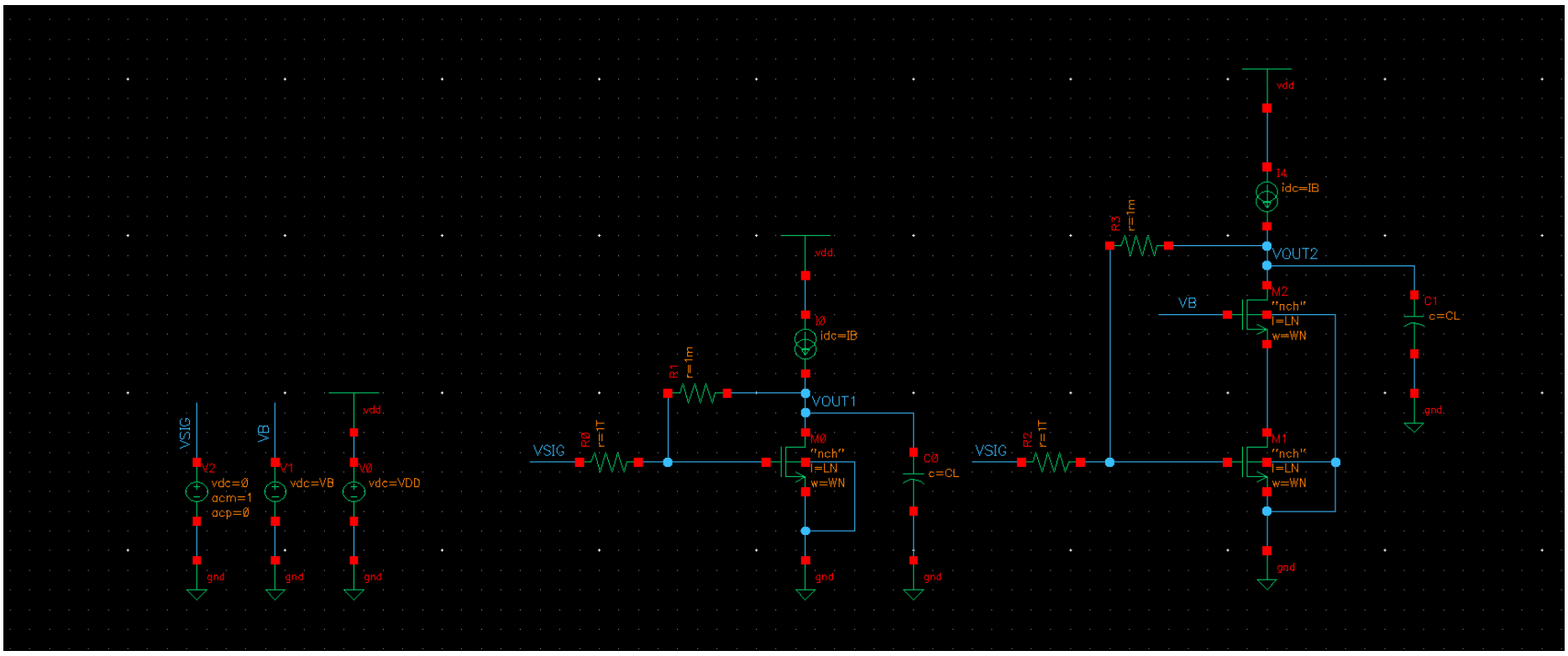
- Now back to the assumption that we made that W = 10μm. This is not the actual value that we will use for our design. But the good news is that ID is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be IDQ = 15μA as given in the specs, So we Calculate W as shown below.
- Then actual width = 2.56u
- And by using the cross-multiplication method again we get:

➢ gmq = 189.04u
➢ gdsq 1.859u
➢ roq = 1/gdsq = 537.9k Ω

Part 2 (Cascode for gain):

1st OP Analysis

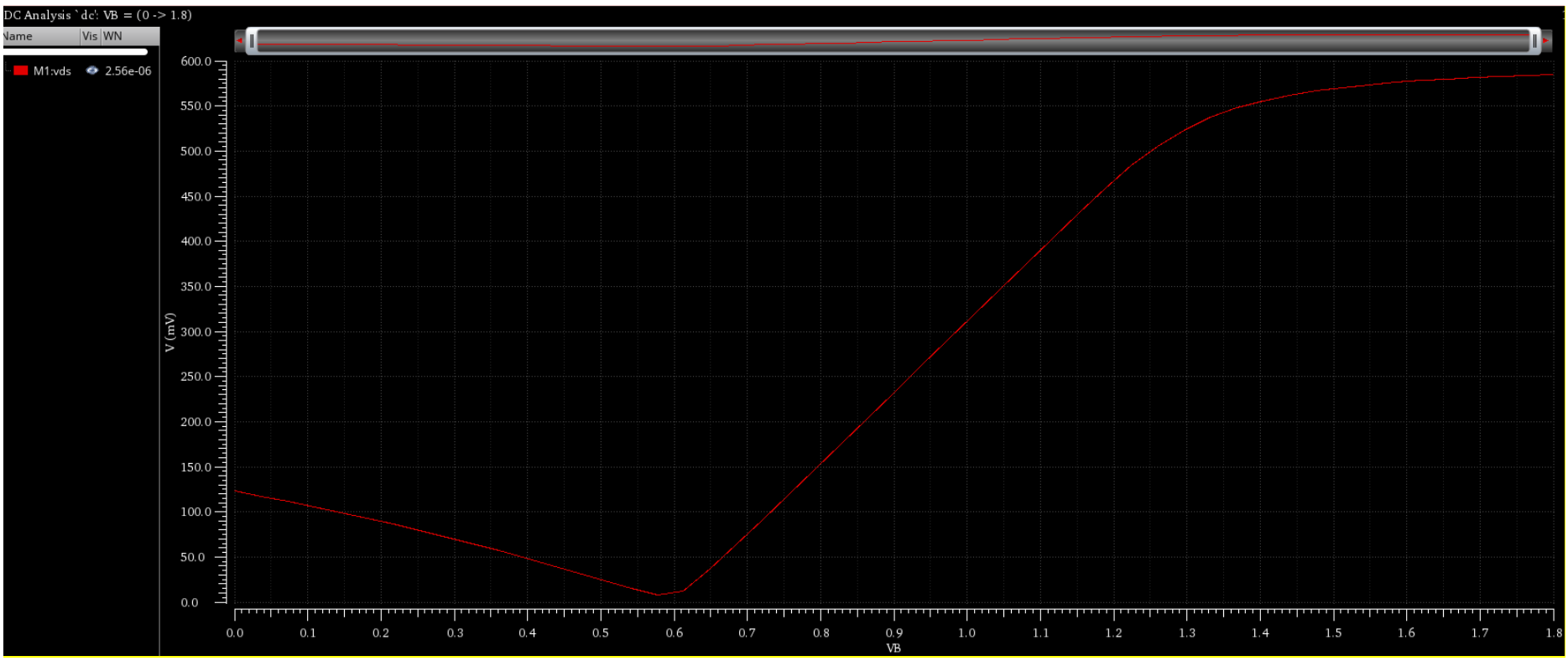
Circuit:



//comments:

- We will choose Vb such that we put VDS margin on the transistor as we don't want our bias to be at the edge of the triode saturation.
- So we will Choose VB (the cascode device bias voltage) such that M2 has $VDS \approx V* + 100mV (260\text{m V})$ so we will sweep VB and plot VDS vs VB to help in choosing a good value for VB).
- We need to bias transistors in saturation; however, the output node is a high impedance node; thus, it is difficult to control its DC voltage. As a workaround in simulation, we use a feedback loop and resistors with different resistances in DC/AC to change the circuit connections in DC/AC simulations (use the AC property in ideal_resistor). The input transistor is diode connected for DC simulation (always in saturation), while in AC simulation the feedback is disconnected, and the AC input source is connected. Set the feedback resistance $1m\Omega$ DC and $1T\Omega$ AC and set the source resistance oppositely.

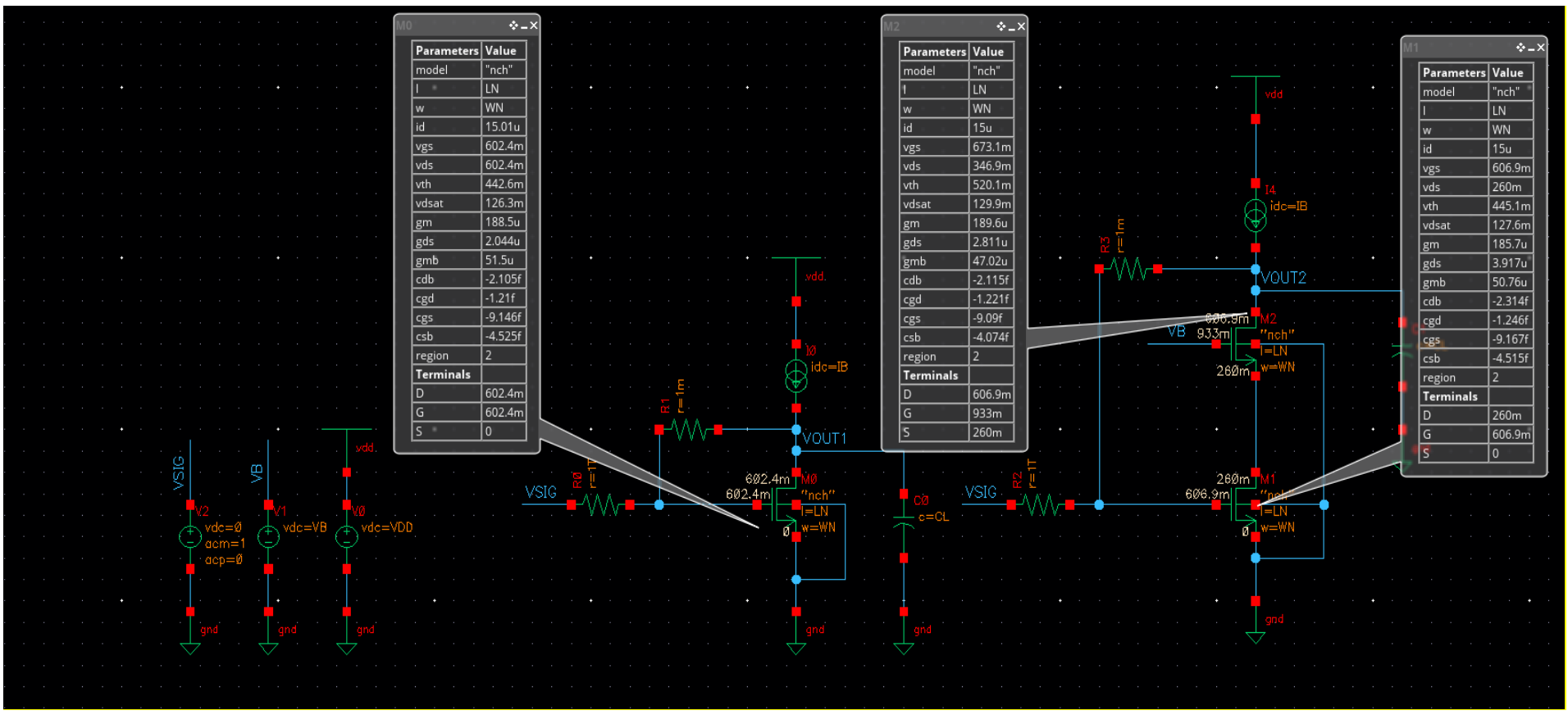
VDS vs VB:



//comments:

- Then we get the best value for Vb at M1 vds =260m V.
- Then best value for Vb = 933.045m V.

DC OP:



//comments:

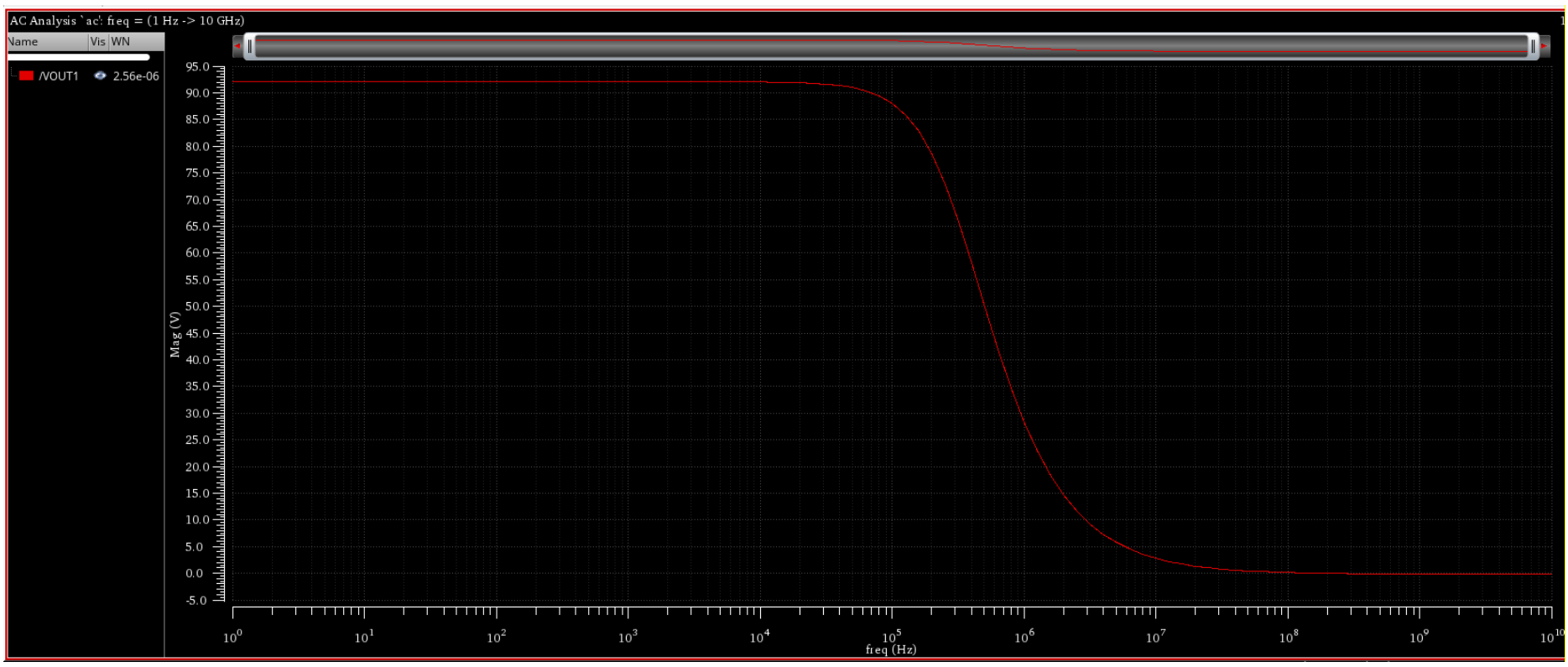
- It is clear that all transistors operate in saturation.
- They have different Vth due to the body effect.
- Gm >> gds (as Gm/gds >10)
- Gm > gmb →as the ratio between them is technology dependent and depend on ratio of junction capacitance to oxide capacitance.
- Cgs > cgd → due to pinch off
- Csb > cbd → because they are reverse biased junctions where depletion capacitance decreases as applied reverse voltage increases and since drain current is at potential higher than source then csb>cbd.

2nd AC Analysis

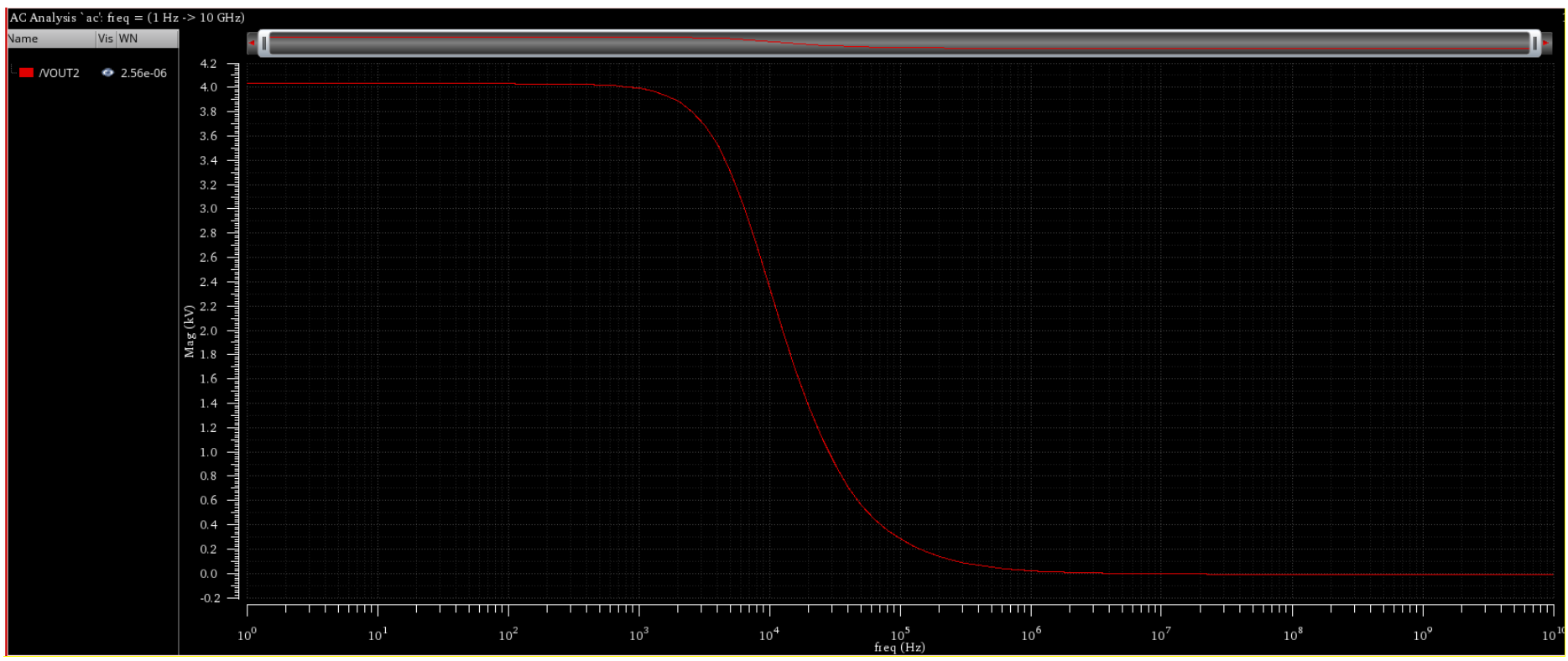
//comments:

- An AC analysis is made (1Hz:10GHz, logarithmic, 10points/decade).

Gain VOUT_1:



Gain VOUT_2:



//comments:

- Since Vin = 1 ,then gain = Vout.

bandwidth VOUT_1:

bandwidth(mag(v("/VOUT1" ?result...

	WN	bandwid..."low")
1	2.560E-6	323.9E3

bandwidth VOUT_2:

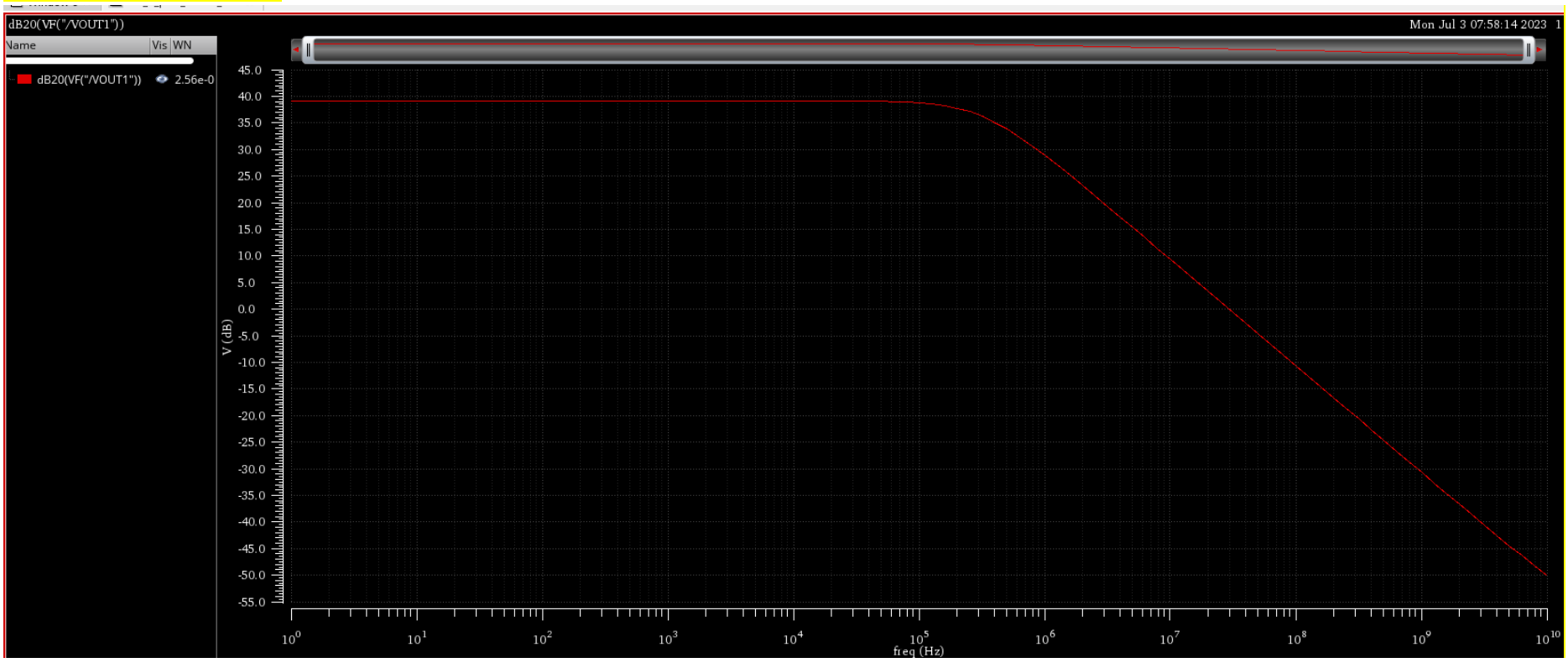
bandwidth(mag(v("/VOUT2" ?result...

	WN	bandwid..."low")
1	2.560E-6	7.181E3

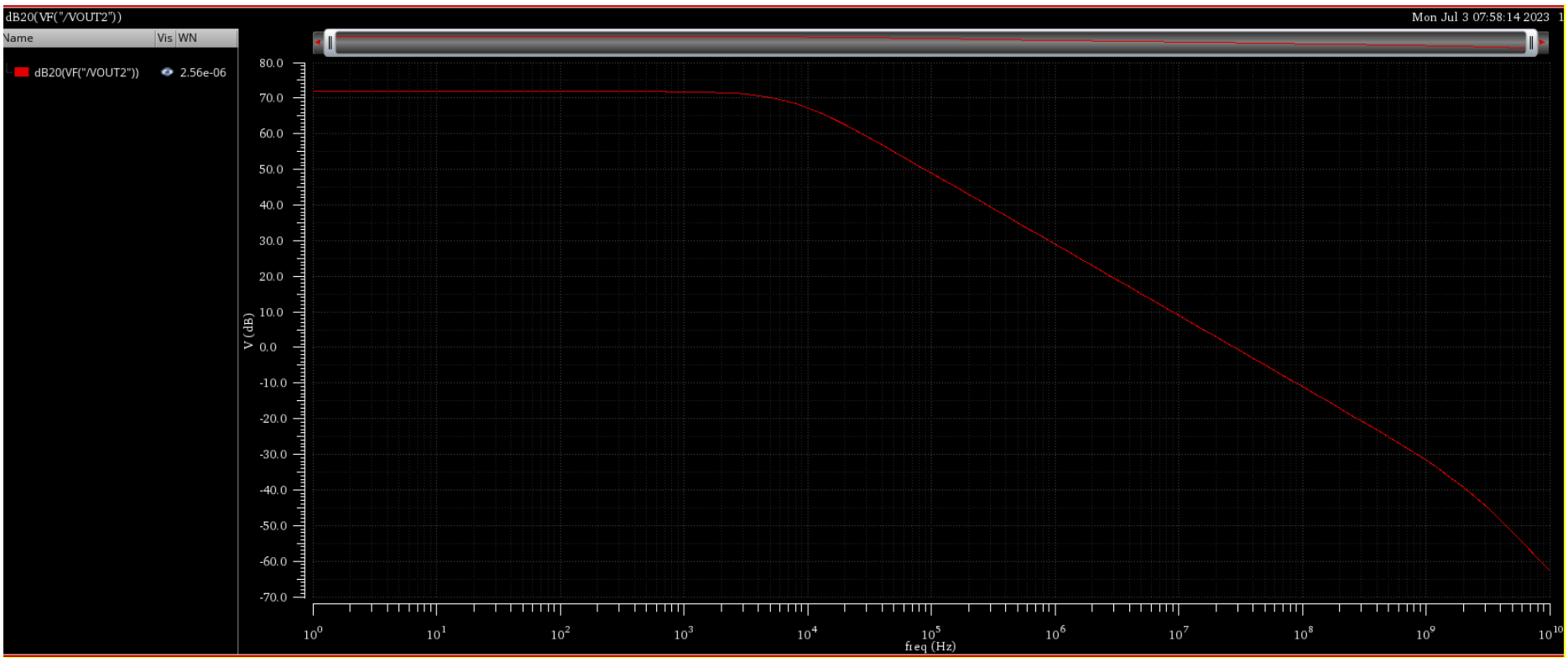
Expressions for VOUT_1 & VOUT_2:

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab_3_part_2:lab3_tb:1	bandwidth(mag(v("/VOUT1" ?result "ac")) 3 "low")	323.9k			
lab_3_part_2:lab3_tb:1	bandwidth(mag(v("/VOUT2" ?result "ac")) 3 "low")	7.181k			
lab_3_part_2:lab3_tb:1	dB20(VF("/VOUT1"))				
lab_3_part_2:lab3_tb:1	ymax(dB20(VF("/VOUT1")))	39.3			
lab_3_part_2:lab3_tb:1	ymax(mag(VF("/VOUT1")))	92.24			
lab_3_part_2:lab3_tb:1	gainBwProd(VF("/VOUT1"))	29.95M			
lab_3_part_2:lab3_tb:1	dB20(VF("/VOUT2"))				
lab_3_part_2:lab3_tb:1	ymax(dB20(VF("/VOUT2")))	72.12			
lab_3_part_2:lab3_tb:1	ymax(mag(VF("/VOUT2")))	4.038k			
lab_3_part_2:lab3_tb:1	gainBwProd(VF("/VOUT2"))	29.06M			

DC gain VOUT_1:



DC gain VOUT_2:



BODE plot :