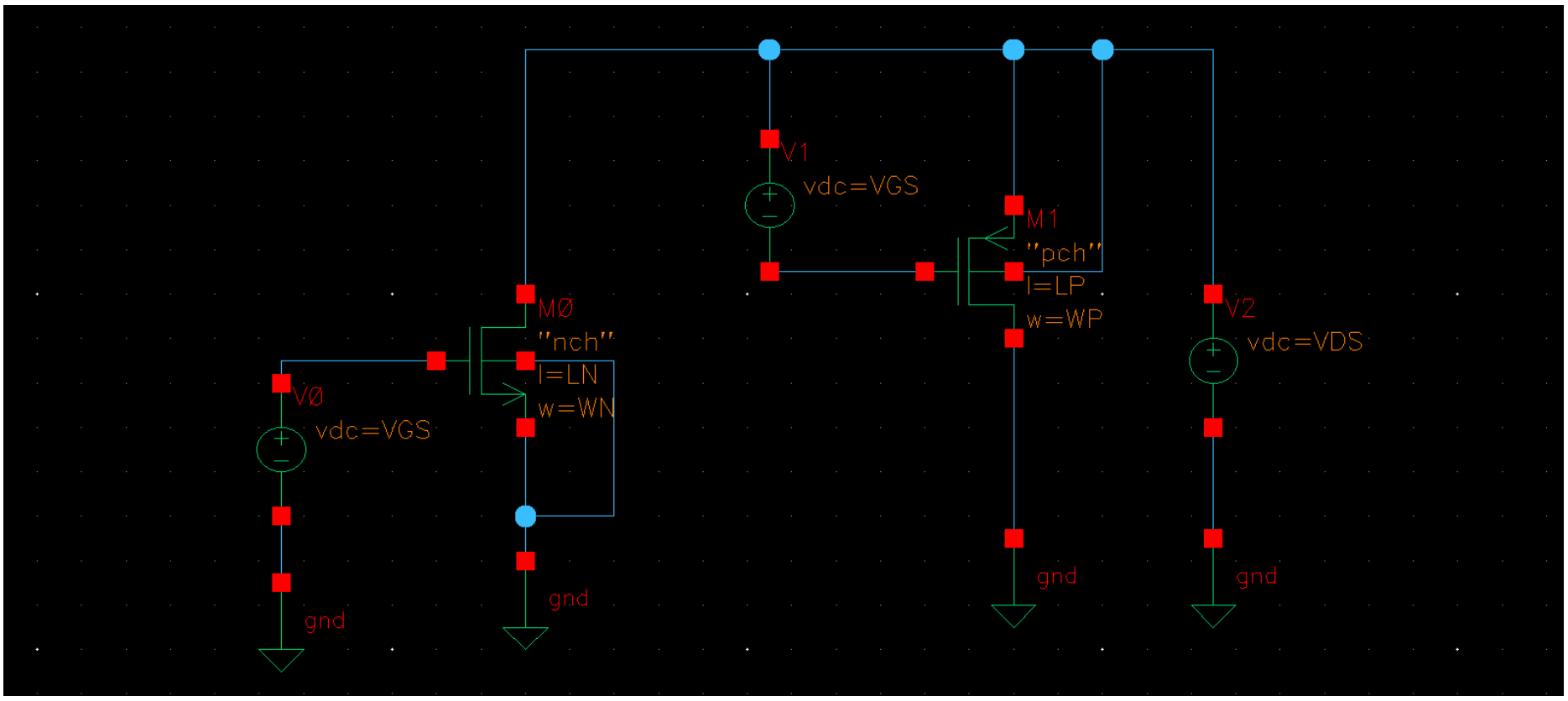
LAB 2

PART 1 (Sizing chart):

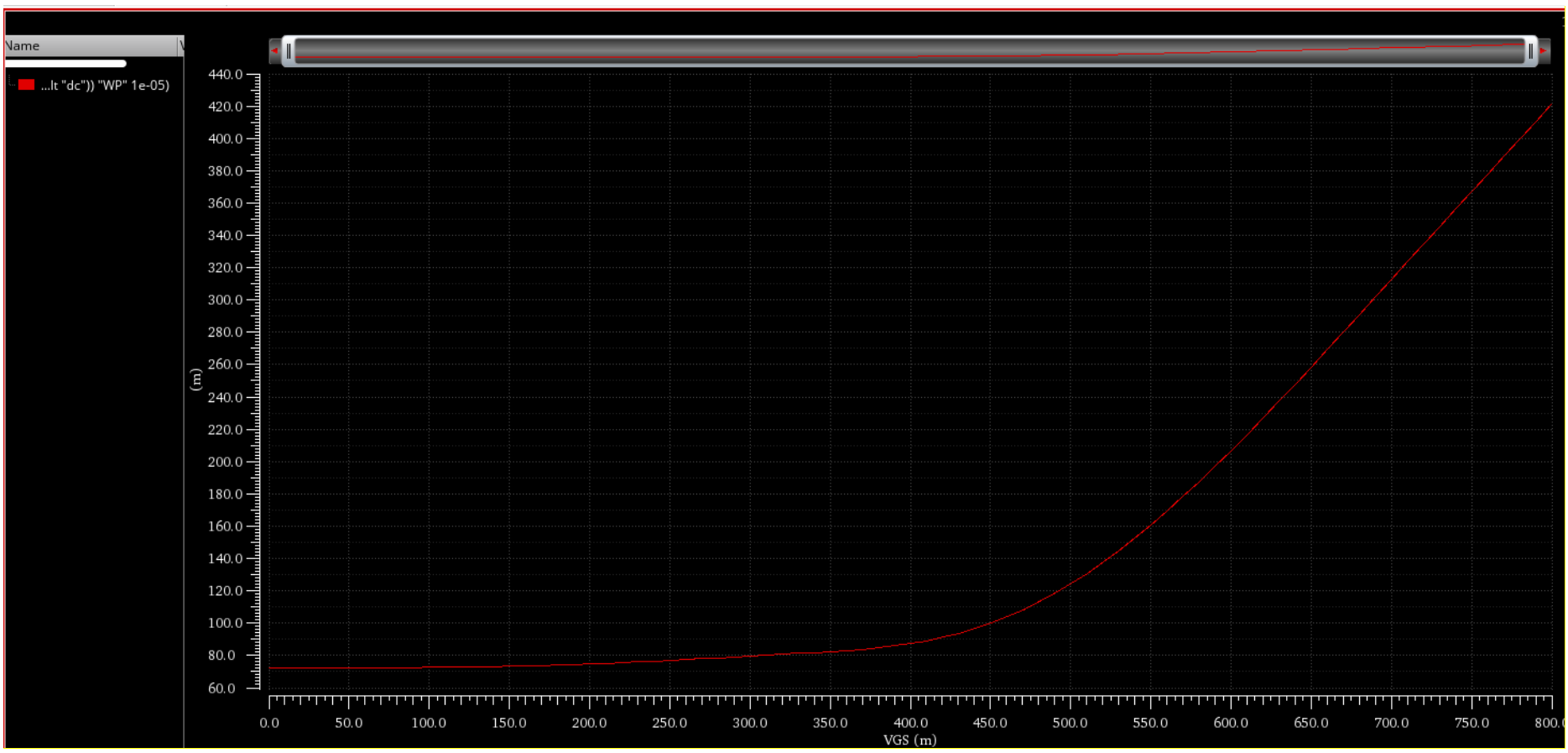
Circuit:



//comments:

- To design a resistive loaded CS amplifier that meets our specifications. The design process involves selecting the sizing of the transistor (W and L), the bias point (VGS), and the resistive load (RD).
- A relatively long L is chosen to provide large ro and avoid short channel effects.

V* plot:

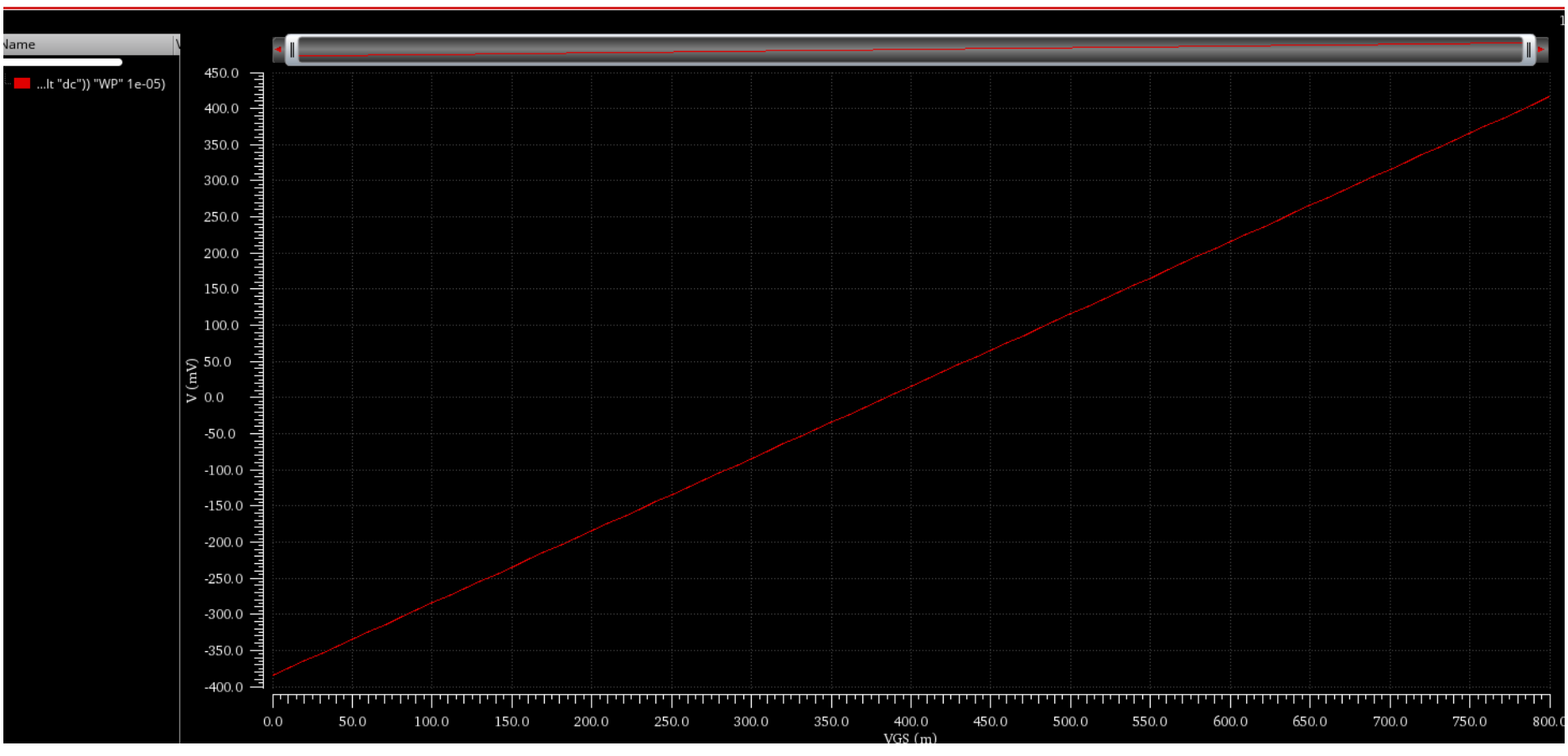


//comments:

First, a DC analysis is made and VGS is swept from 0 to vth+0.4(0.8) with a step size equal to 10m V.

V* = 2*ID/gm, so v* is plotted by sending the ID and gm to the calculator to get their expressions then v* equation is built.

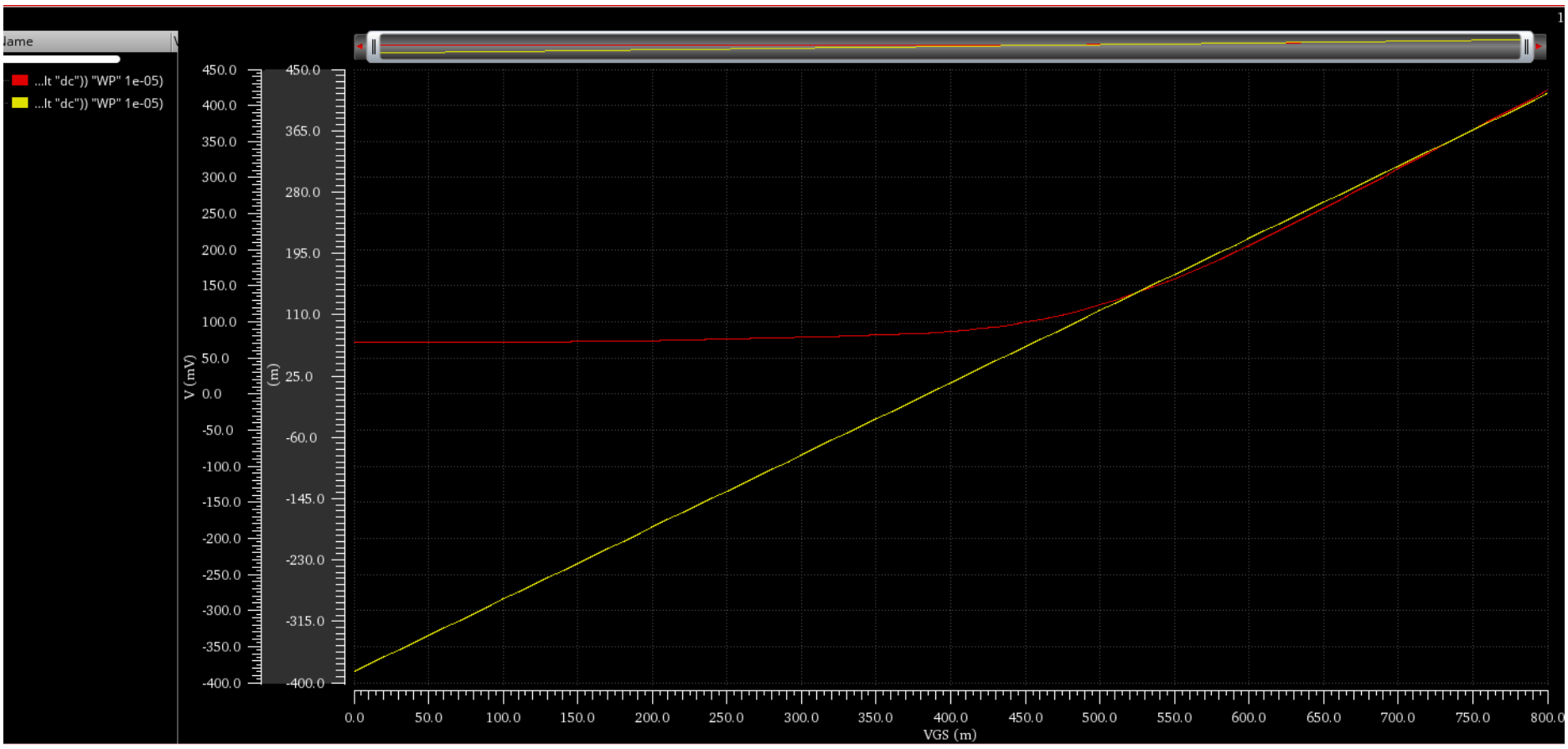
Vov plot:



//comments:

Vov = Vgs-Vth, so Vov is plotted by sending Vgs and Vth to that calculator to get their expressions, then Vov is plotted.

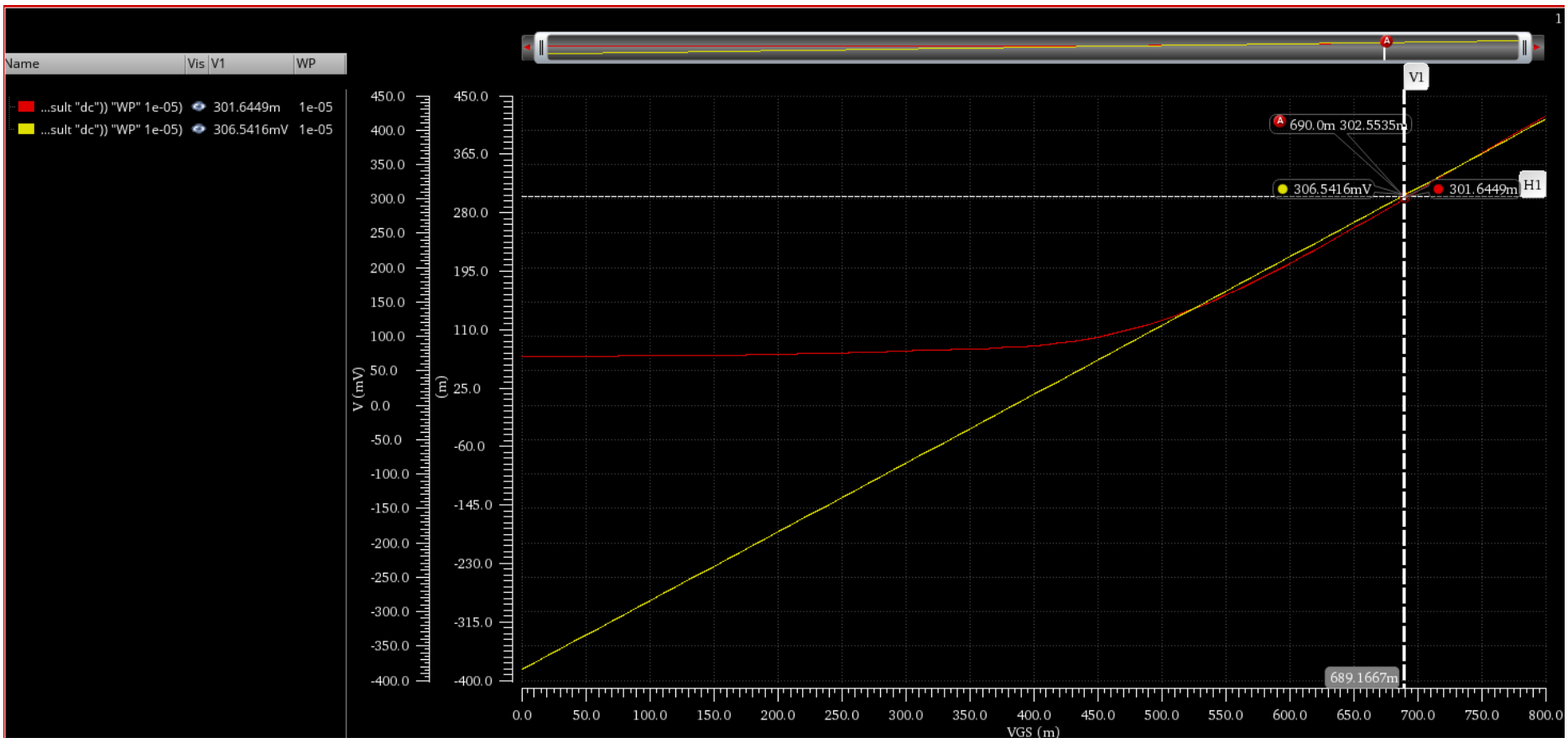
V* and Vov plot (after modifying the Y-axis):



//comments:

- The Y-axis constraints were modified to have the same range.
- From the plotting, it is clear that before the subthreshold operation as we go down the threshold value it is found that the deviation is large between the V* & Vov.
- And they are very close at the moderate values (moderate inversion) which is between subthreshold and under saturation.
- In saturation there is discrepancy as the device is still short channel, but this discrepancy is somehow acceptable.
- Generally, in real VDsat of a transistor the curve of V* and Vov will be closer than this.
- And, You will notice that at the beginning of the strong inversion region, $V*$ and Vov are relatively close to each other (i.e., square-law is relatively valid). For deep strong inversion (large Vov: velocity saturation and mobility degradation) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law (although we are using $L = 2\mu m$).
- Since, V*Q = 2Vrd/Av, Vrd = Vdd/2 →Then, V*Q = 2*0.9/6 = 300m V.

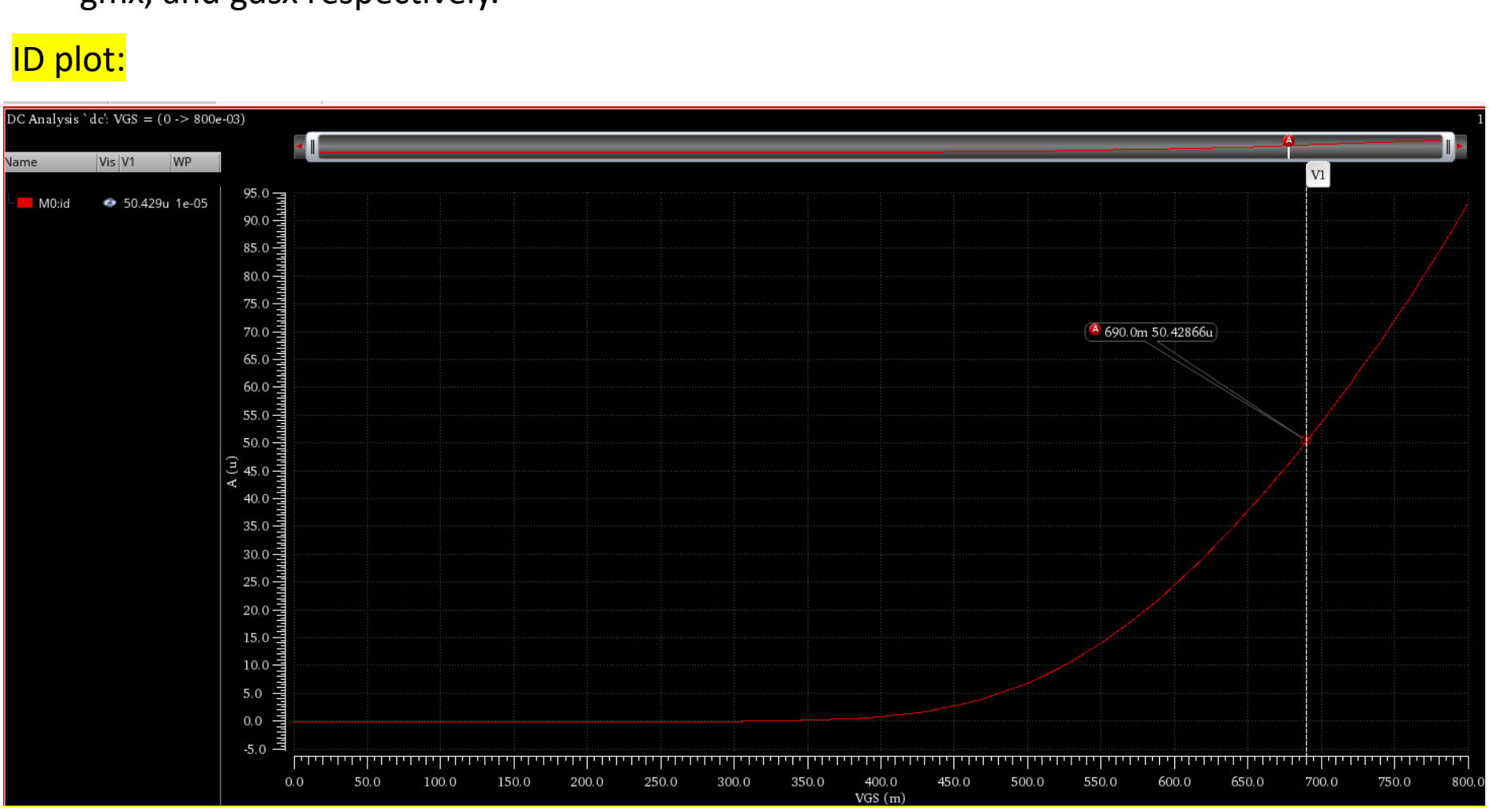
VgsQ and VovQ conclusion from the (V*-Vov) plot:



//comments:

- Then, VgsQ = 689m V & VovQ = 307m V & V*Q = 300m V{calculated in the previous page}.
- Then, we get the values of Id, gm and gds at the VgsQ (689m V) and will be named IDx, gmx, and gdsx respectively.

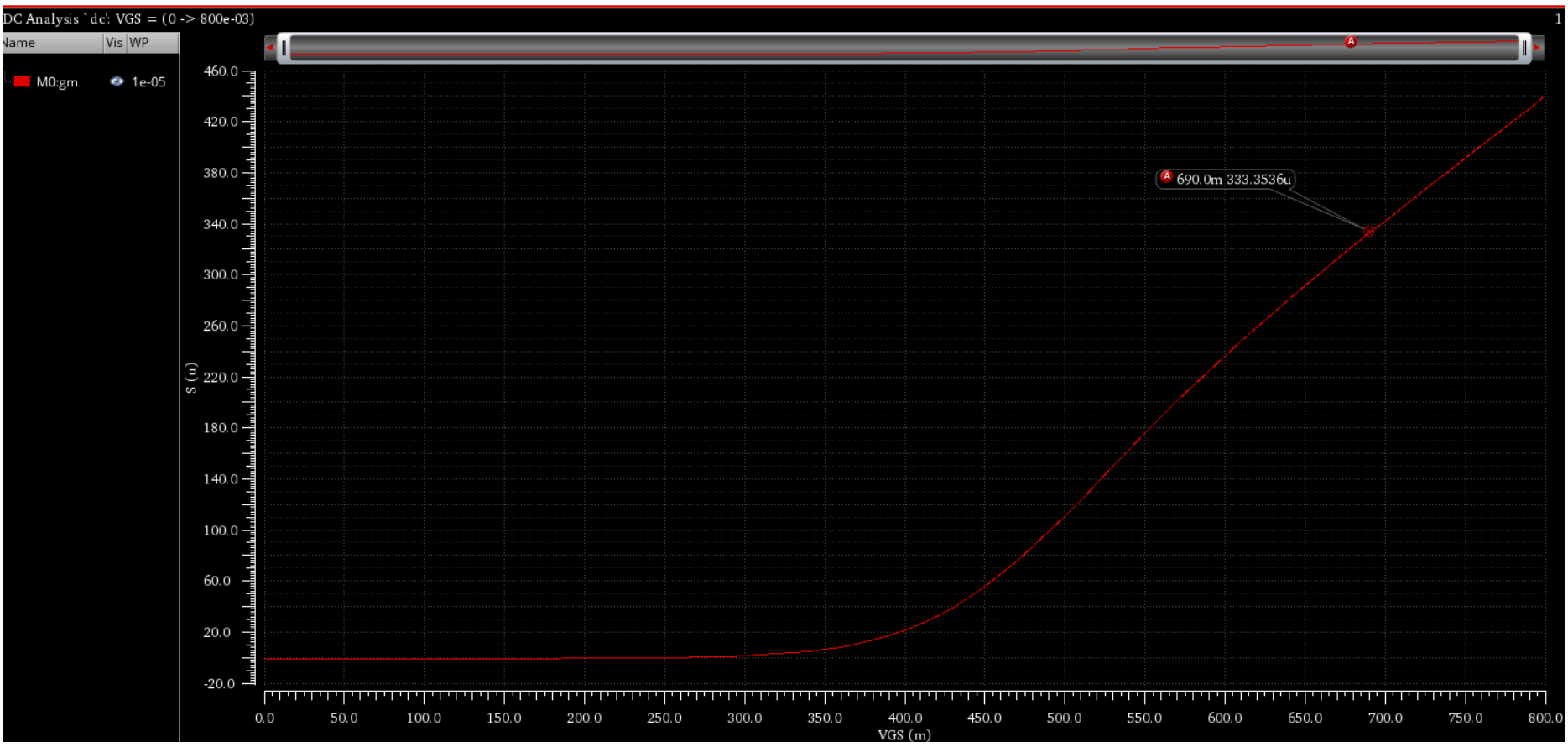
ID plot:



//comments:

- Then, IDx = 50.5u A
- There is difference between required Id and Idx due to linearity between device width and current, so a simple scaling is done to get the actual width _ *in the next pages*

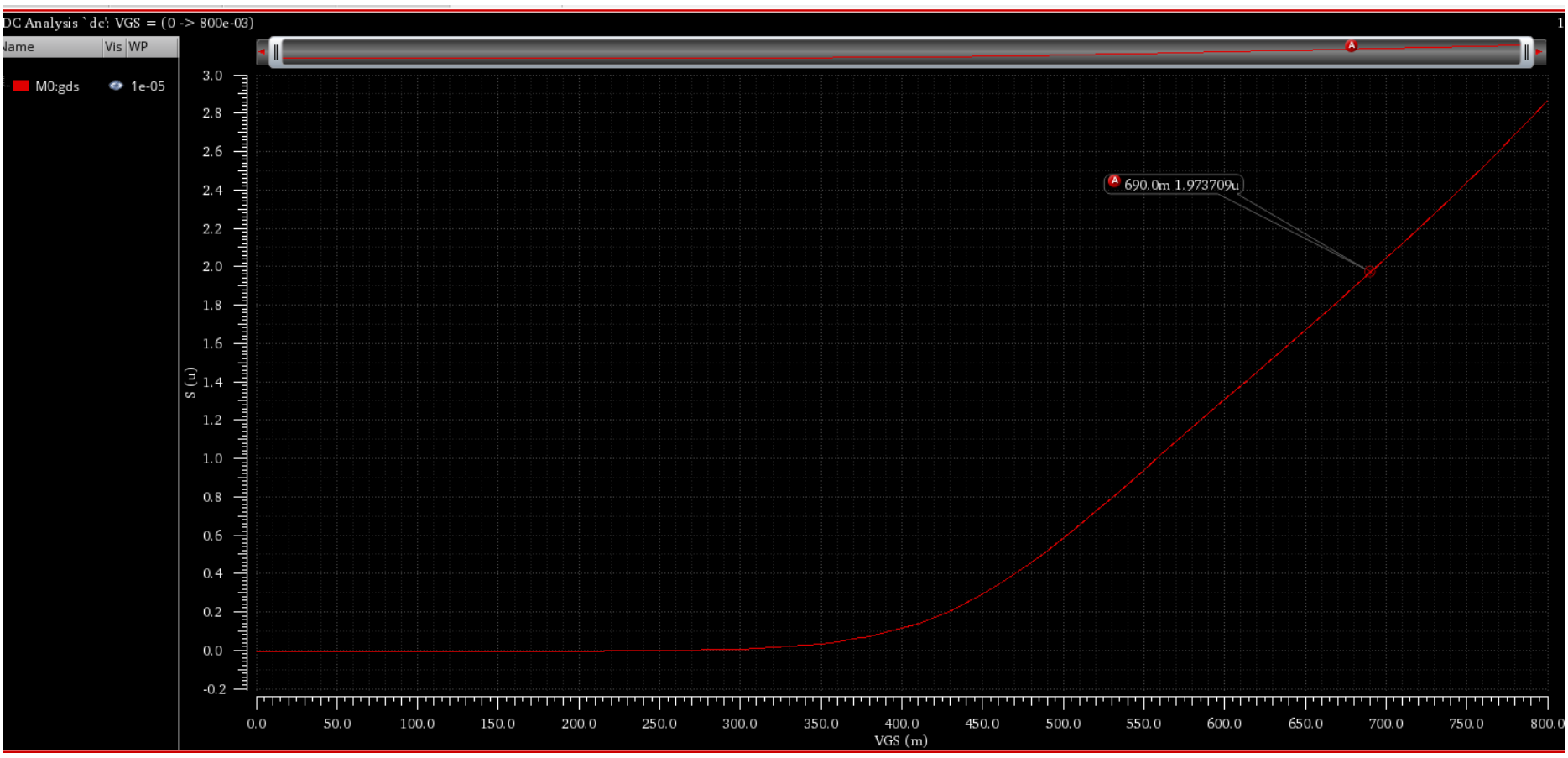
gm plot:



//comments:

- Then, gmx = 333.3536u

gds plot:



//comments:

- Then, gdsx = 1.973707u

//comments:

- Now back to the assumption that we made that W = 10μm. This is not the actual value that we will use for our design. But the good news is that ID is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be IDQ = 150μA as given in the specs So we Calculate W as shown below.
- Then actual width = 29.7u
- And by using the cross-multiplication method again we get:

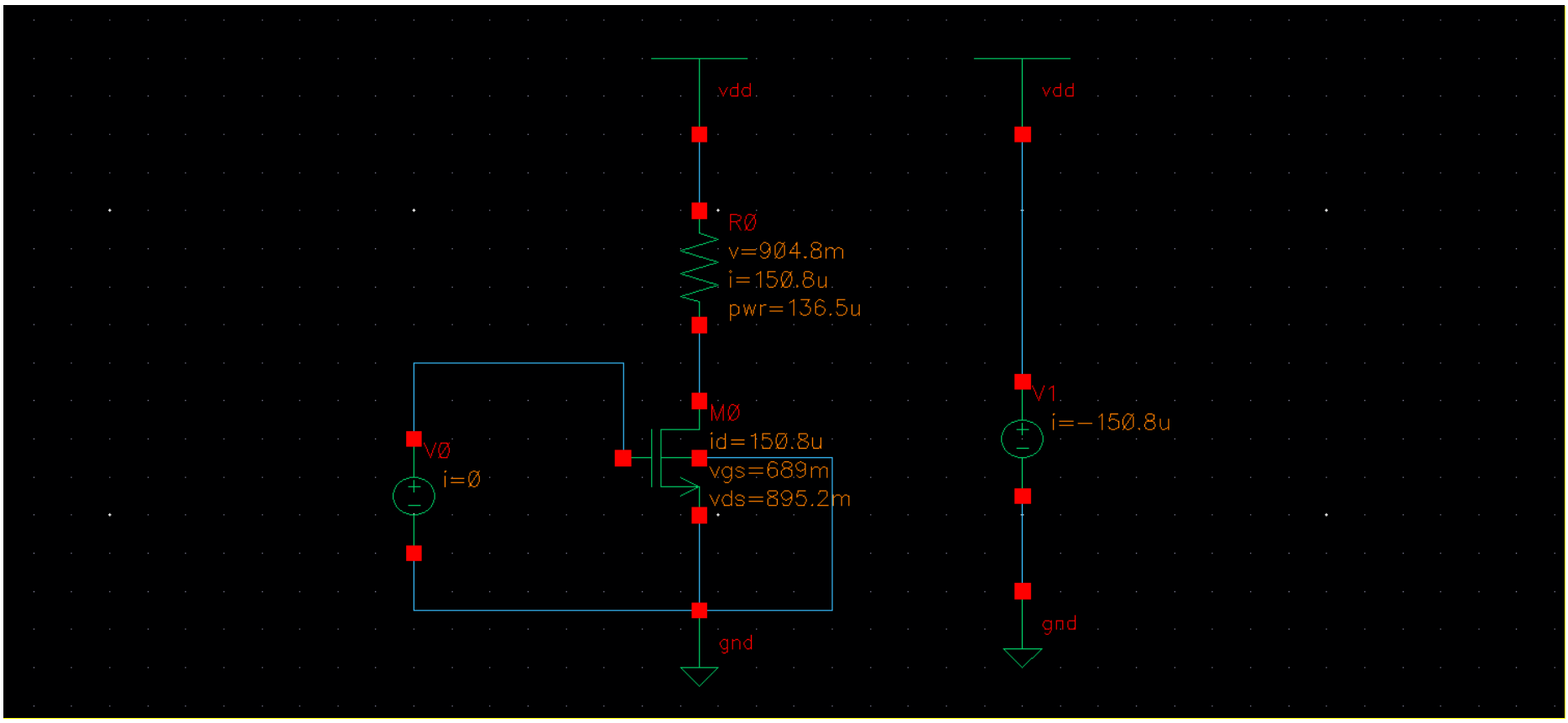
➢ gmq = 992.12u
➢ gdsq = 5.874u
➢ roq = 1/gdsq = 1.7*10^5 Ω

- Then, Av = $-gm(RD||ro)$ meet the required gain spec.

PART 2 (CS amplifier):

1st: OP & AC analysis

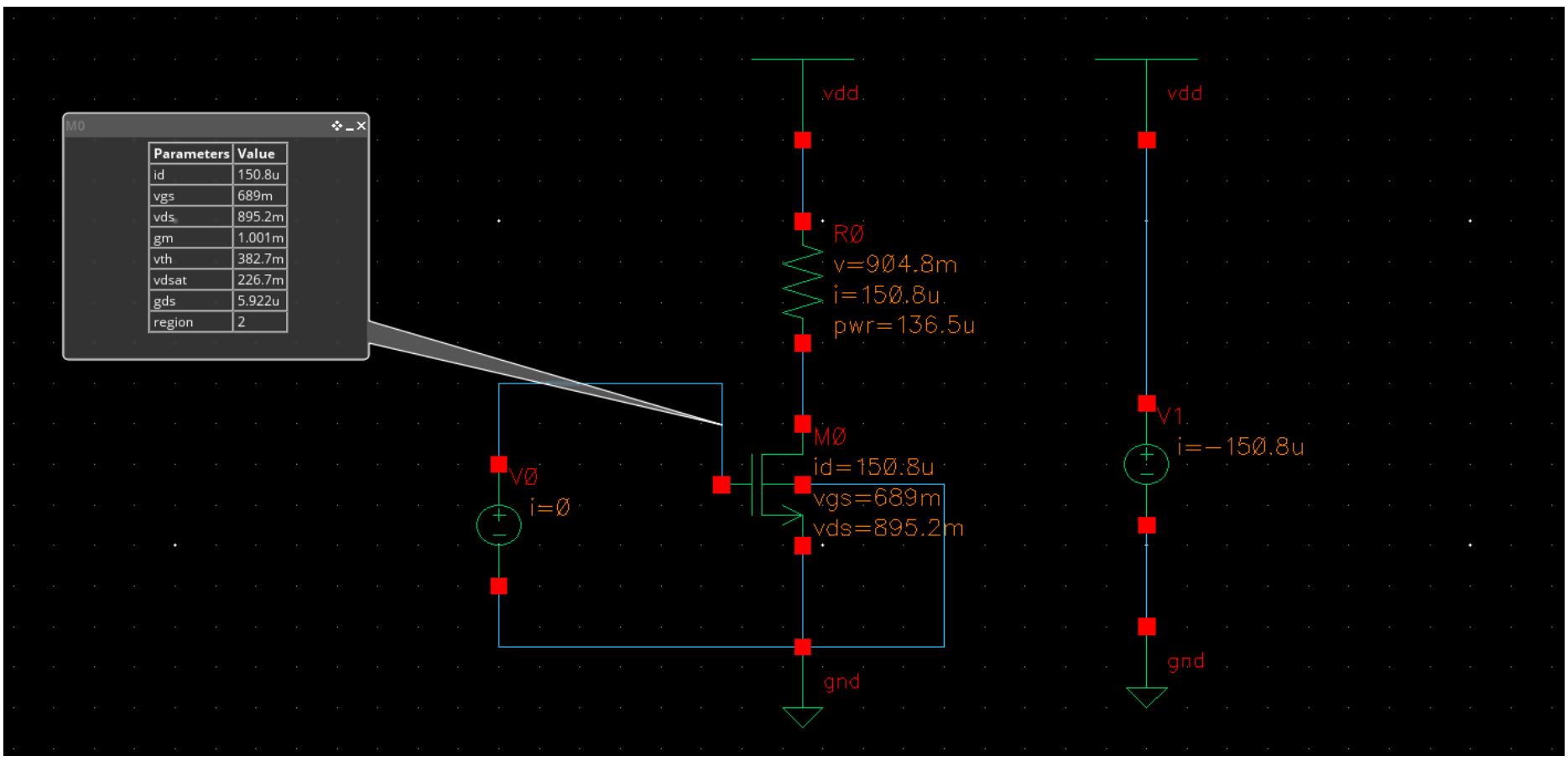
circuit:



//comments:

- A testbench is created for the resistive loaded amplifier using VgsQ, Rd, L and W that we get from the previous part.
- Since Rd = Vrd/Id then Rd = 6k Ω _*other variables are calculated before*

DC OP:



//comments:

- Results are pretty similar to that we used before in chart-based design.

//follow comments on DC OP results:

- Since that we got VDsat = 226.7m V and V* = 300m V, Then this shows how the V* put a safety margin on the expected value of the VDsat.
- Since gm scale is linear with Width, then gm of new device almost have the same scale of the old one.
- Gds scale decreases with the same factor the id scale increases with.
- Then, the design is almost on point.

//comments:

- Since ro = 1/gds ≈ 1/6u ≈ 166.6k Ω , Then very large value in the Q range
- Then ro >> Rd (6k Ω), Then approximation is justified and assumption of ignoring ro is justified and error value is not to be considered.
- If we used min L → the assumption will not be justified as when L decreases, then the output resistance decreases.

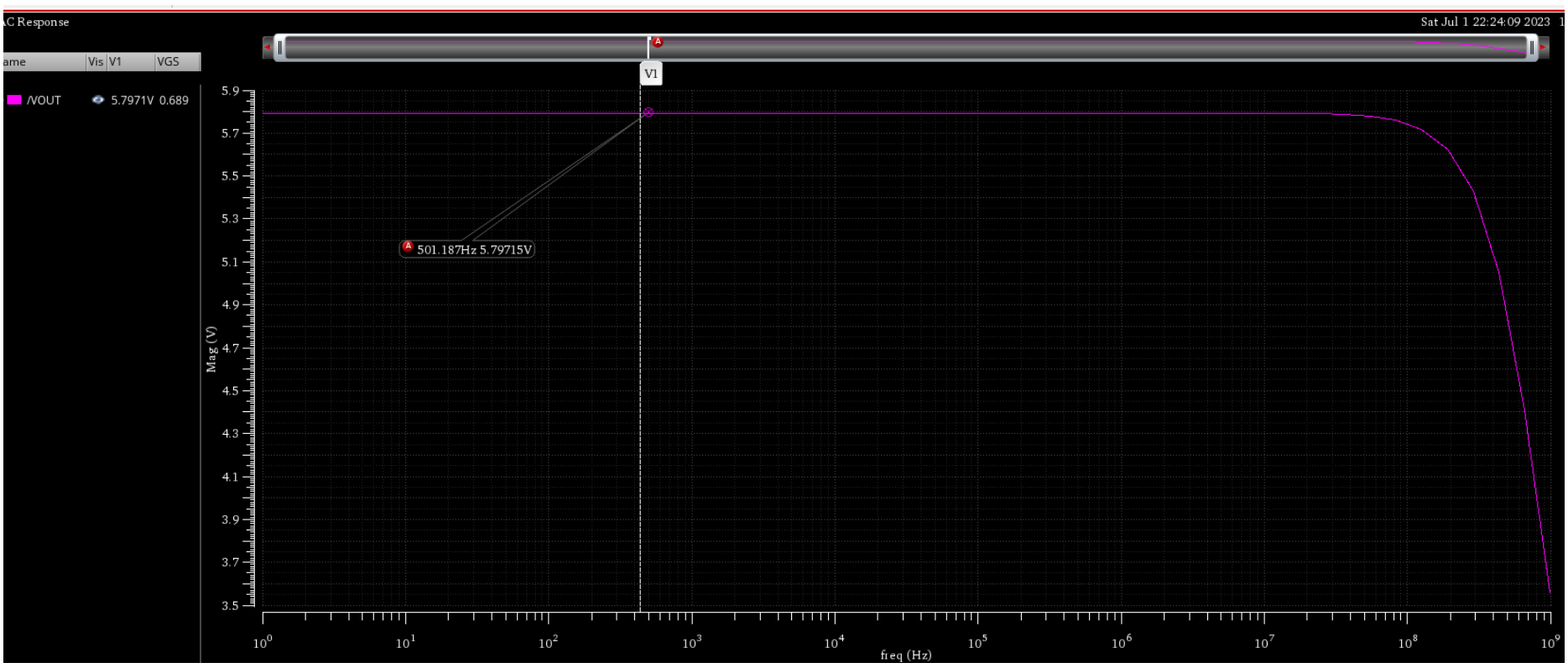
//comments:

- Intrinsic gain is when CS device is loaded with current source or loaded in AC with open load (NO load).
- Intrinsic gain = gm/gds = 1m/6u = 166.6
- Intrinsic gain is the highest gain I can reach.

//comments:

- Amplifier gain ≈ $-gm*Rd = -10^{-3} *10^{3} *6=-6$
- Then intrinsic gain >> amplifier gain.

AC analysis(gain vs frequency):

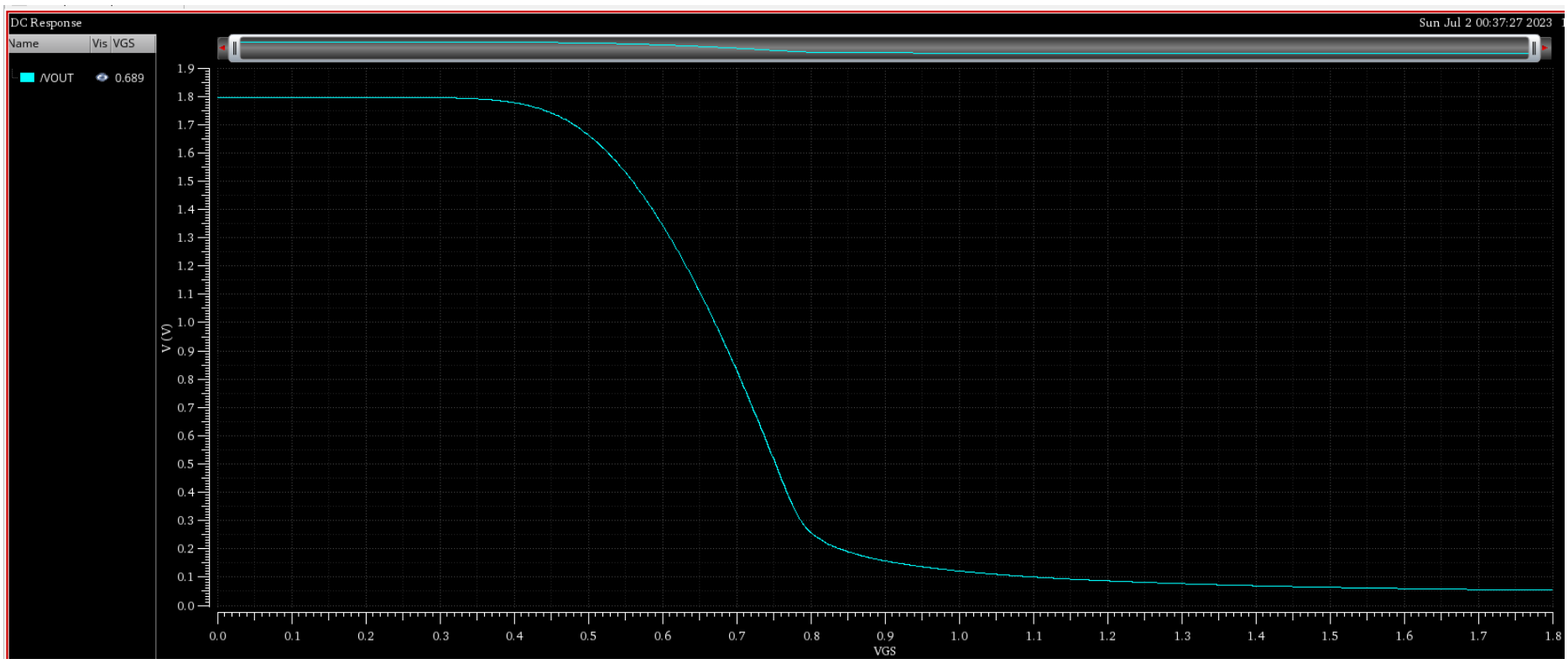


//comments:

- An AC analysis is done from 1hz to 1G hz .
- We out the vin = 1 then the gain equal the Vout.
- From the graph the DC gain is almost 6 then it meets the specs.

2nd: gain Non-linearity:

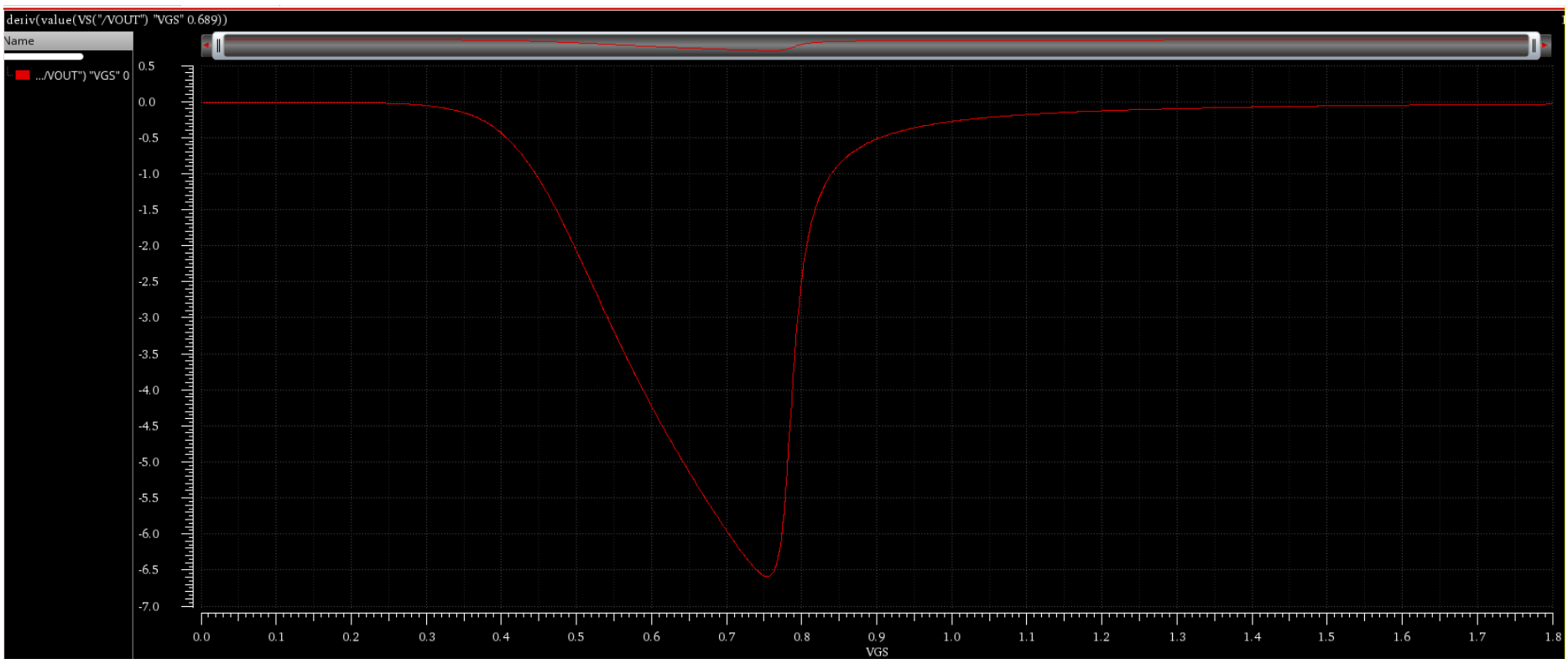
Vout vs Vin:



//comments:

- A DC analysis is made to sweep for the input voltage from 0 to VDD with a 2m V step size.
- Relation is not linear.
- It is obvious that the inverter characteristics that is present in any inverting stage.
- Then gain non-linearity is obvious.
- It starts quadratically with large Vds then the device is saturated.
- Then Vds starts to decrease gradually.
- Then device is in triode and acts as a resistor.
- Then gain expression is a function in Vin.

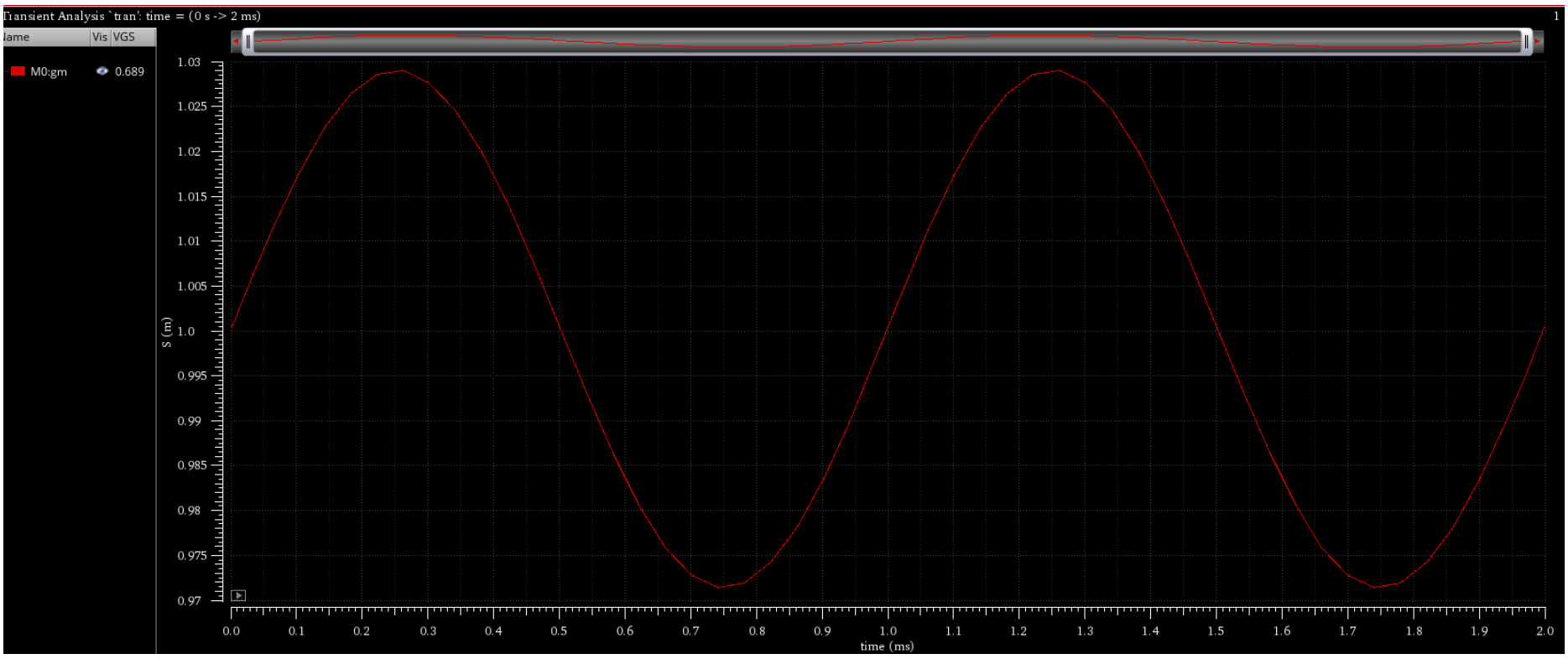
Vout derivative vs Vin:



//comments:

- The Vout is sent to the calculator to get its derivative.
- It starts with no gain.
- Then nonlinear relation.
- In derive curve it appears that at first the gain increases as if it is linearly till it reaches a value near to the -6.5, then device goes in triode region.
- One of the problems of this technology is that the gain depends on the Vrd as Rd increases, I sacrifice with the swing, and I go to swing clipping occurs and goes to triode.

Gm vs time:



//comments:

- the properties of the voltage source to apply a transient stimulus is set (sine wave of 1kHz frequency and 10mV amplitude superimposed on the DC input voltage).
- Then a transient analysis is done for 2 ms.
- It is obvious that gm varies with the input signal.
- Which means that this is a non linear relation.

//comments:

- The amplifier is not linear as gm varies with the input signal, and variation in input changes the bias points.