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Synchronous FIFO

SV project

FIFO design before modification has 3 Bugs which are:

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|--|
| Underflow is designed to be combinational |
| Almostfull is assigned to be (FIFO_depth-2) |
| Reset doesn't clear all the sequential flags |

Verification plan:

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|---|
| Randomize input data and pass randomized values to object from FIFO_transaction class |
| Then that object will be passed to two parallel threads (using fork join) → sample function and check data function |
| Check data will compare the DUT and reference objects |
| Reference function will be built |
| If the data is correct, contents of the queue will be displayed and correct_count ++ |
| Else, an error message will be displayed and error_count++ |
| A test_finished signal is asserted in the Testbench |
| If test_finished signal == 1, then simulation stops |

RTL design with bugs:

```
FIFO_project > fifo_beforeeeeeee.sv
1 //////////////////////////////////////////////////////////////////////////////////////////////////////////////////
2 // Author: Kareem Waseem
3 // Course: Digital Verification using SV & UVM
4 //
5 // Description: FIFO Design ===== with bugs =====
6 //
7 //////////////////////////////////////////////////////////////////////////////////////////////////////////////////
8 module FIFO(FIFO_if.fifo_dut interface_object);
9 // parameter interface_object.FIFO_WIDTH = 16;
10 // parameter interface_object.FIFO_DEPTH = 8;
11 // input [interface_object.FIFO_WIDTH-1:0] interface_object.data_in;
12 // input interface_object.clk, interface_object.rst_n, interface_object.wr_en, interface_object.rd_en;
13 // output reg [interface_object.FIFO_WIDTH-1:0] interface_object.data_out;
14 // output reg interface_object.wr_ack, interface_object.overflow;
15 // output interface_object.full, interface_object.empty, almostinterface_object.full, almostempty, underflow;
16
17 localparam max_fifo_addr = $clog2(interface_object.FIFO_DEPTH);
18
19 reg [interface_object.FIFO_WIDTH-1:0] mem [interface_object.FIFO_DEPTH-1:0];
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21 reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
22 reg [max_fifo_addr:0] count;
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```

```

100 property p6;
101 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (count == interface_object.FIFO_DEPTH) |-> interface_object.full ;
102 endproperty
103 full_assertion : assert property(p6);
104 full_cover : cover property(p6);
105
106 property p7;
107 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (count == 0) |-> interface_object.empty ;
108 endproperty
109 empty_assertion : assert property(p7);
110 empty_cover : cover property(p7);
111
112 property p8;
113 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (count == interface_object.FIFO_DEPTH-1) |-> interface_object.almostfull ;
114 endproperty
115 almostfull_assertion : assert property(p8);
116 almostfull_cover : cover property(p8);
117
118 property p9;
119 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (count == 1) |-> interface_object.almostempty ;
120 endproperty
121 almostempty_assertion : assert property(p9);
122 almostempty_cover : cover property(p9);
123
124 //endif
125
126 endmodule

```

Coverage ➔ with bugs:

//the full coverage report will be found in the .rar file

```

FIFO_project > fcover_report.txt
1 Coverage Report by instance with details
2
3 =====
4 === Instance: /FIFO_coverage_pkg
5 === Design Unit: work.FIFO_coverage_pkg
6 =====
7
8 Group Coverage:
9   Covergroups          1      na      na      85.20%
10  Coverpoints/Crosses  16      na      na      na
11  Covergroup Bins      56      47      9      83.92%
12 =====

```

```

FIFO_project > fifocoveragereport.txt
1 Coverage Report by instance with details
2
3 =====
4 === Instance: /\TOP /interface_object
5 === Design Unit: work.FIFO_if
6 =====
7
8 Toggle Coverage:
9   Enabled Coverage      Bins      Hits      Misses      Coverage
10  -----
11  Toggles                86      84      2      97.67%

```

Questa snippets ➔ with bugs

error counter ==> 141, correct counter ==> 11

| Name | Assertion Type | Language | Enable | Failure Count | Pass Count | Active Count | Memory | Peak Memory | Peak Memory Time | Cumulative Threads | ATV | Assertion Expression | Included |
|----------------------|----------------|----------|--------|---------------|------------|--------------|--------|-------------|------------------|--------------------|-----|--------------------------------------|----------|
| TOP/rfo_dut/writ... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@(posedge interface_objec... | ✓ |
| TOP/rfo_dut/over... | Concurrent | SVA | on | 52 | 0 | - | 0B | 0B | 0 ns | 0 | off | assert(@(posedge interface_objec... | ✓ |
| TOP/rfo_dut/incre... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@(posedge interface_objec... | ✓ |
| TOP/rfo_dut/decr... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@(posedge interface_objec... | ✓ |
| TOP/rfo_dut/full... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@(posedge interface_objec... | ✓ |
| TOP/rfo_dut/emp... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@(posedge interface_objec... | ✓ |
| TOP/rfo_dut/alm... | Concurrent | SVA | on | 12 | 0 | - | 0B | 0B | 0 ns | 0 | off | assert(@(posedge interface_objec... | ✓ |
| TOP/rfo_testbech... | Immediate | SVA | on | 0 | 1 | - | - | - | - | - | off | assert(randomize(...)) | ✓ |
| TOP/rfo_testbech... | Immediate | SVA | on | 0 | 1 | - | - | - | - | - | off | assert(randomize(...)) | ✓ |
| TOP/rfo_testbech... | Immediate | SVA | on | 0 | 1 | - | - | - | - | - | off | assert(randomize(...)) | ✓ |

After fixing the bugs:

Top module:

```
FIFO_project > top.v
1  module TOP;
2      bit clk;
3      initial begin
4          clk = 0;
5          forever begin
6              #50 clk = ~clk;
7          end
8      end
9      FIFO_if interface_object(clk);
10     FIFO_fifo_dut (interface_object);
11     FIFO_tb fifo_testbench (interface_object);
12     FIFO_monitor fifo_monitor (interface_object);
13 endmodule
```

RTL design after fixing the bugs:

```
FIFO_project > fifo_rtl_noBugs.v
1  module FIFO(FIFO_if, fifo_dut interface_object);
2
3      // declaration of max. FIFO address
4      localparam max_fifo_addr = $clog2(interface_object.FIFO_DEPTH); // max_fifo_addr = 3
5
6      // declaration of Memory (FIFO)
7      reg [interface_object.FIFO_WIDTH-1:0] mem [interface_object.FIFO_DEPTH-1:0];
8
9      // Declaration of read & write pointers
10     reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
11     reg [max_fifo_addr:0] count; // extra bit to distinguish between full & empty flags & it represents the fill level of the FIFO
12
13     // always block specialized for writing operation
14     always @(posedge interface_object.clk or negedge interface_object.rst_n) begin
15         if (!interface_object.rst_n) begin
16             wr_ptr <= 0;
17             interface_object.overflow <= 0;
18             interface_object.wr_ack <= 0; // reset the sequential outputs as wr_ack , overflow
19         end
20         else if (interface_object.wr_en && count < interface_object.FIFO_DEPTH) begin
21             mem[wr_ptr] <= interface_object.data_in;
22             interface_object.wr_ack <= 1;
23             wr_ptr <= wr_ptr + 1;
24         end
25         else begin
26             interface_object.wr_ack <= 0;
27             if (interface_object.full && interface_object.wr_en)
28                 interface_object.overflow <= 1;
29             else
30                 interface_object.overflow <= 0;
31         end
32     end
33 end
```

```
34     // always block specialized for reading operation
35     always @(posedge interface_object.clk or negedge interface_object.rst_n) begin
36         if (!interface_object.rst_n) begin
37             rd_ptr <= 0;
38             interface_object.underflow <= 0;
39             interface_object.data_out <= 0; // reset the sequential outputs as data_out , underflow
40         end
41         else if (interface_object.rd_en && count != 0) begin
42             interface_object.data_out <= mem[rd_ptr];
43             rd_ptr <= rd_ptr + 1;
44         end
45         else begin
46             if(interface_object.empty && interface_object.rd_en)
47                 interface_object.underflow <= 1;
48             else
49                 interface_object.underflow <= 0;
50         end
51     end
52 end
53
```

```

54 // always block specialized for counter signal
55 always @(posedge interface_object.clk or negedge interface_object.rst_n) begin
56     if (!interface_object.rst_n) begin
57         count <= 0;
58     end
59     else begin
60         if ( (interface_object.wr_en, interface_object.rd_en) == 2'b10) && !interface_object.full)
61             count <= count + 1;
62         else if ( (interface_object.wr_en, interface_object.rd_en) == 2'b01) && !interface_object.empty)
63             count <= count - 1;
64         else if ((interface_object.wr_en, interface_object.rd_en) == 2'b11) && interface_object.full) // priority for write operation
65             count <= count - 1;
66         else if ((interface_object.wr_en, interface_object.rd_en) == 2'b11) && interface_object.empty) // priority for read operation
67             count <= count + 1;
68     end
69 end

```

```

70
71 // continous assignment for the combinational outputs
72 assign interface_object.full = (count == interface_object.FIFO_DEPTH)? 1 : 0;
73 assign interface_object.empty = (count == 0)? 1 : 0;
74 assign interface_object.almostfull = (count == interface_object.FIFO_DEPTH-1)? 1 : 0;
75 assign interface_object.almostempty = (count == 1)? 1 : 0;
76

```

```

88 property p1;
89 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (interface_object.wr_en && !interface_object.full) |>= interface_object.wr_ack ;
90 endproperty
91 write_acknowledge : assert property(p1);
92 write_acknowledge_cover : cover property(p1);
93
94 property p2;
95 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (interface_object.empty && interface_object.rd_en) |>= interface_object.underflow ;
96 endproperty
97 underflow_assertion : assert property(p2);
98 underflow_cover : cover property(p2);
99
100 property p3;
101 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (interface_object.full & interface_object.wr_en) |>= interface_object.overflow ;
102 endproperty
103 overflow_assertion : assert property(p3);
104 overflow_cover : cover property(p3);
105
106 property p4;
107 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (!interface_object.full & interface_object.wr_en & !interface_object.rd_en) |>= (count == $past(count) + 4'b0001) ;
108 endproperty
109 increment_assertion : assert property(p4);
110 increment_cover : cover property(p4);
111
112 property p5;
113 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (!interface_object.empty && interface_object.rd_en && !interface_object.wr_en) |>= (count == $past(count) - 4'b0001) ;
114 endproperty
115 decrement_assertion : assert property(p5);
116 decrement_cover : cover property(p5);
117
118 property p6;
119 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (count == interface_object.FIFO_DEPTH) |>= interface_object.full ;
120 endproperty
121 full_assertion : assert property(p6);
122 full_cover : cover property(p6);
123

```

```

124 property p7;
125 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (count == 0) |>= interface_object.empty ;
126 endproperty
127 empty_assertion : assert property(p7);
128 empty_cover : cover property(p7);
129
130 property p8;
131 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (count == interface_object.FIFO_DEPTH-1) |>= interface_object.almostfull ;
132 endproperty
133 almostfull_assertion : assert property(p8);
134 almostfull_cover : cover property(p8);
135
136 property p9;
137 @(posedge interface_object.clk) disable iff(!interface_object.rst_n) (count == 1) |>= interface_object.almostempty ;
138 endproperty
139 almostempty_assertion : assert property(p9);
140 almostempty_cover : cover property(p9);
141
142 //endif
143
144 endmodule

```

Package 1:

```
FIFO_project > ≡ pkg_1.sv
1 package FIFO_transaction_pkg; //pkg_1
2 class FIFO_transaction;
3 //parameters:
4 parameter FIFO_WIDTH = 16;
5 parameter FIFO_DEPTH = 8;
6 //inputs
7 rand bit [FIFO_WIDTH-1:0]data_in;
8 rand bit rst_n, wr_en, rd_en;
9 //outputs
10 logic [FIFO_WIDTH-1:0]data_out;
11 logic wr_ack, overflow, full, empty, almostfull, almostempty, underflow;
12 //the 2 integers WR_EN_ON_DIST and RD_EN_ON_DIST
13 int WR_EN_ON_DIST = 70;
14 int RD_EN_ON_DIST = 30;
15
16 //constraint rst
17 constraint constrained_rst{ rst_n dist{0:/1, 1:/99}; }
18
19 //constraint write and read as required
20 constraint constrained_write{ wr_en dist{0:/(100-WR_EN_ON_DIST), 1:/WR_EN_ON_DIST}; }
21 constraint constrained_read{ rd_en dist{0:/(100-RD_EN_ON_DIST), 1:/RD_EN_ON_DIST}; }
22
23 //additional constraints =====> write_only and read_only
24 constraint write_only{ rst_n == 1; rd_en == 1; wr_en == 1;}
25 constraint read_only{ rst_n == 1; rd_en == 1; wr_en == 0;}
26
27 endclass
28 endpackage
```

Package 2:

```
FIFO_project > ≡ pkg_2.sv
1 package FIFO_coverage_pkg;
2 //import the prev pkg(FIFO_transaction_pkg)
3 import FIFO_transaction_pkg::*;
4
5 class FIFO_coverage;
6 //object from the FIFO_transaction class
7 FIFO_transaction F_cvg_txn = new();
8 //function with no return value
9 function void sample_data (input FIFO_transaction F_txn);
10 F_cvg_txn = F_txn;
11 cover_group.sample();
12 endfunction
13
14 covergroup cover_group;
15 //coverpoints to be used in the cross coverage
16 //the coverage needed is cross coverage between 3 signals which are write enable, read enable and each output control signals
17 //except outputs except data_out
18 //wr_ack, overflow, full, empty, almostfull, almostempty, underflow
19 wr_en_cover_point:coverpoint F_cvg_txn.wr_en;
20 rd_en_cover_point:coverpoint F_cvg_txn.rd_en;
21 wr_ack_cover_point:coverpoint F_cvg_txn.wr_ack;
22 overflow_cover_point:coverpoint F_cvg_txn.overflow;
23 full_cover_point:coverpoint F_cvg_txn.full;
24 empty_cover_point:coverpoint F_cvg_txn.empty;
25 almostfull_cover_point:coverpoint F_cvg_txn.almostfull;
26 almostempty_cover_point:coverpoint F_cvg_txn.almostempty;
27 underflow_cover_point:coverpoint F_cvg_txn.underflow;
28 //cross coverage to make sure that all combinations of (write and read enable) took place
29 //in all state of the FIFO ==> with all o/p except d_out.
30 //then we make 7 cross coverages(7 outputs, each o/p individually with both the wr_en and rd_en)
31 //since, all coverpoints are 1 bit the bins will have only two states 0 or 1
32 //bin(1) will be the high state
33
34 wr_en_rd_en_wr_ack:cross wr_en_cover_point, rd_en_cover_point, wr_ack_cover_point {
35 ignore_bins wr_en_low_wr_ack_high = !binsof(wr_en_cover_point) intersect(1) && binsof(wr_ack_cover_point) intersect(1);
36 ignore_bins read_write_active_with_wr_ack = !binsof(wr_en_cover_point) intersect(1) && binsof(rd_en_cover_point) intersect(1) && binsof(wr_ack_cover_point) intersect(1);
37 }
38 wr_en_rd_en_overflow:cross wr_en_cover_point, rd_en_cover_point, overflow_cover_point {
39 ignore_bins wr_en_low_overflow_high = !binsof(wr_en_cover_point) intersect(1) && binsof(overflow_cover_point) intersect(1);
40 }
41 wr_en_rd_en_full:cross wr_en_cover_point, rd_en_cover_point, full_cover_point {
42 ignore_bins wr_en_low_full_high = !binsof(wr_en_cover_point) intersect(1) && binsof(full_cover_point) intersect(1);
43 ignore_bins rd_en_high_full_high = binsof(rd_en_cover_point) intersect(1) && binsof(full_cover_point) intersect(1);
44 }
45 wr_en_rd_en_empty:cross wr_en_cover_point, rd_en_cover_point, empty_cover_point{
46 ignore_bins rd_en_low_empty_high = !binsof(rd_en_cover_point) intersect(1) && binsof(empty_cover_point) intersect(1);
47 ignore_bins wr_en_low_empty_high = !binsof(wr_en_cover_point) intersect(1) && binsof(empty_cover_point) intersect(1);
48 }
49 wr_en_rd_en_almostfull:cross wr_en_cover_point, rd_en_cover_point, almostfull_cover_point{
50 ignore_bins wr_en_low_almostfull_high = !binsof(wr_en_cover_point) intersect(1) && binsof(almostfull_cover_point) intersect(1);
51 }
52 wr_en_rd_en_almostempty:cross wr_en_cover_point, rd_en_cover_point, almostempty_cover_point{
53 ignore_bins rd_en_low_almostempty_high = !binsof(rd_en_cover_point) intersect(1) && binsof(almostempty_cover_point) intersect(1);
54 ignore_bins wr_en_low_rd_en_high_almostempty_high = !binsof(wr_en_cover_point) intersect(1) && binsof(rd_en_cover_point) intersect(1) && binsof(almostempty_cover_point) intersect(1);
55 }
56 wr_en_rd_en_underflow:cross wr_en_cover_point, rd_en_cover_point, underflow_cover_point {
57 ignore_bins rd_en_low_underflow_high = !binsof(rd_en_cover_point) intersect(1) && binsof(underflow_cover_point) intersect(1);
58 ignore_bins wr_en_high_underflow_high = !binsof(wr_en_cover_point) intersect(1) && binsof(underflow_cover_point) intersect(1);
59 }
60 endgroup
61
62 function new();
63 cover_group = new();
64 //F_cvg_txn = new();
65 endfunction
66 endclass
67 endpackage
68
```

Package 3:

```
FIFO_project > pkg3.sv
1  package FIFO_scoreboard_pkg;
2      //import the prev pkg(FIFO_transaction_pkg)
3      import FIFO_transaction_pkg ::*;
4      //import the shared pkg
5      import shared_pkg ::*;
6
7      class FIFO_scoreboard;
8          //parameters:
9          parameter FIFO_WIDTH = 16;
10         parameter FIFO_DEPTH = 8;
11         //outputs
12         bit [FIFO_WIDTH-1:0] data_out_ref;
13         bit wr_ack_ref, overflow_ref, full_ref, empty_ref, almostfull_ref, almostempty_ref, underflow_ref;
14
15         //counter that will be used in determining full, empty, almostfull, almostempty in the queue
16         int counter;
17         bit [FIFO_WIDTH-1:0] fifo[$]; // $ ==> means that this is a dynamic array which can be modified during runtime
18         //object from the FIFO_transaction class
19         FIFO_transaction dut_object = new();
20         //function to assign the combinational outputs of type void
21         //full, empty, almostfull, almostempty ==> the reference model
22         function void combinational_outputs();
23             full_ref = (counter == FIFO_DEPTH)? 1:0;
24             empty_ref = (counter == 0)? 1:0;
25             almostfull_ref = (counter == FIFO_DEPTH-1)? 1:0;
26             almostempty_ref = (counter == 1)? 1:0;
27         endfunction
```

```
29
30     //check data function to compare the dut and ref models
31     function void check_data(input FIFO_transaction dut_object);
32
33         //for simplicity in comparing dut and ref , the flags are concatenated
34         logic[6:0] dut_flags;
35         logic[6:0] ref_flags;
36
37         reference_model(dut_object);
38         //wr_ack_ref, overflow_ref, full_ref, empty_ref, almostfull_ref, almostempty_ref, underflow_ref
39         dut_flags = {dut_object.wr_ack, dut_object.overflow, dut_object.full, dut_object.empty, dut_object.almostfull, dut_object.almostempty, dut_object.underflow};
40         ref_flags = {wr_ack_ref, overflow_ref, full_ref, empty_ref, almostfull_ref, almostempty_ref, underflow_ref};
41         if ((dut_object.data_out != data_out_ref) || (dut_flags != ref_flags)) begin
42             $display("DUT is NOT EQUAL REF AT TIME = %t", $time);
43             error_count++;
44         end
45     else begin
46         correct_count++;
47         $display("WELL DONE, The FIFO = %p", fifo);
48     end
49 endfunction
```

```
50     //reference model function with type void
51     function reference_model(input FIFO_transaction ref_object);
52         //fork join will be used to make read and write occur in parallel and then in Join counter will be updated
53         fork
54             begin
55                 //write operation
56                 if (!ref_object.rst_n) begin
57                     wr_ack_ref = 0;
58                     //data_out_ref = 0;
59                     overflow_ref = 0;
60                     full_ref = 0;
61                     //empty_ref = 1; //rst will not clear the fifo contents
62                     almostfull_ref = 0;
63                     //almostempty_ref = 0;
64                     //underflow_ref = 0;
65                     fifo.delete();
66                 end
67                 else if (ref_object.wr_en && counter < ref_object.FIFO_DEPTH) begin
68                     wr_ack_ref = 1;
69                     fifo.push_back(ref_object.data_in);
70                 end
71                 else begin
72                     wr_ack_ref = 0;
73                     if (ref_object.wr_en && full_ref) overflow_ref = 1;
74                     else overflow_ref = 0;
75                 end
76             end //end write
77         begin
78             //read operation
79             if (!ref_object.rst_n) begin
80                 //wr_ack_ref = 0;
81                 data_out_ref = 0;
82                 //overflow_ref = 0;
83                 //full_ref = 0;
84                 empty_ref = 1; //rst will not clear the fifo contents
85                 //almostfull_ref = 0;
86                 almostempty_ref = 0;
87                 underflow_ref = 0;
88                 //fifo.delete();
89             end
90             else if (ref_object.rd_en && counter != 0)
91                 data_out_ref = fifo.pop_front();
92             else begin
93                 if (ref_object.rd_en && empty_ref) underflow_ref = 1;
94                 else underflow_ref = 0;
95             end
96         end
```

```
97     join
98         if (!ref_object.rst_n) counter = 0;
99
100     //counter will be updated, after the read and write operations took place
101     //it will be updated depending on the states of the fifo
102
103     else if (ref_object.wr_en && !ref_object.rd_en && !full_ref) counter++; //write
104     else if (!ref_object.wr_en && ref_object.rd_en && !empty_ref) counter--; //read
105     else if (ref_object.wr_en && ref_object.rd_en && full_ref) counter--; //read as the fifo is full
106     else if (ref_object.wr_en && ref_object.rd_en && empty_ref) counter++; //write as the fifo is empty
107
108     //to update the combinational
109     combinational_outputs();
110 endfunction
111 endclass
```

Package 4:

```
FIFO_project > ≡ pkg_4.sv
1  package shared_pkg;
2      int error_count, correct_count;
3      bit test_finished;
4  endpackage
```

Interface:

```
FIFO_project > ≡ interface.sv
1  interface FIFO_if(clk);
2      input bit clk;
3      //interface includes all ports
4
5      //parameters:
6      parameter FIFO_WIDTH = 16;
7      parameter FIFO_DEPTH = 8;
8      //inputs
9      logic [FIFO_WIDTH-1:0]data_in;
10     logic rst_n, wr_en, rd_en;
11     //outputs
12     logic [FIFO_WIDTH-1:0]data_out;
13     logic wr_ack, overflow, full, empty, almostfull, almostempty, underflow;
14     //modport dut
15     modport fifo_dut (
16         input clk, data_in, rst_n, wr_en, rd_en,
17         output data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow
18     );
19     //modport tb=>
20     modport fifo_testbench (
21         input clk, data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow,
22         output data_in, rst_n, wr_en, rd_en
23     );
24     //modport monitor=>
25     modport fifoMonitor (input clk, data_in, rst_n, wr_en, rd_en, data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow);
26
27
28
29 endinterface
```

Monitor:

```
FIFO_project > ≡ monitor.sv
1  import FIFO_transaction_pkg ::*;
2  import FIFO_scoreboard_pkg ::*;
3  import FIFO_coverage_pkg ::*;
4  import shared_pkg ::*;
5
6  module FIFO_monitor(FIFO_if.fifoMonitor interface_object);
7      //object from each class
8      FIFO_transaction trans_object;
9      FIFO_scoreboard score_object;
10     FIFO_coverage cove_object;
11     initial begin
12         trans_object = new();
13         score_object = new();
14         cove_object = new();
15         forever begin
16             @(negedge interface_object.clk); //interface clk
17             //sample the data of the interface and assign it to the data of the object of class FIFO_transaction
18             //data_in, wr_en, rd_en, rst_n, full, empty, almostfull, almostempty, wr_ack, overflow, underflow, data_out
19             trans_object.data_in = interface_object.data_in;
20             trans_object.wr_en = interface_object.wr_en;
21             trans_object.rd_en = interface_object.rd_en;
22             trans_object.rst_n = interface_object.rst_n;
23             trans_object.full = interface_object.full;
24             trans_object.empty = interface_object.empty;
25             trans_object.almostfull = interface_object.almostfull;
26             trans_object.almostempty = interface_object.almostempty;
27             trans_object.wr_ack = interface_object.wr_ack;
28             trans_object.overflow = interface_object.overflow;
29             trans_object.underflow = interface_object.underflow;
30             trans_object.data_out = interface_object.data_out;
```

```
31
32         fork
33             begin //first one is calling a method named sample_data of the object of class FIFO_coverage
34                 cove_object.sample_data(trans_object);
35             end
36             begin //second process is calling a method named check_data of the object of class FIFO_scoreboard
37                 @(posedge interface_object.clk) //checking should happen at the posedge
38                 //delay of 20 ms to gaurantee that the o/p is changed at the posedge before checking
39                 #20;
40                 score_object.check_data(trans_object);
41             end
42         join
43         if(test_finished) begin
44             $display("final values are ==> %p", score_object.fifo);
45             $display("error counter ==> %d, correct counter ==> %d", error_count, correct_count);
46             $stop;
47         end
48     end
49 end
50 endmodule
```


Testbench:

```
FIFO_project > testbench.v
1  import FIFO_transaction_pkg ::*;
2  // import FIFO_scoreboard_pkg ::*;
3  // import FIFO_coverage_pkg ::*;
4  import shared_pkg ::*;
5  module FIFO_tb (FIFO_if.fifo_testbench interface_object);
6      //create an object from the fifo_transaction class to randomize
       FIFO_transaction tb_object;
7      initial begin
8          tb_object = new();
9
10         interface_object.rst_n = 0;
11         @(negedge interface_object.clk);
12         @(negedge interface_object.clk);
13         //check write only, disable all constraints except that of write_only
14         interface_object.rst_n = 1;
15         tb_object.constraint_mode(0);
16         tb_object.write_only.constraint_mode(1);
17         //randomize inputs ==> data_in, wr_en, rd_en, rst_n
18         repeat(50)begin
19             assert(tb_object.randomize());
20             interface_object.data_in = tb_object.data_in;
21             interface_object.wr_en = tb_object.wr_en;
22             interface_object.rd_en = tb_object.rd_en;
23             interface_object.rst_n = tb_object.rst_n;
24             @(negedge interface_object.clk);
25         end
26     end
end
```

```

27 //check read only, disable all constarints except that of read_only
28 tb_object.constraint_mode(0);
29 tb_object.read_only.constraint_mode(1);
30 repeat(50)begin
31     assert(tb_object.randomize());
32     interface_object.data_in = tb_object.data_in;
33     interface_object.wr_en = tb_object.wr_en;
34     interface_object.rd_en = tb_object.rd_en;
35     interface_object.rst_n = tb_object.rst_n;
36 end
37
38
39 //check for write and read , disable constarints  of read_only and write_only and enable others
40 tb_object.constraint_mode(1);
41 tb_object.write_only.constraint_mode(0);
42 tb_object.read_only.constraint_mode(0);
43 repeat(100)begin
44     assert(tb_object.randomize());
45     interface_object.data_in = tb_object.data_in;
46     interface_object.wr_en = tb_object.wr_en;
47     interface_object.rd_en = tb_object.rd_en;
48     interface_object.rst_n = tb_object.rst_n;
49     @(negedge interface_object.clk);
50 end
51 //At the end of the test, the tb will assert a signal named test_finished
52 test_finished = 1;
53 end
54 endmodule

```

Do file:

```
FIFO_project > run_FIFO.do
1 vlog -f src_files.list -mfcu +define+SIM +cover
2 vsim -voptargs+=acc work.TOP -cover
3 add wave *
4 coverage save fifocoveragereport.ucdb -onexit -du work.TOP
5 run -all
6 coverage report -detail -cvg -directive -comments -output fcover_report.txt /FIFO_coverage_pkg/FIFO_coverage/cover_group
7 #quit -sim
8 vcover report fifocoveragereport.ucdb -details -annotate -all -output fifocoveragereport.txt
9
```

Src files.list:

```
FIFO_project > src_files.list
1  pkg_4.sv
2  pkg_1.sv
3  pkg_2.sv
4  pkg_3.sv
5  fifo_rtl_noBug
6  interface.sv
7  monitor.sv
8  testbench.sv
9  top.sv
```

Some of Questa snippets:

```
# error counter ==>          0, correct counter ==>          152

# WELL DONE, The FIFO = '{51082, 29829, 37721}'
# WELL DONE, The FIFO = '{51082, 29829, 37721, 20300}'
# WELL DONE, The FIFO = '{51082, 29829, 37721, 20300}'
# WELL DONE, The FIFO = '{51082, 29829, 37721, 20300, 17834}'
# WELL DONE, The FIFO = '{51082, 29829, 37721, 20300, 17834, 63099}'
# WELL DONE, The FIFO = '{51082, 29829, 37721, 20300, 17834, 63099}'
# WELL DONE, The FIFO = '{51082, 29829, 37721, 20300, 17834, 63099}'
# WELL DONE, The FIFO = '{29829, 37721, 20300, 17834, 63099, 35717}'
# WELL DONE, The FIFO = '{29829, 37721, 20300, 17834, 63099, 35717, 47571}'
# WELL DONE, The FIFO = '{29829, 37721, 20300, 17834, 63099, 35717, 47571}'
# WELL DONE, The FIFO = '{29829, 37721, 20300, 17834, 63099, 35717, 47571}'
# WELL DONE, The FIFO = '{29829, 37721, 20300, 17834, 63099, 35717, 47571, 44223}'
# WELL DONE, The FIFO = '{37721, 20300, 17834, 63099, 35717, 47571, 44223}'
# WELL DONE, The FIFO = '{37721, 20300, 17834, 63099, 35717, 47571, 44223, 41132}'
# WELL DONE, The FIFO = '{37721, 20300, 17834, 63099, 35717, 47571, 44223, 41132}'
# WELL DONE, The FIFO = '{37721, 20300, 17834, 63099, 35717, 47571, 44223, 41132}'
# WELL DONE, The FIFO = '{20300, 17834, 63099, 35717, 47571, 44223, 41132}'
# WELL DONE, The FIFO = '{20300, 17834, 63099, 35717, 47571, 44223, 41132, 61290}'
# WELL DONE, The FIFO = '{20300, 17834, 63099, 35717, 47571, 44223, 41132, 61290}'
# WELL DONE, The FIFO = '{20300, 17834, 63099, 35717, 47571, 44223, 41132, 61290}'

# WELL DONE, The FIFO = '{31950}'
# WELL DONE, The FIFO = '{54164}'
# WELL DONE, The FIFO = '{61019}'
# WELL DONE, The FIFO = '{37750}'
# WELL DONE, The FIFO = '{23018}'
# WELL DONE, The FIFO = '{56936}'
# WELL DONE, The FIFO = '{19112}'
# WELL DONE, The FIFO = '{30214}'
# WELL DONE, The FIFO = '{29687}'
# WELL DONE, The FIFO = '{55586}'
# WELL DONE, The FIFO = '{52846}'
# WELL DONE, The FIFO = '{54785}'
# WELL DONE, The FIFO = '{18859}'
# WELL DONE, The FIFO = '{38847}'
# WELL DONE, The FIFO = '{36683}'
```

| Assertions | | | | | | | | | | | | | |
|------------------------|----------------|----------|--------|---------------|------------|--------------|--------|-------------|------------------|--------------------|-----|-------------------------------------|----------|
| Name | Assertion Type | Language | Enable | Failure Count | Pass Count | Active Count | Memory | Peak Memory | Peak Memory Time | Cumulative Threads | ATV | Assertion Expression | Included |
| TOP/ffifo_dut/writ... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@posedge interface_objec... | ✓ |
| TOP/ffifo_dut/und... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@posedge interface_objec... | ✓ |
| TOP/ffifo_dut/over... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@posedge interface_objec... | ✓ |
| TOP/ffifo_dut/incre... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@posedge interface_objec... | ✓ |
| TOP/ffifo_dut/decr... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@posedge interface_objec... | ✓ |
| TOP/ffifo_dut/full... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@posedge interface_objec... | ✓ |
| TOP/ffifo_dut/emp... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@posedge interface_objec... | ✓ |
| TOP/ffifo_dut/almo... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@posedge interface_objec... | ✓ |
| TOP/ffifo_dut/almo... | Concurrent | SVA | on | 0 | 1 | - | 0B | 0B | 0 ns | 0 | off | assert(@posedge interface_objec... | ✓ |
| TOP/ffifo_testbech... | Immediate | SVA | on | 0 | 1 | - | - | - | - | - | off | assert (randomize(...)) | ✓ |
| TOP/ffifo_testbech... | Immediate | SVA | on | 0 | 1 | - | - | - | - | - | off | assert (randomize(...)) | ✓ |
| TOP/ffifo_testbech... | Immediate | SVA | on | 0 | 1 | - | - | - | - | - | off | assert (randomize(...)) | ✓ |

Coverage: ➔ after fixing the bugs:

//the full code and functional coverage are included in the .rar file

//I failed to make the coverage 100%

```
FIFO_project > fcover_report.txt
1 Coverage Report by instance with details
2
3 =====
4 === Instance: /FIFO_coverage_pkg
5 === Design Unit: work.FIFO_coverage_pkg
6 =====
7
8 ▾ Covergroup Coverage:
9 ▾   Covergroups           1      na      na    98.75%
10 ▾   Coverpoints/Crosses  16      na      na      na
11   Covergroup Bins       56      55      1    98.21%
12
```

```
FIFO_project > fifocoveragereport.txt
1 Coverage Report by instance with details
2
3 =====
4 === Instance: /\TOP /interface_object
5 === Design Unit: work.FIFO_if
6 =====
7 Toggle Coverage:
8   Enabled Coverage      Bins      Hits      Misses  Coverage
9   -----
10  Toggles |              86       82        4    95.34%
11
```