8-bit ripple counter

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ECEN312: Analysis and Design of Digital Circuits

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Contents

Introduction

1. This report covers the design, implementation, and simulation of an 8-bit ripple counter using JK-Flipflops. The project is implemented in Cadence Virtuoso using CMOS transistors. The primary components utilized are 2-input NAND gates and 3-input NAND gates. Each JK-Flipflop is built from these basic gates.

Design and Implementation

JK-Flipflop Design

2. A JK-Flipflop is a fundamental sequential logic component that can be implemented using NAND gates. The JK-Flipflop has two inputs, J and K, and outputs Q and Q'. The flip-flop toggles its state based on the values of J and K.

Schematic of JK-Flipflop

1. **2-input NAND Gate**: Constructed using PMOS and NMOS transistors.
    - **PMOS Transistor**: Conducts when gate voltage is low.
    - **NMOS Transistor**: Conducts when gate voltage is high.
2. **3-input NAND Gate**: Similar construction but with three transistors in the pull-down network.

Ripple Counter Design

3. A ripple counter consists of multiple flip-flops connected in series, where the output of one flip-flop serves as the clock input for the next flip-flop.

Schematic of Ripple Counter

4. **Flip-Flop Connections**: The Q output of each flip-flop is connected to the clock input of the subsequent flip-flop.
5. **Input and Output**: The initial clock input drives the first flip-flop, and the outputs are taken from the Q outputs of each flip-flop.

CMOS Implementation

1. **PMOS Transistors**: Used in the pull-up network of NAND gates.
2. **NMOS Transistors**: Used in the pull-down network of NAND gates.
3. **NAND Gate Construction**: Each 2-input and 3-input NAND gate is built using a combination of PMOS and NMOS transistors.

Simulation

Simulation Setup

- **Tool**: Cadence Virtuoso
- **Parameters Measured**:
- **Propagation Delay**: Time taken for a signal to propagate through a flip-flop.
- **Power Consumption**: Average power consumed during operation.
- **Frequency Response**: Maximum operating frequency of the counter.

Ripple Counter

1. **Input Waveforms**: Clock signal with a specified frequency.

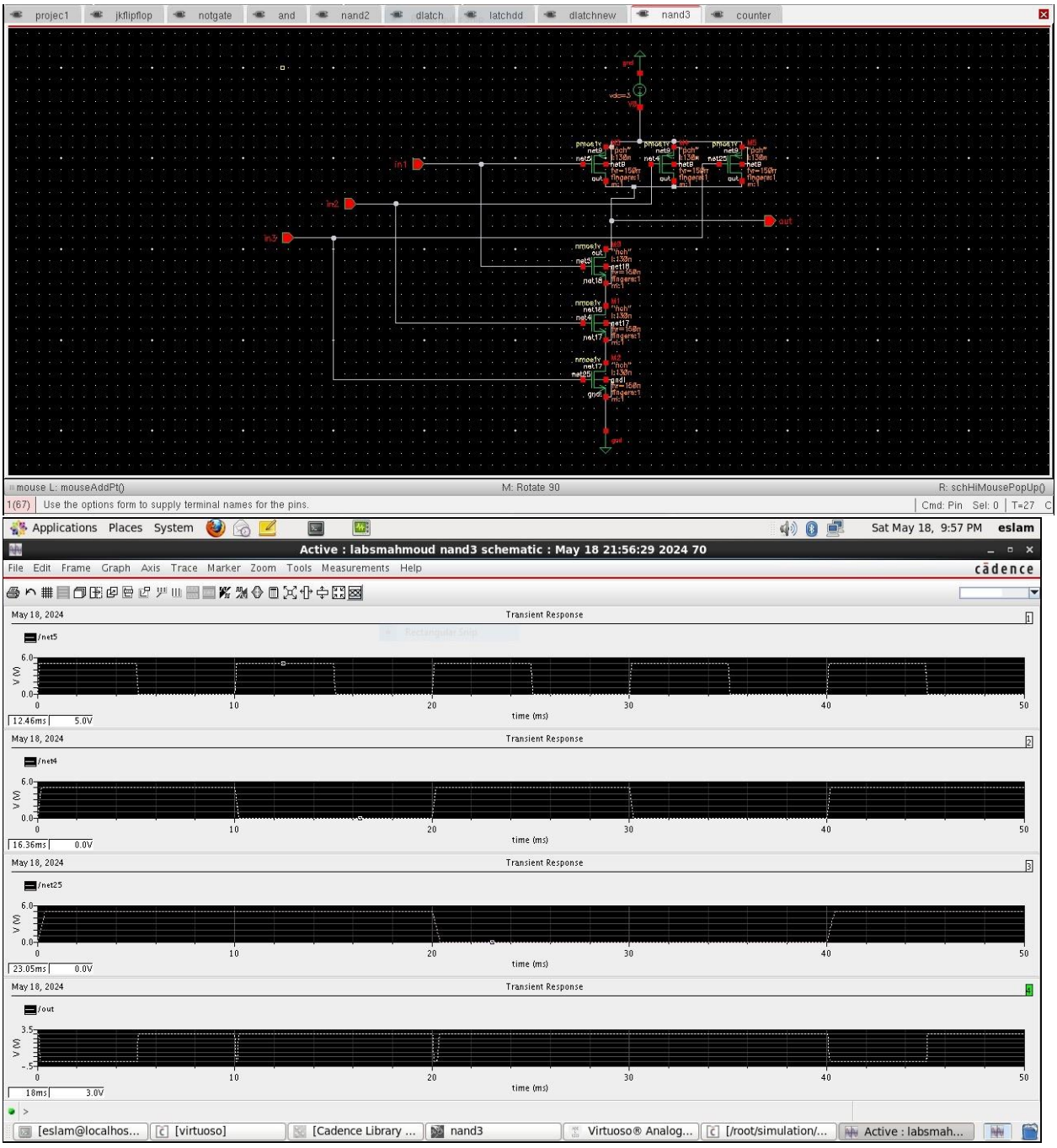
2. **Output Waveforms**: Outputs from each flip-flop are observed to verify the counting sequence.
3. **Efficiency Parameters**:
    - **Propagation Delay**: Measured for the entire counter from the clock input to the final output.
    - **Power Consumption**: Total power consumption of the 8-bit counter.
    - **Frequency Response**: Determined by varying the clock frequency and observing correct counting.

8-bit ripple counter

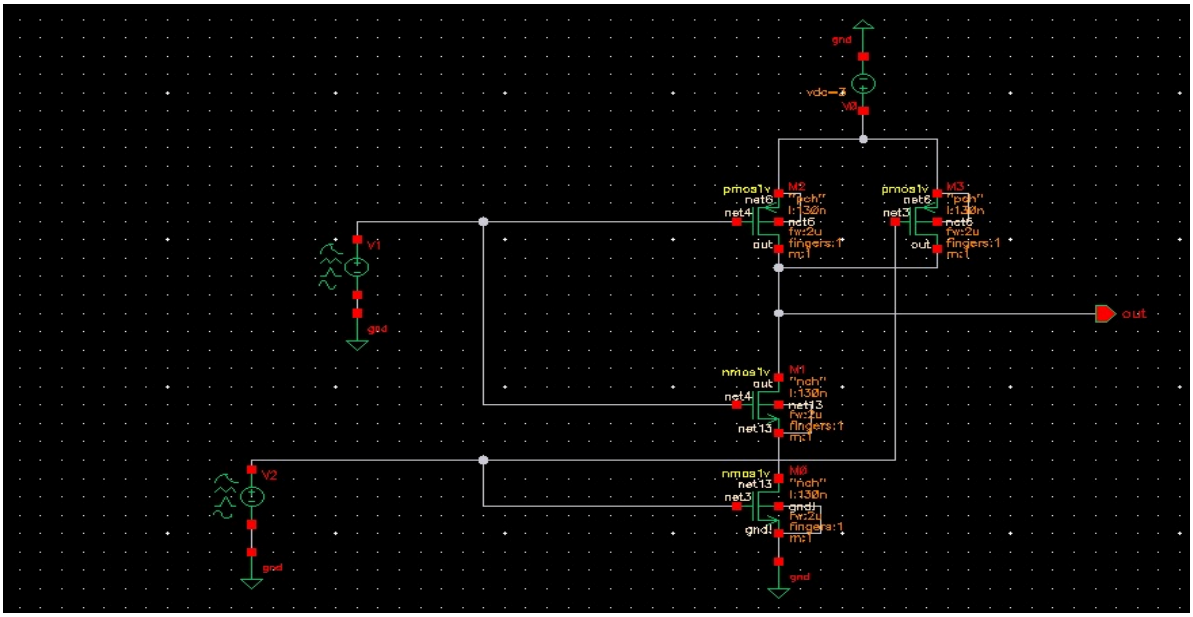
Results

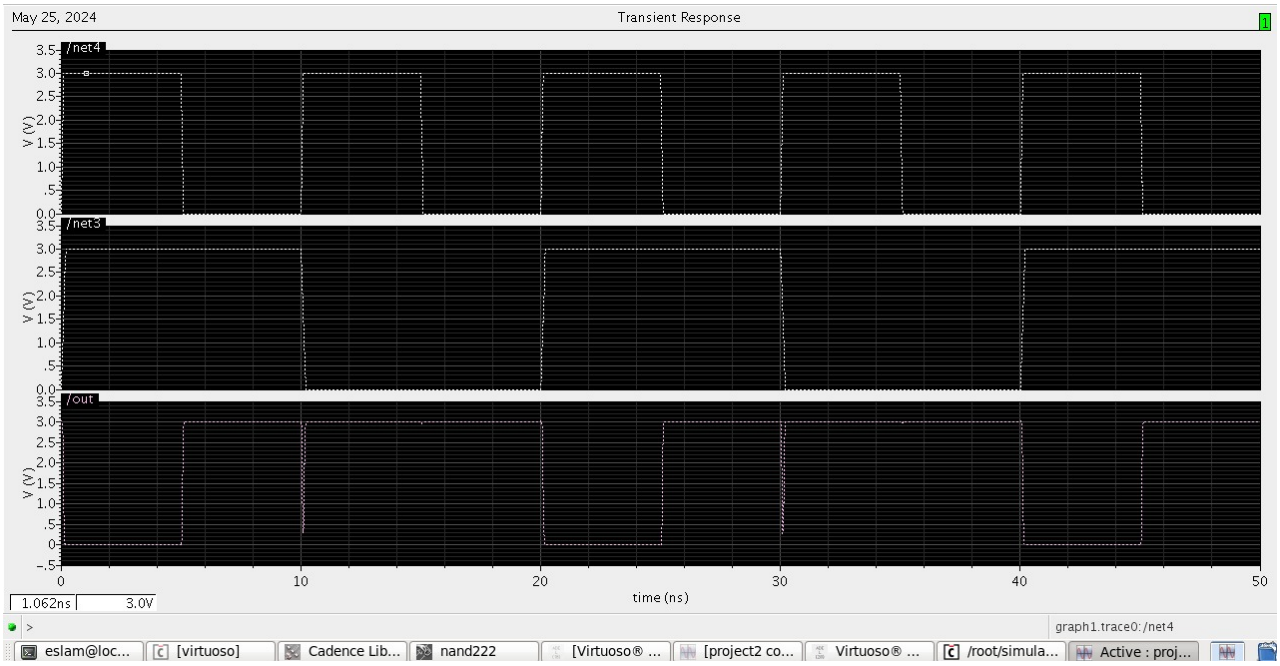
- **Figures**

3 INPUT NAND CIRCUIT & GRAPH

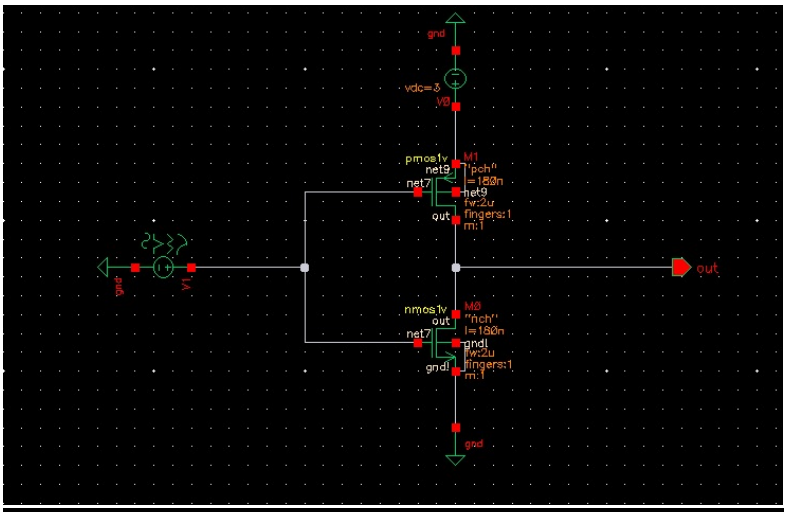


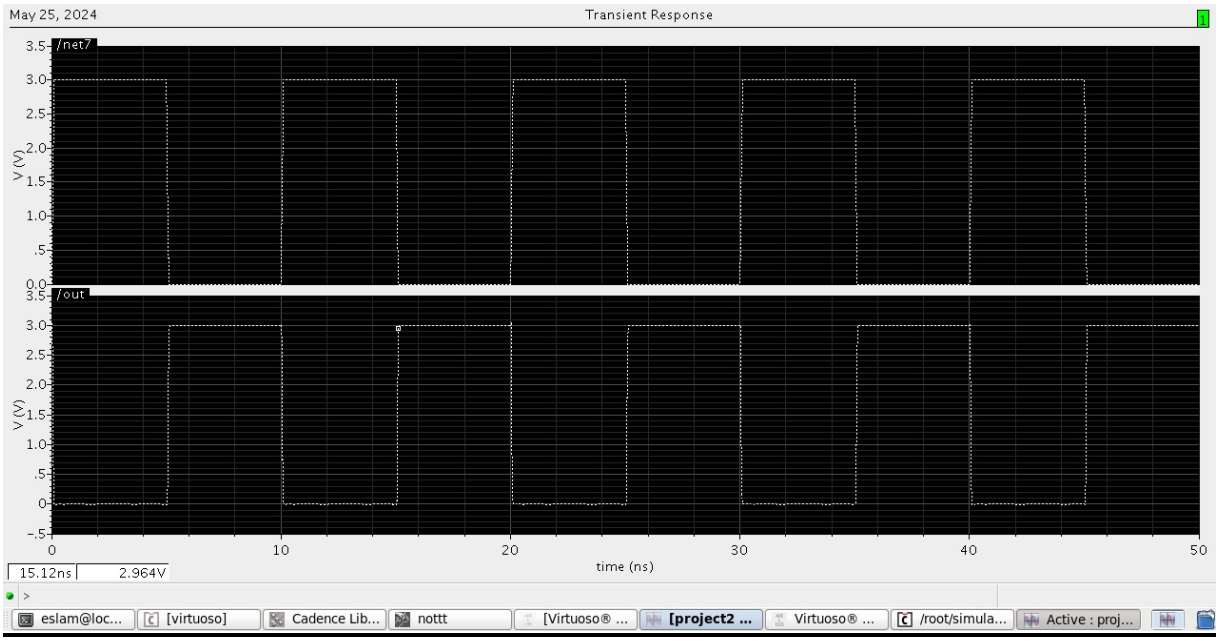
2 INPUT NAND CIRCUIT &GRAPH



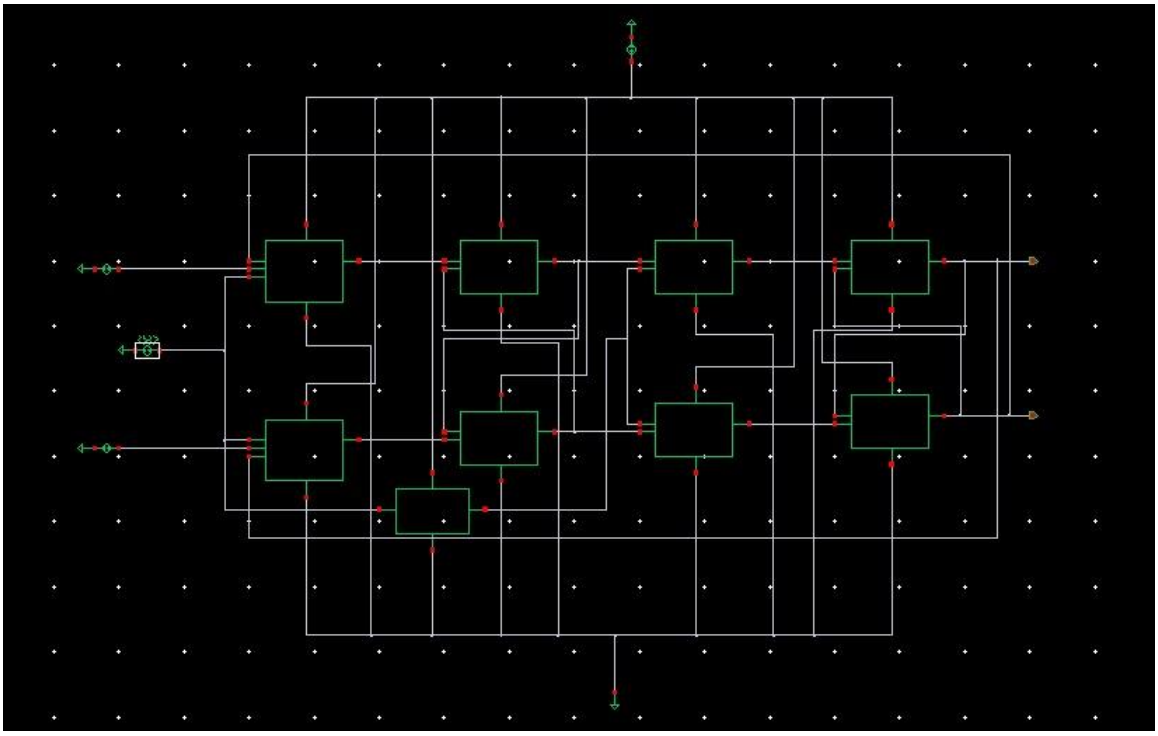


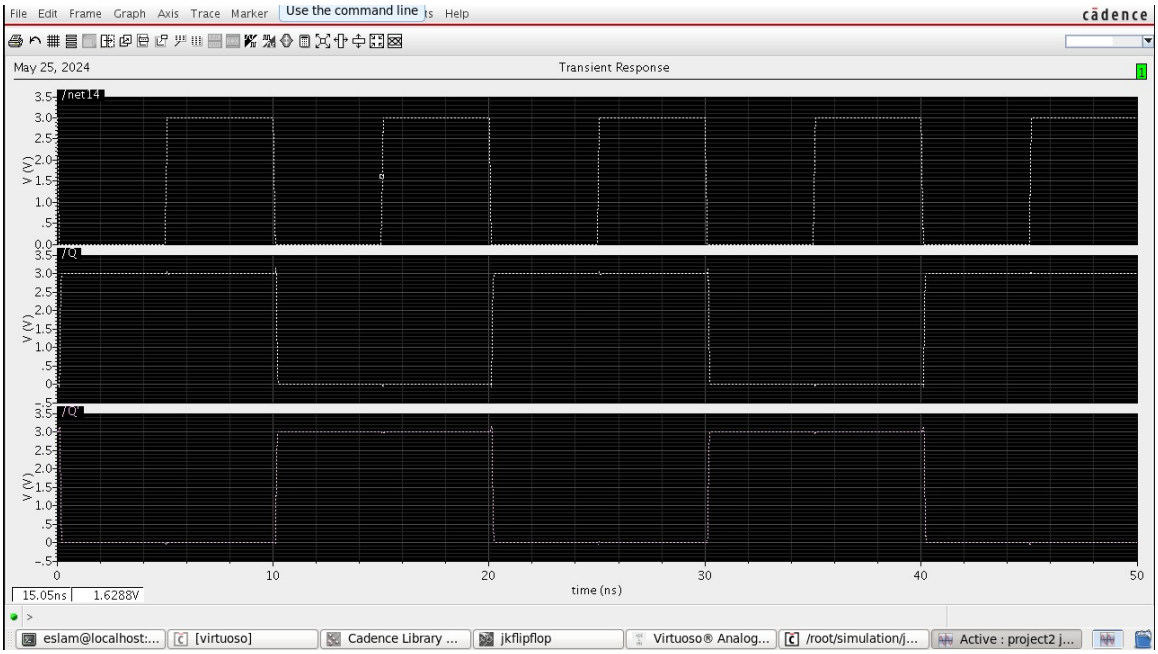
NOT GATE CIRCUIT & GRAPH



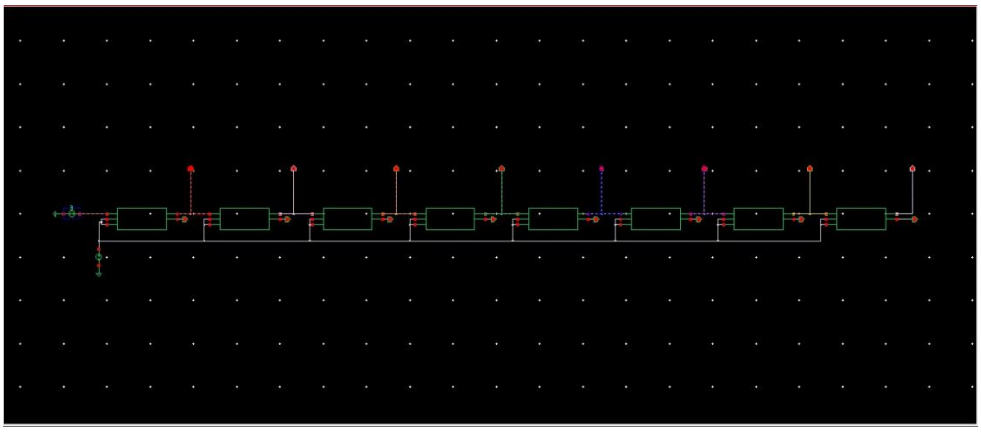


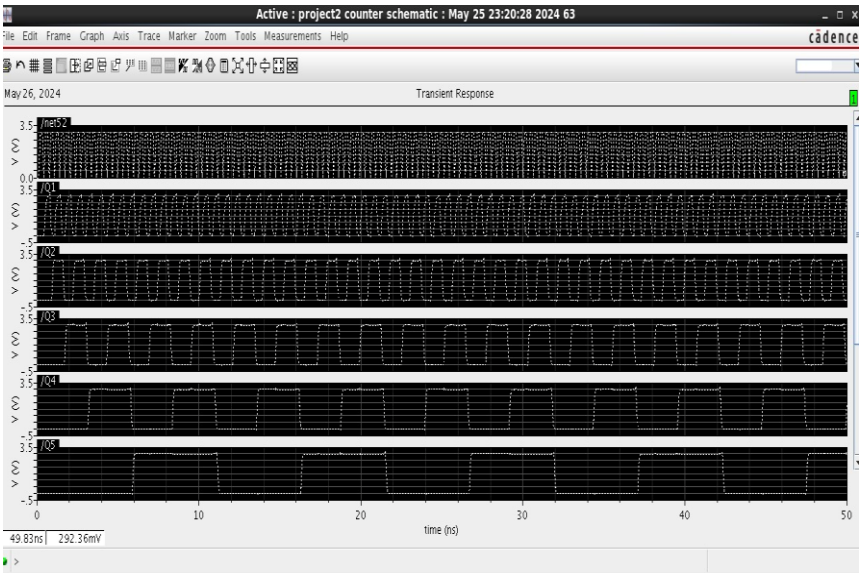
JK FLIPFLOP CIRCUIT

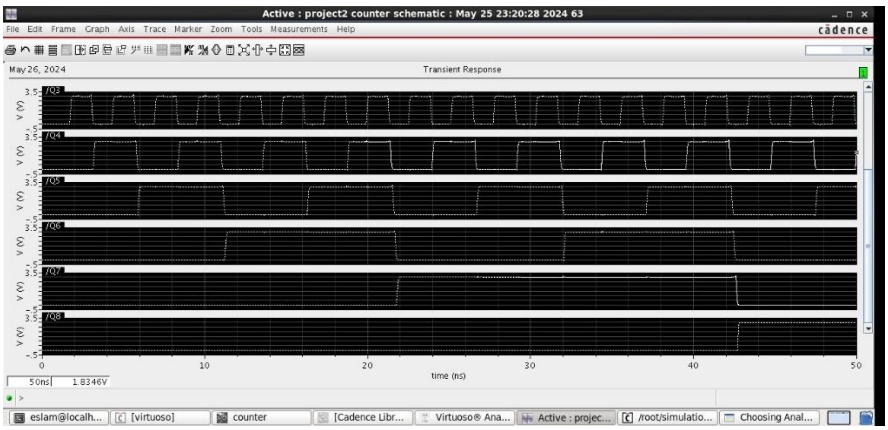




8 BIT RIPPLE COUNTER



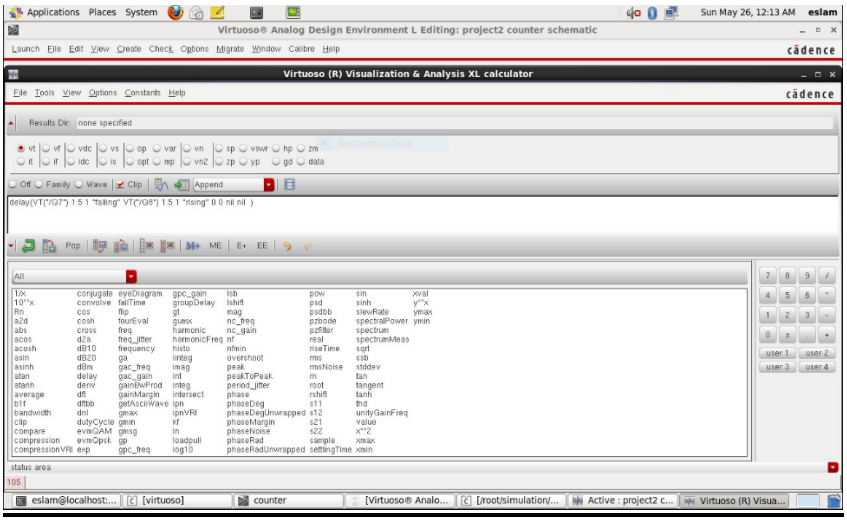


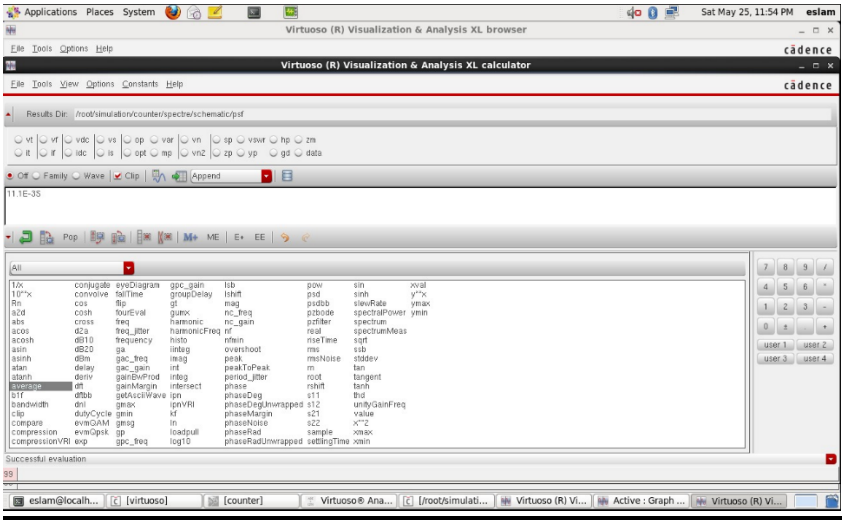


8-bit ripple counter

Power Calculation

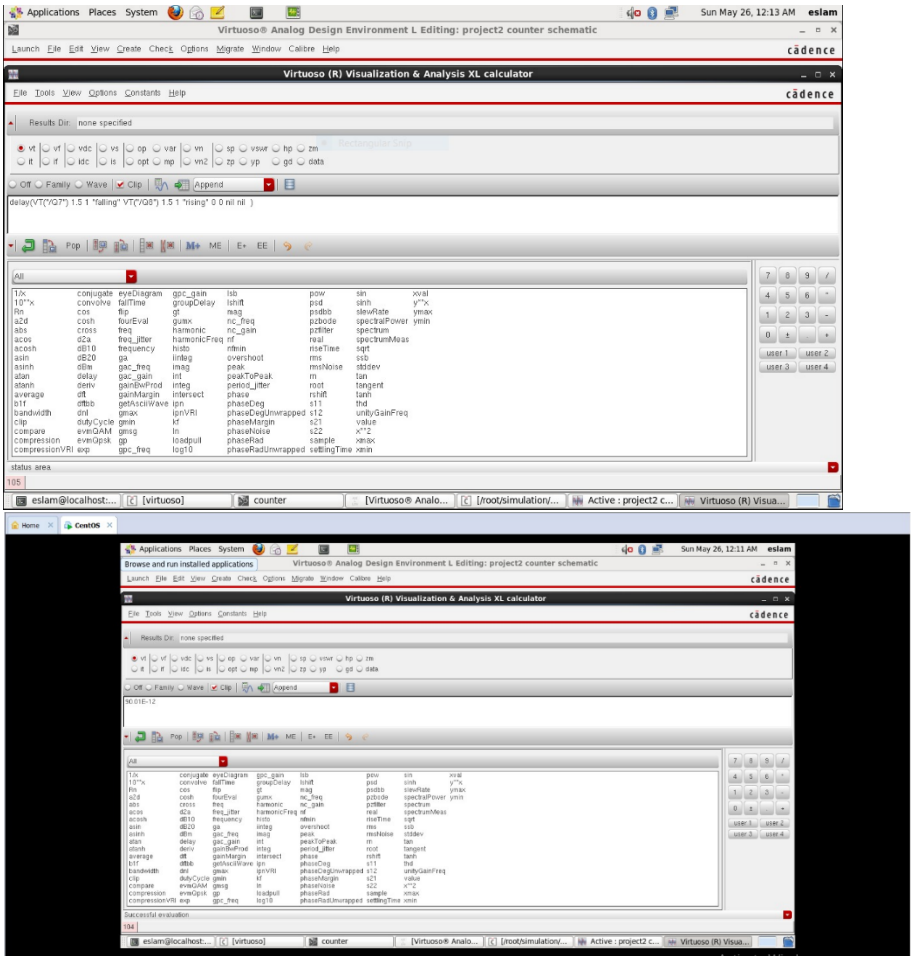
Power = 11.1×10^{-3}





Delay Calculation

Delay=90.01×10^{-12}



Conclusion

6. The design and implementation of an 8-bit ripple counter using JK-Flipflops in Cadence with CMOS transistors have been successfully completed. The simulation results confirm that the counter performs efficiently in terms of propagation delay, power consumption, and frequency response. This project demonstrates the effectiveness of using CMOS technology for designing digital sequential circuits.