ALU verification plan

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Si-vision hiring process

Introduction

After analyzing the requirements to define the enter criteria or definition of ready (DOR) we sometimes need to add some implicit requirements to achieve a testable requirements plan.

Requirements analysis

The following table shows some notes about requirements.

spec	Issues	Modification
Spec #3	The set of operation related to a_op specidied in spec #8 not spec #7	Replace spec #7 by spec #8
Spec #4	The set of operation related to a_op specidied in spec #9 not spec #8	Replace spec #8 by spec #9
Spec #9	Signal b_op is 2 bit signal not 3 bit	Replace “3 bit” by “2 bit”

Implicit Requirements requests

The following table shows some assumptions.

spec	Issues	Modification
Spec #10	The set of operation related to a_op specidied in spec #8 not spec #7	In case of a_op and b_op = ‘0’ A operand will be passed to the output without any operation
Spec #11	The set of operation related to a_op specidied in spec #9 not spec #8	In case of ALU_en is disabled the output will be set to ‘0’
Spec #12	Signal b_op is 2 bit signal not 3 bit	In case of NULL operation A operand will be passed to the output without any operation