Ministry of Higher Education		
Higher Institute for Engineering and Technology at Manzala		
First semester S_1 : 2022/2023		Date: 18/1/2023
Final Exam		Level: 1
Department: Electronic Engineering.		Time allowed: 3 hrs.
Total Marks: 90		Code: COM111
Course title: Fundamentals of Electronic Engineering		Examiner: Dr. Mohamed Abd Elrahman

Question (1) اسس الهندسة الإلكترونية [25 marks]

Part .I (Multiple Choice Questions) [10 marks]

1) What are the applications of the PN junction diode?
   a) can be used as a photodiode b) Can be used as solar cell
   c) can be used as rectifiers d) All of the above.....

2) Which one of the following has a large energy gap?
   a) Semiconductors b)Conductors c) Insulators d) None of the above

3) Which type of transformer is required to create a 180 degree input to a rectifier?
   a) center-tapped secondary b) step-down secondary
   c) stepped-up secondary d) split winding primary

4) In photodiode, when there is no incident light, the reverse current is almost negligible and is called.....
   a) zener current b) dark current
   c) photo current d) none of the above

5) If the doping level in a crystal diode is increased, the width of depletion layer.....
   a) remains the same b) is decreased c) in increased d) none of the above

6) A series resistance is connected in the zener circuit to.....
   a) properly reverse bias the zener b) protect the zener
   c) properly forward bias the zener d) none of the above

7) A zener diode is used as .....
   a) an amplifier b) voltage regulator c) rectifier d) multivibrator

8) In a reverse-biased PN junction, the current through the junction increases abruptly at
   a) 0.5 V b) 1.1 V c) 0.72 V d) breakdown voltage

9) The varactor is usually.....
   a) forward biased b) reverse biased c) operated in the breakdown d) unbiased

10) The depletion layer across a p-n^+ junction lies
   a) mostly in the p-region b) mostly in the n^+-region
   c) equally in both the p and n^+-region d) none of the above

11) When the graph between current through and voltage across a device is a straight line, the device is referred to as .....
   a) linear b) active c) nonlinear d) passive

12) The most widely used rectifier is .....
   a) half-wave rectifier b) center-tap full-wave rectifier
   c) bridge full-wave rectifier d) none of the above

P.T.O

Part. II

Aided with the configurations, draw a bridge rectifier and illustrate the output voltage waveform in case of : i) filter capacitor ii) without filter capacitor
Also derive the relation for the ripple factor as a function of C, f and I_{DC} [5 marks]

c) A full-wave rectifier is fed from **50 Hz** ac source with **120V** (rms) at the secondary coil. It is connected to a load drawing a DC current of **50 mA** and using a filter capacitor **100** μF.

Determine the following:

i) DC output voltage V_{DC} and the resistor R_L.

ii) The peak to peak ripple voltage V_r and its rms value.

iii) Ripple factor γ. [10 marks]

Question (2) [15 marks]

a) Sketch the charge density distributions ρ, electric field intensity E, and potential V across the pn junction under equilibrium. [5 marks]

b) An abrupt silicon p-n junction having doping of $N_A = 10^{18}\text{cm}^{-3}$; $N_D = 10^{16}\text{cm}^{-3}$ and a circular cross section with diameter of 0.02 inch. Consider $n_i = 1.5\times10^{10}\text{cm}^{-3}$ for silicon at room temperature, relative permittivity of silicon $\varepsilon_s = 11.9$ and $\varepsilon_o = 8.85\times10^{-14}$ F/cm.

Determine the following:

i) The value of barrier voltage V_b.
ii) The depletion width in n-region x_{no}.
iii) The depletion width in p-region x_{po}.
iv) Total depletion width W_d.
v) The charges Q_p and Q_n in the depletion region.
vi) The value of maximum electric field. [10 marks]

Question (3): [15 marks]

a) Write down the parameters of both LED and Varactor according to the following table [5 marks]

No.	Parameters	Light emitting diode (LED)	Varactor
1	Function		
2	Schematic symbol		
3	Bias for normal operation		
4	Applications (at least two)		

b) An SCR in Fig.1 has $V_g - I_g$ characteristics given as $V_g = 1.5 + 8I_g$. In a certain application the gate voltage consists of rectangular pulses of 12 V and duration 50 μs with duty cycle 0.2 . Find

i) R_g in gate circuit to limit the peak power dissipation in gate to 5 Watt.

ii) Average power dissipation in gate. [10 marks]

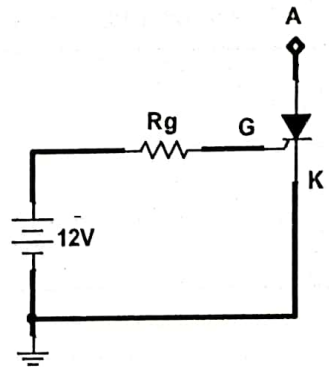

Fig.1 SCR Circuit

Question (4): [20 marks]

a) Draw and explain one of the applications for the zener diode. [5 marks]

b) Consider a zener diode regulator circuit as shown in Fig. 2. $V_{ss} = 120\,V$, $R_L = 10\,k\Omega$, $R = 5\,k\Omega$ and $V_z = 50\,V$. Compute the following: [10 marks]

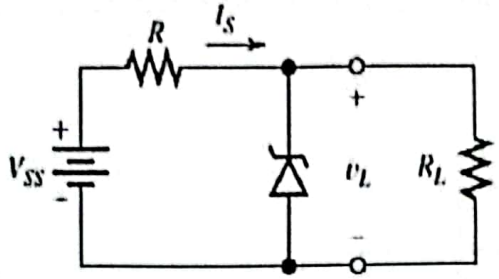

Fig.2

i) The current flowing through the load, I_L = ...

ii) The source current, I_S = ...

iv) The zener current at full load I_Z = ...

v) Power of zener diode P_Z. = ...

vi) Power supplied by the source, P_S = ...

v) Output voltage with removing the zener diode .....

c) Compare between zener and avalanche breakdown. [5 marks]

No.	Parameters	Zener breakdown	Avalanche breakdown
1	Doping		
2	Depletion region		
3	Reverse voltage		
4	Electric Field		
5	Junction		
6	Ionization		

d) Draw the breakdown characteristic of both zener and avalanche junctions

Question (5) [15 marks]

a) For the common emitter BJT amplifier circuit shown in Fig. 3, calculate I_B, I_C, V_{CE}, V_B, V_C and V_{CB}. Also draw its ac equivalent circuit and compute the voltage gain A_v. and the input resistance R_{inp}. [5 marks]

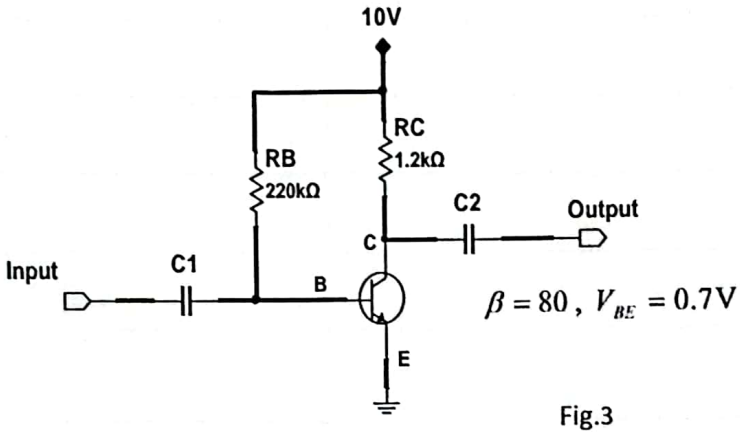

Fig.3

b) Compare the following parameters for the BJT and JFET devices. [5 marks]

No.	Parameters	JFET	BJT
1	Control element		
2	Device type		
3	Types of carriers		
4	Input resistance		
5	Thermal stability		
6	Schematic symbol		
7	Gain		

c) Aided with the configurations, draw the structure of **n** and **p** channels for both **JFET** and **MOSFET** devices. Also discuss and explain the physical operation for each one of them. [5 marks]