Proyecto Arquitectura de computadoras

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- FADD
- IMPLEMENTACIÓN EN LA PLACA

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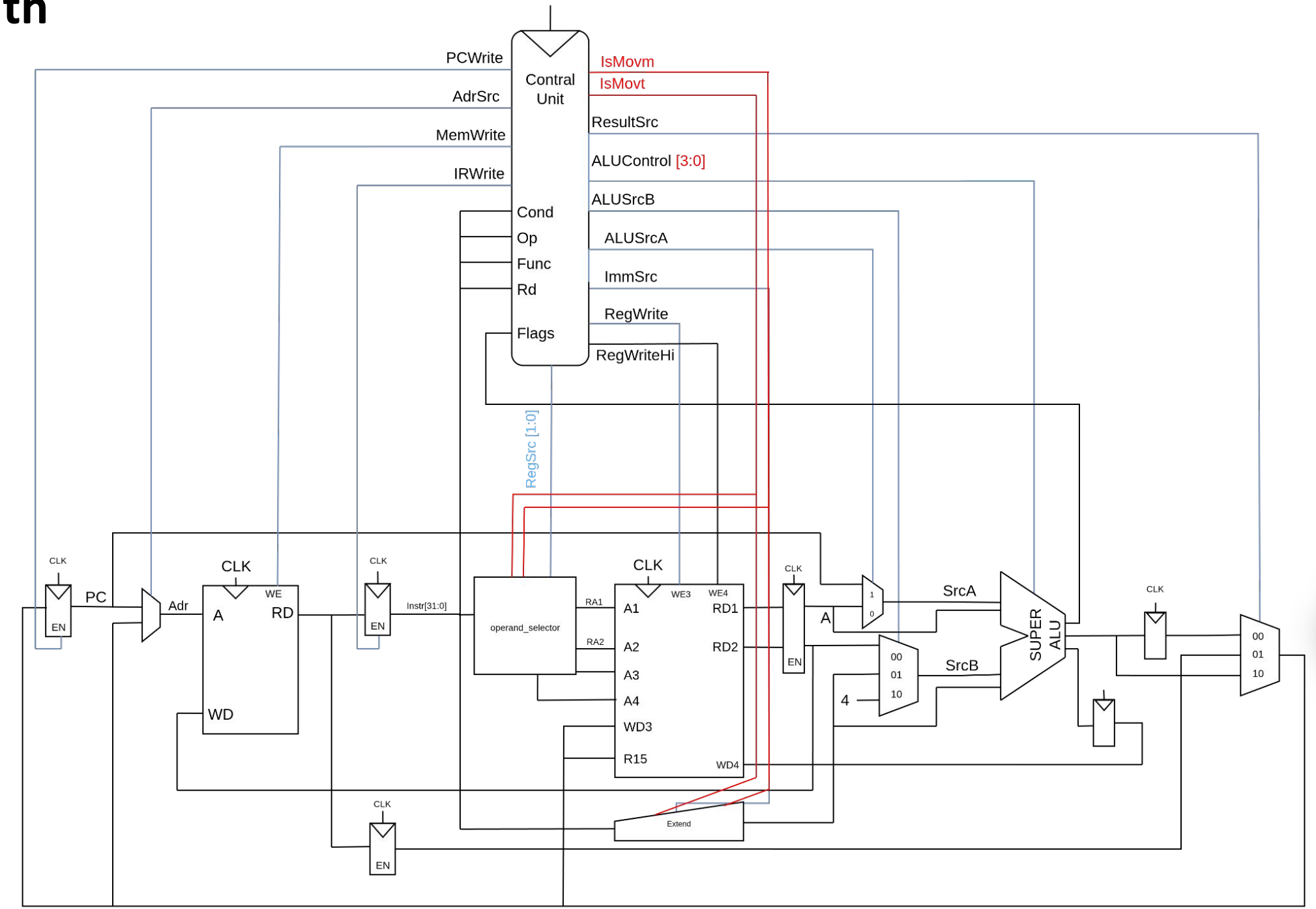
1 FMUL

Datapath


PCWrite
AdrSrc
MemWrite
IRWrite
Contral Unit
Cond
Op
Func
Rd
Flags
IsMovm
IsMovt
ResultSrc
ALUControl [3:0]
ALUSrcB
ALUSrcA
ImmSrc
RegWrite
RegWriteHi
RegSrc [1:0]
CLK
EN
PC
Adr
A
WE
RD
WD
Instr[31:0]
operand_selector
RA1
RA2
A1
A2
A3
A4
WD3
R15
WE3
WE4
RD1
RD2
WD4
Extend
1
0
SrcA
SrcB
SUPER ALU
00
01
10
4

PASOS PARA FMUL - IEEE 754 de 32 bits

Formato IEEE 754 (32 bits)

- **Signo**: 1 bit [31]
- **Exponente**: 8 bits [30:23] (sesgo = 127)
- **Mantisa**: 23 bits [22:0] (bit implícito = 1)

Pasos de Implementación:

1. **Detectar operandos cero**
2. **Extraer componentes**
3. **Sumar exponentes** y restar sesgo (127)
4. **Multiplicar mantisas** (24×24 = 48 bits)
5. **Normalizar resultado** (verificar MSB)
6. **XOR signos** para signo final

Ejemplo: R1 × R2 = 0.5 × 2.4 = 1.2

Exp_result = 126 + 128 - 127 = 127

Mult_mantisas = 1.0 × 1.2 = 1.2

Signo Result = 0 ⊕ 0 = 0

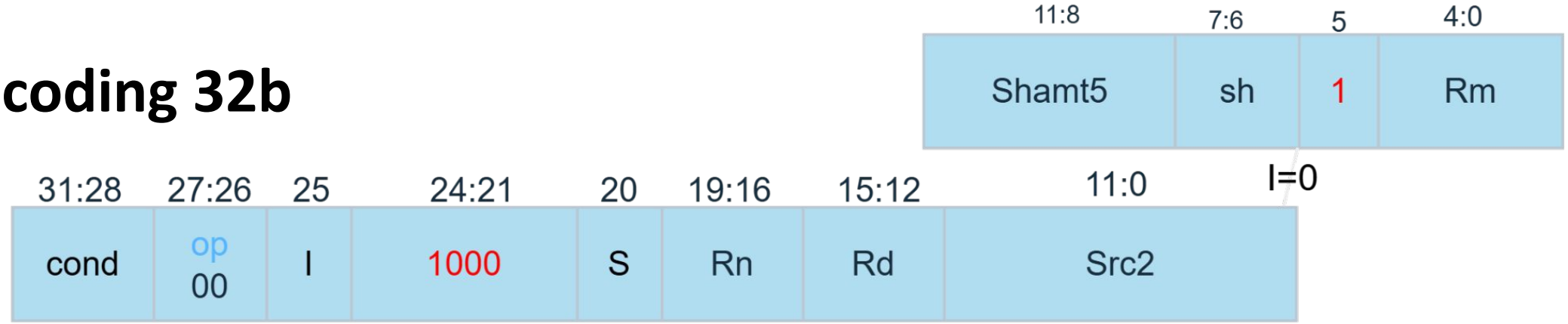
Resultado: 3F99999A ≈ 1.2

Tabla de ALU/main decoder

ALUOp	$Funct_{4:1}$ (cmd)	$Funct_0$ (S)	Type	ALUControl	$FlagW_{1:0}$
0	X	X	Not DP	000 (Add)	00
1	1000	0	FADDS	1000 (FADDS)	00
1	1000	0	FMULS	1001 (FMULS)	00

Op	$Funct_{4:1}$	$Funct_0$ (S)	Tipo	RegWHi	RegW	ALUOp
00	1000	0	DP FP32 Add (FADDS)	0	1	1
	(Opcode=1000, S=0)					
00	1000	1	DP FP32 Mul (FMULS)	0	1	1
	(Opcode=1000, S=1)					

Encoding 32b



Instrucciones

```
MOV R1, #0x000
MOVM R1, #0x00
MOVT R1, #0x3F0 //MOV R1, #0x3f000000
MOV R2, #0x99A
MOVM R2, #0x99
MOVT R2, #0x401 //MOV R2, #0x4019999a
FADD R0, R1,R2
FMUL R0,R1,R2
```

Codificación

```
E3A01000
E3C01000
E34013F0
E3A0299A
E3C02099
E3402401
E1010002
E1010012
```

Encoding

Instrucción FMUL

```
FMUL R0,R1,R2
```

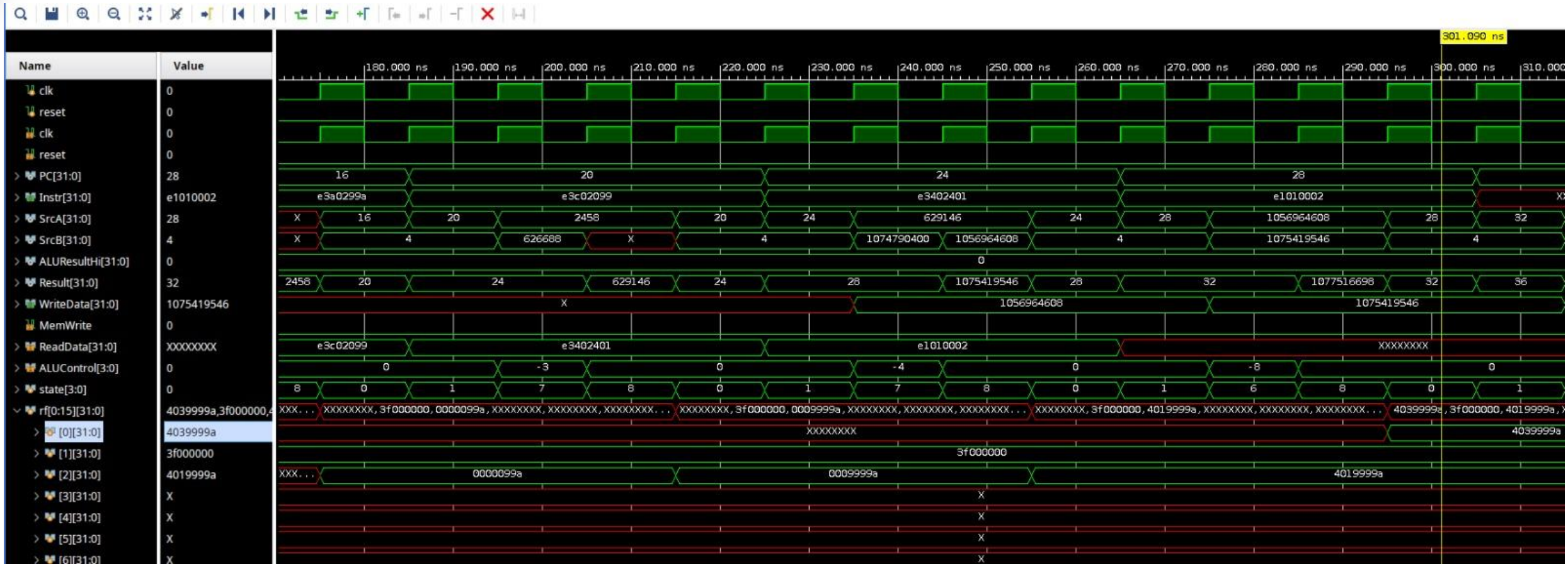
31:28	27:26	25	24:21	20	19:16	15:12	11:7	6:5	4	3:0
1110	op 00	0	1000	0	0001	0000	00000	00	1	0001

11100001000000010000000000010010

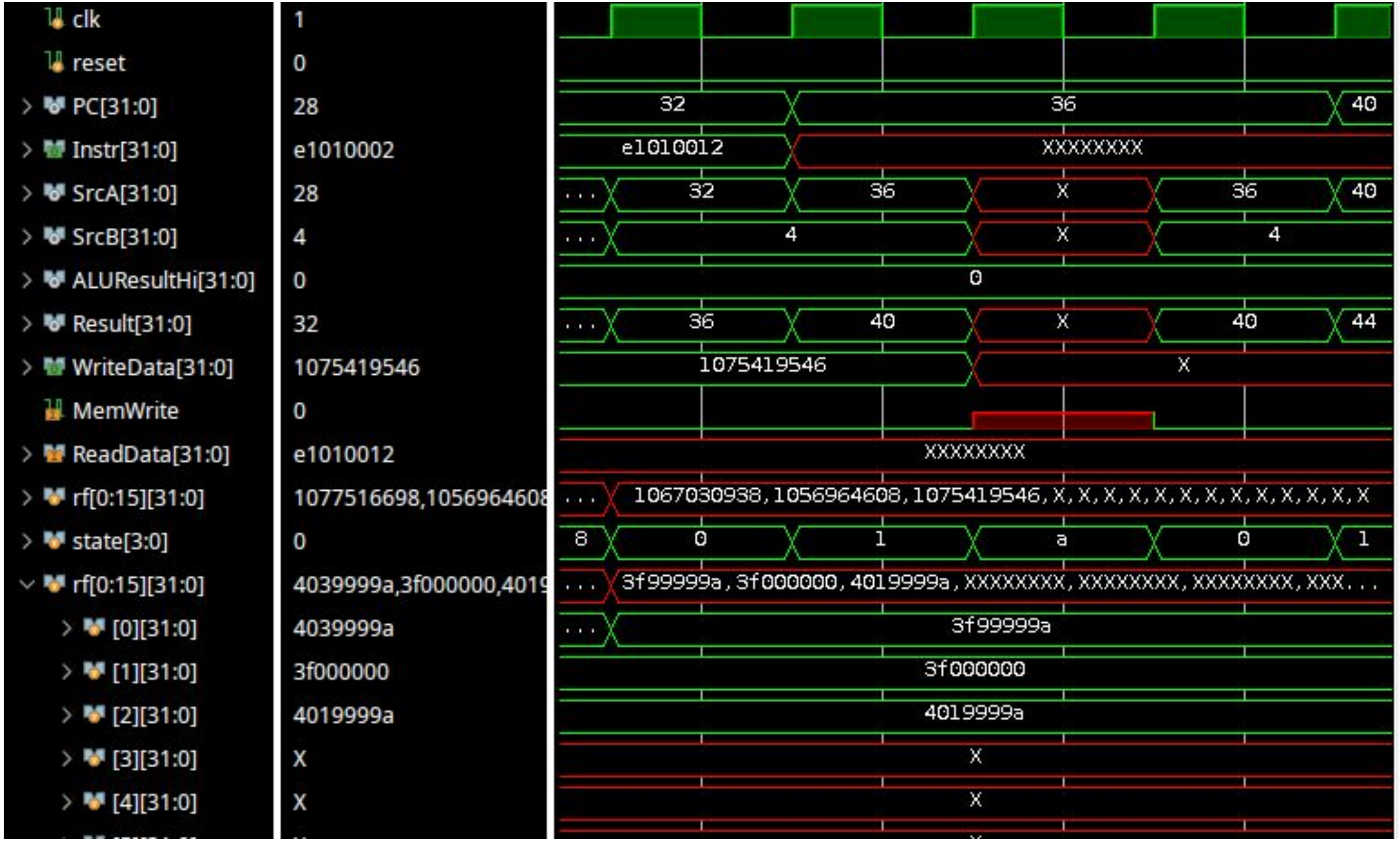
Codificación:

E1010012

Waveform


Name
Value
clk
reset
clk
reset
PC[31:0]
Instr[31:0]
SrcA[31:0]
SrcB[31:0]
ALUResultHi[31:0]
Result[31:0]
WriteData[31:0]
MemWrite
ReadData[31:0]
ALUControl[3:0]
state[3:0]
rf[0:15][31:0]
[0][31:0]
[1][31:0]
[2][31:0]
[3][31:0]
[4][31:0]
[5][31:0]
[6][31:0]
301.090 ns
180.000 ns
190.000 ns
200.000 ns
210.000 ns
220.000 ns
230.000 ns
240.000 ns
250.000 ns
260.000 ns
270.000 ns
280.000 ns
290.000 ns
300.000 ns
310.000

Waveform


clk
1
reset
0
PC[31:0]
28
32
36
40
Instr[31:0]
e1010002
e1010012
XXXXXXXX
SrcA[31:0]
28
32
36
X
36
40
SrcB[31:0]
4
4
X
4
ALUResultHi[31:0]
0
0
Result[31:0]
32
36
40
X
40
44
WriteData[31:0]
1075419546
1075419546
X
MemWrite
0
ReadData[31:0]
e1010012
XXXXXXXX
rf[0:15][31:0]
1077516698,1056964608
1067030938,1056964608,1075419546,X,X,X,X,X,X,X,X,X,X,X,X
state[3:0]
0
8
0
1
a
0
1
rf[0:15][31:0]
4039999a,3f000000,4019
3f99999a,3f000000,4019999a,XXXXXXXX,XXXXXXXX,XXXXXXXX,XXX...
[0][31:0]
4039999a
3f99999a
[1][31:0]
3f000000
3f000000
[2][31:0]
4019999a
4019999a
[3][31:0]
X
X
[4][31:0]
X
X

Resultado

IEEE 754 Converter, 2024-02

	Sign	Exponent	Mantissa
Value:	+1	2^0	1 + 0.20000004768371582
Encoded as:	0	127	1677722
Binary:	☐	☑☑☑☑☑☑☑☑	☐☐☑☑☐☐☑☑☐☐☑☑☐☐☑☑☐☐☑☑☐☑☐

Decimal Representation: 1.2

Value actually stored in float: 1.200000047683715820312 5

Error due to conversion: 0.000000047683715820312 5

Binary Representation: 00111111100110011001100110011010

Hexadecimal Representation: 3f99999a

1

-1

Tabla de ALU/main decoder

ALUOp	$Funct_{4:1}$ (cmd)	$Funct_0$ (S)	Type	ALUControl	$FlagW_{1:0}$
0	X	X	Not DP	000 (Add)	00
1	1001	0	FADDH	1110 (FADDH)	00
1	1001	0	FMULH	1111 (FMULH)	00

Op	$Funct_{4:1}$	$Funct_0$ (S)	Tipo	RegWHi	RegW	ALUOp
00	1000	0	DP FP32 Add (FADDS)	0	1	1
	(Opcode=1000, S=0)					
00	1000	1	DP FP32 Mul (FMULS)	0	1	1
	(Opcode=1000, S=1)					

31:28	27:26	25	24:21	20	19:16	15:12	11:7	6:5	4	3:0
1110	op 00	0	1001	0	0001	0000	00000	00	1	0001

2 FADD

Datapath

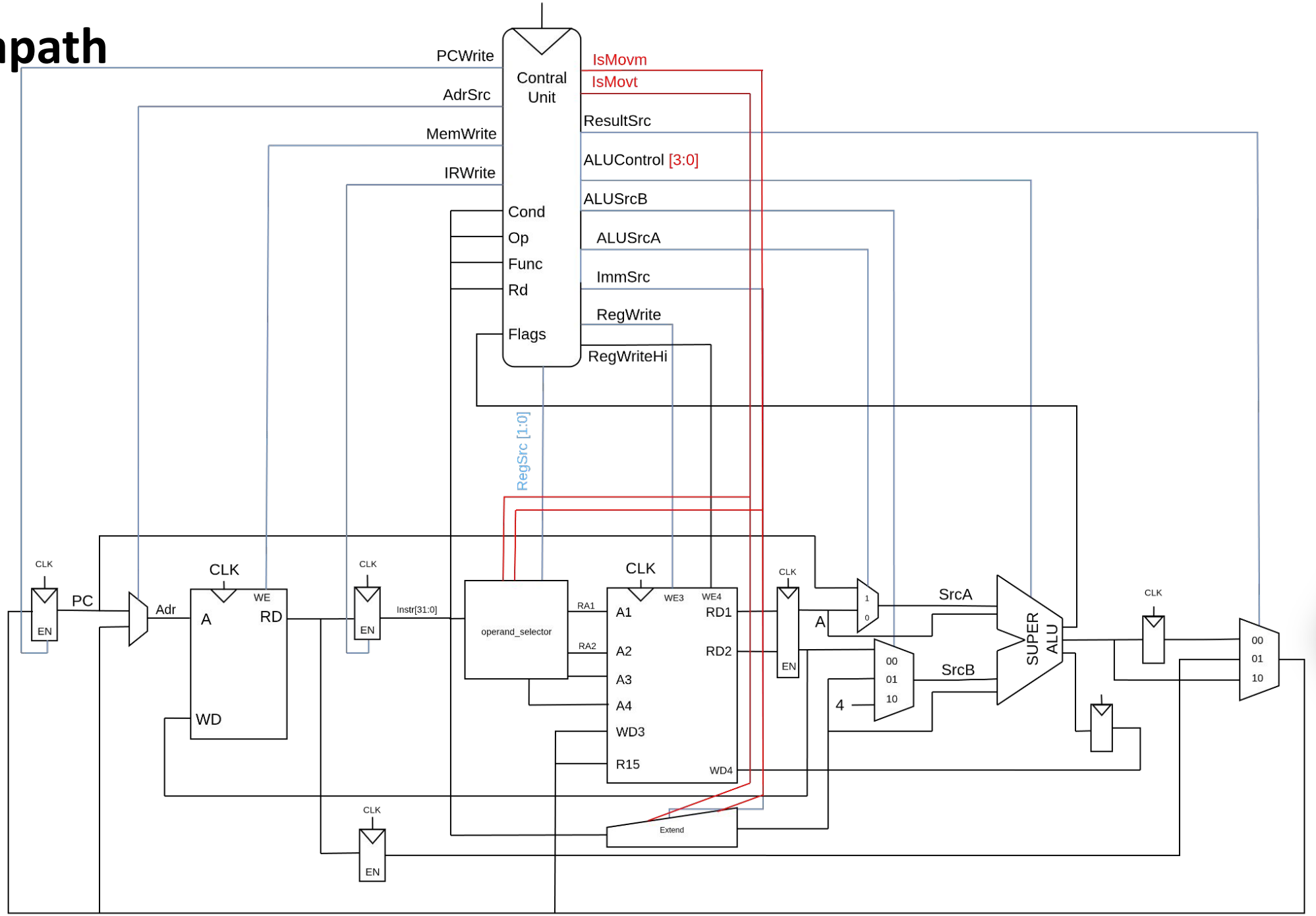

PCWrite
AdrSrc
MemWrite
IRWrite
Contral Unit
Cond
Op
Func
Rd
Flags
IsMovm
IsMovt
ResultSrc
ALUControl [3:0]
ALUSrcB
ALUSrcA
ImmSrc
RegWrite
RegWriteHi
RegSrc [1:0]
CLK
EN
PC
Adr
A
WE
RD
WD
Instr[31:0]
operand_selector
RA1
RA2
A1
A2
A3
A4
WD3
R15
WE3
WE4
RD1
RD2
WD4
Extend
1
0
SrcA
SrcB
SUPER ALU
4
00
01
10

Tabla de ALU/main decoder

ALUOp	$Funct_{4:1}$ (cmd)	$Funct_0$ (S)	Type	ALUControl	$FlagW_{1:0}$
0	X	X	Not DP	000 (Add)	00
1	1000	0	FADDS	1000 (FADDS)	00
1	1000	0	FMULS	1001 (FMULS)	00

Op	$Funct_{4:1}$	$Funct_0$ (S)	Tipo	RegWHi	RegW	ALUOp
00	1000	0	DP FP32 Add (FADDS)	0	1	1
	(Opcode=1000, S=0)					
00	1000	1	DP FP32 Mul (FMULS)	0	1	1
	(Opcode=1000, S=1)					

PASOS PARA FADD - IEEE 754 de 32 bits

Formato IEEE 754 (32 bits)

- **Signo**: 1 bit [31]
- **Exponente**: 8 bits [30:23] (sesgo = 127)
- **Mantisa**: 23 bits [22:0] (bit implícito = 1)

Pasos de Implementación:

1. **Extraer componentes** (signo, exponente, mantisa)
2. **Agregar bit implícito** (1.mantisa)
3. **Comparar exponentes** y calcular diferencia
4. **Alinear mantisa** menor (desplazar a la derecha)
5. **Sumar/restar mantisas** según signos
6. **Normalizar resultado** y ajustar exponente

Ejemplo: R1 + R2 = 0.5 + 2.4 = 2.9

Proceso:

- Exp_diff = 128-126 = 2
- Alinear R1: 1.0 >> 2 = 0.25
- Sumar: 1.2 + 0.25 = 1.45
- Normalizar: $1.45 \times 2^1 = 2.9$
- **Resultado: 40399999** ≈ 2.9

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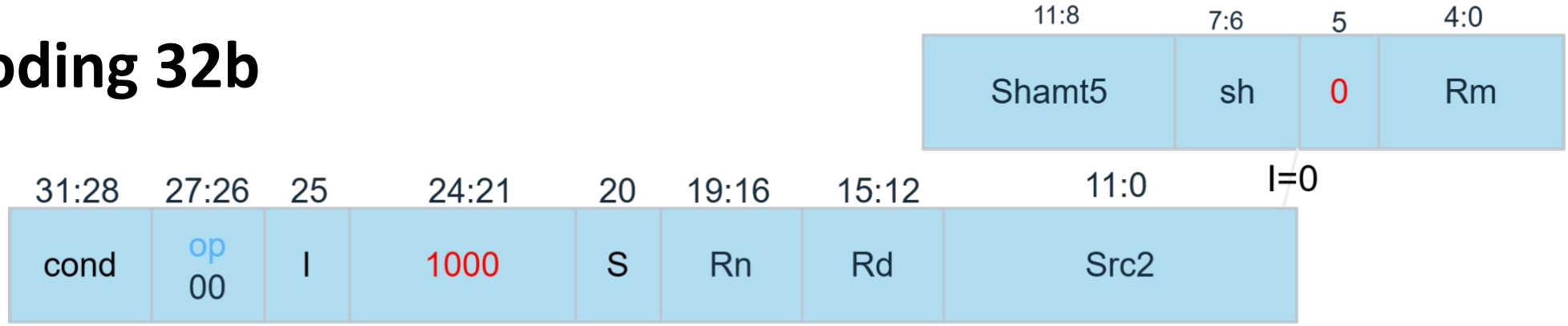
Encoding 32b



Instrucciones

```
MOV R1, #0x000
MOVM R1, #0x00
MOVT R1, #0x3F0   //R1=3F000000
MOV R2, #0x99A
MOVM R2, #0x99
MOVT R2, #0x401   // R1=4019999A
FADD R0,R1,R2
```

Codificación

```
E3A01000
E3C01000
E34013F0    //R1 = 3F000000: 0.5
E3A0299A
E3C02099
E3402401   //R2 = 4019999A: 2.4
E1010002    //FADD
```

Encoding

Instrucción FADD

```
FADD R0,R1,R2
```

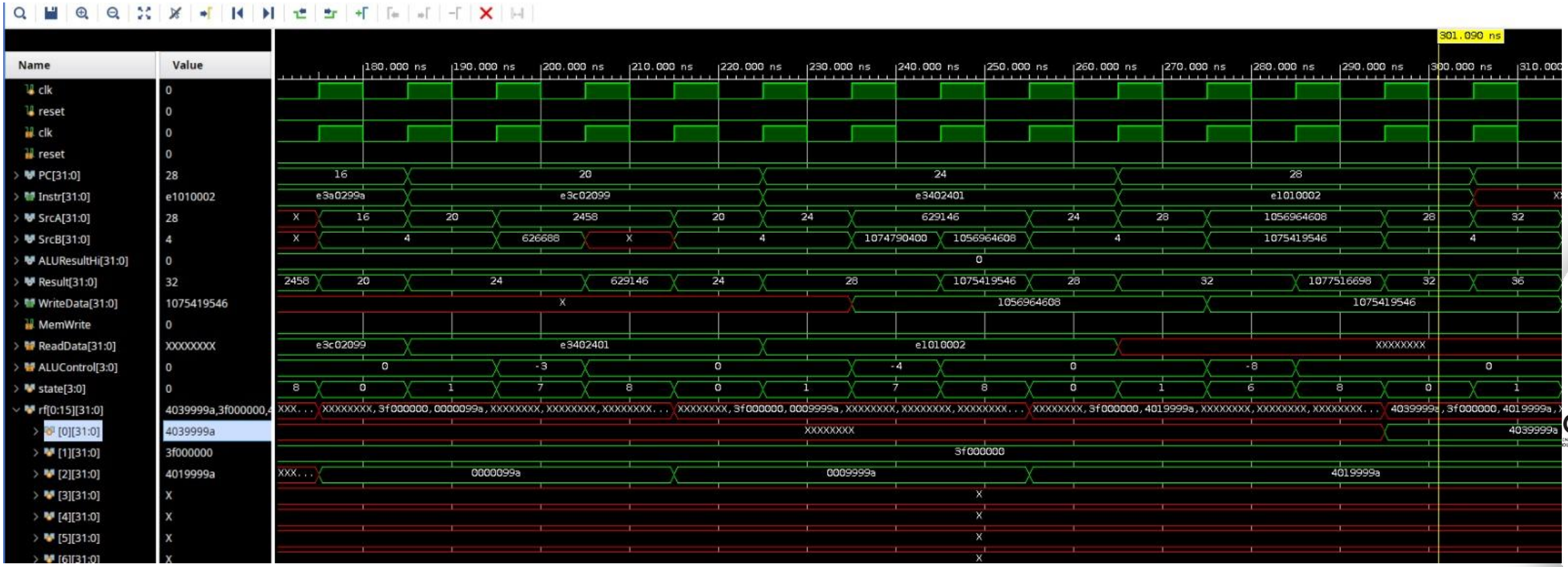
31:28	27:26	25	24:21	20	19:16	15:12	11:7	6:5	4	3:0
1110	op 00	0	1000	0	0001	0000	00000	00	0	0001

11100001000000010000000000000010

Codificación:

E1010002

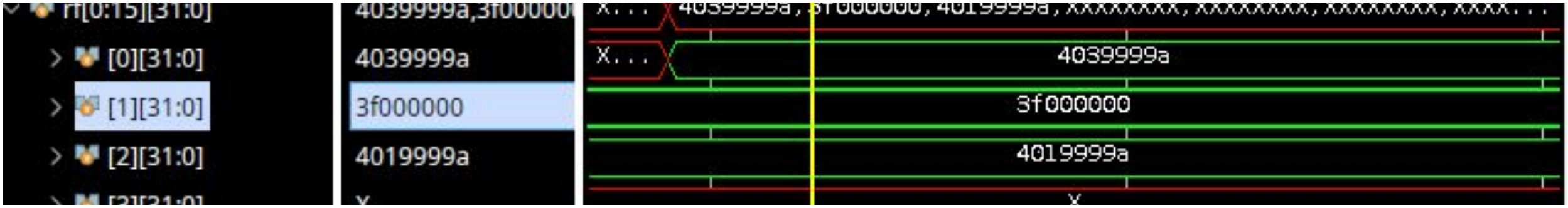
Waveform


Name
Value
clk
reset
clk
reset
PC[31:0]
Instr[31:0]
SrcA[31:0]
SrcB[31:0]
ALUResultHi[31:0]
Result[31:0]
WriteData[31:0]
MemWrite
ReadData[31:0]
ALUControl[3:0]
state[3:0]
rf[0:15][31:0]
[0][31:0]
[1][31:0]
[2][31:0]
[3][31:0]
[4][31:0]
[5][31:0]
[6][31:0]
0
0
0
0
28
e1010002
28
4
0
32
1075419546
0
XXXXXXXX
0
0
4039999a
3f000000
4019999a
X
X
X
X
301.090 ns
180.000 ns
190.000 ns
200.000 ns
210.000 ns
220.000 ns
230.000 ns
240.000 ns
250.000 ns
260.000 ns
270.000 ns
280.000 ns
290.000 ns
300.000 ns
310.000

Waveform


clk
reset
PC[31:0]
Instr[31:0]
SrcA[31:0]
SrcB[31:0]
ALUResultHi[31:0]
Result[31:0]
WriteData[31:0]
MemWrite
ReadData[31:0]
rf[0:15][31:0]
state[3:0]
rf[0:15][31:0]
[0][31:0]
[1][31:0]
[2][31:0]
[3][31:0]
[4][31:0]
[5][31:0]
0
0
32
XXXXXXXX
32
4
0
36
1075419546
0
XXXXXXXX
1077516698,10569
1
4039999a,3f00000
4039999a
3f000000
4019999a
X
X
X
28 32 36 40 44
e1010002 XXXXXXXX
1... 28 32 X 32 36 X 36 40 X 40 44
1... 4 X 4 X 4 X 4
0
1... 32 36 X 36 40 X 40 44 X 44 48
1075419546 X
XXXXXXXX
X... 1077516698,1056964608,1075419546,X,X,X,X,X,X,X,X,X,X,X,X,X
8 0 1 a 0 1 a 0 1 a 0 1
X... 4039999a,3f000000,4019999a,XXXXXXXX,XXXXXXXX,XXXXXXXX,XXXX...
X... 4039999a
3f000000
4019999a
X
X
X

Resultado



IEEE 754 Converter, 2024-02

	Sign	Exponent	Mantissa
Value:	+1	2^{1}	1 + 0.4500000476837158
Encoded as:	0	128	3774874
Binary:	☐	☑☐☐☐☐☐☐☐	☐☑☑☑☐☐☑☑☐☐☑☑☐☐☑☑☐☑☐

Decimal Representation: 2.9

Value actually stored in float: 2.900000953674316406250

Error due to conversion: 0.000000953674316406250

Binary Representation: 01000000011100110011001100110011010

Hexadecimal Representation: 4039999a

1

-1

Tabla de ALU/main decoder

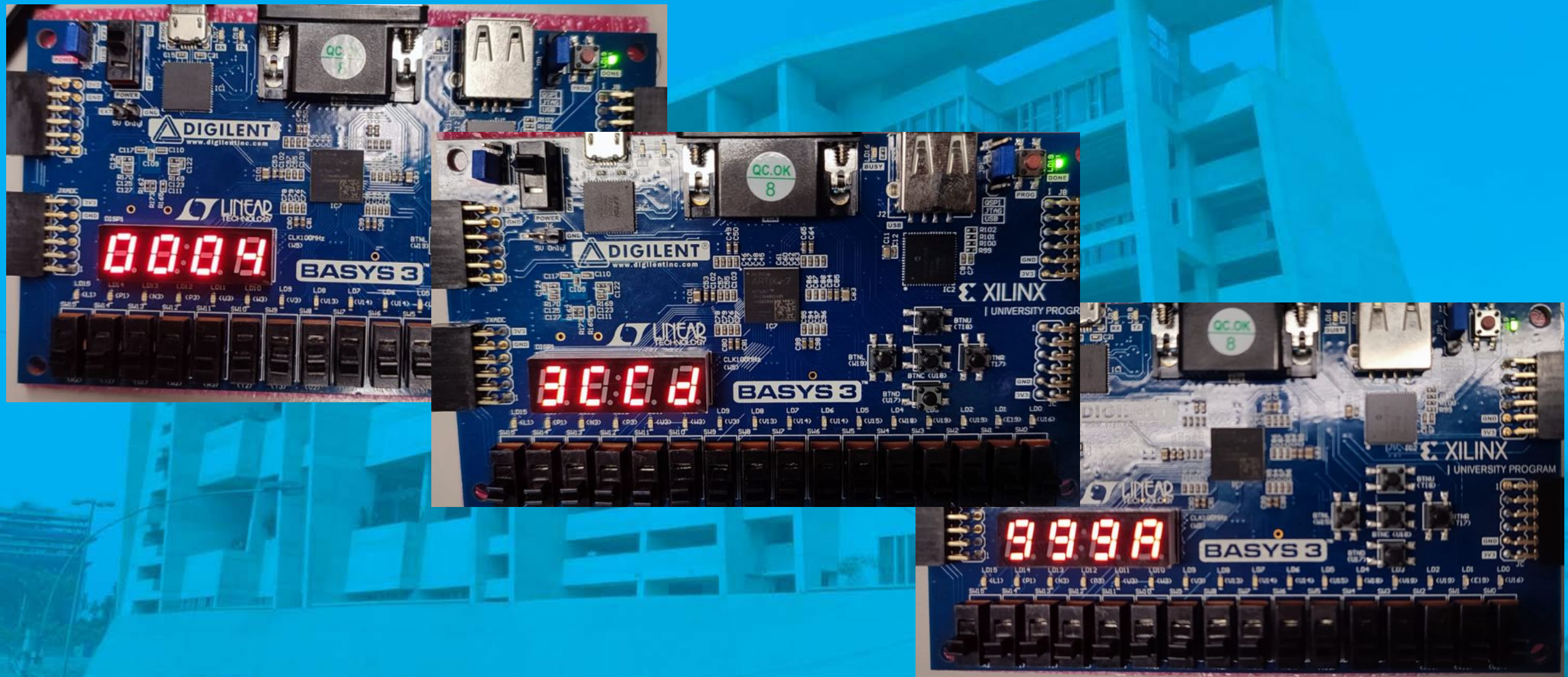
ALUOp	$Funct_{4:1}$ (cmd)	$Funct_0$ (S)	Type	ALUControl	$FlagW_{1:0}$
0	X	X	Not DP	000 (Add)	00
1	1001	0	FADDH	1110 (FADDH)	00
1	1001	0	FMULH	1111 (FMULH)	00

Op	$Funct_{4:1}$	$Funct_0$ (S)	Tipo	RegWHi	RegW	ALUOp
00	1000	0	DP FP32 Add (FADDS)	0	1	1
	(Opcode=1000, S=0)					
00	1000	1	DP FP32 Mul (FMULS)	0	1	1
	(Opcode=1000, S=1)					

31:28	27:26	25	24:21	20	19:16	15:12	11:7	6:5	4	3:0
1110	op 00	0	1001	0	0001	0000	00000	00	0	0001

3 IMPLEMENTACIÓN EN LA PLACA

ENLACE PARA LOS VIDEOS



Gracias

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