Low Power RF Signal Processing for Internet of Things Applications

Von der Fakultät für Elektrotechnik und Informationstechnik
der Rheinisch-Westfälischen Technischen Hochschule Aachen
zur Erlangung des akademischen Grades eines
Doktors der Ingenieurwissenschaften (Dr.-Ing.) genehmigte Dissertation

vorgelegt von

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Tag der müdlichen Prüfung: 13.Dezember 2016
Diese Dissertation ist auf den Internetseiten der Universitätsbibliothek online verfügbar

Chair of Integrated Analog Circuits and RF Systems

RWTH AACHEN UNIVERSITY

Low Power RF Signal Processing for Internet of Things Applications

PhD Thesis

Ye Zhang

Abstract

In this work, low effort architectures for Internet of Things (IoT) applications are proposed to support multiple short-range wireless standards on single die. Appropriate solutions for low power RF transceiver are provided, which emphasize the high-efficient, low-cost, low-power performance but with satisfactory data rate. By comparing the characteristic trade-offs of the various architectures, analyzing the typical transceiver non-ideality factors and discuss the specifications and requirements of typical short distance standards, the PLL based two-point modulation transmitter and low-IF receiver architectures are selected.

In the transmitter design, a current-reuse VCO technique in the frequency synthesizer is presented to significantly reduce the power consumption with excellent phase noise performance. Subsequently a digital architecture for $\Sigma\Delta$ quantizer and noise cancellation is proposed in the PLL modulation loop, which can dramatically reduce the hardware complexity without degrading the Synthesizer performance. To enhance the two-point modulation bandwidth, an adaptive calibration technique for phase noise cancellation based on the modified classical loop filter structure is proposed, where an additional port from the loop filter is used as the reference for the Least Mean Square (LMS) algorithm to avoid DC offset. The gain mismatch between signal path and noise cancellation path is detected and calibrated outside of the PLL loop without introducing any additional spurs into the system. Comparing to the previous works, the proposed technique provides a straightforward solution for wideband PLL designs, and the quantization noise is successfully eliminated with smaller area and lower power consumption.

In the receiver design, the proposed low-power low-effort digital demodulator architecture for low-IF receivers can compensate I/Q mismatch due to the impairment

within the frontend, and thus it improves the robustness against interference presented at the image frequency. And the group delay is compensated with a digital IIR based equalizer, which improves the BER performance significantly compared to the original case. In the clock data recovery block, the typical synchronization problems including symbol timing recovery and carrier frequency offset calibration are solved based on a simplified Data-Aided (DA) scheme. The $\Sigma\Delta$ NCO provides wide range IF signals with high resolution and SNR. A Viterbi decoder which uses multi-order differential discriminators provides a robust decoding performance. Hence, it can be demonstrated that the proposed multi-standard receiver architecture not only greatly enhances the performance with wide range data rates and IF frequencies, but also provides an easy, feasible and flexible solution for the fully integrated implementation.

Acknowledgment

Foremost, I would like to express my sincere gratitude to my adviser Prof. Dr.-Ing. Stefan Heinen for the continuous support of my Ph.D study and research, for his motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of research of this thesis. I could not have imagined having a better adviser and mentor for my Ph.D study.

I would like to express my deep sense of gratitude to Dr.-Ing. Ralf Wunderlich for all of his support, covering all fields from circuit design to administration.

My sincere thank also goes to my IAS colleagues Jan Henning Mueller, Bastian Mohr, Lei Liao, Aytac Atac, Zhimiao Chen for their tremendous contribution and support to our successful low power transceiver tapeout. I would like to thank Markus Scholl, Yishan Wang and Durgham Al-Shebanee for our joint tapeout. And I also want to thank Soheil Aghaie, Iyappan Subbiah and Arun Ashok for proof reading my paper and thesis.

Last but not the least, I would like to thank my family for supporting me throughout my life.

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List of Abbreviations

AWGN Additional White Gaussian Noise . . . 86
DFE Decision Feedback Equalizer . . . 111
BT Bluetooth . . . 2
BTLE Bluetooth Low Energy . . . 2
CDMA Code Division Multiple Access . . . 19
CDR Clock Data Recovery . . . 98
CFO Carrier Frequency Offset . . . 96
CIC Cascaded Integrator–Comb . . . 77
CM Common Mode . . . 51
CORDIC COordinate Rotation DIgital Computer . . . 9
CP Charge Pump . . . 26
CPM Continuous Phase Modulation . . . 95
CSMA Carrier Sense Multiple Access . . . 19
DA Data-Aided . . . 97
DAC Digital-to-Analog Converter . . . 6
DC Direct Current . . . 7
DDC Digital Down Converter . . . 101
DDS Direct Digital Synthesizer . . . 98
DM Differential Mode . . . 51

DSSS	Direct Sequence Spread Spectrum	19
EVM	Error-Vector Magnitude	17
FFD	Fractional Frequency Divider	98
FFT	Fast Fourier Transform	67
FHSS	Frequency-Hop Spread Spectrum	18
FSM	Finite State Machine	31
GFSK	Gaussian Frequency-Shift Keying	30
IF	Intermediate frequency	11
IIP	Input Intercept Point	13
INTF	Image Noise Transfer Function	71
IoT	Internet of Things	1
IQ	Inphase/Quadrature	6
IRR	Image Rejection Ratio	69
ISI	Inter-Symbol Interference	110
ISTF	Image Signal Transfer Function	70
LINC	LInear system with Nonlinear Components	7
LO	Local Oscillator	6
LMS	Least Mean Square	66
LNA	Low Noise Amplifier	11
LPF	Loop Filter	26
MAP	Maximum-A-Posteriori	67
ML	Maximum Likelihood	67
NCO	Numerical Controlled Oscillator	3
NDA	Non-Data-Aided	97
NF	Noise Factor	12
NTF	Noise Transfer Function	27
OFDM	Orthogonal Frequency Division Modulation	19
OQPSK	Offset Quadrature Phase-Shift Keying	47
PAPR	Peak-to-Average Power Ratio	8
PFD	Phase Frequency Detector	26
PLL	Phase Locked Loop	20

RF	Radio Frequency	5
RHC	Relative Hardware Complexity	45
ROM	Read-Only Memory	101
RTWO	Rotary Traveling Wave Oscillator	127
SIR	Signal-to-Interference Ratio	17
SNR	Signal-to-Noise Ratio	12
SOC	System-on-Chip	2
STF	Signal Transfer Function	27
SUN	Smart metering Utility Network	2
TED	Timing Error Detector	100
WBAN	Wireless Body Area Network	2
WLAN	Wireless Local Area Network	2
WuRX	Wake-up Receiver	132
VC	Voltage-to-Current	52
VCO	Voltage Controlled Oscillator	20
VGA	Variable Gain Amplifier	7

Chapter 1

Introduction

1.1 Motivation

In the last few years a great explosion has been seen in Internet of Things (IoT) devices and connected products, such as wireless sensors, smart meters, home automation systems and wearables. The lowered cost of components such as sensors and processors along with increasing wireless connectivity has resulted in many products being made "smart" and able to communicate with each other without human intervention. Successful products must meet often competing requirements including long time reliable wireless connectivity, higher processing power and especially low power consumption. Because wireless nodes are usually deployed in remote or inaccessible locations and requirement of thousands of wireless nodes in a large scale network, and in most case they have to be powered by batteries. It's not acceptable to frequently replace batteries of wireless nodes, thus an ultra low power solution has to be adopt to guarantee a several-year lifetime. RF transceiver is the critical block in wireless nodes and consumes the majority of battery energy.

On the other side, IoT applications are built based on a previous generation of networked embedded systems by adding sensors, Internet gateways and cloud applications. It increases the flexibility and power of networked embedded systems by providing Internet on-ramps and end-to-end access. As more applications emerge, architectures need to be flexible enough to adapt to varying requirements and feature sets where the

functionality may be located anywhere along the IoT components. Many IoT applications require the RF transceiver must support combination of the short range standards namely Bluetooth (BT), Bluetooth Low Energy (BTLE), ZigBee, Smart metering Utility Network (SUN), Wireless Body Area Network (WBAN) and Wireless Local Area Network (WLAN). The variety of these applications and their implementation requirements are generating the demand of the co-integration System-on-Chip (SOC) solutions. However, it is typically challenging to find enough room inside an IoT device to support multiple wireless communication standards, whose form-factor expectations are set by increasingly thin tablets and smart-phones. Meanwhile the IoT market is surprisingly price-sensitive than other smart devices.

Moreover, IoT brings diverse technologies of a range of developments and acquisitions closer together, from silicon to software. It is more likely someone who might have limited RF experience is assigned to develop the end-to-end IoT products. The device manufacturers must rely on RF solutions so that they can quickly and cost-effectively add to their IoT products instead of having to develop the entire RF components or heavily customize the products. The more development overhead, the tougher it is for manufacturers to price their products competitively yet profitably. Therefore, a flexible and easily customizable platform for IoT is highly needed in the open market.

In general, the variety of these IoT application and implementation requirements are generating the demand of low power, low cost, high flexibility and easy co-integration SOC. However, the system complexity, chip area, power consumption and product cost grow rapidly when more wireless communication standards and signal processing functions need to be supported.

1.1.1 Goal of the Work

The goal of this thesis is to provide simple, low effort and efficient solutions for short-range IoT communications, which needs to handle multiple short-range wireless standards on one single die. To support the multiple short-distance standards with low cost hardware, the feasible transceiver solution must be compromised among some key specifications, such as data rate, signal bandwidth, integration level, noise suppression and power consumption. For the short-range wireless communication applications where the constant envelope modulation schemes are usually employed, an optimal solution is to emphasize the high-efficient, low-cost, low-power performance but with satisfactory data rate.

1.1.2 Structure of the Thesis

The whole thesis is organized as follows:

Chapter 2 gives a general background introduction of the variable transceiver architectures, and their tradeoffs are analyzed and compared. Subsequently the typical non-ideal issues presented in the transceiver are introduced. The specifications of

different IoT standards are discussed. Finally the appropriate architecture is selected resulting in the use of a PLL based polar transmitters.

In Chapter 3, Section 1 presents two low power techniques in the frequency synthesizer design. Based on the current-reuse VCO, excellent phase noise is achieved with low power consumption. This section has been published in Radio Frequency Integrated Circuits Symposium (RFIC), June 2013. In Section 2 a new digital architecture is introduced for the direct modulation PLL, which can dramatically reduce the hardware complexity without degrading the frequency synthesizer performance. This section has been published in Microelectronics Journal, July 2014.

Chapter 4 outlines a novel wideband frequency synthesizer architecture for direct frequency/phase modulation. With the help of an adaptive calibration mechanism, the DAC gain is adjusted, resulting in better matching between the PLL signal path and noise cancellation path. Thus the quantization noise and fractional spurs are largely suppressed, which provides an effective and flexible solution for high data rate PLL based transmitters. This chapter has been published in Radio Frequency Integrated Circuits Symposium (RFIC), May 2015.

Chapter 5 provides a low power demodulator architecture for low-IF receivers, which overcomes the issues of image interference and group delay resynchronization with low effort computation. A BT modulated GFSK signal is used as an example, the received signal is robust against image and adjacent channel interferences, and the corresponding SNR requirements are largely relaxed. This chapter has been published in IEEE Transactions on Circuits and Systems I: Regular Paper, September 2013.

Chapter 6 provides a low-effort all-digital clock data recovery system, which can successfully recover the clock signal over the different data rates and resample the received data at the optimum phases. And the carrier frequency offset caused by clock mismatches is fully compensated through a fractional Numerical Controlled Oscillator (NCO). This chapter has been published in IEEE Transactions on Circuits and Systems I: Regular Paper, December 2015.

Chapter 7 concludes the thesis and summarizes the implementation. In the end an outlook containing other low power techniques is provided for further development.

Chapter 2

Fundamentals of Transceivers

2.1 Overview

A block diagram of a wireless communication system in Fig. 2.1 reveals the transformation process the signal undergoes from origination to reception. To a certain degree,the receiver can be considered a reverse implementation of the transmitter.

The transmitter generates a baseband signal and translates into a waveform so that it can be effectively transmitted through the channel. Before the transformation from baseband to a radio frequency channel, the waveform is digitized and coded from bit rate into symbol rate. The coded symbol is then modulated and filtered so that the power efficiency in the interest bandwidth is optimized and the influences of noise and interference are minimized. After converting from the baseband to the Radio Frequency (RF) band, the transmitted signal is amplified and radiated through the antenna. In the non-ideal wireless channel, the transmitted signal gets faded, scattered, distorted by the white and colorful noise, as well as disturbed by the co and adjacent channels. The receiver can be implemented several ways, but certain components exist in all topologies. It extracts the RF signal in the presence of potential interference. A low noise amplifier boosts the desired signal level while minimally adding to the noise of the radio signal. A mixer downconverts the RF signal to baseband with a local oscillator signal. The baseband filter attenuates unwanted frequency components generated by the mixer and signals from adjacent frequency channels. Finally the

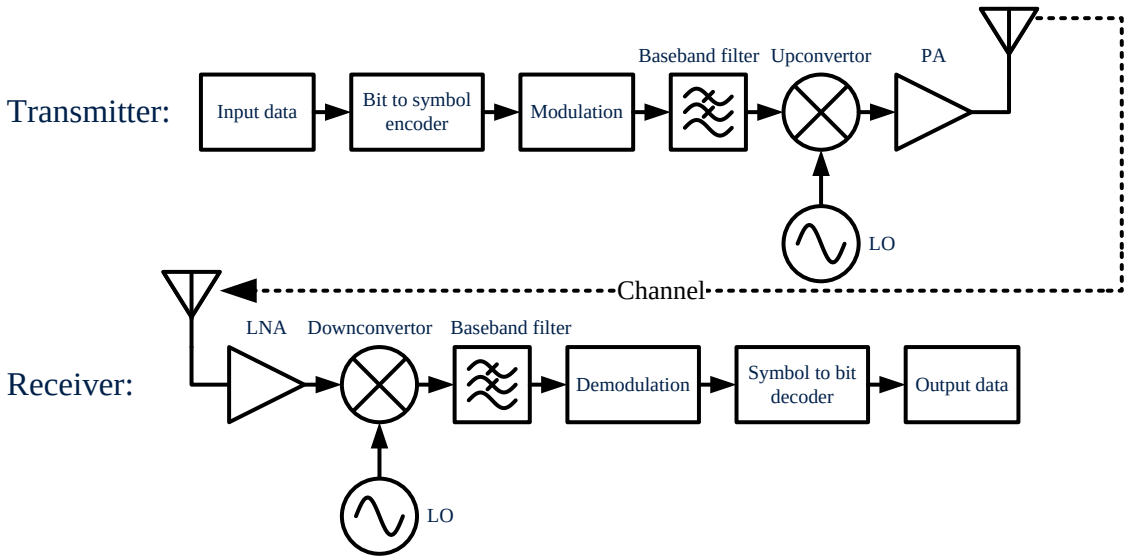


Figure 2.1: System level block diagram of a general transceiver.

baseband signal is demodulated and decoded into the bit rate. Through the correction algorithm, the decision is made, thus the input data is recovered at the receiver side.

In this chapter, various architectures of transmitters and receivers are categorized, and their characteristic performance trade-offs are compared. Then the typical transceiver non-ideality factors quantifying the behavior are summarized. In the following section, the specifications and requirements of several typical short distance standards are discussed. Finally the appropriate transceiver architecture for the short-range standards is conducted.

2.2 Transmitter and Receiver Architectures

2.2.1 Direct-Conversion Transmitter

The most commonly used RF transmitter architecture is direct-conversion (homodyne) modulation transmitter as shown in 2.2. Direct conversion transmitter is very concise in topology compared to other architectures, and it usually occupies minimal chip area.

For a direct-conversion transmitter, the Local Oscillator (LO) frequency is equal to the transmitted carrier frequency. Therefore, the frequency translation from baseband to RF band is implemented in one step. The transmitter features a digital baseband processor which handles symbol coding, pulse shaping filtering and Cartesian modulation, where the Inphase/Quadrature (IQ) signals are generated. Utilizing oversampled Digital-to-Analog Converter (DAC)s, the digital baseband signal is converted to the analog

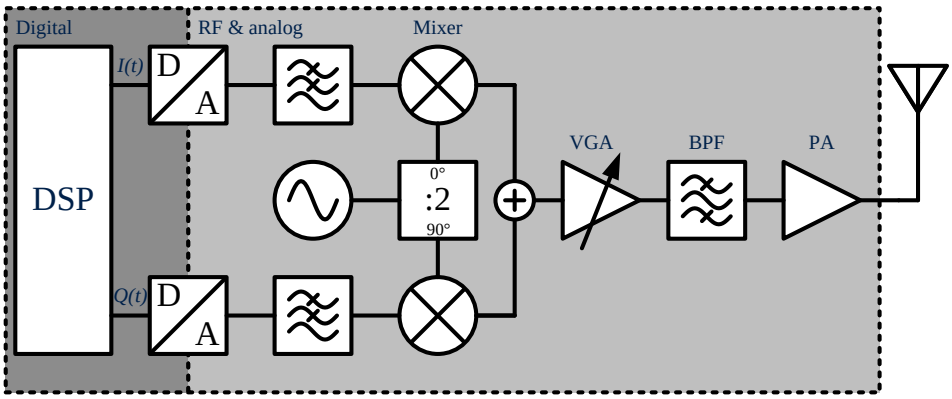


Figure 2.2: Transmitter architecture.

domain. Low-pass filters are used to remove the harmonics caused by zero-order holder style output signal from the DAC. A quadrature upconversion mixer translates the I/Q baseband signals to the RF carrier frequency. The Variable Gain Amplifier (VGA) can be either located at baseband or RF band to adjust an appropriate dynamic range of output power. In the final stage, a power amplifier is used to deliver the optimal signal power to the antenna. The PA is connected to the antenna, which typically has a $50\,\Omega$ input impedance via an impedance transformation network. Finally, an optimum load impedance is obtained at the PA in order to maximize its output power and energy efficiency.

However, the major issues in direct-conversion including LO leakage, Direct Current (DC) offsets, and distortion performance, have made practical implementations difficult. For example, the local oscillator energy can leak through the mixer stage back and feedback to the antenna input and then re-enter the mixer stage. The overall effect is that the local oscillator energy will self-mix and create a DC offset signal. The offset could be large enough to overload the amplifiers and overwhelm the wanted signal transmission. There are subsequent modifications to deal with this issue but added to the complexity of the transmitter.

2.2.2 Outphasing Transmitter

The outphasing, also known as LInear system with Nonlinear Components (LINC) architecture is aiming to solve low power high efficiency issue by using saturated PA and power combination technique. The idea behind outphasing transmitter is to overcome the non-equal envelope amplifier power loss problem. As shown in Fig. 2.3, the to-be-transmitted variable envelope waveform is decomposed into two constant envelope signals $S_1(t)$ and $S_2(t)$, which are individually amplified. Hence, the output power of the amplifiers $S_{out}(t)$ is combined to reconstruct the variable-envelope signal:

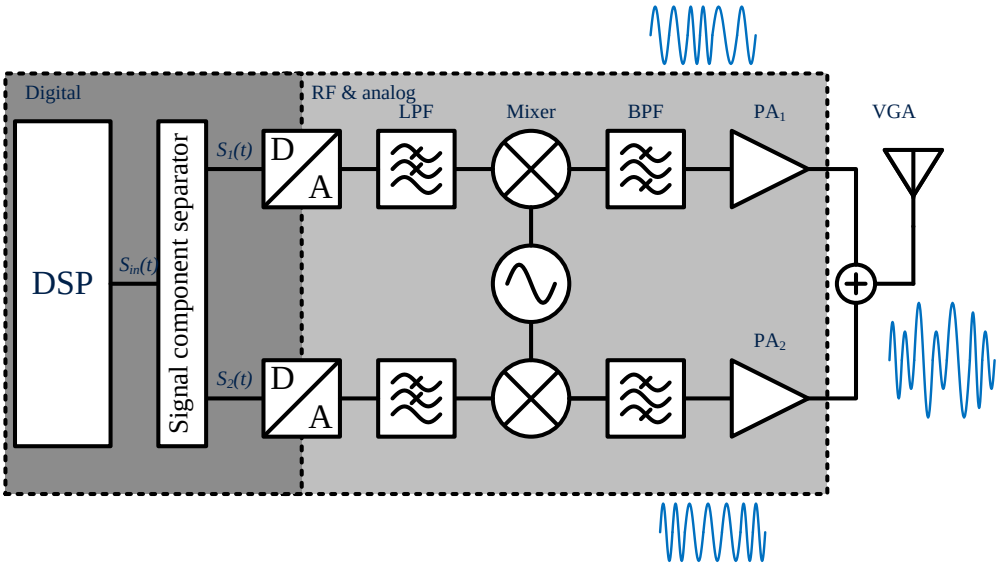


Figure 2.3: Outphasing transmitter Architecture.

$$
\begin{aligned}
S_1(t) =& A_{max}(t)e^{\omega_c t+\theta_1(t)} \\
S_2(t) =& A_{max}(t)e^{\omega_c t+\theta_2(t)} \\
S_{out}(t) =& G(S_1(t)+S_2(t))
\end{aligned}
\tag{2.1}
$$

For the multi-level outphasing transmitters, two power amplifiers can provide a discrete set of envelope amplitudes individually. Fine envelope amplitude modulation is still done by outphasing modulation. Since the PAs in the outphasing system only deal with constant-envelope signals, they keep operating in saturation with peak efficiency. It is capable of transmitting very wideband signals and are thus suitable for wideband communication in multi-standard applications. Usually for an RF bandwidth above 20 MHz such as broadband OFDM modulation, the outphasing transmitter concept provides a promising solution.

However, comparing to direct-conversion architecture, the outphasing receiver needs additional power combiner. Thus the chip area is almost doubled. There is possible chance to optimize the onchip circuit since only the phase signal of each branch needs to be tuned. Due to the large bandwidth of the phase signal, direct phase control of each branch needs at least 3 times the bandwidth than original IQ signal.

The main limitation of outphasing transmitter is that the power efficiency of outphasing stays poor at large power back-off, which is a critical drawback for wideband signals with high Peak-to-Average Power Ratio (PAPR). It will cause signal distortion such as in-band distortion and out-of band radiation due to the non-linearity of the high power amplifier and a worse bit error rate.

2.2.3 Polar Transmitter

The polar transmitter can overcome the low efficiency issue at the power amplifier, because its input power is dynamically controlled by the envelop signal, and its power amplifier is always operating in the saturation mode. A polar modulator transmitter is based on the decomposition of the RF signal into a magnitude and phase component. The phase component is an RF signal with a constant envelope, and the magnitude component is essentially the envelope of the modulated signal. The envelope signal is extracted from the baseband signal and then multiplied with phase modulated RF oscillating carrier signal. The signal translation from Cartesian domain to polar domain is expressed as:

$$\begin{aligned} A(t) =& \sqrt{I(t)^2 + Q(t)^2}, \\ \theta(t) =& \tan^{-1} \frac{I(t)}{Q(t)}. \end{aligned} \tag{2.2}$$

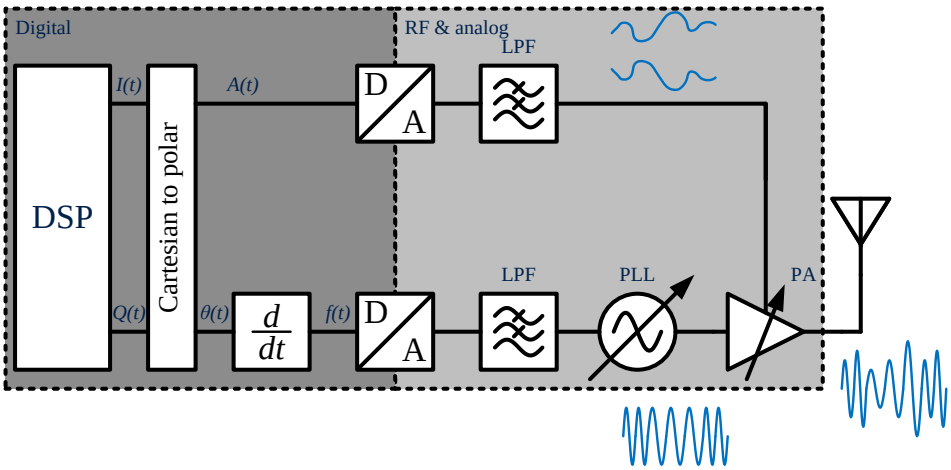


Figure 2.4: Polar transmitter Architecture.

A typical implementation example of a polar modulator is shown in Fig. 2.4. The polar signal components $A(t)$ and $\theta(t)$ can be generated by digital signal processing using the COordinate Rotation DIgital Computer (CORDIC) algorithm or a look-up table. The amplitude component $A(t)$ is amplified by a linear low frequency power amplifier or supply voltage modulator. The phase component $\theta(t)$ has to be modulated on the RF carrier. The phase modulation could be converted to frequency modulation to control a PLL, given that the PLL bandwidth is high enough.

In direct-conversion architecture, the phase carrier signals exist in both I/Q paths to up-convert the baseband signal, so the impact of phase noise to cause signal quality loss

is doubled. And the PLL phase noise requirement is reduced in the polar architecture. However, it needs a careful matching of the phase path and amplitude path. And the bandwidth of the amplitude and phase modulation signal are needed to extend to at least 2 times larger than Cartesian modulation.

Since the power efficiency is the key performance in relatively narrowband IoT communication standards, Polar modulation transmitter is more feasible than outphasing transmitter for the complete CMOS integration solution.

2.2.4 Heterodyne Receiver

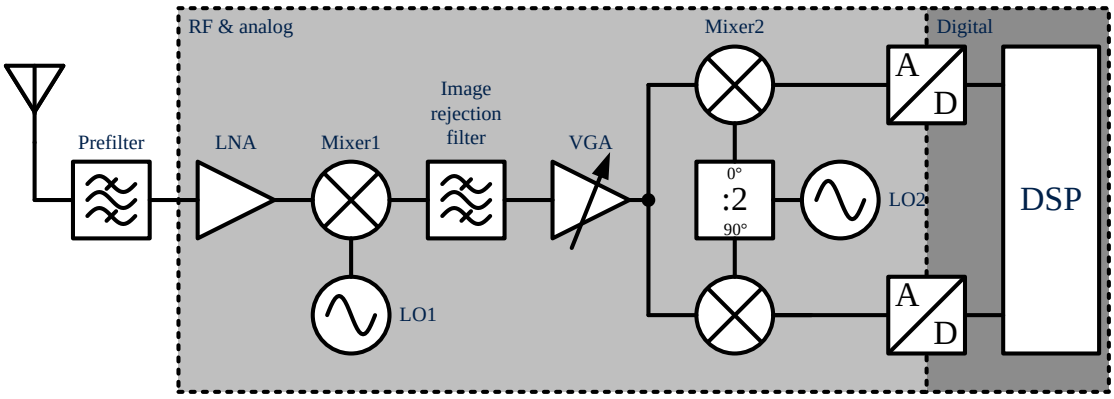


Figure 2.5: Heterodyne receiver architecture.

Unlike the direct-conversion architecture, heterodyne receiver translates the desired RF frequency to one or more intermediate frequencies before demodulation. As shown in Fig. 2.5. Following the LNA, the first mixer with a tunable local oscillator (LO1) downconverts the received signal from radio frequency to an intermediate frequency. A high-Q bandpass filter is used to extract the wanted signals from the neighboring channels and remove the interference. Subsequently a second quadrature mixer is implemented to shift the selected IF signal to the baseband. Finally the baseband ADCs digitize the baseband signals for the further signal process.

Compared to the zero-IF architecture, heterodyne receiver has higher inherent immunity to DC offsets and 1/f noise. But the undesired Spurious at the IF frequency in addition to the desired signal may degrade the receiver sensitivity. This Spurious known as an image interference must be filtered out before reaching mixer stages in the Heterodyne receiver. Thus the IF channel filter is required for protection against the image. However, the IF channel filter in particular requires high Q resonators for its implementation, as it needs to greatly attenuate the image interference. It makes Heterodyne more difficult for the high level integration. In some cases discrete components are still needed to provide the high Q bandpass filtering.

2.2.5 Homodyne Receiver

The task of a wireless receiver is to select a wanted signal at the antenna and make it accessible for further signal processing. Usually, signal processing is implemented at low frequencies and thus frequency down-conversion of the received signal is required. Moreover, the receiver is subject to interferences from the environment, which requires filtering to separate the wanted signal from disturbances. Different receiver architectures have been invented to address these issues in different ways, among which the homodyne (direct-conversion) and heterodyne (Intermediate frequency (IF)-conversion) receiver architectures are the most well known.

A homodyne, direct-conversion, or zero-IF receiver is shown in Fig. 2.6. It translates the desired RF frequency directly to baseband for information recovery. An off-chip bandpass prefilter is placed after the antenna for the band selection. The received signal is amplified by a Low Noise Amplifier (LNA), which has enough gain to amplify a weak signal above the noise of the mixer. The mixer directly converts the RF signal to the baseband. The channel is directly selected by tuning LO frequency to the center of the desirable channel. The subsequent lowpass filter removes neighboring channels and interferer prior to ADC. Because of the simplicity, it provides one of the best opportunities for system-on-chip solutions. Baseband signals are typically at frequencies substantially below the carrier frequencies. On the low end of baseband, signals may approach or include DC. A nonlinear circuit known as a mixer translates the RF frequency directly to baseband. The LO signal, tuned to the same frequency as the desired RF signal, is injected into the mixer. The RF and LO signals get mixed to produce the baseband frequency. Some digital radios also employ an I/Q mixer to recover baseband information.

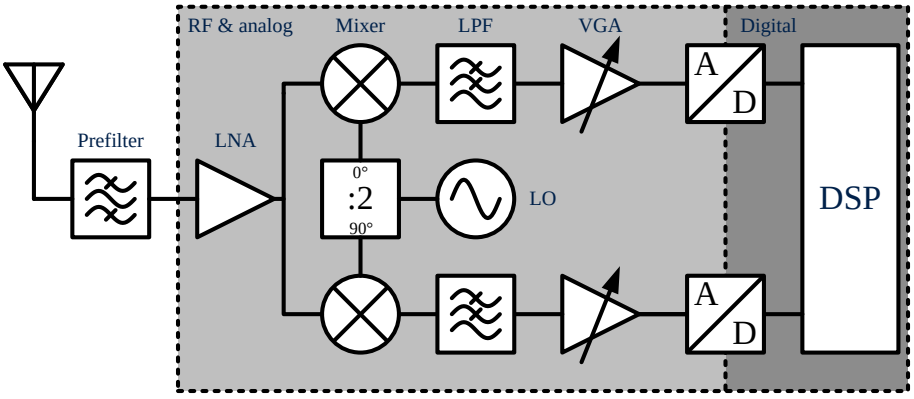


Figure 2.6: Homodyne receiver architecture.

An advantage of the zero-IF receiver is easy for higher levels of integration, as no image exists and an image-reject filter is not required. But the problems are associated

with this architecture. The unintentionally transmitted LO signal may reflect off of nearby objects and be "re-received", consequently be self-mixed with the LO resulting in a time-varying DC offset. Additionally, because the sideband image resulted from the I/Q phase and gain mismatch is located at the baseband frequency and overlaps with the desired carrier signal, an appropriate adaptive digital signal processing used to correct the image component must be considered.

2.3 Non-Idealities in Transceiver

Most communication theory works with idealized transceiver assumptions neglecting imperfections and defects of practical transceiver designs. In reality, there exists challenges and opportunities in understanding wireless transceiver non-idealities. The key imperfection factors in the transceiver design are illustrated in the following.

2.3.1 Noise Figure

Random fluctuations of physical quantities such as current and voltage are called noise. Because these random signal variations are unrelated to the wanted signal, they can deteriorate detection of the wanted signal when its signal power is close to the noise power. Therefore, the minimum detectable signal power is set by the noise power present in a circuit.

Noise in CMOS circuits is mainly caused by three different processes: thermal noise, shot noise, and flicker noise. Thermal noise is the electronic noise generated by the thermal agitation of the charge carriers inside an electrical conductor at equilibrium, which happens regardless of any applied voltage. Shot noise is caused by charging carriers randomly passing a potential barrier such as a pn-junction or the gate barrier if significant gate leakage is present in a MOS transistor. Both of the above noise have a constant spectral power density and can be modeled as white noise. Flicker noise is caused by trapping and releasing of charge carriers at imperfections at the interface between silicon and oxide. Typically the time constants of these processes give rise 1/f frequency dependence.

The noise of a circuit block is represented in terms of input referred noise voltage or noise current so that the actual circuit itself can be considered as noiseless. The Noise Factor (NF) is an easy measurement for the Signal-to-Noise Ratio (SNR) degradation:

$$F = \frac{SNR_{in}}{SNR_{out}}. \tag{2.3}$$

In a receiver, several noisy circuit blocks are cascaded to form the complete chain. If the noise figure of each individual circuit block have been characterized by simulations or measurements, the total receiver noise figure can be calculated. For the case of power matched inputs and outputs, Friis formula is used to calculate the cascade noise

figure. If the input impedance is not well defined, as is usually the case for all blocks succeeding the LNA in an integrated receiver, a description in terms of input referred noise sources is preferred. According to the Friis formula, the cascade noise factor is calculated as :

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \tag{2.4}$$

Note that the total noise factor is dominated by the first stages G_1 as the noise factor of the stages downstream is scaled down by the preceding gain. Therefore, it is vital for overall noise performance to have low noise and high gain in the first stage.

2.3.2 Nonlinearity

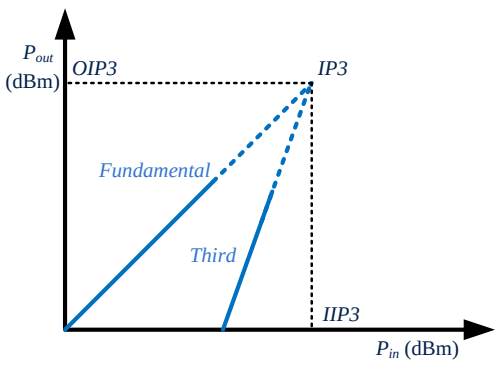


Figure 2.7: Intercept point $IP3$.

The linearity of a receiver plays an important role in the overall performance. It affects the receiver sensitivity and link budget. The linearity of the receiver is best summarized in the concept of equivalent Input Intercept Point (IIP) of the receiver, which takes into consideration the effect of non-linearity of each stage. A third-order Intercept Point ($IP3$) illustrated in Fig. 2.7 is a popular specification for weakly nonlinear systems. It is based on the idea that the device non-linearity can be modeled using a low-order polynomial, derived by means of Taylor series expansion. 3rd-order products lie near in frequency to the two input tones and are therefore very likely to fall inband at the output. As a device is driven further into its nonlinear region, the amplitude of the third order products increases while the power of the input tones decreases. If the device is not limited in output power, then the powers of the intermodulation products would increase in power until they are eventually equal in power with the input tones at the output. Calculating the cascaded values for $IP3$ for the system budget requires the the gain and $IIP3$ value for each stage through the Friis formula:

$$\frac{1}{P_{IIP3_{all}}} = \frac{1}{P_{IIP3_1}} + \frac{G_1}{P_{IIP3_2}} + \frac{G_1 G_2}{P_{IIP3_3}} + ... \tag{2.5}$$

Note that the overall IIP3 is dominated by the IIP3 of the latter stages of the receive chain because it is scaled down by the total preceding gain.

2.3.3 Adjacent Channel and Co-Channel Interference

One of the most important issues that need to be considered while designing a multi-channel multi-radio wireless transceiver is the adjacent and co-channel interference effects due to the close proximity of the radios in a node. As shown in Fig. 2.8, the adjacent channel interference is that the channel directly above or below the neighboring channel causes unwanted emission at the wanted channel in the receiver since it can not be sufficiently suppressed. Any signal in the pass band of the filter will be considered as a desired signal. There fore, the attenuation in the stop band should be enough to avoid that any interference in adjacent channels affects the dtected signal. Co-channel interference is crosstalk from two different radio transmitters using the same frequency.

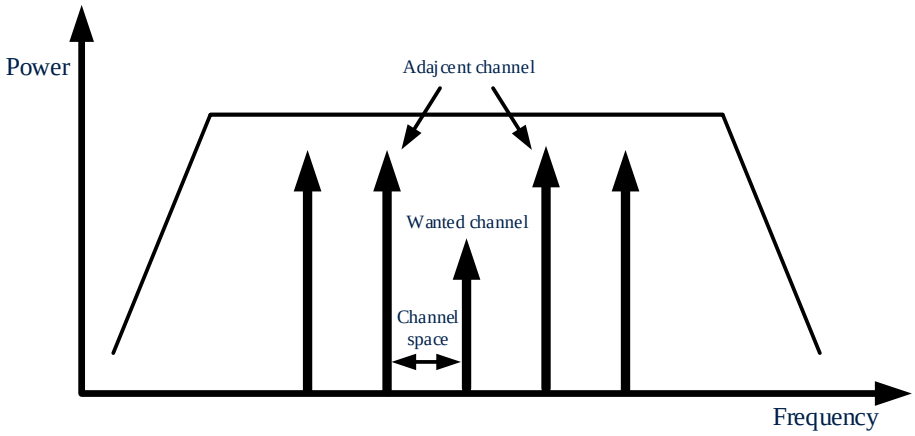


Figure 2.8: Adjacent channel interference

Due to the large dynamic range of mobile radio signals, the adjacent channel and co-channel interference can be significant. Hence, the minimum requirement for transceiver hardware so that adjacent-channel interference is limited to values that do not affect the performance significantly needs to be investigate. If the requirement is not fulfilled, the users within a cluster can interfere with each other, and this interference has to be taken into account for the link budget.

2.3.4 I/Q Mismatch and Image Interference

I/Q signal processing receiver architectures like the homodyne receiver and Heterodyne receiver are of great value for reconfigurable radio applications. Since no fixed analog image rejection filter is needed, such architectures allow cheap and highly flexible analog front-ends. In theory, in the finite image rejection is provided if the complex analog oscillator has equal amplitudes and a phase difference of exactly 90° between the I and the Q branch of the signal processing path. However, unavoidable imbalance between the I and Q branch lead to a limited image attenuation so that the image signal is leaked to the desired band. Fig. 2.9 shows an example of image interference during the downconversion process in the heterodyne receiver.

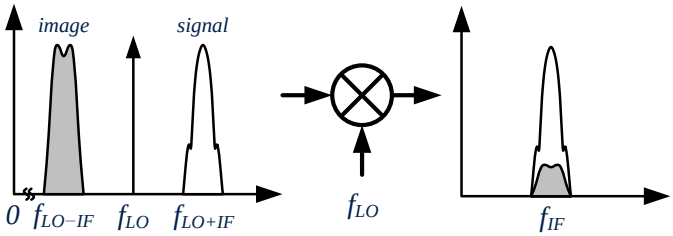


Figure 2.9: Image interference.

The rejection of the image signal is a problem inherent to all receiver architectures. Especially the limited image attenuation is a major concern in low-IF receivers. Due to the non-zero IF, the image signal originates from a different carrier frequency than the desired signal and can therefore be much stronger than the desired signal. For example, the Bluetooth standard specification stats that a signal of −67 dBm must be detected with a maximal 0.1% BER when a signal of −58 dBm is applied at the image frequency.

2.3.5 Clock Synchronization

Having a synchronized clock, i.e., all nodes having a common notion of time, is one of the most fundamental requirements in wireless sensor networks. Clock synchronization is critical for data transmission, localization, sleep scheduling and information fusion. However, due to the imperfect crystal cutting and clock circuit, the output value of a node's local clock, namely the local time, is often different from others' local time, leading to the clock offset. An unregulated clock offset will degrade the network performance and even endanger the proper network functioning.

In modern electronic systems, a crystal oscillator is usually used to generate the clock ticks, which are periodical signals with certain frequency. However, the output frequency of the clock tick is not always the same as the nominal frequency changes

according to the working environment. The deviation of the output frequency results in different clock tick durations and clock skew, which is the instantaneous clock drift rate between two or more clocks. It is the inherent reason for clock de-synchronization. The output value of a clock is the counting number of its ticks and therefore the effect of clock skew will be accumulated and lead to an unbounded clock offset. Thus the clock needs to be re-synchronized to maintain the clock synchronization accuracy. It is obvious that if the clock skew is estimated and compensated, the clock synchronization accuracy can be improved and therefore one can prolong the clock re-synchronization period.

2.3.6 Frequency Offset

In a mobile communication system, a carrier frequency offset is commonly caused by inaccuracy of analog/RF circuits and by an attempt to reduce the final system implementation cost. For example, a 2.4-GHz ZigBee receiver may have an offset frequency of up to 80 ppm when two ZigBee radio transceivers communicate to each other. Due to the oscillator mismatching from individual clocks, a frequency offset usually exists between the transmitter and the receiver. If there is an error in the transmitter carrier frequency and the receiver LO frequency, there will also be an error in the IF frequency. The frame synchronization scheme presented may not work properly under such condition. An additional circuit technique is essentially required to compensate for the large frequency offset.

2.3.7 Group Delay Distortion

Group delay is defined as the derivative of the phase with respect to angular frequency, and it is a measurement of the distortion in the signal introduced by phase differences for different frequencies. For example, ideally the IF filter which attenuates out-of-channel noise should be flat across the frequency band of interest, and its group delay should be constant across the same frequency band. Errors in the design of this filter can affect the overall signal. IF filter problems include filter tilt or ripple in the frequency response and variations in group delay. Filter tilt or ripple in the frequency response causes linear distortion in the signal. Improper matching of any component between the antenna and the IF filter also causes tilt or ripple. For example, mismatch between the preselect filter and the LNA causes reflections that result in distortion of the overall frequency response of the receiver and inconstant group delay.

2.3.8 Phase Noise

A practical oscillator does not produce a carrier at exactly one frequency, but rather a carrier that is phase modulated by random phase jitter. This imperfection translates

into random deviations of instantaneous phase or frequency, typically modeled as phase noise.

Phase noise is a key design parameter for wireless transceiver designs. In the transmitter side, the local oscillator noise is amplified by the subsequent stages and is eventually fed to the antenna together with the wanted signal. Therefore, the wanted signal is surrounded by a band of noise originating from the local oscillator, and spreading over several MHz masking. Since phase noise can have a significant effect on the Error-Vector Magnitude (EVM), it's critical to verify the phase noise performance of the LO during the development process. In the receiver side, during the reciprocal mixing processing, the phase noise from LO signal is translated to the IF or baseband domain. Sensitivity and BER performance of the receiver are influenced.

Based on the required Signal-to-Interference Ratio (SIR) at the output of the mixer, the input blocker level S_B, the desired signal level S_D and the receiver noise bandwidth B, the required LO noise performance L in dBc/Hz can be calculated as:

$$L = S_D - S_B - SIR - 10\log_{10} B. \tag{2.6}$$

For example, Fig. 2.10(a) shows the Bluetooth blocking signal level requirements at the antenna input. The received signal should be corrected demodulated with 0.1% BER performance for the desired signal sensitivity of −70 dBm. SIR is specified to be larger than 11 dB at the channel bandwidth offset of 1 MHz. The LO signal phase noise requirement at different offset frequencies is shown in Fig. 2.10(b). Notice that the actual phase noise specification must be slightly better to account for the degradation due to the frontend thermal noise.

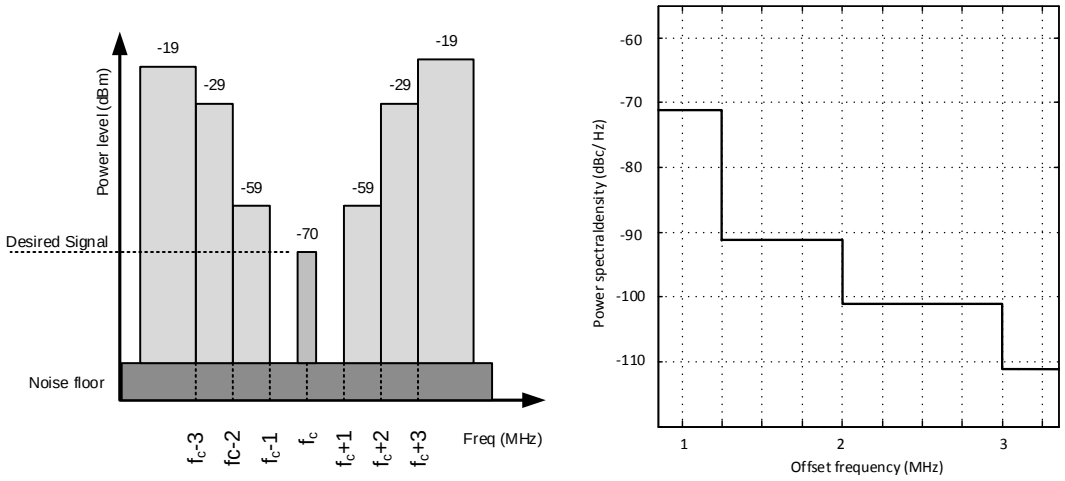
2.4 Short-Range Wireless Standards

A number of different wireless technologies have been developed for very short distances, in which the signals travel from a few centimeters to several meters. Examples of short-range wireless communications are Bluetooth, ZigBee, SUN and WBAN.

2.4.1 Bluetooth

BT is a proprietary open wireless standard for short range communication which was proposed to be a low cost, low power, radio based replacement for cable. It operates in the globally-unlicensed 2.4 GHz ISM-band in 79 channels, where the frequency hopping is deployed across the entire band. It has been optimized to allow for large amounts of uncoordinated communication to take place in the same area. It effectively competes with ANT+.

Unlike most other ad-hoc technologies where all units in range use the same channels, Bluetooth allows for independents channels, with each channel serving a limited numbers of users. Especially the latest Bluetooth Low Energy technology has remarkable an



(a) GSM blocking signal level requirements. (b) Phase noise requirement of LO signal

Figure 2.10: LO signal phase noise calculation

improvement so that theoretically it can connect endless number of devices. By the implementation of Frequency-Hop Spread Spectrum (FHSS) technique, the Bluetooth signal with GFSK modulation is spread on a large frequency range but only a small bandwidth is occupied instantaneously, avoiding most of the potential interferences in the ISM band. Standard range is about 10 meters and up to 100 meters at maximum power with a clear path.

2.4.2 ZigBee

ZigBee (IEEE802.15.4) is a short range wireless standard operating at 868 MHz, 915 MHz and 2.4 GHz which is very similar to Bluetooth. It is optimized for industrial sensors, smart grids, and low-duty cycle operation such as medical applications. Compared to Bluetooth, it offers lower data rate and lower power consumption. Good flexibility is provided with reliable and secure communication. Elements such as sensors and controls of an active network don't need high bandwidth but low battery consumption. A ZigBee network is designed to communicate at 1 mW of radio frequency power. It is the standard technology which is addressed to applications like remote monitoring, control and sensor network functions for short distance communication.

Three basic frequency ranges are defined in ZigBee standard. The most widely used carrier frequency is 2.4 GHz ISM band (16 channels). The basic data rate is 250 kbps. Another range is the 902-928 MHz ISM band in the USA (10 channels) with the data rate of 40 kbps or 250 kbps. There's also the European 868 MHz band (one

channel) with a data rate of 20 kbps. All three ranges use Direct Sequence Spread Spectrum (DSSS) with either BPSK or OQPSK modulation supported by 2 MHz RF bandwidth. The multiple access mode is Carrier Sense Multiple Access (CSMA) with collision avoidance. The minimum defined power levels are −3 dBm and the most common power level is 0 dBm. Typical range is less than 10 meters.

2.4.3 SUN

SUN (IEEE802.15.4g) radio standard is a global wireless networking standard enabling interoperable communications between smart grid devices, including smart meters and smart home appliances, which aims to support low power low data rate and advanced utility management system. Based on FSK modulation involving simple system architecture, the data rate is typically less than 1 Mbps with battery life span of several to ten years. Connectivity to at least 1000 neighboring devices is a principal requirement in the network design. These design characteristics are essential to meet the demands of the large and rapidly growing number of metering devices.

2.4.4 WBAN

WBAN (IEEE 802.15.6) supports a variety of real-time health monitoring and consumer electronics applications such as the long term electron physiology signal (ECG, EEG) monitoring, the digestive tract imaging with the wireless endoscope capsule, and the real-time pressure sensing in artificial joint replacement surgery. It aims to provide an international standard for low power, short range, low-rate and extremely reliable wireless communication within the surrounding area of the human body, supporting a vast range of data rates for different applications. Short-range, wireless communications in the vicinity of, or inside, a human body (but not limited to humans) are specified in this standard. It uses existing ISM band as well as frequency bands approved by national medical and/or regulatory authorities.

2.4.5 Specification Comparison

The use of wireless has expanded geometrically over years thanks to new wireless standards and very low-cost transceiver chips and modules. Wireless has become an easy and relatively low-cost addition to almost any new product where a wireless feature can enhance performance, convenience, or marketability.

In all the mentioned short-rage standards, the demand of low cost, high flexibility, efficiency and long battery life is always emphasized as long as a secure wireless communication is built with sufficient data rate. Also the low complexity modulation schemes such as GFSK, BPSK are preferred rather than Orthogonal Frequency Division Modulation (OFDM) or Code Division Multiple Access (CDMA). Therefore, the low effort short-range technology has opened the door to many new convenient IoT

applications. The key physical layer specifications of these standards are listed in Tab. 2.1.

Table 2.1: Specification comparison of short-range wireless standards.

Standards	Bluetooth	ZigBee	SUN	WBAN
Distance	10 m-100 m	10 m	100 m	very short
Carrier frequency	2.4 GHz	900 MHz 2.4 GHz	900 MHz 2.4 GHz	400 MHz, 900 MHz 2.4 GHz
Modulation schemes	GFSK	OQPSK BPSK	2/4-FSK OFDM	FSK
Data rate	1 Mbps	<250 kbps	FSK <200 kbps OFDM <800 kbps	<200 kbps
Sensitivity	−70 dBm	−85 dBm	−90 dBm	−90 dBm

2.5 Appropriate Transceiver Architecture for Short-Range Standards

2.5.1 Two-Point Modulation PLL Based Transmitter

A technique in polar transmitter which enables relatively high bandwidths is two-point modulation. Fig. 2.11 depicts the block diagram of a Phase Locked Loop (PLL) based two-point modulation transmitter. The purpose of PLL is to allow the phase of one signal to precisely track the phase of another signal. The phase detector compares the phase of the input signal to the phase of a divided-down Voltage Controlled Oscillator (VCO) output signal, and converts any difference between the phases into an error voltage signal. This signal is then applied to the loop filter, and the filtered output signal is used to modulate the VCO. When the system is locked, the VCO output is phase-locked to the input signal, and changes in input signal phase will be developed at the VCO output. The implemented transmitter utilizes a polar loop architecture that consists of phase modulation using two-point modulation and amplitude modulation using a VGA. By splitting the modulated signal into two portions and sending one portion to the VCO input and the other to the $\Sigma\Delta$ modulator, constant modulation sensitivity regardless of the PLL loop bandwidth is achieved.

In the two-point modulation circuits, the strict relation between the PLL bandwidth and modulation bandwidth can be alleviated. Hence, the loop bandwidth can be decided for other requirements, such as a narrow PLL bandwidth for low out-of-band

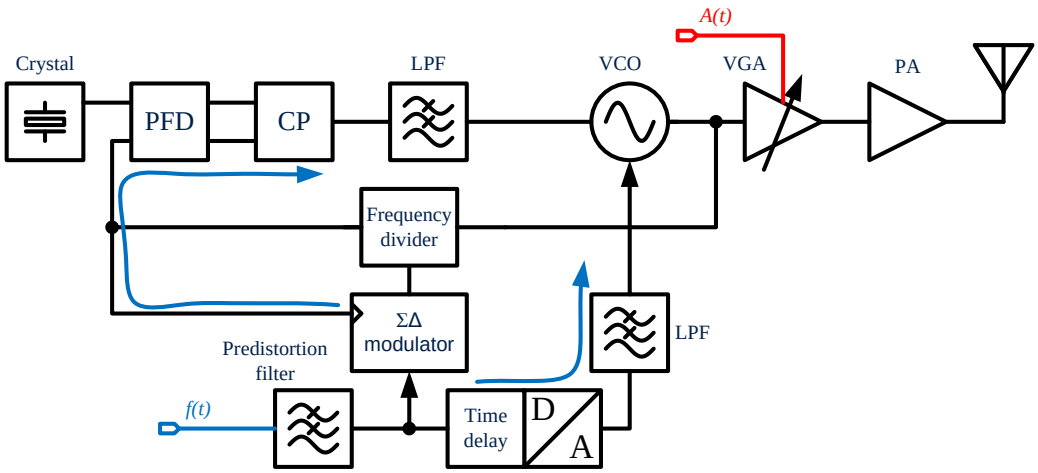


Figure 2.11: Two-point modulation based polar transmitter.

noise. In addition, RF circuitry using two-point modulation can be implemented at low cost with high integration. This method can easily provide multi-band and multi-mode functionality. Therefore, it provides a promising solution for various wireless applications that support a wide bandwidth and various frequency bands. However, in the two-point modulation, the timing and the gain matchings between two modulation paths are challenging issues to prevent signal distortions. In order to resolve these problems, accurate timing control and gain matching should be achieved under process and temperature variations conditions. Besides, the design of the VCO control port is crucial to performance, because the dynamic range and linearity at the VCO control port affect the modulated signal quality. But for the low cost, low power, short range IoT standards with low to moderate data rates, the two-point modulation technique results in an essentially constant modulation sensitivity without regard to the PLL loop bandwidth. It is an effective way to serve the needs of systems requiring a modulation frequency response extending to DC.

2.5.2 Low-IF Receiver

Low-IF receiver combines the advantages of both the IF and zero-IF receiver. The RF signal is downconverted to a frequency close to baseband, but not including DC. Typically IF frequency is chosen within the first or second adjacent channels. Thus the problem of DC-offset is eliminated, and the effects of flicker noise of MOS transistors and distortion are notably reduced. The use of a non-zero IF re-introduces the image issue. However, when there are relatively relaxed image and neighboring channel rejection requirements they can be satisfied by carefully designed low-IF receivers. Image signal and unwanted blockers can be rejected by quadrature down-conversion and subsequent

filtering.

Fig. 2.12 shows an example of the low-IF receiver architecture. After the signals are received by the antenna and amplified by the LNA, the wanted and the image signals from RF band are downconverted to the IF band, but both signals are not superimposed on each other due to complex combination. For example, if the wanted signal is situated at positive IF frequency, the image signal is inversely situated at negative IF frequency. Therefore, the image leakage problem does not take place as the zero-IF architecture. A tunable local oscillator selects the desired RF channel through mixing. The image from down-conversion is now different from the wanted signal, and it has to be taken care of processing after the mixing stage. This can be achieved by an integrated complex bandpass filter. The complex bandpass filter usually is realized with a polyphase filter, which is centered at IF frequency and suppresses its inverse frequency. After filtered by the polyphase filter, the wanted signal is separated from the neighboring channels and is ready for sampling. A bandpass complex ADC also centered at IF frequency is used to digitize the receiving analog signal. In this way, the digital circuit needs to handle signals at IF frequency. A second quadrature mixer is implemented in digital domain, which shifts the complex IF signal to the baseband to implement the digital signal decoding.

Low-IF receiver is an efficient and low cost structure for the IoT applications. Because the low frequency filtering is easy to implement in analog circuits, and the ADC power consumption is also reduced since its sampling frequency is also reduced. On the other side, it maintains the advantage of IF receiver for the DC offset and flicker noise rejection. Using advanced analog and digital signal processing techniques, low cost and high quality performance can be simultaneously achieved.

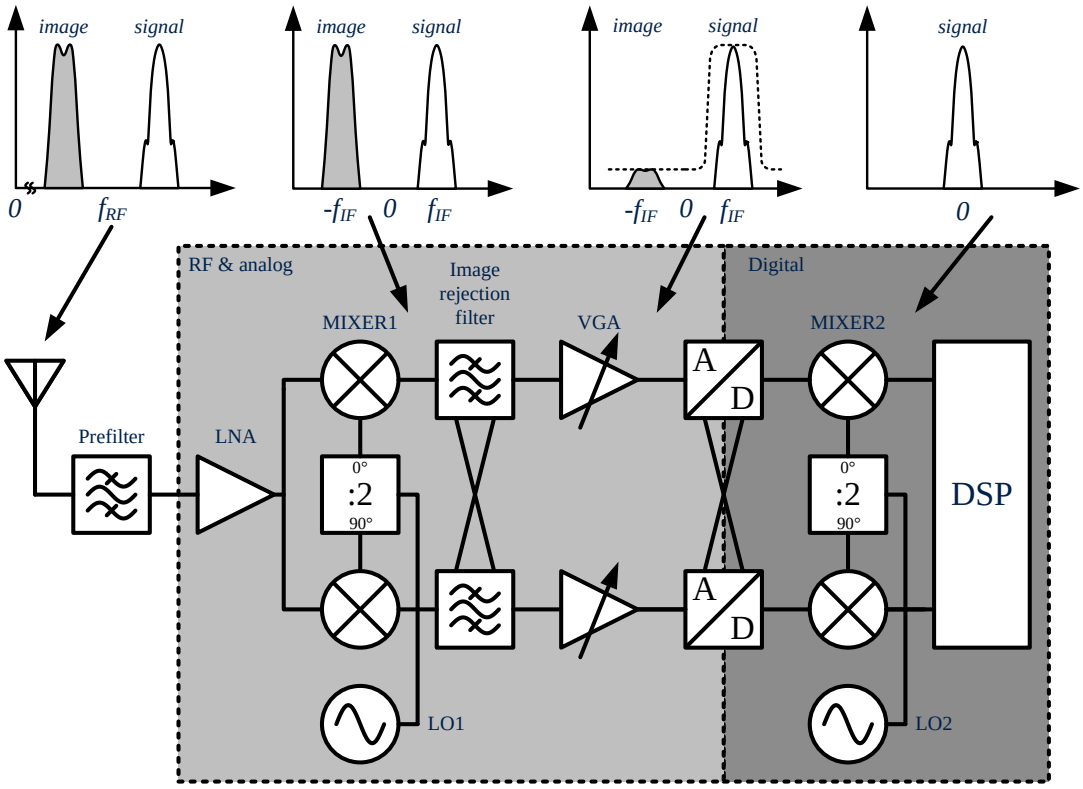


Figure 2.12: Low-IF receiver architecture.

Chapter 3

Low Power Techniques in Frequency Synthesizer Design

In a transceiver chain, the frequency synthesizer plays a crucial role of driving the complex mixers to down-convert the received RF signals into the IF or baseband or up-convert the transmitted baseband signal to the desired RF band. Frequency synthesizer is the engineering discipline dealing with the generation of multiple signal frequencies from a common reference or time base. By changing the frequency division ratio or VCO control voltage with the baseband data rate, the frequency synthesizer can realize frequency/phase modulations. As the frequency synthesizer always operates at the highest frequency in the whole transceiver chain, power reduction in the synthesizer design always draws big attention.

In a fractional-N frequency synthesizer, by shaping the quantization noise towards higher frequency offsets, the $\Sigma\Delta$ modulation technique provides a fine frequency resolution with low phase noise. However, in the direct frequency/phase modulation, high frequency noise and spurs caused by $\Sigma\Delta$ modulator limits the bandwidth extension, since the noise cannot be sufficiently suppressed by the loop filter [Tem+04; MP06]. With the help of an additional noise cancellation path [HKB09; PJG04], the $\Sigma\Delta$ quantization noise is digitally calculated and a compensation charge pump current is injected into the loop filter, where the $\Sigma\Delta$ based digital architecture needs to be optimized to save power and computation complexity.

In this chapter, two techniques for low power low effort frequency synthesizer are introduced. At first, a current-reuse VCO technique is illustrated, where the power consumption of the proposed frequency synthesizer is significantly reduced with excellent phase noise performance. Subsequently a novel digital architecture is presented for the direct modulation PLL, which can dramatically reduce the hardware complexity without degrading the system performance.

3.1 Low Power VCO Design

3.1.1 Overview of Frequency Synthesizer

Frequency synthesizer is a feedback system which causes one signal to track another one. It keeps an output signal synchronizing with a reference input signal in frequency as well as in phase. The basic components are the Phase Frequency Detector (PFD), Charge Pump (CP), VCO, frequency divider and Loop Filter (LPF), as shown in Fig. 3.1. The PFD generates the error signal required in the feedback loop of the synthesizer. Charge pump converts this error signals into currents, which are injected into the loop filter. The output of loop filter controls VCO which generates the output signal of the synthesizer. The VCO output is connected to the divider, generating a relative low frequency feedback signal to compare with references in the phase frequency detector. These components are composed to a negative feedback architecture that allows economic multiplication of crystal frequencies by large variable numbers.

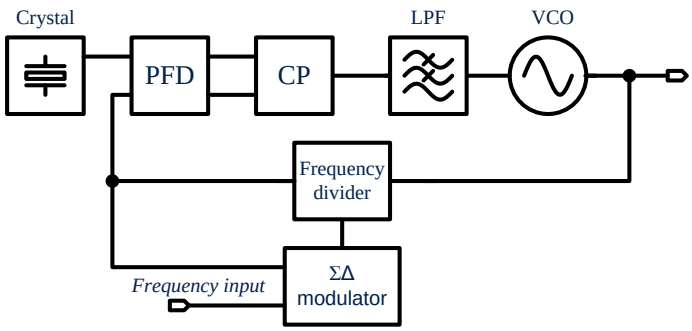


Figure 3.1: Block diagram of a fractional PLL system.

To achieve frequency resolution of a fractional portion, the division ratio of the frequency divider needs to change dynamically during the locked state. For example, if the value of the divider is switched between N and $N+1$ in the correct proportion, an average division ratio can be realized, which is N plus an arbitrary fraction, N_{frac}. This allows the frequency synthesizer to run at a frequency that is not an integer multiplication of reference frequency. $\Sigma\Delta$ modulation is the one of the mostly used

techniques which encodes high resolution signals into lower resolution signals using pulse-density modulation. With the help of oversampling, the Signal Transfer Function (STF) in $\Sigma\Delta$ modulator is unaffected, while the Noise Transfer Function (NTF) is shaped to high frequencies through a high-pass filter. This is the basic meaning of noise shaping: in-band noise is reduced by moving it to out-of-band frequencies.

VCO is an essential building block in the frequency synthesizer, which is operated at the highest frequency in the whole system and attributes large portion of the total power consumption. Low power designs for VCOs have drawn intensive researches recently. Current-reuse techniques for VCO have been proposed and improved in [Yun+05; WCH09; YC05]. It reuses the current from one negative conductance branch and steers it to the other branch to save half the current. However, due to its vulnerable unsymmetrical structure, the current-reuse VCO amplitude is imbalanced, which would lead to a current leakage when differential VCO outputs are used. Secondly, imbalanced amplitude mismatches can greatly degrade the phase noise performance for the frequency synthesizer [HL98].

In this section, a low power frequency synthesizer based on current-reuse VCO with excellent phase noise and reference spur attenuation performance is presented. All the high frequency components are implemented in a single-ended topology to avoid the amplitude mismatch problem. At the same time, the imbalance amplitude problems caused by the unsymmetrical VCO are solved by the pre-tuning mechanism, which automatically chooses the correct frequency band for the certain frequency channel.

3.1.2 Fundamentals of Current-Reuse VCO

Fig. 3.2 shows the simplified schematics of a conventional VCO and a current-reuse VCO. In the conventional VCO, the cross coupled pairs of NMOS transistors provide the negative conductance. In the current-reuse VCO, one of the NMOS transistors is replaced by a PMOS transistor. Hence, both NMOS and PMOS transistors are stacked in series, and the supply current flows from the PMOS to the NMOS. With the current-reuse topology, the coupled negative conductance is generated in one branch. The current consumption can be reduced by half compared to the conventional LC-VCO while providing the same negative conductance [Yun+05].

During the current-reuse VCO operation, both transistors are turned on in the first half period, steering the current to flow from supply to ground through the inductor L; In the second half period, the transistors are both turned off, so the current flows in the opposite direction through the capacitors C. The PMOS and NMOS are switched simultaneously, while the cross coupled NMOS transistors in the conventional LC-VCO are switched alternately. Therefore, the current-reuse VCO has inherently immunity to the phase noise degradation caused by the second harmonic terms at the common source node.

The main drawback of the current-reuse VCO is the amplitude imbalances. In the first half period of the oscillation, both transistors are operated in triode region so

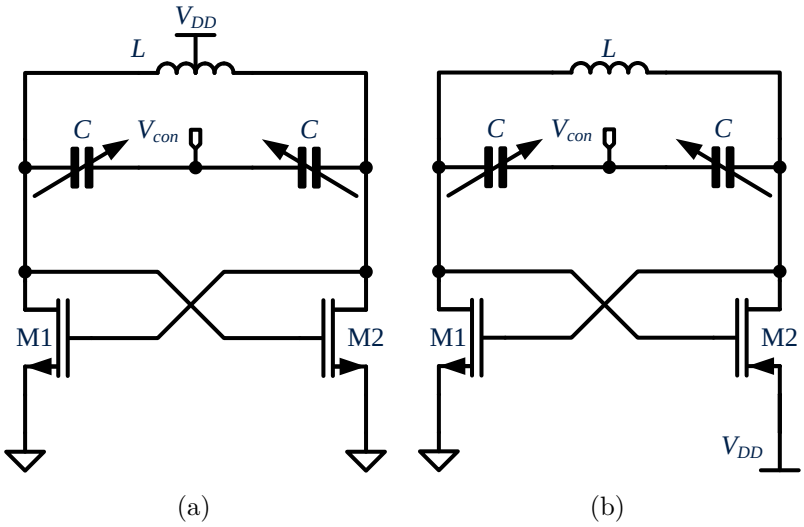


Figure 3.2: (a). Conventional LC-VCO; (b). Current-reuse LC-VCO.

that the VCO output voltage swing is limited to the supply voltage. In the second half period, both transistors are turned off, and the voltage caused by current flowing through the capacitor can be larger than the supply voltage, which leads to waveform distortion. Inserting resistors between the supply nodes to the transistor source nodes can help to balance the amplitudes. They control the DC current as well as limit the dynamic current. However, the VCO resonating amplitude is still very sensitive since it fully depends on the resistor mismatches. Moreover, the g_m mismatches of PMOS and NMOS can not be perfectly compensated. [YC05] uses transistors in the triode mode as the adjustable resistors to match the NMOS and PMOS transconductance. However, with all these efforts, the amplitude imbalance problem is inevitable as long as the VCO losses its symmetry.

3.1.3 Proposed Current-Reuse VCO

In the frequency synthesizer design, the VCO output is connected to the feedback loop, at the same time it is also connected to the mixer as the LO signal generator. Differential topology is commonly used to compensate the common noise. The proposed VCO schematic for the frequency synthesizer is shown in Fig. 3.3. The left node is connected to the feedback loop while the right node is connected to the mixer as LO generator. This connection approach sacrifices the phase noise performance to obtain low power and to avoid mismatches. M1, M2, Rs_1 and Rs_2 are selected to ensure the differential oscillation waveform to be as symmetric as possible by making $g_{m1}Rs_1 = g_{m2}Rs_2$. Besides, they can limit the VCO current. Although the oscillator voltage swing is reduced by 250 mV, two inverter buffers can provide rail-to-rail signals

for each note. Hence, the two outputs share a common oscillating frequency but not differential, since the phase delay in between is unknown. Separate applications for these two outputs connecting will not be harmful for this topology.

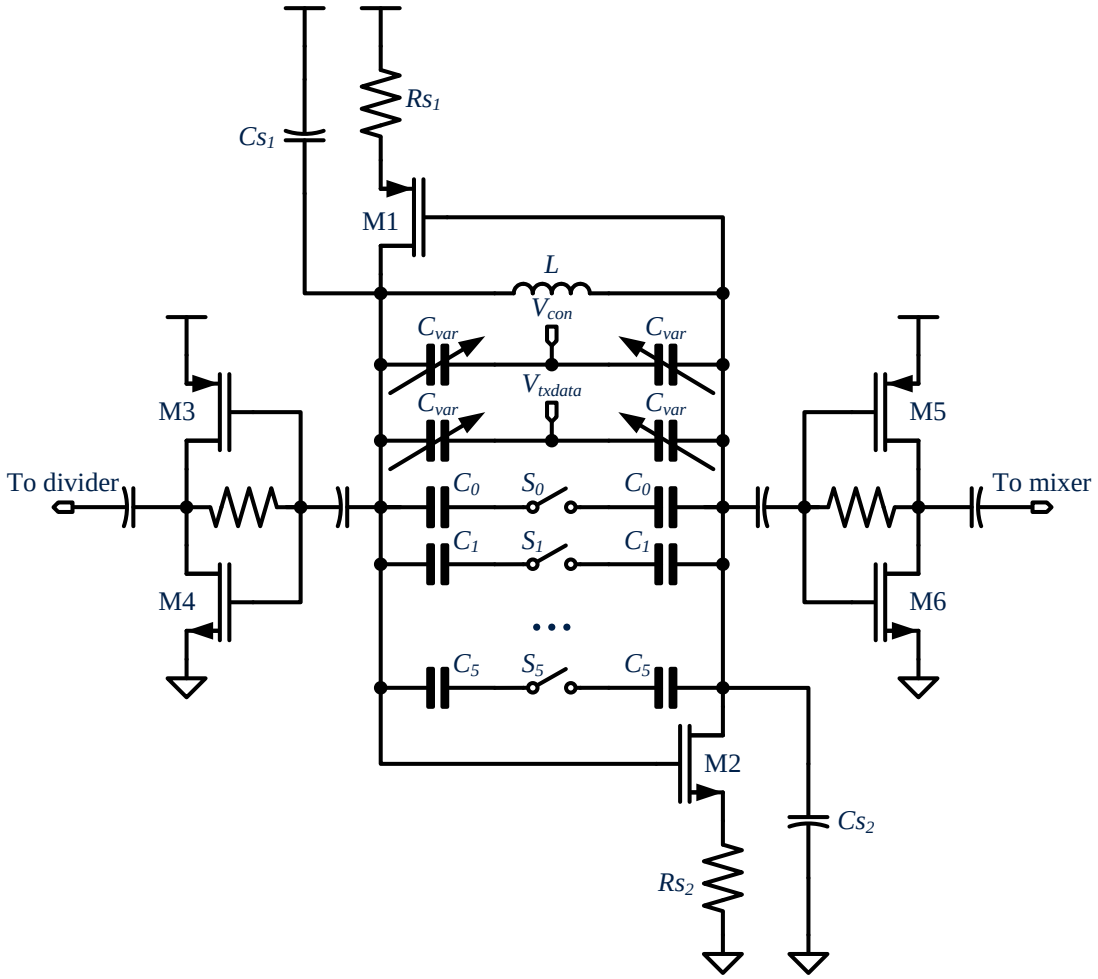


Figure 3.3: Proposed current-reuse VCO for frequency synthesizer.

To compensate the high oscillating frequency deviation, the varactor consists of an array of binary weighted PMOS varactor blocks. As shown in Fig. 3.3, 6-bit coarse tuning inputs are implemented. Three MSB bits are used as the pre-tuning. As long as the initial oscillation frequency is finalized, these bits alignment is stored externally for the further applications. The other three bits can ensure the flexible choice of the output frequency for frequency hopping. Besides, one analog tuning capacitor is controlled by the loop filter voltage, the other one is directly controlled by the transmitted data in TX mode.

3.1.4 Proposed PLL Architecture Based on Current-Reuse VCO

Fig. 3.4 shows the frequency synthesizer architecture both in TX and RX mode. For a frequency hopping system, short settling time is required when the baseband signal is transmitted in TX mode. Two-point modulation scheme is implemented for the signal transmitting. Gaussian Frequency-Shift Keying (GFSK) modulation is realized at two different paths. The transmit path takes the 1-bit data and applies the low-pass Gaussian filter. After passing the DAC, the signal directly modulates the VCO to get ±250 kHz frequency deviation. The other path controls the division ratio in the feedback loop by adding the modulated inputs to the ΣΔ modulator. Phase mismatches between the two paths are calibrated by the digital controlled time delay cell. The core building block is a ΣΔ fractional-N synthesizer. It can also be configured as the LO signal generator in RX mode.

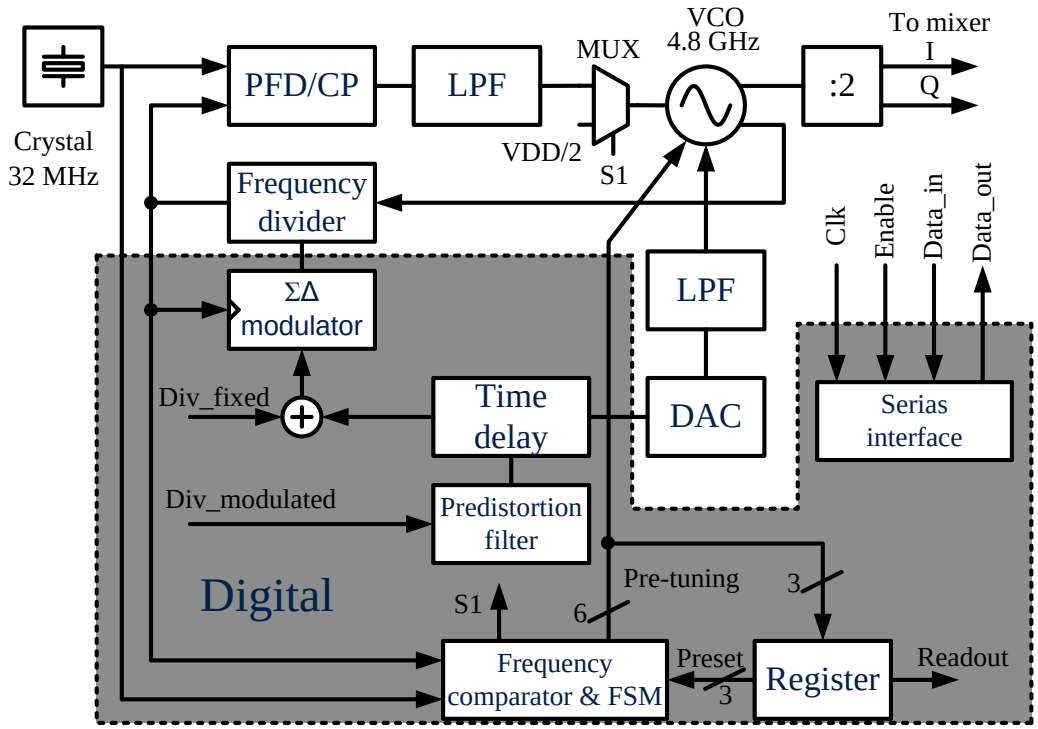


Figure 3.4: Architecture of the proposed frequency synthesizer.

The digital frequency comparator uses the one input frequency reference to count the other input in a long cycle and calculates the frequency difference. For example, if the feedback frequency is estimated much higher than the reference frequency, the tuning word is incremented by a large step, lowering the frequency band of the VCO to a far away bank; If the feedback frequency is slightly higher than the reference

frequency, the tuning word is incremented by one bit, lowering the frequency band to the next bank. The correct frequency band is finalized when the frequency comparator cannot detect the frequency difference in one cycle. Initially S1 is switched to zero, the PLL loop is open and half of the supply voltage is selected to control the VCO. The pre-tuning system automatically finds the suitable alignment by comparing the feedback frequency with the reference frequency. When the comparator cannot detect the tiny frequency difference, the Finite State Machine (FSM) switches S1 to one. Then the loop filter is connected into the system while the reference voltage is separated to the VCO. The alignments from the pre-tuning bits are sent to an external memory by the serias interface. These values will be reused every time when the frequency synthesizer is switched on as fixed preset value. Thus, large frequency deviations from the current-reuse VCO are mostly calibrated at the very beginning stage.

The pre-tuning working process is shown in Fig. 3.5 with a large variation VCO resonate frequency range from 4.5 GHz to 6 GHz. It can be seen that pre-tuning process is finished in 25 µs when the correct alignments are found. Subsequently the PLL loop is closed and the PLL is then locked in 10 µs. With this mechanism, in spite of large frequency variations, the PLL can be automatically locked at the desired frequency in all the cases.

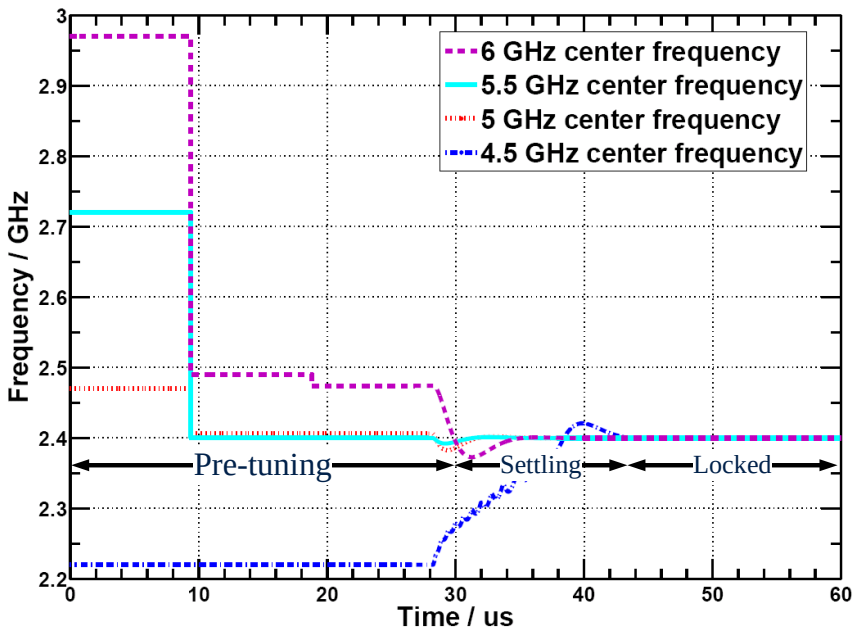


Figure 3.5: Pre-tuning process of the proposed frequency synthesizer.

3.1.5 Measurement Performance

The proposed frequency synthesizer was fully integrated in 130 nm technology. The mixed-signal and RF parts were a full custom design, and the digital block was synthesized using hardware description language. The micrograph of the frequency synthesizer is shown in Fig. 3.6, occupying 540 µm x 310 µm area. The power consumption for the proposed frequency synthesizer is 5.8 mW with 1.2 V supply voltage in RX mode. In TX mode, the transmitter can achieve 0 dBm output power when the synthesizer consumes about 10 mW. The internal loop filter is located out of the power ring to make fully use of the chip area. All the digital circuits, including ΣΔ modulator, baseband signal modulator, received signal demodulator and the series interface are synthesized in a single block.

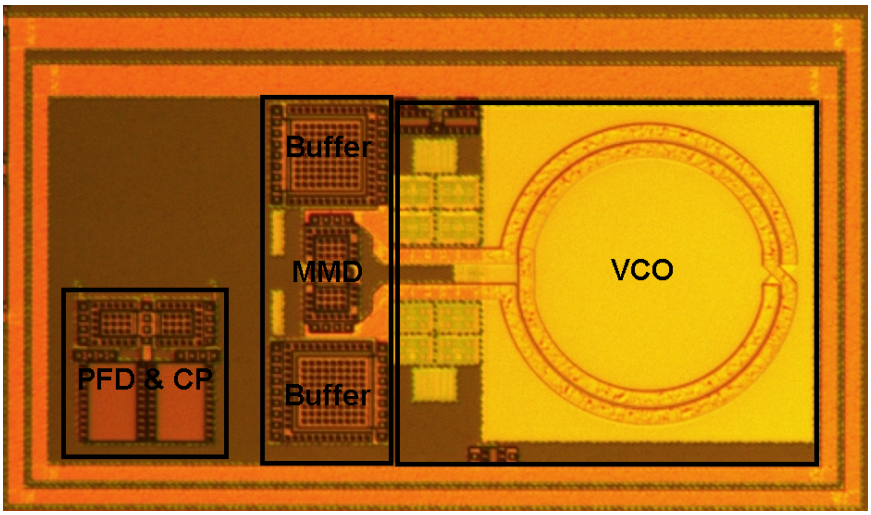


Figure 3.6: Synthesizer micrograph.

The proposed frequency synthesizer provides a frequency band between 2.35 GHz and 2.55 GHz. Fig. 3.7 shows the measured phase noise at 2.433 GHz output. The loop filter bandwidth is set as 100 kHz to limit the ΣΔ quantization noise. −131 dBc/Hz at 1 MHz offset phase noise performance and 0.45 ps rms jitter are achieved.

The reference spur level is −75 dB at 32 MHz, as shown in Fig. 3.8. For the two-point modulated transmitter, 1 Mbps GFSK signals with 250 kHz frequency deviation is generated at 2.433 GHz output. They are measured using signal analyzer and demodulated to observe the eye diagram. A clear eye pattern can be obtained.

Tab. 3.1 shows a comparison between the proposed design and other published works. The proposed approach exhibits comparable phase noise and reference spur suppression performance among other works with lower power consumption.

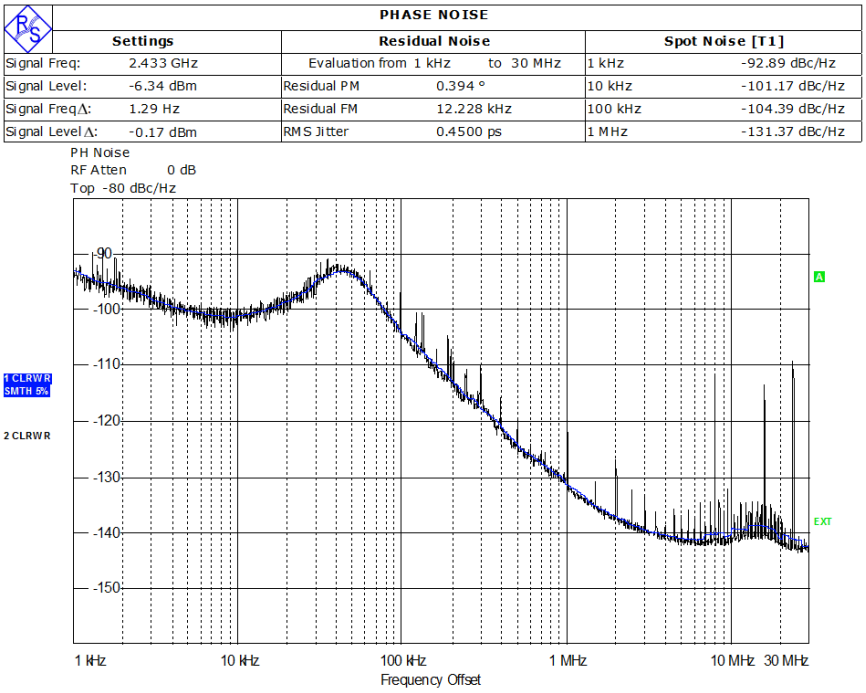


Figure 3.7: Phase noise performance of the frequency synthesizer.

Table 3.1: Performance comparison with prior works

Parameter	[SWG07]	[Xu+10]	This work
Technology (nm)	180	65	130
Frequency (GHz)	2.4	2.4	2.4
Bandwidth (kHz)	460	40	100
Phase noise (dBc/Hz)	−124 @3 MHz	−120 @1 MHz	−131 @1 MHz
Ref spur (dBc)	−65	-	−75
Core area (mm^2)	4.8	0.24	0.3
Core power (mW)	38	12	5.8

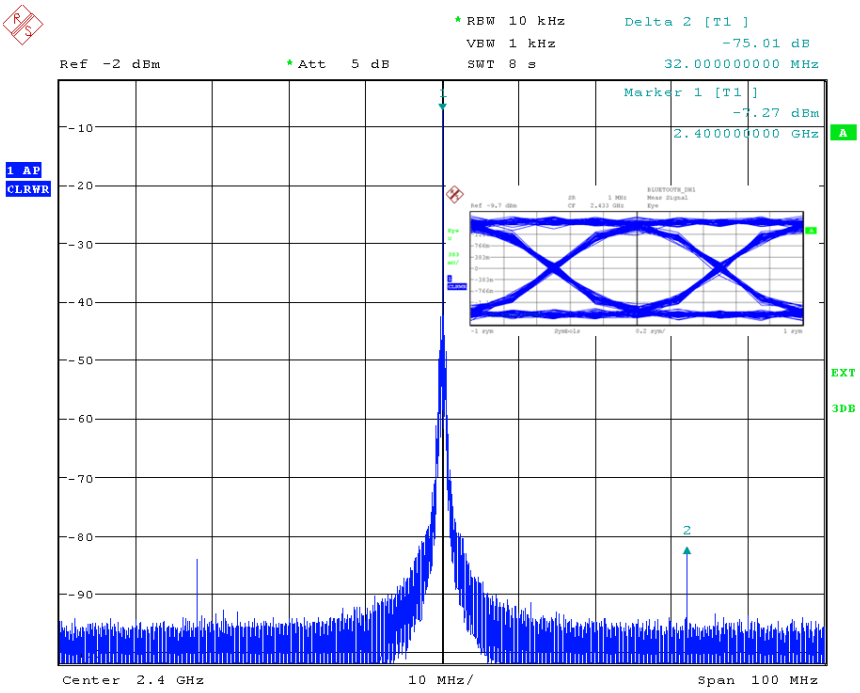


Figure 3.8: Reference noise rejection performance of the frequency synthesizer.

3.2 ΣΔ Modulator Hardware Simplification

In this section, a novel digital architecture for the PLL direct based frequency/phase modulation is presented, which can greatly reduce the wordlength in the MASH ΣΔ modulator. And meanwhile the spurious tones are eliminated using a non-overload differentiator instead of the ΣΔ requantizer, which further dramatically reduces the hardware complexity and improves SNR. Using the error masking methodology, the optimum wordlength is determined meanwhile the generated noise is fully hidden by the existing noise without degrading the system performance.

The block diagram of the direct modulation transmitter is shown in Fig. 3.9. The digital circuits for signal modulation and noise cancellation are indicated in the grey region. In additional to the conventional frequency synthesizer components, the phase noise cancellation path is added, where the quantization error from ΣΔ residue $E_Q[n]$ is accumulated, requantized and converted via segmented mismatch shaping DAC banks [PJG04]. 1-bit LSB dithering is allocated to both quantizers to break the periodicity of cycles and ensure that the inputs of ΣΔ modulators are white [PWG07].

Implementing the segmented-shaped or binary-weighted DAC with the same resolution as the ΣΔ modulator costs unfeasible area. Moreover, its LSB needs to correspond to a current in nA range. Therefore, the DAC input wordlength should be reduced by

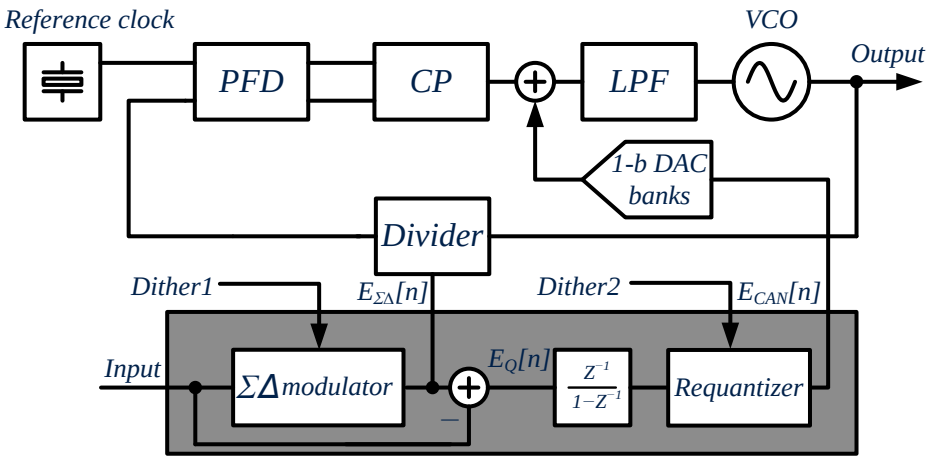


Figure 3.9: PLL based direct frequency/phase modulation architecture.

another ΣΔ modulator as a requantizer, and its noise $\Phi_{RQ}[n]$ also needs to be pushed to higher frequency offsets.

3.2.1 Fundamentals

The system model in frequency domain is shown in Fig. 3.10 by taking Fourier transform of the analog blocks and z-transform of the digital blocks [PTS02]. The derived parametrization allows straightforward calculation of the synthesizer noise performance as a sum of various noises from charge pump ($S_{\Phi CP}$), VCO ($S_{\Phi VCO}$), ΣΔ quantization noise ($S_{\Phi\Sigma\Delta}$) and cancellation path noise ($S_{\Phi CAN}$).

$S_{\Phi CP}$ is calculated from the input-referred noise of the charge pump current $\overline{i_{CP}^2}$ and exhibits a lowpass characteristic:

$$S_{\Phi CP}(f) = \overline{i_{CP}^2}(\frac{2\pi N_{div}}{I_{CP}})^2|G(f)|^2, \tag{3.1}$$

where N_{div} denotes the division ratio and $G(f)$ denotes the PLL closed-loop transfer function.

$S_{\Phi VCO}(f)$ is calculated from the input-referred noise of the VCO voltage $\overline{v_{VCO}^2}$ and exhibits a highpass characteristic:

$$S_{\Phi VCO}(f) = \overline{v_{VCO}^2}|\frac{K_{VCO}}{jf}|^2|1 - G(f)|^2 \tag{3.2}$$

The actual amount of charge in each DAC pulse that deviates from its ideal value can be represented by a factor of $1 + \beta$, where β represents the normalized path mismatch. Assuming the residue from ΣΔ modulator is accumulated and requantized into K-bit,

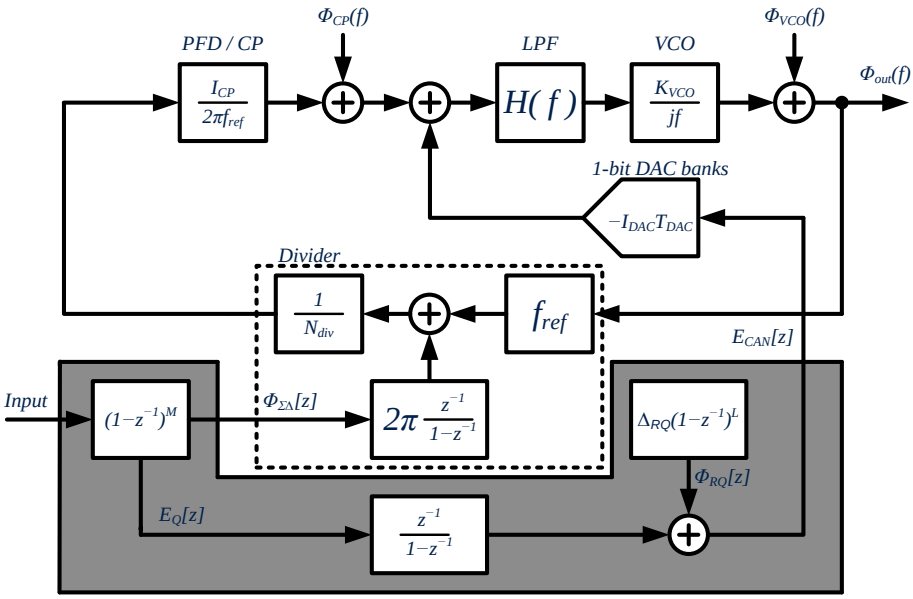


Figure 3.10: Frequency synthesizer model in frequency domain.

the total digital noise $S_{\Phi D}(f)$ is composed of remaining M^{th}-order $\Sigma\Delta$ quantization noise and the uncompensated L^{th}-order requantization noise:

$$\begin{aligned} S_{\Phi CAN}(f) =& (1+\beta^2)S_{\Phi\Sigma\Delta}(f) + S_{\Phi RQ}(f) \\ S_{\Phi D}(f) =& S_{\Phi CAN}(f) - S_{\Phi\Sigma\Delta}(f) \\ =& \frac{\beta^2}{12}\frac{4\pi^2}{f_{ref}}|2\sin(\frac{\pi f}{f_{ref}})|^{2(M-1)}|G(f)|^2 \\ &+ \frac{\frac{1}{2^{2K}}}{12}\frac{4\pi^2}{f_{ref}}|2\sin(\frac{\pi f}{f_{ref}})|^{2L}|G(f)|^2 \end{aligned} \tag{3.3}$$

The order of $S_{\Phi\Sigma\Delta}$ is reduced by one due to the frequency divider, while the requantization noise $S_{\Phi RQ}$ order remains. The requantization noise must be negligible compared to remaining $\Sigma\Delta$ noise. Hence, it is recommended that M is 3 and L is 2 to ensure that requantization noise is fully hidden by $\Sigma\Delta$ noise with the same noise shaping over the whole frequency.

3.2.2 Proposed Architecture

In contrast to the classical topology, where two $\Sigma\Delta$ modulators and one accumulator are employed, the proposed digital circuit only uses one reduced complexity (RC) $\Sigma\Delta$ modulator [YK07], one delay cell and one differentiator to generate the same high-pass

noise shaping. The linearized model of the proposed structure including quantization errors is shown in Fig. 3.11.

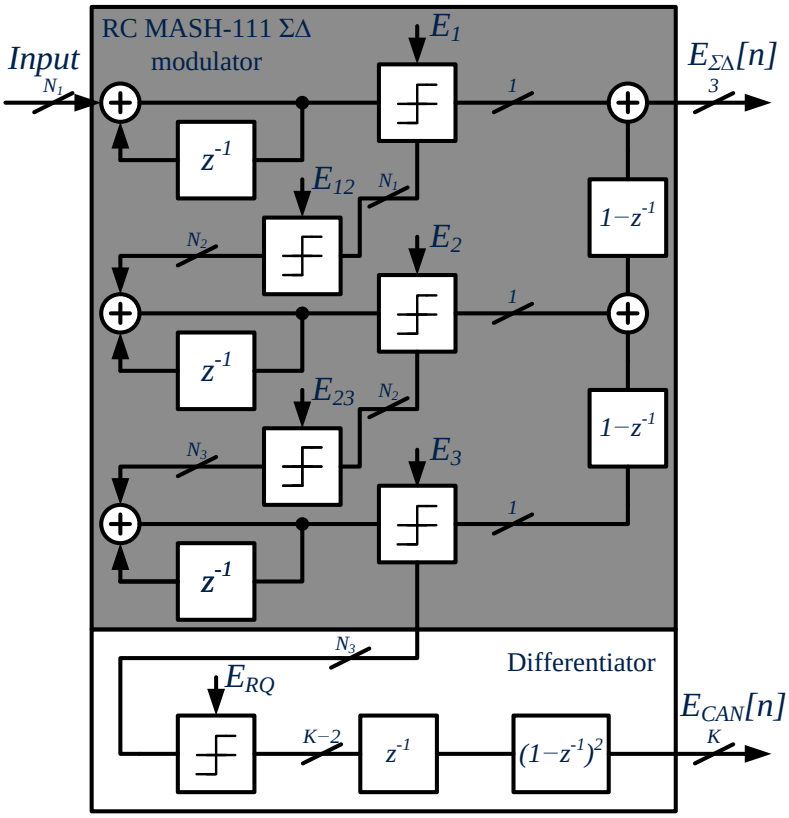


Figure 3.11: Proposed digital circuit block diagram.

RC MASH-111 ΣΔ Modulator

The upper grey region of Fig. 3.11 displays the RC MASH-111 modulator. Only the first stage has full-width of N_1-bit, and its residue passes through N_2 interstage quantizer before being fed forward to the next stage. Between the second and the third stage, the wordlength is reduced further to N_3. Hence, the RC ΣΔ noise transfer function $E_Q^{'}(z)$ contains the two additional errors from interstage quantizers E_{12} and E_{23}:

$$\begin{aligned} E_Q^{'}(z) =& E_Q(z) + E_{RC}(z) \\ E_Q(z) =& E_{\Sigma\Delta}(z) = E_3(z)(1-z^{-1})^3 \\ E_{RC}(z) =& E_{12}(z)(1-z^{-1})z^{-1} + E_{23}(z)(1-z^{-1})^2 \end{aligned} \tag{3.4}$$

ΣΔ Requantizer vs Differentiator

As shown in Fig. 3.12, the accumulator with the transfer function of $\frac{z^{-1}}{1-z^{-1}}$ is employed between two ΣΔ modulators to compensate the integration operation from the divider, which brings one additional pole. A 2nd-order ΣΔ modulator requantizes the accumulator output into K-bit. The cancellation path output $E'_{CAN1}(z)$ transfer function is:

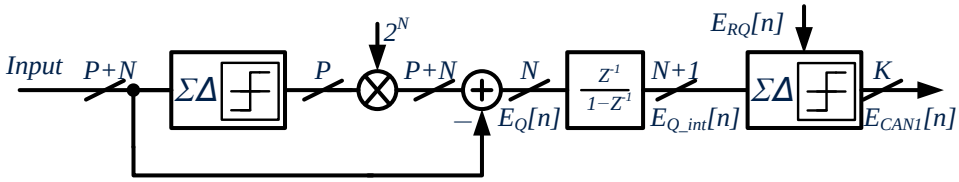


Figure 3.12: ΣΔ requantizer based ΣΔ noise cancellation.

$$
\begin{aligned}
E'_{CAN1}(z) =& E'_Q(z)\frac{z^{-1}}{1-z^{-1}} + E_{RQ1}(z)(1-z^{-1})^2 \\
=& (E_3(z)z^{-1} + E_{RQ1})(1-z^{-1})^2 + \frac{E_{RC}(z)z^{-1}}{1-z^{-1}} \\
=& (z^{-1} + \frac{\frac{1}{2^{2K}}}{12})E_3(z)(1-z^{-1})^2 + \frac{E_{RC}(z)z^{-1}}{1-z^{-1}}.
\end{aligned} \tag{3.5}
$$

As shown in (3.5), the original noise E_3 is shaped by 40 dB/dec, meanwhile the additional noise E_{RC} contains other components with different noise shaping, which would influence the old noise shaping at low frequency offsets.

The mean value of quantization noise $E_Q(n)$ during the period of ΣΔ modulator output N is zero:

$$
E_Q(n) = \sum_{n=1}^{N} Q(n) = 0 \tag{3.6}
$$

However, due to the new pole generated by $\frac{z^{-1}}{1-z^{-1}}$, it brings an constant offset at the cancellation path and changes mean value of the integrator output $E_{Q_{int}}(n)$:

$$
\begin{aligned}
Q_{int}(n+1) =& Q_{int}(n) + Q(n) \\
E_{Q_{int}}(n) =& \sum_{n=i}^{N}\sum_{i=1}^{n} Q(i) \\
=& \sum_{n=1}^{N}(N-n)Q(n) \neq 0
\end{aligned} \tag{3.7}
$$

Hence, the ΣΔ requantizer introduces an unknown DC offset at charge pump output, bringing additional large spurs due to the mismatches between the charging and discharging currents. And more bits in DAC are needed to avoid the overflow issues due to the DC offset.

In order to recover the whole RC ΣΔ quantization noise, independent noise sources need to be summed, as shown in Fig. 3.13. Thus, if the noise contributions of E_{12} and E_{23} are negligible, by applying a differentiator in forward path to perform both $(1-z^{-1})^2$ and noise shaping function, the computation complexity is highly reduced. On the other hand, the whole wordlength can be fully used to achieve the maximum SNR without overflow. Hence, the same performance of the cancellation path can be obtained by one delay cell and a second-order differentiator.

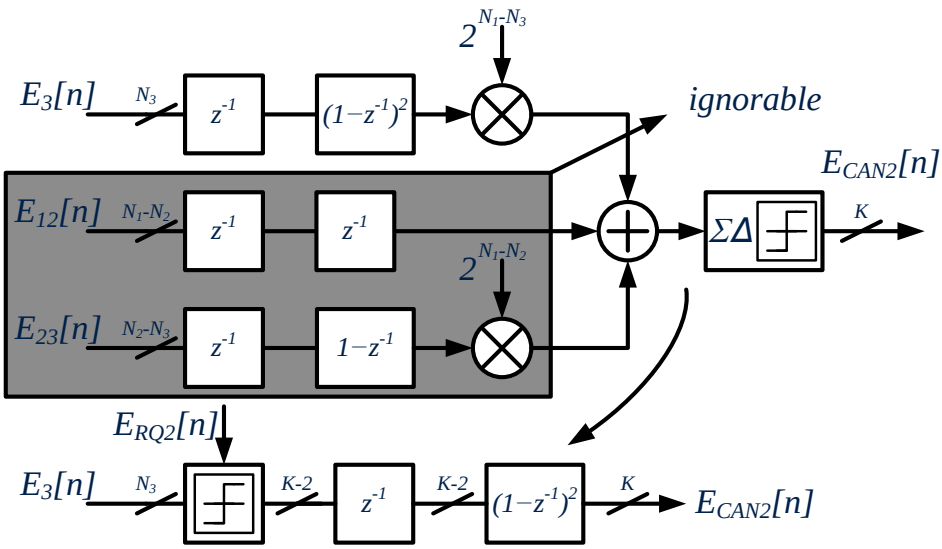


Figure 3.13: Ideal MASH-111 RC ΣΔ modulation residue signal recovery and simplified residue signal recovery.

$$\begin{aligned} E'_{CAN2}(z) =& (E_3(z) + E_{RQ2})z^{-1}(1-z^{-1})^2 \\ =& (1 + \frac{\frac{1}{2^{2(K-2)}}}{12})E_3(z)z^{-1}(1-z^{-1})^2. \end{aligned} \tag{3.8}$$

In this way, both $E_3(z)$ and quantization noise are highpass filtered by 40 dB/dec. As shown in Fig. 3.14, compared to the requantizer based design, the inband noise is significantly reduced, since the differentiator converts all the previous signals and noises to 2nd-order high pass shape.

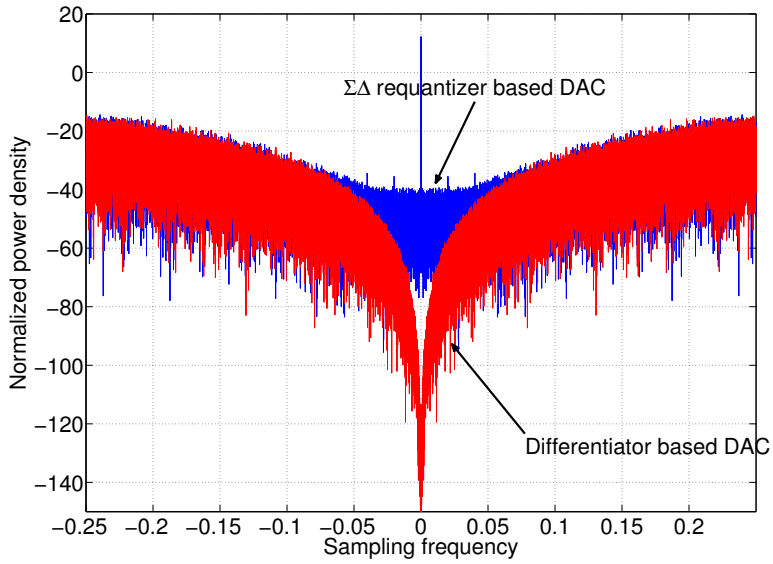


Figure 3.14: Comparison of requantizer based noise cancellation and differentiator based noise cancellation.

3.2.3 Wordlength Optimization

The digital processing power grows exponentially with the wordlength. Following the error masking methodology presented in [YK04; FKM11], 20 % area savings can generally be achieved when using 1-bit LSB dithering at the input. However, in relation to the PLL system level design, a more relaxed error-mask standard can be derived without sacrificing the phase noise performance.

Assuming all the quantization noises are independent, the ΣΔ noise contribution to the PLL is:

$$S'_{\Phi_{\Sigma\Delta}}(f) = S_{\Phi 3}(f) + S_{\Phi RC}(f), \tag{3.9}$$

where

$$\begin{aligned} S_{\Phi 3}(f) =& \frac{1}{12}\frac{4\pi^2}{f_{ref}}|2\sin(\frac{\pi f}{f_{ref}})|^4|G(f)|^2, \\ S_{\Phi RC}(f) =& S_{\Phi 12}(f) + S_{\Phi 23}(f) \\ =& [\frac{1}{2^{2N_2}} + \frac{1}{2^{2N_3}}|2\sin(\frac{\pi f}{f_{ref}})|^2]|G(f)|^2. \end{aligned} \tag{3.10}$$

The noise contribution from the cancellation path is:

$$E'_{\Phi_{CAN}}(f) = (1+\beta^2)S_{\Phi\Sigma\Delta}(f) + S_{\Phi RQ}(f). \tag{3.11}$$

At first, the phase noise at low frequency offsets plays the most critical role in the whole PLL performance. At this range only $S_{\Phi 12}$ and $S_{\Phi CP}$ contain DC components. Thus, the generated RC quantization noise from $S_{\Phi 12}$ must be masked by the charge pump noise. This constraint can be written as:

$$\begin{aligned} S_{\Phi 12} &< S_{\Phi CP}, @f = DC \\ \frac{1}{2^{2N_2}}|G(f)|^2 &< \overline{i_{CP}^2}(\frac{2\pi N_{div}}{I_{CP}})^2|G(f)|^2 \\ N_2 &> \log_2 \frac{I_{CP}^2}{12\overline{i_{CP}^2}N_{div}^2 f_{ref}}. \end{aligned} \tag{3.12}$$

Secondly, the power spectrum density of $S_{\Phi 23}(f)$ increases over frequency and achieves its highest density at f_{BW}. If one can guarantee that $S_{\Phi 23}(f)$ is smaller than $S_{\Phi 12}(f)$ even when its maximum power is reached, its noise can be fully hidden:

$$\begin{aligned} S_{\Phi 23} &< S_{\Phi 12}, @f = f_{BW} \\ \frac{1}{2^{2N_3}}|2\sin(\frac{\pi f_{BW}}{f_{ref}})|^2|G(f_{BW})|^2 &< \frac{1}{2^{2N_2}}|G(f_{BW})|^2 \\ N_3 &> N_2 + 2\log_2 2\sin\frac{\pi f_{BW}}{f_{ref}}. \end{aligned} \tag{3.13}$$

In addition, the requantization noise must be covered by the quantization noise over the whole frequency range, as discussed in Section II:

$$\begin{aligned} S_{\Phi RQ} &< S_{\Phi\Sigma\Delta} \\ \frac{\frac{1}{2^{2K}}}{12}\frac{4\pi^2}{f_{ref}}|2\sin(\frac{\pi f}{f_{ref}})|^{2L}|G(f)|^2 &< \frac{\beta^2}{12}\frac{4\pi^2}{f_{ref}}|2\sin(\frac{\pi f}{f_{ref}})|^{2L}|G(f)|^2 \\ K &> \log_2\frac{1}{\beta} + 2. \end{aligned} \tag{3.14}$$

The abandoned signals E_{12} and E_{23} from the differentiator structure should not be ignorable compared to the dominated signal E_3. So the differentiator output is also limited:

$$K < N_3 + 2. \tag{3.15}$$

The proposed phase noise contribution is shown in Fig. 3.15. It can be seen that generated RC noise $S_{\phi 12}$ is masked by $S_{\phi CP}$, and $S_{\phi 23}$ is masked by $S_{\phi 12}$ and $S_{\phi \Sigma\Delta}$. Therefore, the phase noise performance of the proposed digital architecture is similar to the classical structure but requires significantly reduced circuit complexity. On the other hand, the differentiator structure avoids offset issues, so that the spurs will be attenuated, which is not visible from the calculation curves.

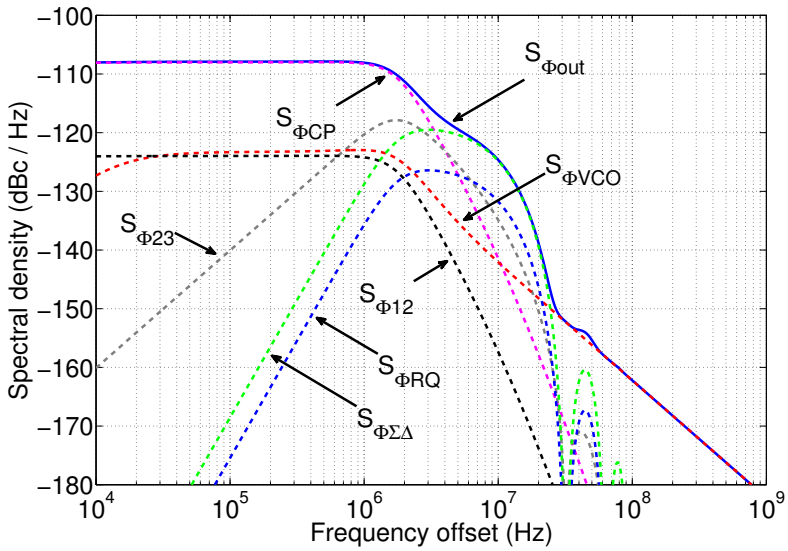


Figure 3.15: Noise contribution in PLL system.

3.2.4 Design Example

Simulation Setup

To compare the performance of the new topology with the conventional one, a fully integrated frequency synthesizer is designed and simulated in TSMC 65 nm CMOS technology. It generates 3.2 GHz output with 32 MHz reference clock. The ΣΔ modulator has 20-bit wordlength at the first stage ($N_1 = 20$). The normalized mismatch is expected to be at most 10 % [PG03], 5 % is an optimized estimation. The poles and zeros from loop filter are chosen to ensure that the PLL has 55° phase margin. Two banks of 8-bit segmented mismatching shaping DACs constitute the noise cancellation path. Other parameters and noise sources of the PLL are listed in Tab. 3.2.

According to (3.12), (3.13), (3.14), (3.15) and Tab. 3.2, the overall constraints for N_2, N_3 and K are summarized as:

Table 3.2: Parameters for proposed PLL design example

Parameter	Value
Reference frequency (f_{ref})	32 MHz
VCO frequency (f_{VCO})	1.6 GHz
CP current (I_{CP})	40 µA
CP current mismatch	5 %
CP current noise ($\overline{i_{CP}^2}$)	3×10^{-25} A^2/Hz
VCO phase noise	−121 dBc/Hz @ 1MHz
K_{VCO}	100 MHz/V
PLL bandwidth (f_{BW})	1.5 MHz
DAC LSB current	625 nA
DAC pulse width (T_{DAC})	$4T_{VCO}$
Cancellation path mismatch β	5 %

$$\begin{cases} N_2 > & 8.12 \\ N_3 > & N_2 - 4.7 \\ K > & 6.32 \\ K < & N_3 + 2 \end{cases} \tag{3.16}$$

Hence, the optimum wordlength of the first, second, third stages of RC ΣΔ modulator and segmented shaped DAC are selected as 20, 9, 6 and 7, respectively ($N_1 = 20, N_2 = 9, N_3 = 6, K = 7$).

3.2.5 Performance and Hardware Comparison

The effect of quantization, requantization and mismatch errors on the PLL phase noise from different conditions are compared in Fig. 3.16. If there is no gain mismatch between two paths ($\beta = 0$), the PSD curve from the proposed design exceeds the conventional curve by 10 dB in the worst case, since the RC quantization noise from differentiator cannot be fully compensated. However, its performance outmatches the conventional design at the low frequency offset due to its pure highpass noise shaping. When the normalized gain mismatch is 5 %, the noise floor is increased by 20 dB, and the large spurious tones can be seen because of the mismatches and nonlinearities between the two ΣΔ modulators. Meanwhile, the proposed noise cancellation circuits retain the same noise shaping. It is also noted that differentiator eliminates the spurs from previous ΣΔ modulator in this architecture.

Fig. 3.17 shows the simulated phase noise performance of the synthesizer. The RF and analog circuits are implemneted in VerilogAMS event-driven model, considering the typical non-idealities, such as mismatch and linearity issues in CP [SP10] and

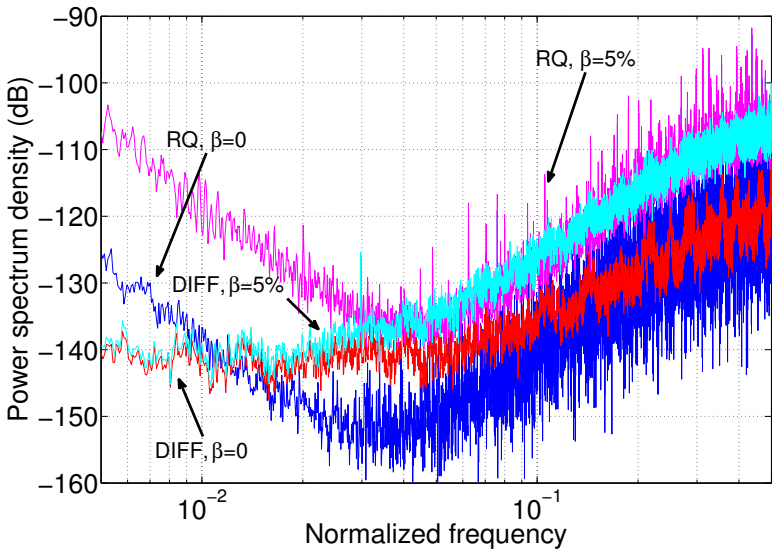


Figure 3.16: Comparison of phase noise contribution from conventional digital circuits and proposed circuits.

Table 3.3: Hardware reduction comparison.

Conventional		RC in [YK04]		Proposed	
Cells	Area	Cells	Area	Cells	Area
20-bit ΣΔ	2027 µm^2	20-14-7 ΣΔ	1633 µm^2	20-9-6 ΣΔ	1366 µm^2
20-bit ACC	670 µm^2	20-bit ACC	671 µm^2	5-bit delay	45 µm^2
15-bit ΣΔ	1114 µm^2	15-10 ΣΔ	940 µm^2	6-bit DIFF	323 µm^2
Total area	3810 µm^2	Total area	3245 µm^2	Total area	1668 µm^2
Power	396 µW	Power	338 µW	Power	204 µW

DAC, dead-zone in PFD etc [Kun03]. From the calculation and simulation results, it can be seen that the additional noises resulting from the proposed circuit are well masked by other noise sources, so that the proposed circuit achieves the identical phase noise performance as the conventional circuit. The simulated spectra also matches the predicted curve well. The visible inband spurs are dominated by nonlinearities in the PLL and the ΣΔ noise.

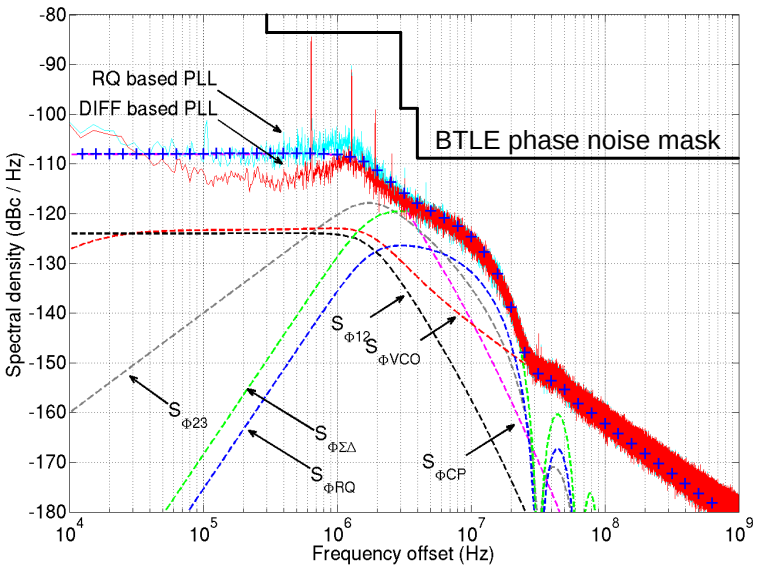


Figure 3.17: Comparison of simulated frequency synthesizer phase noises.

The classical and proposed digital circuits are both synthesized in integrated circuits. The conventional topology consists of a 3rd-order N_1-bit ΣΔ modulator, N_1-bit accumulator and a 2nd-order (N_1-K)-bit ΣΔ modulator, while the proposed topology consists of an RC ΣΔ modulator and a K-bit 2nd-order differentiator. Hence, the Relative Hardware Complexity (RHC) can be estimated as:

$$RHC \approx \frac{(N_1 + N_2 + N_3) + 2K}{3N_1 + N_1 + 2(N_1 - K)} = 45\ \% \tag{3.17}$$

The synthesized hardware specifications for conventional and proposed architectures are summarized in Tab. 3.3. Note that the proposed circuit requires 44 % of the area and 51 % of the power as the conventional solution. Compared to a general RC structure for ΣΔ modulators [YK04], significantly more area and power are saved. Thus, for a given spectral performance, the hardware requirements for this topology are significantly lower.

3.3 Conclusion

In the first part, a fractional-N frequency synthesizer based on a current-reuse VCO has been demonstrated to achieve low power low phase noise performance. Practical issues for current-reuse VCO in synthesizer applications are discussed and solved with proposed techniques. The pre-tuning system uses external memory to store the initial VCO alignment and reuses it in further implementation to calibrate against the large frequency deviation and save the settling time. The reference spurs are greatly suppressed by the proposed symmetric charge pump. Measurement results show that the proposed frequency synthesizer meets the design target and validates the design choices.

In the second part, the noise contributions in a PLL based frequency/phase modulation system are analyzed, and a new digital architecture for PLL signal modulation and quantization is proposed. Using the error masking methodology, the proposed RC MASH and differentiator are implemented, allowing approximately 50% savings in area and power reduction without degrading the spectral performance. Through the design example, it can be seen that the simulation results confirm the analytical predictions.

Chapter 4

Wideband Frequency Synthesizer for Direct Modulation

In Low-power short-range wireless standards, constant envelope modulation schemes such as GFSK, Offset Quadrature Phase-Shift Keying (OQPSK) are usually employed for the short-range wireless standards, where the direct frequency/phase modulation is preferred to reduce the hardware complexity. Thus the PLL bandwidth needs to be extended to pass through the modulation signal. However, the $\Sigma\Delta$ shaped quantization noise becomes the bottleneck since it cannot be sufficiently suppressed anymore.

In this chapter, a low effort adaptive calibration technique for phase noise cancellation based on the modified classical loop filter structure is proposed. An additional port from the loop filter is used as the reference for the LMS algorithm to avoid DC offset; meanwhile the whole system maintain in the single-ended topology. The gain mismatch is detected and calibrated outside of the PLL loop, no more spurs are introduced into the system. As long as the desired reference current is achieved, the calibration circuits are disabled to save power and disconnected to avoid the crosstalk. Comparing to the previous works, the proposed technique provides a straightforward solution for wideband PLL designs, where the quantization noise is successfully canceled with smaller area and lower power consumption.

4.1 ΣΔ Quantization Noise Cancellation

In order to realize the fractional division ratio, the integer value is modulated with a ΣΔ modulator, whose quantization noise $E_Q[n]$ is highpass shaped. Since it is only possible for the divider edge to occur after an integer multiple of the VCO period, instantaneously the divider output will never be phase locked to the reference. The PLL acts on this sequence as a low-pass filter in the process of converting it to output phase noise. Therefore, spectral components of $E_Q[n]$ outside the bandwidth of the PLL are suppressed, but those inside the bandwidth of the PLL are amplified through the discrete-time integration and can add significantly to the overall phase noise of the PLL.

At the CP output, the current pulses are always added to subtracting charge from the loop filter, whose average charge added to the loop filter is zero. So the CP charge deposited each VCO period is expressed as:

$$Q_{CP}[n] = I_{CP}T_{VCO}\sum_{k}^{n-1} E_Q[k] = I_{CP}T_{VCO}E_{ACC}[n]. \tag{4.1}$$

Where $E_{ACC}[n]$ denotes the accumulated ΣΔ quantization error.

The typical solution to suppress the PLL phase noise that would otherwise result from quantization noise has been addressed using a DAC cancellation path to suppress $E_Q[n]$, as shown in Fig. 4.1. By inserting an additional quantization noise cancellation path, the digital ΣΔ residue error is accumulated, translated to the DAC compensation current, and injected into the loop filter. The DAC converts $E_{ACC}[n]$ into current pulses which have a charge nominally equal in magnitude and opposite in sign to the CP charge. If the DAC has sufficient precision and the correct gain, the added signal nearly cancels the component of the charge pump output corresponding to $E_Q[n]$.

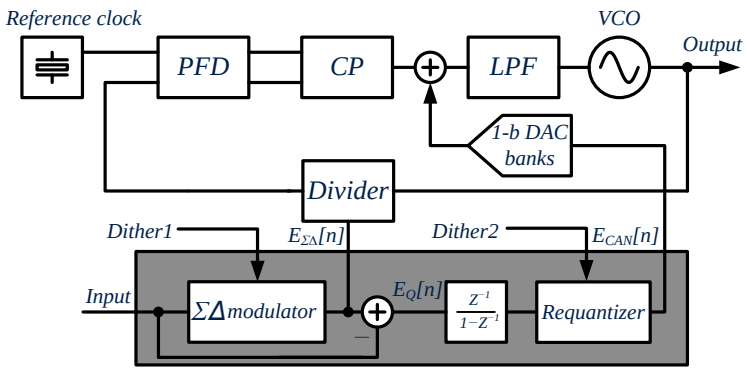


Figure 4.1: PLL based direct frequency/phase modulation architecture.

In most fractional-N PLLs of this type, the compensation current is generated using one or two digital error accumulator structures designed to ensure that the sum of

$E_Q[n]$ is bounded. The resulting $E_{ACC}[n]$ sequence tends to have a large dynamic range, a high spurious tone content, and significant spectral power within the PLL bandwidth. Therefore, excellent cancellation accuracy is required, if $E_Q[n]$ is only partially canceled because of gain errors, distortion, or insufficient dynamic range in the DAC cancellation path, the remaining portion of $E_Q[n]$ contains in-band noise and spurious tones which can contribute significant phase noise.

A more recent technique that circumvents the DAC precision and gain matching problems uses a digital ΣΔmodulator to generate the compensation current such that $E_{ACC}[n]$ has at least one zero at dc with most of its power concentrated at high frequencies, outside the passband of the PLL. Provided the bandwidth of the PLL is sufficiently narrow, most of the quantization noise is suppressed by the PLL so a DAC cancellation path is not necessary. Nevertheless, the need to suppress out-of-band quantization noise imposes a fundamental bandwidth versus phase noise tradeoff in ΣΔ fractional-N PLLs that causes problems in many applications. Furthermore, $E_{ACC}[n]$ must be nearly free of spurious tones, or else high gain accuracy would again be required in the DAC cancellation path to properly cancel the spurious tones. Hence, ΣΔ requantization and a segmented mismatch-shaping current pulse DAC are usually used to obtain high DAC cancellation path dynamic range and linearity, and 1-bit dithering is used to eliminate spurious tones.

However, the quantization noise and the compensation current go through two different paths, thus the gain of the noise cancellation path cannot be perfectly matched to the signal path. Since the charge pump pulses have a fixed amplitude and variable widths, whereas the DAC pulses have a fixed width and variable amplitudes, generating the width-modulated DAC pulses corresponding to the ΣΔ modulation is difficult. The DAC pulses can be mismatched from the CP pulses due to static current mismatch or pulse with mismatches. This results in a residual charge error remaining on the loop filter, limiting the achievable phase noise cancellation.

4.1.1 LMS Algorithm for DAC Gain Calibration

As the DAC gain mismatch can be continuously detected since it results in a fraction of the original CP charge being deposited into the loop filter each reference period, the LMS algorithm can be used to minimize the mismatches by adjusting the DAC gain according to the errors at loop filter output adaptively.

Fig. 4.2 shows the ideal of LMS algorithm based DAC gain calibration in [GS06]. In this work, two additional blocks are added to the conventional PLL system. The spur cancellation block cancels the ΣΔ divider ratio noise, and the spur correlation block detects the CP/DAC gain mismatch error. Together they complete an adaptive zero forcing feedback based on a sign-sign LMS algorithm. It relies on the direct correlation of the actual accumulated ratio error because of CP/DAC mismatch at the loop filter with the sign of the integrated phase error. A ΣΔ modulator converts this correlation to a 1-bit stream, which is fed into the digital block for lowpass filter. The strength of this

algorithm lies in correction of CP/DAC mismatch based on the actual perturbations occurring at the loop filter.

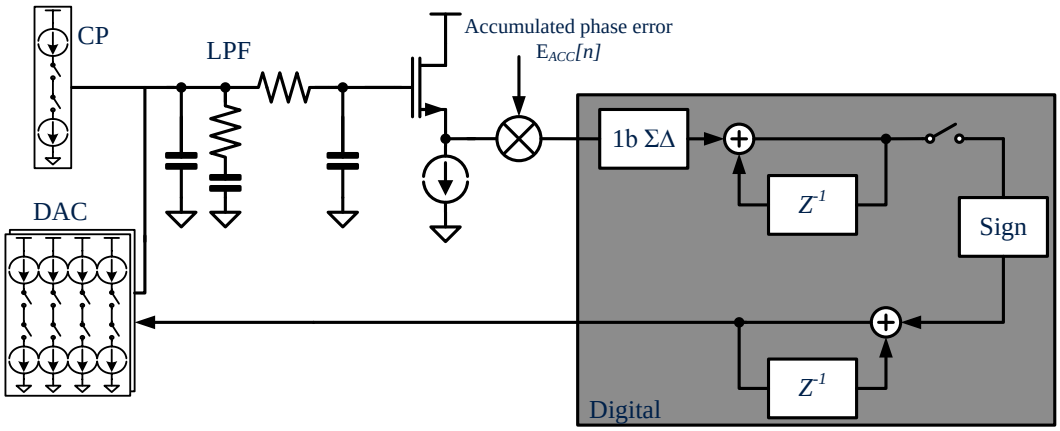


Figure 4.2: LMS Algorithm for DAC Gain Calibration in [GS06].

In the first step, after the CP and DAC pulses occur, the loop filter voltages settles to a constant value related to this charge. The mismatch is estimated by multiplying this loop filter voltage with a binary correlation signal at each reference period. Therefore, if the DAC gain is greater or less than the CP gain, the correlated loop filter voltage will have a net positive or negative dc value respectively. This DC value is accumulated and used to modify the DAC gain by adjusting the DAC bias current. The feedback of the calibration loop adjusts the DAC gain to minimize the DC component of the correlated loop filter voltage.

However, the noise arising from the multiplication of the correlation signal with the DC loop filter voltage, and quantization noise from the ΣΔ modulator must be filtered prior to adjusting the DAC bias current. This results in a long transient response of the calibration circuit. Secondly the buffer needs to provide isolation for the loop filter and thus requires a significant amount of power consumption. And the DC loop filter voltage varies according to the output frequencies, which needs to be estimated and eliminated in digital signal processing.

4.1.2 Differential Topology in LMS Error Detection

[SWG07] improves the LMS calibration techniques in that the existing PLL loop is modified so that minimal extra circuitry is required for calibration. As show in Fig. 4.3, an analog, continuous-time fully differential technique is utilized to reduce the noise from quantization and correlation of the DC loop filter voltage, and eliminate the sampling of the loop filter voltage. The issues mentioned in the previous subsection

such as reference clock feedthrough, the calibration loop bandwidth limitation, and the loop filter DC voltage variation are avoided.

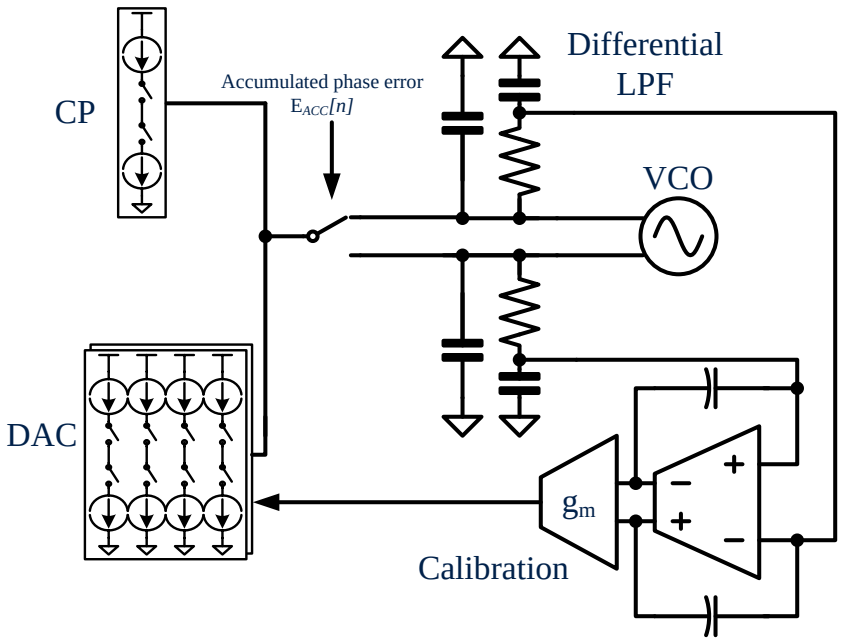


Figure 4.3: Differential LMS Gain Calibration in [SWG07].

The VCO has two equal half-sized inputs, each of which is connected to a loop filter with identical component values. If both input terminals of the VCO are connected together, the VCO would have identically to a normal single input VCO. In this way the output frequency is proportional to the sum of the two input voltages, but insensitive to the difference between the two input voltages. Hence the correlation signal is constant over the duration of a CP/DAC pulse, and it switches the CP/DAC currents between two equivalent loop filters.

The accumulated quantization error $E_{ACC}[n]$ is related to the CP and DAC charge, the switching of the CP and DAC current is equivalent in Differential Mode (DM) to multiply I_{CP} and I_{DAC} by $E_{ACC}[n]$, and results in a change in the DM voltage. In practice, I_{CP} and I_{DAC} are large pulses of current occurring over a short duration. It causes a significant change at the input of the calibration loop during the DAC pulse, which results in a significant change in the DAC bias current during the duration of the DAC pulse. The differential lowpass filtered voltages in the calibration loop are used to reduce the variation in the DAC bias current for the duration of a DAC pulse. Therefore it contains the correlate signal information necessary for calibration loop operation.

Similar to the VCO operation, the calibration loop is a differential circuit and can be designed to obtain very low sensitivity against Common Mode (CM) signal. In this

way, the CM voltage is used in the PLL signal path, and the DM voltage is used in the calibration signal path. Therefore, the LMS calibration technique by differential topologies of the VCO, loop filter and the integrator to reject the DC common voltage. The sign-bit multiplication is implemented as a pair of switches in front of the loop filter so that the mismatching error can be continuously fedback to the DAC in analog domain. The settling time is dramatically shortened without the limitation of calibration bandwidth.

However, several potential issues come up: The mismatches in the two signal paths results in a CM-DM conversion in the calibration loop, and a DM-CM conversion in the PLL, which affect the PLL system sensitivity and linearity, especially for the VCO control voltage; The mismatches between the loop filter halves and between the varactor halves cause phase noise performance degradation; The differential switches triggered at reference clock are located inside the signal correlation path, generating additional spurs at reference and its harmonic frequencies.

4.2 Proposed Wideband Synthesizer Architecture

The toplevel block diagram of the proposed wideband synthesizer is shown in Fig. 4.4. Excluding the crystal, all the elements are fully integrated as well as a 3-wire configuration interface and a high speed data interface. Two functional blocks added to a conventional synthesizer are quantization noise cancellation circuits and DAC gain calibration circuits. In the noise cancellation path, the residue of the 3rd-stage quantizer in MASH-111 is directly truncated and differentiated in 2nd-order instead of another $\Sigma\Delta$ modulator. The characteristic comparison between the conventional $\Sigma\Delta$ requantizer and the differentiator was illustrated in the previous chapter. In this way the identical noise shaping is achieved with lower computation complexity without concerning the stability issues. Subsequently the residue error from $\Sigma\Delta$ quantizer is segmented aligned to control the two 32-bit DAC banks, respectively for coarse and fine currents. A 4th-order loop filter is adopted from the classical structure to generate the desired and reference signal for LMS noise cancellation process.

The calibration circuits consist of a multiplier, an integrator and a Voltage-to-Current (VC) converter between the modified loop filter and the DAC current bias. The 4-bit MSB of the residue error is differentially coded into analog domain and connected to the calibration circuits for multiplication. If there is a gain mismatch between the signal path and noise cancellation path, a residue quantization error voltage will be left in the loop filter, which modulates the VCO and hence generates fractional spurs. Since each charge pump output pulse contains an error term proportional to the accumulated quantization noise, the DAC gain can be adjusted adaptively based on the LMS algorithm by multiplying the buffered loop filter voltage with the accumulated quantization error. However, the challenge of the calibration circuit is how to detect the small residue error accumulated in the loop filter, and how to correlate it fast and

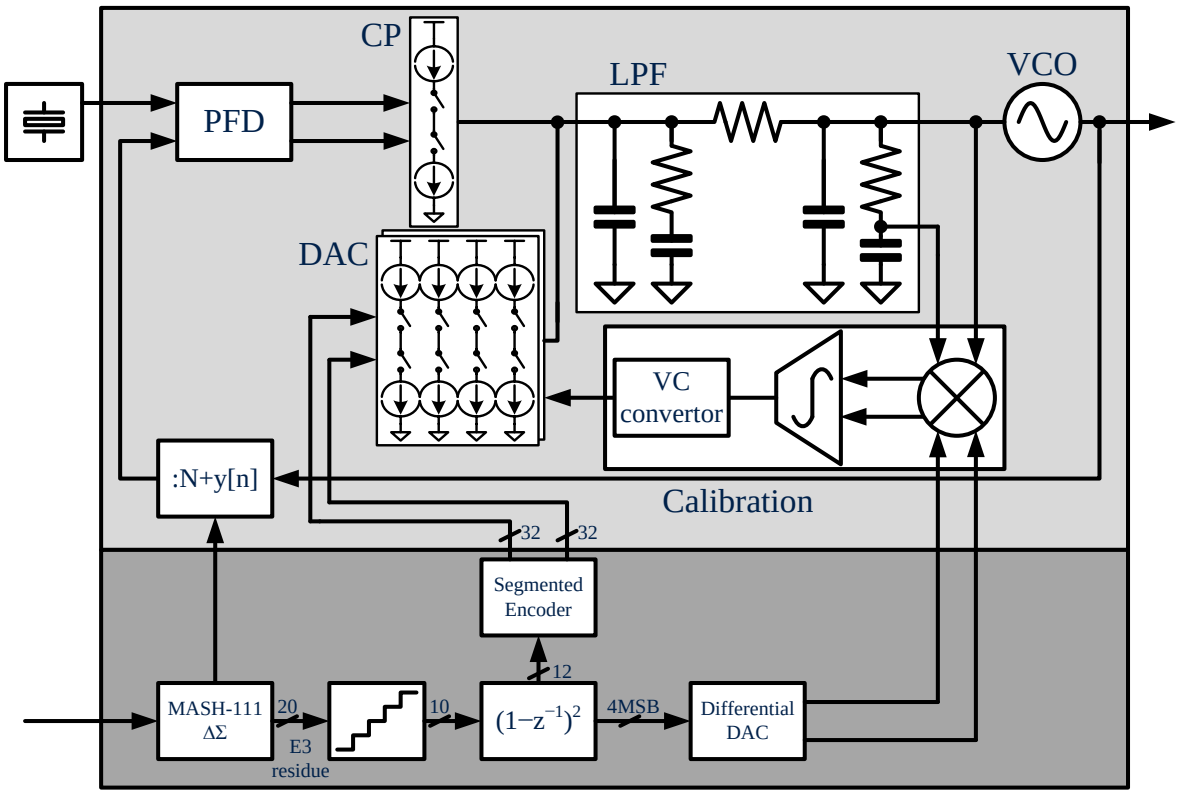


Figure 4.4: Toplevel block diagram of the proposed synthesizer.

precise without disturbing other circuits. The key building blocks are illustrated in the next section.

4.3 Circuit Implementation

4.3.1 Loop Filter

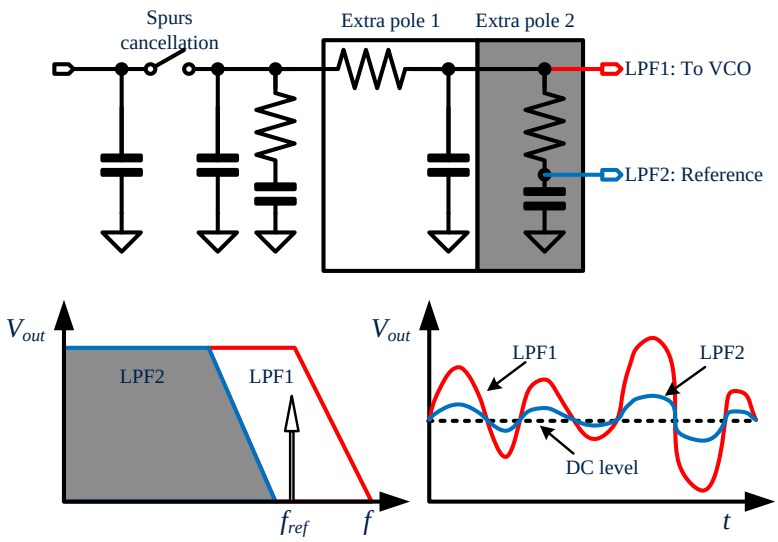


Figure 4.5: Proposed loop filter structure and characteristic.

Fig. 4.5 shows the structure and characteristic of the 4th-order loop filter. In the first stage, a switch is used for the spur cancellation. Since the CP pulses have a fixed amplitude and modulated width whereas the DAC pulses have a fixed width and modulated amplitude, their occurring time can not be exactly synchronized. The spur cancellation switch turns off when the CP or DAC current exist, isolating the charging/discharging current errors from the VCO control signal. It turns on when neither CP nor DAC current is enabled so that the total current pulses due to CP/CP mismatch are smoothly converted to the voltage domain in the loop filter.

The following stage contains a cascaded low-pass RC filter and generates two extra poles. The first extra pole is located at high frequency. It is directly connected to VCO and determines the PLL bandwidth. It passes through the modulated baseband signals and can not completely block the reference frequency signals. Therefore, the residue voltage resonated at the reference frequency according to the current mismatches between CP and DAC can be obviously seen at LPF1 port. The second extra pole is located far below the reference frequency, so a flatter waveform is obtained at LPF2 port.

The group delay difference between LPF1 and LPF2 can be ignorable. By subtracting the voltages at these two ports, the cancellation error information can be extracted, as they share the same DC level voltage.

4.3.2 Calibration Circuits

Fig. 4.6 shows the schematic of the calibration circuits. In the first stage the residue errors are linearly copied by the source-followers. The differential 4-bit residue quantization errors E_Q and $\overline{E_Q}$ are connected to the gate voltages of the cross-coupled switches for multiplication. Instead of sign-bit multiplication in [GS06; SWG07], faster settling time and higher accuracy are achieved in the error detection process. When the MOS switches operate in the linear region, their impedance are changed linearly according to the gate voltage. The output voltage difference ΔV is proportional to the product of the input voltage difference and the residue quantization error:

$$\Delta V(t) \propto [V_{LPF1}(t) - V_{LPF2}(t)]E_Q[n]. \tag{4.2}$$

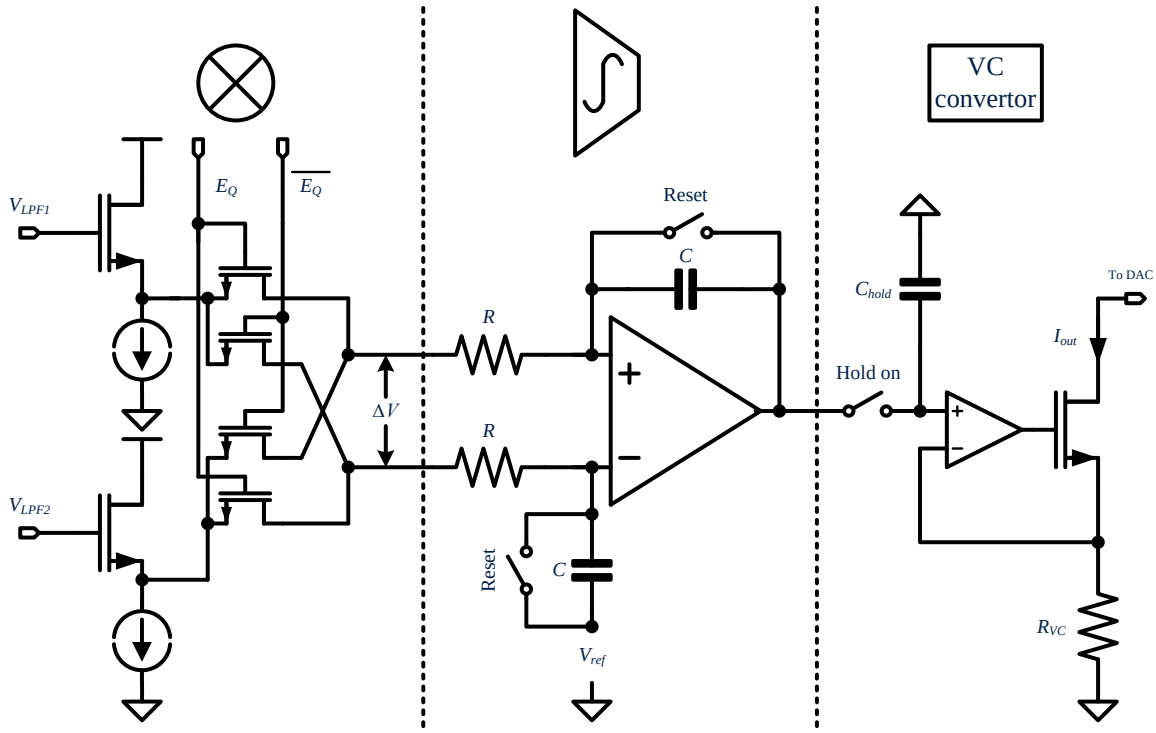


Figure 4.6: Proposed gain calibration circuits.

In the second stage, the RC-integrator is used to accumulate the correlated signal information which contains the CP/DAC mismatches. The OP has 80 dB DC gain to

detect small errors, and a wide input common range for the loop filter voltage variation over the PLL frequency range. Comparing to the fully differential integrator, the input offset of OP cannot lead to the DAC current mismatches since the static current offset will be calibrated by the feedback loop in the following calibration process. When the reset switches are turned on, the integrator output is set as an initial value V_{ref}. The LMS filter bandwidth is determined by switched-capacitor arrays with a maximum value of 4 pF. Thus the integrator output signal is expressed as:

$$V_{out}(t) = \int_0^t -\frac{\Delta V(t)}{RC} dt + V_{ref}. \tag{4.3}$$

In the final stage, the integrated voltage is converted to a current and mirrored to use as the DAC reference current:

$$I_{out}(t) = \frac{V_{out}(t)}{R_{VC}}. \tag{4.4}$$

With the same principle, the voltage offset in the VC convertor and the mismatch of the resistance are also not harmful during the LMS calibration process.

Fig. 4.7 shows the waveforms of the VCO control voltage and the DAC bias current in the calibration process. After PLL gets locked, there is a large VCO control voltage modulation. Then the DAC is enabled so that the default reference current $\frac{V_{ref}}{R_{VC}}$ is used for noise cancellation. The VCO control voltage variation is clearly reduced. It is assumed that still 10% current mismatches remains with the default setting. When the LMS is enabled, DAC bias current gets converged after 20 µs and reaches the desired current, meanwhile the VCO control voltage variation is decreased gradually. Finally the hold on switch isolates the DAC bias current from the calibration circuits. At the same time the multiplication and integration circuits are switched off, saving 1.2 mA current (14% of the system). Therefore, the DAC reference current stays constant and immune to other blocks.

4.3.3 Charge Pump and DAC Banks

As shown in Fig. 4.8, CP and DAC are implemented in the same block because they are composed of the same unit cell and share the same biasing and output nodes. The MSB and LSB banks of the DAC are thermometer coded to achieve monotonicity. Inside the unit cell, the loads for differential control signals are equalized with one PMOS and one NMOS to compensate rising/falling timing mismatches and charge injection, as illustrated in [Y Z+13b]. A wide input range amplifier stabilizes the differential output voltages so that the common nodes in CP and DAC can be pushed or pulled to the same level, making the currents of both paths identical over the PLL frequency range. A dummy capacitor is used to equalize the loads. With the symmetric topology of CP and DAC, the fractional and reference spurs due to the charging/discharging current mismatches are greatly attenuated.

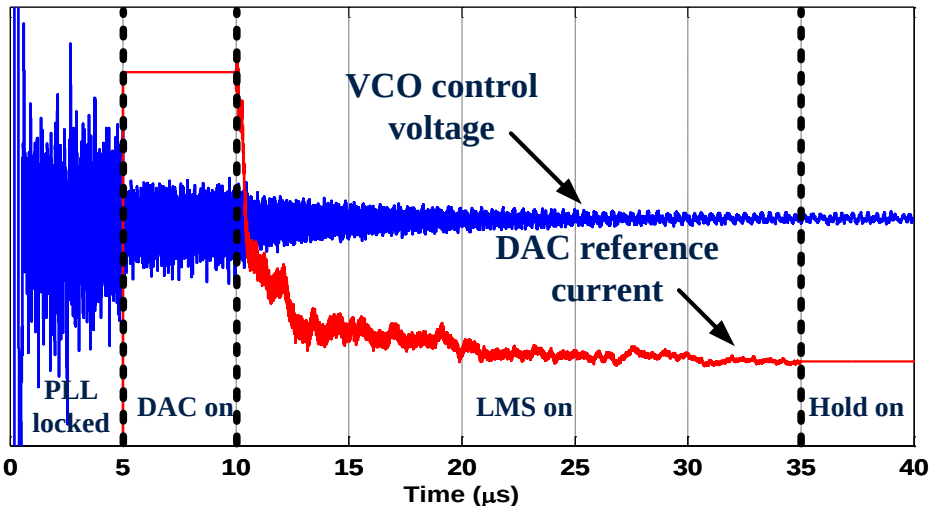


Figure 4.7: Calibration process.

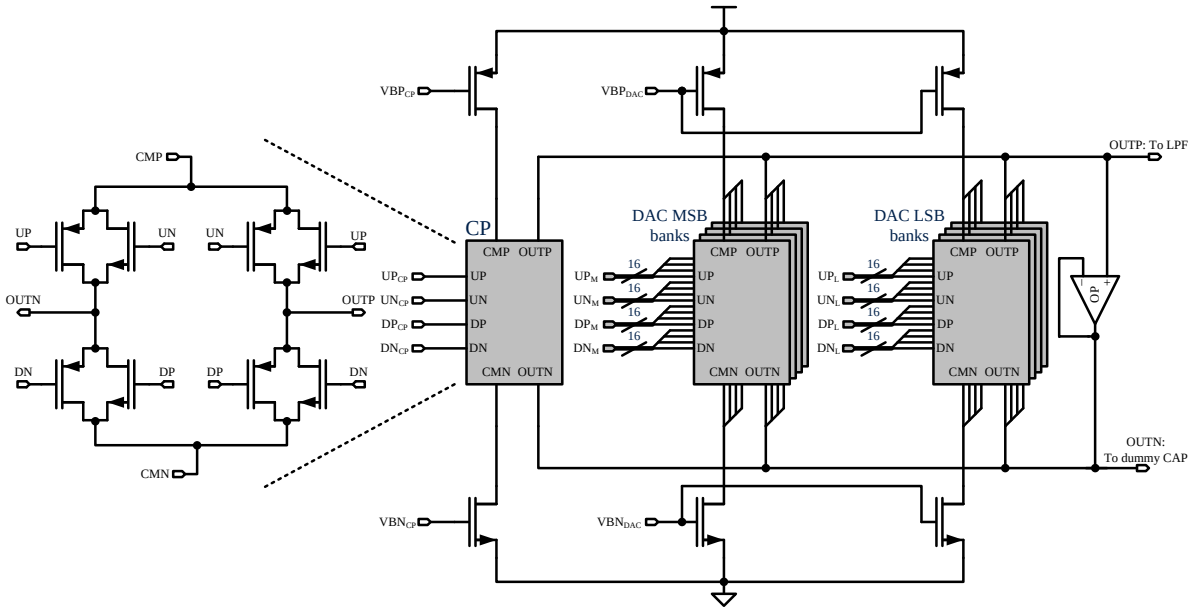


Figure 4.8: Charge pump and DAC current generator.

4.4 Measurement Results

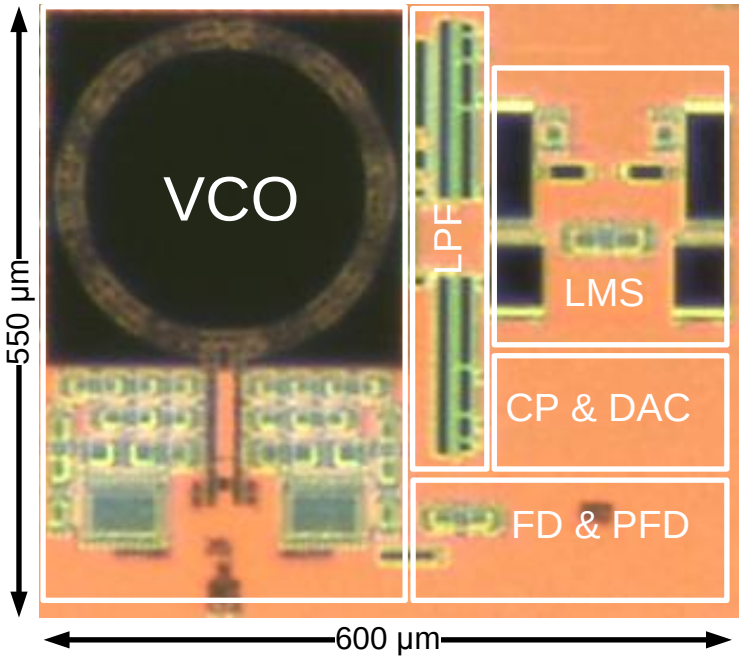


Figure 4.9: PLL micrograph.

A 1.8 GHz fractional-N synthesizer was fabricated in 130 nm CMOS, where the mixed-signal and RF parts were full custom design and the digital block was synthesized using the standard logic cells. The die micrograph is shown in Fig. 4.9. It occupies 0.33 mm^2 and consumes 8.3 mW core power, excluding a differential 3.5 mA CML buffer to drive the PLL output. The PLL output frequency range is from 1.6 GHz to 1.8 GHz, and its loop bandwidth is adjustable from 150 kHz to 1.5 MHz with crystal reference clock of 32 MHz. The VCO is a symmetric LC oscillator with a nominal sensitivity of 75 MHz/V. The multi-modulus divider consists of 6-stage 2/3 prescaler resulting a division ratio from 64 to 127. ESD protection is implemented on all pins.

Fig. 4.10 shows the phase noise and spectral comparison with the initial state, DAC enabled and calibration enabled conditions at 1.76 GHz carrier frequency. Starting from the initial state, it can be seen the $\Sigma\Delta$ quantization noise are suppressed after the DAC is turned on. The outband phase noise performance at 3 MHz offset is improved from −110 dBc/Hz to −122 dBc/Hz. When the CP/DAC gain calibration technique is enabled, the phase noise performance is further improved as well as the fractional and reference spurs are greatly attenuated. In the final hold on state, the phase noise performance at 3 MHz offset finally achieves −129 dBc/Hz with the proposed technique.

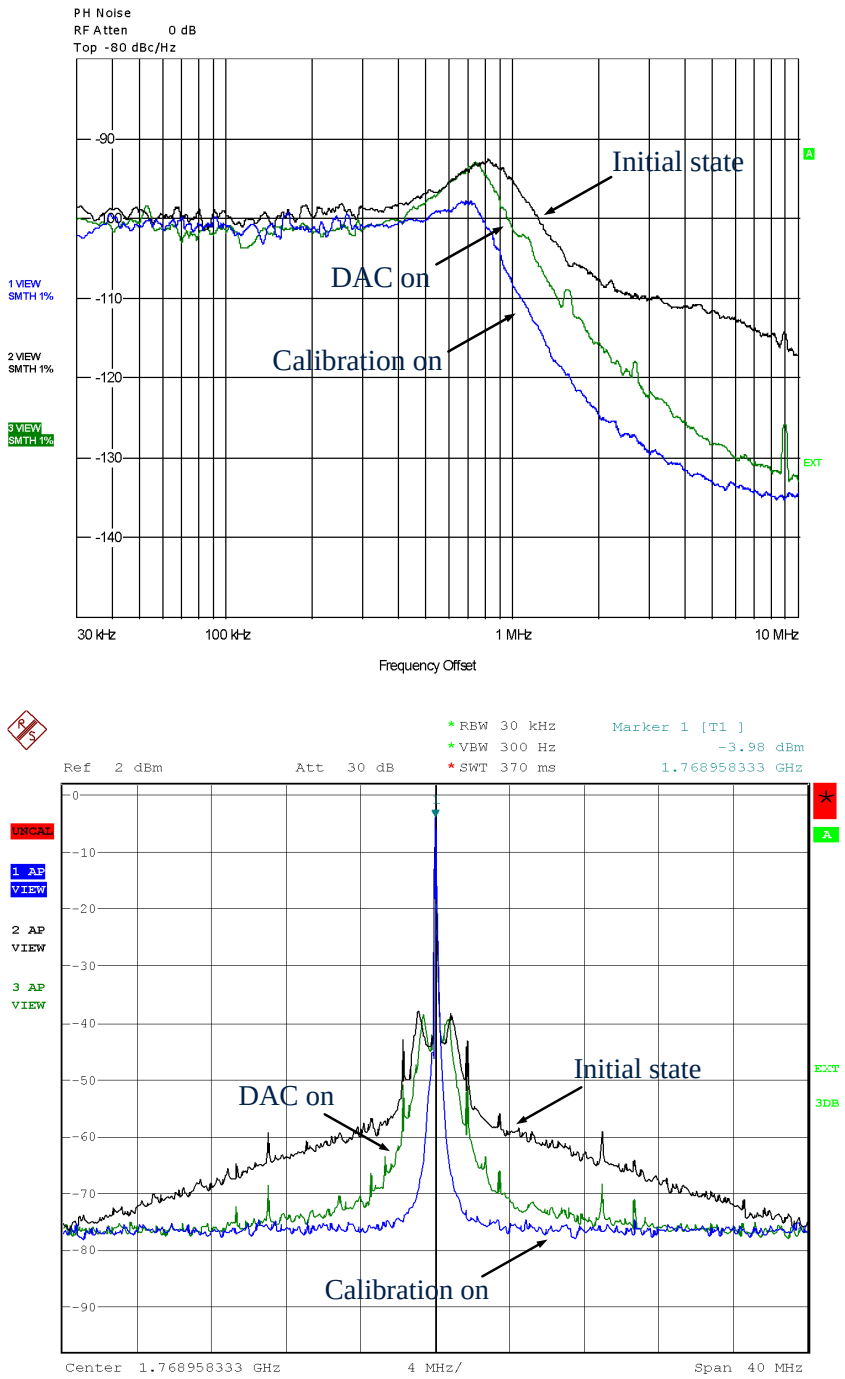


Figure 4.10: (a). Phase noise comparison; (b). Spectral comparison.

Fig. 4.11 shows the reference spur in fractional mode is −68 dBc. In the integer mode it is reduced to −72 dBc, which indicates good immunity of the PLL system to the ΣΔ modulated switching process. The fractional spur in worst case is −56 dBc.

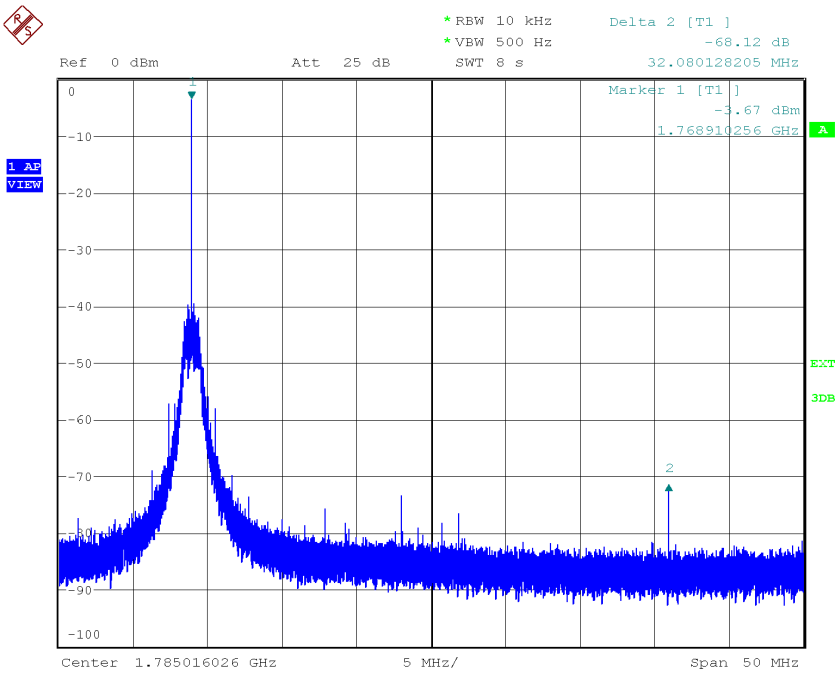


Figure 4.11: Reference spur performance.

Fig. 4.12 shows the PLL output spectral of 1 Mbps data rate, 250 KHz frequency deviation GFSK modulated Bluetooth LE baseband signal. When the loop filter bandwidth is set as 1 MHz, an obvious improvments can be seen when the proposed calibration technique is enabled. The wideband noise is highly attenuated. To compare with the 300 kHz two-pint modulation technique, the proposed calibration technique with direct modulation demonstrates the same excellent performance.

Fig. 4.13 shows the eye patterns at 1.76 GHz carrier frequency with 200 kbps 4FSK SUN standard and 1 Mbps GFSK in Bluetooth LE standard baseband signals. It can be seen that under different circumstances of data rates, frequency deviations and modulation schemes, the eyes are clearly open.

Fig. 4.14 shows the block diagram of dual conversion process. The 1.6 GHz PLL output is connected to a frequency divide, mixed up with itself to obtain 2.4 GHz carrier frequency, and finally the output power is adjusted by a high frequency VGA. Fig. 4.15 shows the corresponding eye patterns at VGA output with 0 dBm power. The eyes are clearly open, so the transmitted signal can be successfully demodulated and determined at the receiver side.

Tab. 4.1 shows a comparison between the proposed design and other relevant prior

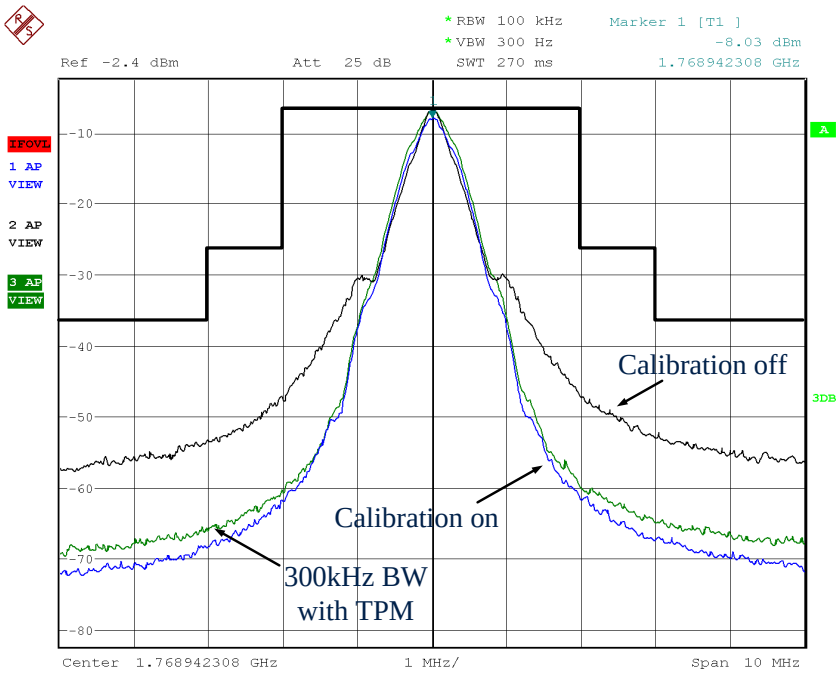


Figure 4.12: Modulation performance.

art. The proposed approach exhibits the excellent phase noise and spur suppression performance with lower power consumption and smaller area.

4.5 Conclusion

A low effort adaptive phase noise cancellation calibration technique for the fully integrated wideband fractional-N synthesizer based on the classical loop filter structure is presented. This calibration technique demonstrates fast settling time, low spurs and excellent phase noise performance with low power consumption and small area. Due to its simplicity and flexibility, it can be directly added as a straightforward phase noise enhancement for wideband PLLs, and also provides an easy and feasible solution of direct frequency/phase modulation for short-range wireless standards.

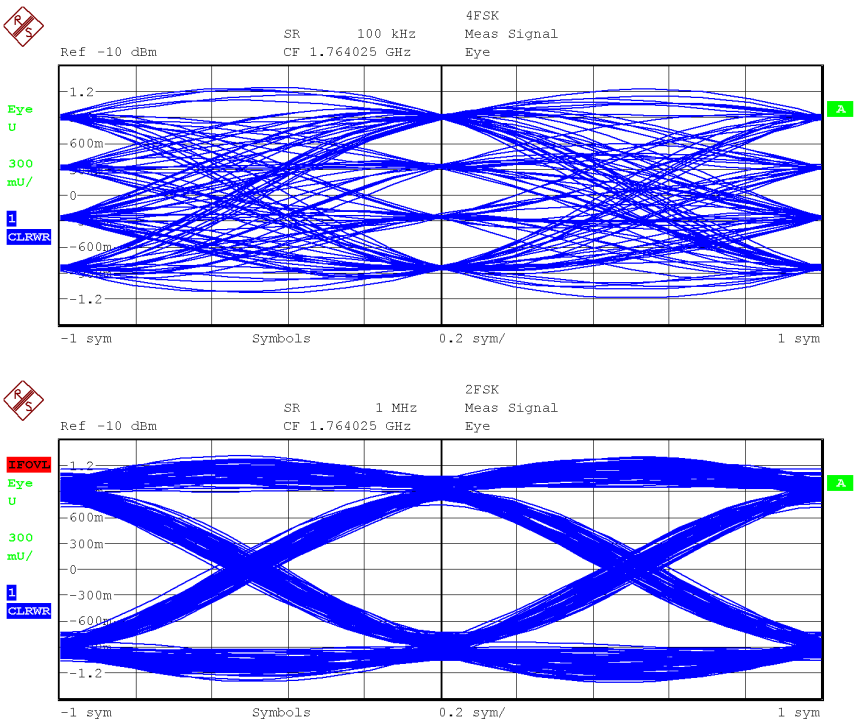


Figure 4.13: (a). 200 kbps 4FSK in SUN standard at 1.76 GHz; (b). 1 Mbps GFSK in Bluetooth LE standard at 1.76 GHz.

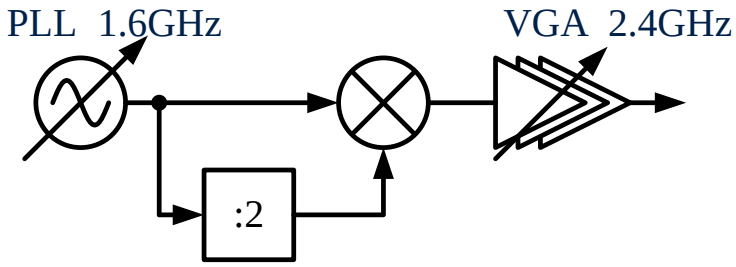


Figure 4.14: Dual-conversion block diagram.

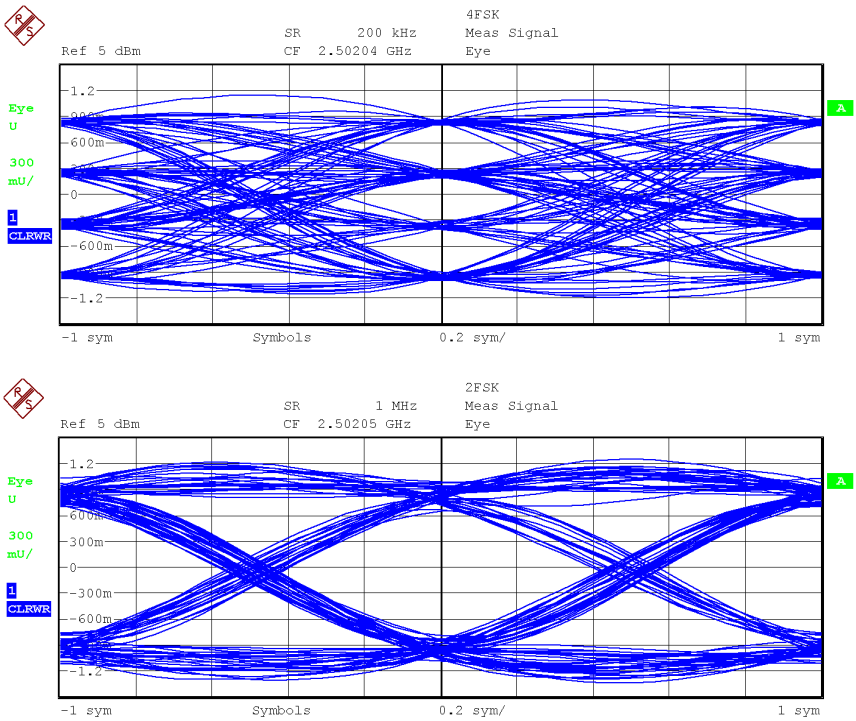


Figure 4.15: (a). 200 kbps 4FSK in SUN standard at 2.4 GHz with 0 dBm power; (b). 1 Mbps GFSK in Bluetooth LE standard at 2.4 GHz with 0 dBm power.

Table 4.1: Performance comparison with prior works.

Parameter	[SWG07]	[Jee+13]	[PPC12]	This work
Technology (nm)	180	130	130	130
Frequency (GHz)	2.4	1	2.4	1.8
Reference (MHz)	12	32	60	32
Bandwidth (MHz)	0.75	3.2	2	1
Cancellation method	DAC	FIR	SubPLL	DAC
VCO type	LC	Ring	LC	LC
Inband phase noise (dBc/Hz) @100 kHz	−101	−106	−102	−101
Outband phase noise (dBc/Hz) @3 MHz	−126	−115	−106	−129
Reference spur (dBc)	−53	−66	−55	−68
Fractional spur (dBc)	−47	N.A.	−55	−56
Core area (mm^2)	4.8	0.31	0.46	0.33
Core power (mW)	38	16.8	9.6	8.3

Chapter 5

Low Power Demodulator in Low-IF Receiver

5.1 Background

Low power short range wireless systems are commonly used today, where the applications are ranging from PC peripherals over health and life style to sensor networks. Constant envelope modulation schemes in particular GFSK are mainly using in different flavors for these low tier applications. Over the last years, the relevant standards namely Bluetooth, Bluetooth LE, ANT+, ZigBee and DECT 6.0 have been and will be applied in a rapidly increasing number of applications. The variety of these applications and their implementation requirements are generating the demand low power implementation in moderately scaled CMOS technology nodes. The push for mode more than Moore in the 130 nm node will require the co-integration of low power radios for many new applications e.g. in the field of smart lighting, smart home, health care and gaming. Within the reminder of this chapter Bluetooth will be used as a reference standard for the implementation due to its popularity. The described techniques can be utilized for all GFSK based system e.g. DECT 6.0, ANT+ or ZigBee, which can be fully integrated in a cost-effective way today.

In a low-IF receiver, the RF signal is mixed down to a low intermediate frequency. It is an efficient low-power low-cost architecture [CS98]. Compared to the zero-IF

architecture, it has higher inherent immunity to DC offsets and 1/f noise [Raz97]. A typical low-IF receiver consist of two parts: down conversion and demodulation. During the down conversion process, the wanted signal is filtered and selected from its neighbors, and converted from its carrier frequency to a frequency which is more suitable for the demodulator. Due to the high frequency and high performance specifications, its implementation is fully analog. The demodulator is operated in a lower frequency, thus it can be implemented fully digitally. However, the main drawback of low-IF architecture is the interference caused by a signal at the image frequency. Because in low-IF systems, the image signal can be leaked into the signals, because of the imperfections from the analog circuits in the down conversion, such as gain and phase errors from the quadrature mixer, coefficient mismatches and feedback imbalance from the ΣΔADC.

This imperfection from the analog circuits leads to I/Q path mismatch, which degrades the image rejection performance of the receiver [Mah06]. Several different I/Q mismatch compensation approaches are discussed in prior arts, such as digital [GKL07], analog [Beh+01],[Hor+01],[Yue+04] and mixed mode [DR03],[EE04]. Most of these methods are based on Least Mean Square (LMS) algorithm, which needs a reference signal to separate the images from the desired signal. However, obtaining the desired and reference signals are the challenge tasks: Some LMS algorithms are strongly dependent on the characteristic of input signals, for example, they are only valid if the input signals have narrow band [Hen+05] or the mismatches are relatively small [LS06]; some algorithms need additional circuits for subsampling or offset time measurements, and they are too complicated to be synthesized in hardware [CH01],[LL10],[VR04]; some algorithms are simple and efficient, but they need to operate at IF frequency, which leads to a high power consumption [YS99],[EMB06],[VRK01]. The proposed demodulator system uses a novel symmetric frequency conversion circuit: signals at positive frequency are down converted to baseband as the desired signals, while the images at negative frequency are also up converted to baseband as the reference signals. A complex LMS algorithm operating at baseband frequency is applied to separate the signal of interest from its image. Since the desired and reference signals for LMS filter are generated and processed in a symmetric way, the leakage from signal to image is identical to the leakage from image to signal. Therefore only one coefficient data is necessary to eliminate the leakages both from the desired and reference signals, resulting an easier fully integrated solution.

The group delay is another issue caused by the polyphase filter, which has a constant and flat magnitude response in the passband and a high attenuation in the image band. However, the group delay response of the polyphase filter is not constant, especially in the vicinity of the band-edge, leading to a error in the decimation. A recursive all-pass filter with a prescribed group delay response is desired to equalize the phase response to make the group delay approximately constant in the interested bandwidth. In the mobile communication environments, the frequency offset, the carrier phase offset and the symbol timing errors are often encountered due to oscillator instabilities and Doppler

effects. It is important to build a robust and fast method to estimate and compensate the frequency offset and symbol timing errors when the data is transmitted in the burst mode. The prior theoretical approaches for jointly estimating and frequency offset use an optimality criterion, such as Maximum Likelihood (ML) [Chi11], Maximum-A-Posteriori (MAP) [DCH01; CV01] or Fast Fourier Transform (FFT) [HFH00]. They are precise, but too complicated to be integrated. A simple but suboptimal structure is preferred in Bluetooth applications. The proposed frequency offset estimation is implemented at the latest demodulation stage, adjusting the decision threshold during a preamble period in a straight forward manner.

In this chapter, at first the system model and imperfection issues occurring in the low-IF receiver are analyzed, including I/Q imbalance, frequency offset and inconstant group delay. Subsequently the proposed demodulator architecture and its mechanism to overcome the above imperfection issues are explained and verified in details. Finally through the simulation, the performance of this receiver architecture is verified.

5.2 Demodulator System Analysis

The general low-IF receiver structure and its corresponding spectrals at each stage are shown in Fig. 5.1. The incoming RF signal $v_{RF}(t)$ received from the antenna is applied to a LNA, mixed down with the output of the quadrature VCO through the mixer, producing the IF signal $v_{IF}(t)$. Ideally the LO signals for the I and Q branches should have equal amplitude and a phase difference of 90°. In reality due to the mismatch, the image at $-f_{IF}$ is leaked into the signal at $-f_{IF}$. The resulting IF signal is filtered by the polyphase filter, generating the signal $v_{poly}(t)$ which has more image power suppression. At the final stage, it is converted by the single bit ΣΔADC into the digital domain. The ΣΔADC is a over sampled ADC which removes the quantization noise out of the band of interest[JMS97].

5.2.1 System Modeling for I/Q Imbalance

Assuming the RF incoming signal $v_{RF}(t)$ consists the wanted signal $v_{sig}(t)$ at $f_{LO} - f_{IF}$ from the desired channel and the unwanted image signal $v_{img}(t)$ at $f_{LO} + f_{IF}$ from another channel, it can be expressed as:

$$v_{RF}(t) = Re[v_{sig}(t)e^{j(\omega_{LO}-\omega_{IF})t} + v_{img}(t)e^{j(\omega_{LO}+\omega_{IF})t}] \tag{5.1}$$

Notice both $v_{sig}(t)$ and $v_{img}(t)$ are baseband real signals. $v_{sig}(t) = v^*_{sig}(t)$ and $v_{img}(t) = v^*_{img}(t)$.

For the impairment in the quadrature mixer, the gain and phase imbalance between I and Q channels are defined as α and θ respectively. So the normalized LO signal $v_{LO}(t)$ from the mixer is given as:

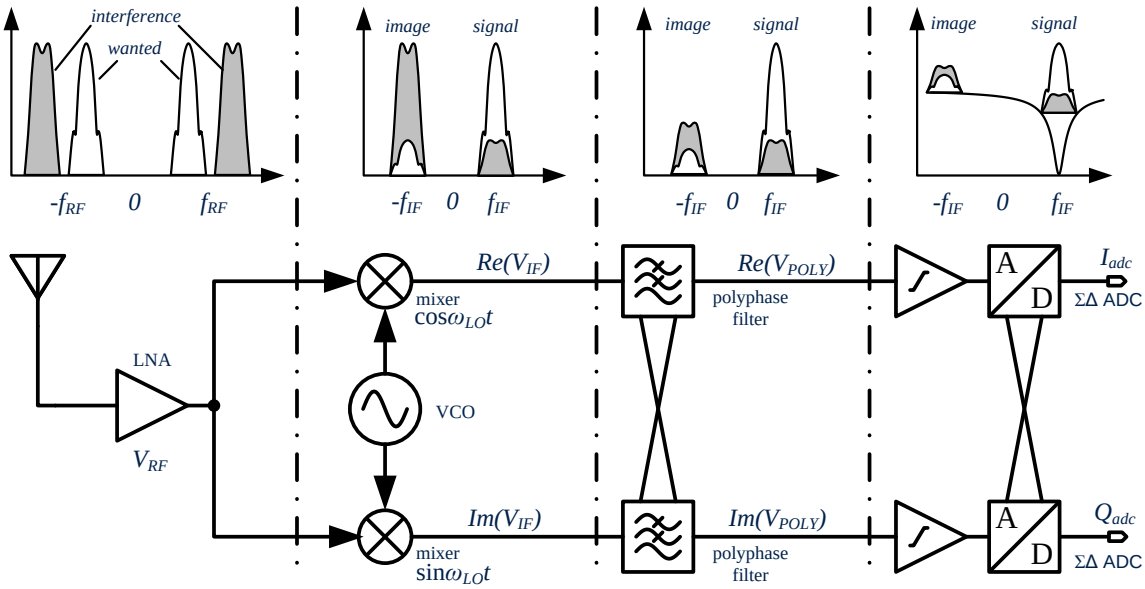


Figure 5.1: Low-IF receiver frontend structure.

$$
\begin{aligned}
v_{LO}(t) =&(1+\frac{\alpha}{2})\cos(\omega_{LO}t+\frac{\theta}{2})+(1-\frac{\alpha}{2})\sin(\omega_{LO}t-\frac{\theta}{2}) \\
=&\frac{1}{2}\{[(1+\frac{\alpha}{2})e^{j\frac{\theta}{2}}+(1-\frac{\alpha}{2})e^{-j\frac{\theta}{2}}]e^{j\omega_{LO}t} \\
&+[(1+\frac{\alpha}{2})e^{-j\frac{\theta}{2}}-(1-\frac{\alpha}{2})e^{j\frac{\theta}{2}}]e^{-j\omega_{LO}t}\}
\end{aligned}
\tag{5.2}
$$

To simplify the equations, define

$$
\begin{aligned}
\beta_1 &= \frac{1}{2}[(1+\frac{\alpha}{2})e^{j\frac{\theta}{2}}+(1-\frac{\alpha}{2})e^{-j\frac{\theta}{2}}] \\
\beta_2 &= \frac{1}{2}[(1+\frac{\alpha}{2})e^{-j\frac{\theta}{2}}-(1-\frac{\alpha}{2})e^{j\frac{\theta}{2}}]
\end{aligned}
\tag{5.3}
$$

The LO signal $v_{LO}(t)$ can be rewritten as:

$$
v_{LO}(t) = \beta_1 e^{j\omega_{LO}t} + \beta_2 e^{\omega_{LO}t} \tag{5.4}
$$

The I/Q imbalanced down-converted IF signal $v_{IF}(t)$ can be expressed as:

$$
\begin{aligned}
v_{IF}(t) =&LPF(v_{RF}(t)\cdot v_{LO}(t)) \\
=&\beta_1 v_{sig}(t)e^{j\omega_{IF}t}+\beta_2 v_{img}(t)e^{j\omega_{IF}t} \\
&+\beta_2 v_{sig}(t)e^{-j\omega_{IF}t}+\beta_1 v_{img}(t)e^{-j\omega_{IF}t}
\end{aligned}
\tag{5.5}
$$

Where LPF denotes the lowpass filtering function. In the frequency domain, the spectrum of $v_{IF}(t)$ is derived as:

$$\begin{aligned} V_{IF}(\omega) =& \beta_1 V_{sig}(\omega - \omega_{IF}) + \beta_2 V_{img}(\omega - \omega_{IF}) \\ &+ \beta_2 V_{sig}(\omega + \omega_{IF}) + \beta_1 V_{img}(\omega + \omega_{IF}) \end{aligned} \tag{5.6}$$

It can be seen from $V_{IF}(\omega)$ that the image is leaked into the desired band, on the other hand there is also a leakage from the desired signal into the image channel. Desired band signal $V_{sig_{IF}}(\omega)$ and image band signal $V_{img_{IF}}(\omega)$ can be described in matrix:

$$\begin{bmatrix} V_{sig_{IF}}(\omega) \\ V_{img_{IF}}(\omega) \end{bmatrix} = \begin{bmatrix} \beta_1 & \beta_2 \\ \beta_2 & \beta_1 \end{bmatrix} \begin{bmatrix} V_{sig}(\omega) \\ V_{img}(\omega) \end{bmatrix} \tag{5.7}$$

Define $P_{sig}(\omega)$ and $P_{img}(\omega)$ as the power spectral density of $V_{sig}(\omega)$ and $V_{img}(\omega)$ respectively, BW as the bandwidth of the polyphase filter, which is much higher than the input signal bandwidth, the signal and the image power at the positive IF frequency band can be calculated as:

$$\begin{aligned} P_{sig_{IF}} =& \int_{\omega_{IF}-\frac{BW}{2}}^{\omega_{IF}+\frac{BW}{2}} |\beta_1|^2 P_{sig}(\omega - \omega_{IF}) d\omega \\ \approx& |\beta_1|^2 P_{sig} \\ P_{img_{IF}} =& \int_{\omega_{IF}-\frac{BW}{2}}^{\omega_{IF}+\frac{BW}{2}} |\beta_2|^2 P_{img}(\omega - \omega_{IF}) d\omega \\ \approx& |\beta_2|^2 P_{img} \end{aligned} \tag{5.8}$$

The Image Rejection Ratio (IRR) before the IF filter is:

$$\begin{aligned} IRR_{IF} =& \frac{|\beta_1|^2}{|\beta_2|^2} \\ =& \frac{4\cos^2\frac{\theta}{2} + \alpha^2 \sin^2\frac{\theta}{2}}{4\sin^2\frac{\theta}{2} + \alpha^2\cos^2\frac{\theta}{2}} \end{aligned} \tag{5.9}$$

Usually the IF filter bandwidth B is much larger than baseband signal in order to pass through the signals from all the channels. Hence, the polyphase filter can be modeled as a constant gain at the signal band and a high attenuation at the image band. For the polyphase filter mismatching models, the magnitude response of the signal band and the image band is constant over the frequency, according to its wide bandwidth. However, the image rejection ratio varies due to the mismatch, as shown in Fig. 5.2. The nonlinear phase response in the passband will be discussed in the group delay section. The detailed mismatch model and effect depending on the different polyphase structures is illustrated in [Kim+08a].

Assuming a 3rd-order lowpass filter is implemented, the attenuation factor at the negative IF band is D, the three poles are located in the passband, so the phase response at image band is 270° delayed than the inband phase response. The polyphase filter transfer function can be generally expressed as:

$$H_{IF}(\omega) = \begin{cases} 1 & \omega_{IF} - \frac{B}{2} < \omega < \omega_{IF} + \frac{B}{2} \\ \frac{-j}{D} & -\omega_{IF} - \frac{B}{2} < \omega < -\omega_{IF} + \frac{B}{2} \end{cases} \tag{5.10}$$

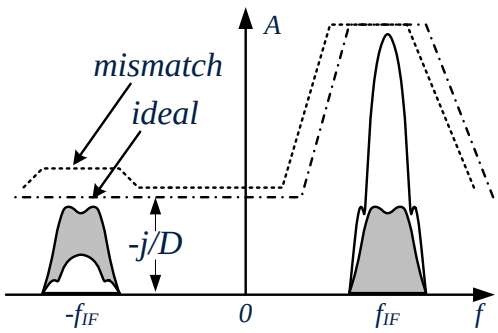


Figure 5.2: Polyphase mismatch model.

The spectral of the polyphase filter output can be written as:

$$\begin{aligned} \begin{bmatrix} V_{sig_{poly}}(\omega) \\ V_{img_{poly}}(\omega) \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ 0 & \frac{-j}{D} \end{bmatrix} \begin{bmatrix} \beta_1 & \beta_2 \\ \beta_2 & \beta_1 \end{bmatrix} \begin{bmatrix} V_{sig}(\omega) \\ V_{img}(\omega) \end{bmatrix} \\ &= \begin{bmatrix} \beta_1 & \beta_2 \\ \frac{-j}{D}\beta_2 & \frac{-j}{D}\beta_1 \end{bmatrix} \begin{bmatrix} V_{sig}(\omega) \\ V_{img}(\omega) \end{bmatrix} \end{aligned} \tag{5.11}$$

A complex bandpass ΣΔ modulator model consists of a filter and a quantizer in the feedback loop. The ΣΔ modulator gains a bandwidth and SNR advantage over its real counterparts, because the extra noise transfer function remains zero in its passband. Therefore, one can assume that in the band of interest, the STF of the ΣΔ modulator has constant gain response, and the NTF is also constant, but much lower. In the actual implementation, the I/Q channel mismatch causes the complex conjugate of the frequency response to be aliased into the wanted the signal, which is disastrous for a ΣΔ modulator, where the quantization noise at the image band gets aliased into the wanted band. Setting one zero of the noise transfer function at its corresponding image frequency is helpful, but it degrades the noise floor at the signal band.

The quantization noise, generated inside the modulator loop, has also an image response in case of mismatch. Therefore, in addition to STF and NTF, the Image

Signal Transfer Function (ISTF) and Image Noise Transfer Function (INTF) are added in this complex model, as shown in Fig. 5.3.

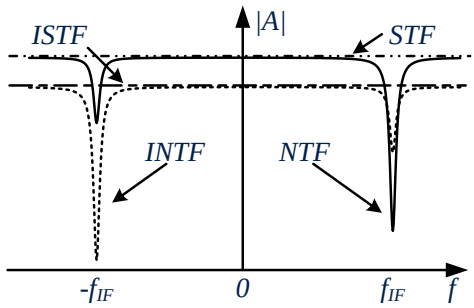


Figure 5.3: ΣΔ modulator mismatch model.

The mismatch model of the ΣΔ modulator should include loop filter mismatch [Kim+08b], input coefficient mismatch [Mar10] and feedback coefficient mismatch [YS99]. The most significant mismatch is from the feedback coefficient mismatch, since the feedback signals from outputs have long paths to crosstalk to each other. It is very difficult to accurately model or calculate the contribution of each mismatching effect. In the general imbalance model, the transfer functions of STF, ISTF, NTF and INTF can be used to define the characteristics of the modulator. Output of the ΣΔ modulator is expressed as:

$$\begin{bmatrix} V_{sig_{adc}}(\omega) \\ V_{img_{adc}}(\omega) \end{bmatrix} = \begin{bmatrix} STF(\omega) & ISTF(\omega) \\ ISTF(\omega) & STF(\omega) \end{bmatrix} \begin{bmatrix} V_{sig_{poly}}(\omega) \\ V_{img_{poly}}(\omega) \end{bmatrix} + \begin{bmatrix} NTF(\omega) & INTF(\omega) \\ INTF(\omega) & NTF(\omega) \end{bmatrix} \begin{bmatrix} E(\omega) \\ E^*(\omega) \end{bmatrix} \tag{5.12}$$

Therefore, the signal and the image power at the positive IF band are:

$$
\begin{aligned}
P_{sig_{adc}} =& \int_{\omega_{IF}-\frac{BW}{2}}^{\omega_{IF}+\frac{BW}{2}} [|STF(\omega)\beta_1|^2 + |\frac{ISTF(\omega)}{D}\beta_2|^2] \\
& P_{sig}(\omega - \omega_{IF})d\omega \\
\approx& (|STF\beta_1|^2 + |\frac{ISTF}{D}\beta_2|^2)P_{sig} \\
P_{img_{adc}} =& \int_{\omega_{IF}-\frac{BW}{2}}^{\omega_{IF}+\frac{BW}{2}} [|STF(\omega)\beta_2|^2 + |\frac{ISTF(\omega)}{D}\beta_1|^2] \\
& P_{img}(\omega - \omega_{IF})d\omega \\
\approx& (|STF\beta_2|^2 + |\frac{ISTF}{D}\beta_1|^2)P_{img}
\end{aligned}
\tag{5.13}
$$

The IRR after the ΣΔADC is:

$$
\begin{aligned}
IRR_{adc} =& \frac{|STF\beta_1|^2 + |\frac{ISTF}{D}\beta_2|^2}{|STF\beta_2|^2 + |\frac{ISTF}{D}\beta_1|^2} \\
=& \frac{4\cos^2\frac{\theta}{2} + |\frac{1}{D}\frac{ISTF}{STF}|^2\alpha^2\sin^2\frac{\theta}{2}}{4\sin^2\frac{\theta}{2} + |\frac{1}{D}\frac{ISTF}{STF}|^2\alpha^2\cos^2\frac{\theta}{2}}
\end{aligned}
\tag{5.14}
$$

The IRR value is plotted as the function of gain and phase mismatch in the mixer, as shown in Fig. 5.4. The upper one describes the IRR performance at the mixer output. The lower one denotes the IRR performance at the ΣΔ modulator output. It is simulated in the case that polyphase filter has 20 dB attenuation at image band, and ΣΔADC has 10% mismatch in the image signal and noise transfer function. The I/Q imbalance issues from the mixer, the polyphase filter and the ΣΔADC are limited by analog design.

These results lead to an imbalance compensation solution necessary in the later signal processing stage. One possible way is to use an LMS adaptive filter to estimate the effect of the image aliasing and subtract it from the signals. This solution compensates for the image interference signal, as well as the image noise is aliased inband. One can see the image interference is frequency independent, and in addition, the signal to image ratio at the positive IF frequency band is the same as the image to signal ratio at the negative IF frequency band. These characteristics can be further used for reduced complexity of LMS filter.

5.2.2 Frequency Offset

Frequency offset between the transmitters and receivers is another problem encountered in wireless communications. For the GFSK modulated Bluetooth signal, an efficient

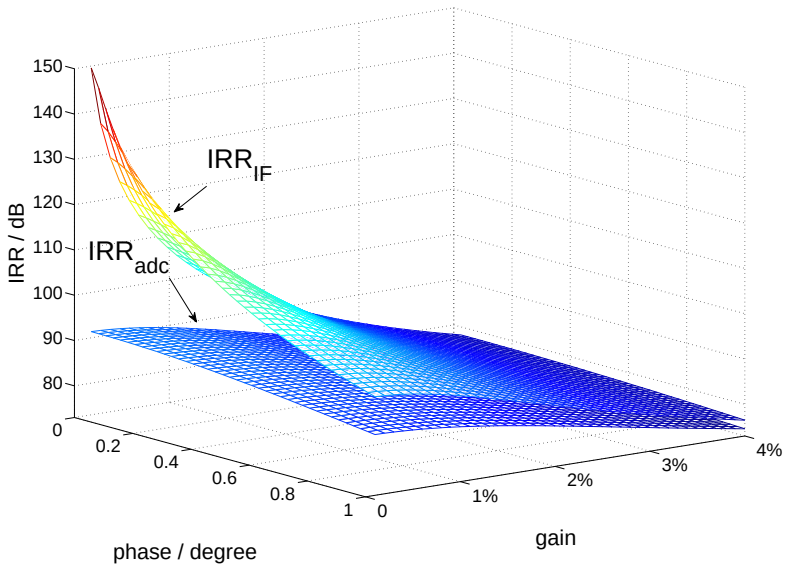


Figure 5.4: IRR performance over mixer gain and phase mismatch.

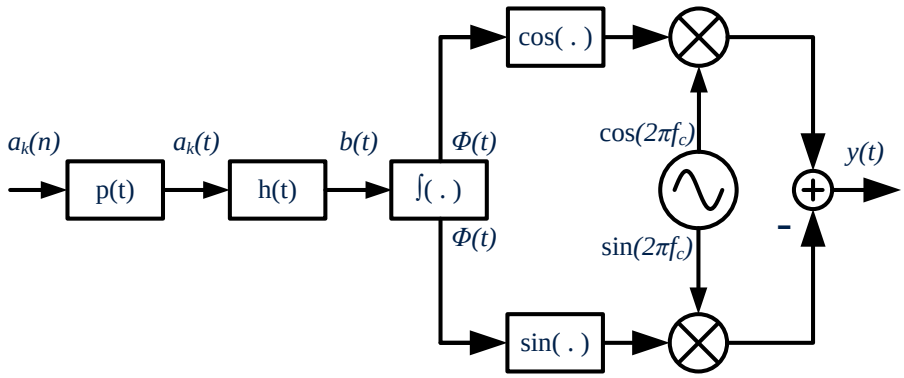


Figure 5.5: GFSK modulation system.

and low complexity offset compensation method is highly desirable. The transmitter structure for the GFSK modulation scheme is shown in Fig. 5.5.

During the modulation, a differential encoded rectangular data stream $a(n)$ is filtered using a Gaussian lowpass filter to get signal $b(t)$:

$$b(t) = \sum_{k=-\infty}^{+\infty} a_k h(t - kT_b) \tag{5.15}$$

Where $a_k \in \{\pm 1\}$ is the bipolar transmitted data with the period of T_b and $h(t)$ is the impulse response of lowpass Gaussian filter. The baseband phase modulation $\phi(t)$ can be expressed as:

$$\phi(t) = \frac{2\pi}{T_b} \int_0^t b(\tau) d\tau = \frac{2\pi}{T_b} \int_0^t \sum_{k=-\infty}^{+\infty} a_k h(\tau - kT_b) d\tau \tag{5.16}$$

So the transmitted signal $y(t)$ is:

$$y(t) = \sqrt{\frac{E_b}{2T_b}} \cos(2\pi f_c t + \phi(t)) \tag{5.17}$$

Where f_c is the carrier frequency and E_b is the bit energy.

For the short range communication standards, the multi-path fading channel and selective Rayleigh fading is not considered because of its short communication distance. The receiver obtains the transmitted signal $y(t)$, mixes it down to IF frequency, then lowpass filtered and down converted to the baseband frequency. The baseband signals from the I and Q paths are:

$$\begin{aligned} I_{base}(t) =& \sqrt{\frac{E_b}{2T_b}} \cos(2\pi \Delta f t + \phi(t - T_d) - \theta) \\ Q_{base}(t) =& \sqrt{\frac{E_b}{2T_b}} \sin(2\pi \Delta f t + \phi(t - T_d) - \theta) \end{aligned} \tag{5.18}$$

Where Δf is the frequency offset due to the carrier frequency and IF frequency mismatch, θ is the phase offset produced by the receiver VCO and T_d is the propagation time delay between the transmitter and the receiver.

For FSK based modulations, the differential discrimination structure is very attractive because carrier phase offset recovery is not necessary. $I_{base}(t)$ and $Q_{base}(t)$ are sent to the baseband frequency discriminator to obtain raw shaped data, the discriminator output $\epsilon(t)$ is:

$$\begin{aligned}\epsilon(t) =& I_{base}(t)\frac{\partial Q_{base}(t)}{\partial t} - Q_{base}(t)\frac{\partial I_{base}(t)}{\partial t} \\ =& \frac{E_b}{2T_b}[2\pi\Delta f + \dot{\phi}(t - T_d)] \\ =& \frac{E_b}{2T_b}[2\pi\Delta f + \frac{2\pi}{T_b}\sum_{k=-\infty}^{+\infty} a_k h(t - kT_b - T_d)]\end{aligned} \tag{5.19}$$

However, the problem of synchronizing the symbol clock and compensating the frequency offset remains. One can observe that the discriminator output consists of a constant DC term $2\pi\Delta f$ and a periodic component.

5.2.3 Group Delay

Type I Chebyshev filters are most commonly used for image rejection because they are equiripple in the passband and monotonic in the stopband. A CMOS G_m-C based 3rd-order type I chebyshev bandpass filter is implemented for this application. The center frequency is 1 MHz, bandwidth is 1 MHz, and the passband ripples are smaller than 1 dB. Switchable capacitors array can guarantee that the center frequency is stable despite the process mismatch.

Group delay is defined as the derivative of the phase with respect to angular frequency, and it is a measurement of the distortion in the signal introduced by phase differences for different frequencies. Fig. 5.6 shows the magnitude and the group delay response of the proposed Chebyshev bandpass filter. It can be seen that in the desired band, from 0.5 MHz to 1.5 MHz, the magnitude ripples are less than 1 dB, meanwhile the group delay deviation is larger than 25 samples.

The image frequency attenuation is another specification for the Chebyshev filter. The trade off between stopband attenuation and group delay difference in the passband is shown in Fig. 5.7. If the group delay response is flatter, the filter bandwidth needs to be extended, so less images will be suppressed; if the high image band attenuation is required, the poles from the filter need to move closer to each other, leading to a larger group delay difference. Therefore, implementing an all-pass IIR based filter to compensate the inconstant group delay is necessary, achieving both a high image suppression and a flat group delay performance.

5.3 Circuits Implementation

The proposed demodulator architecture is described in Fig. 5.8. A 3rd-order single-bit $\Sigma\Delta$ADC quantizes the IF signal and generates a 1-bit digital sequence at I path I_{adc} and Q path Q_{adc}. One pole of the $\Sigma\Delta$ADC is located at the negative band to achieve a high SNR also at the image IF frequency. The down converter circuit shifts both

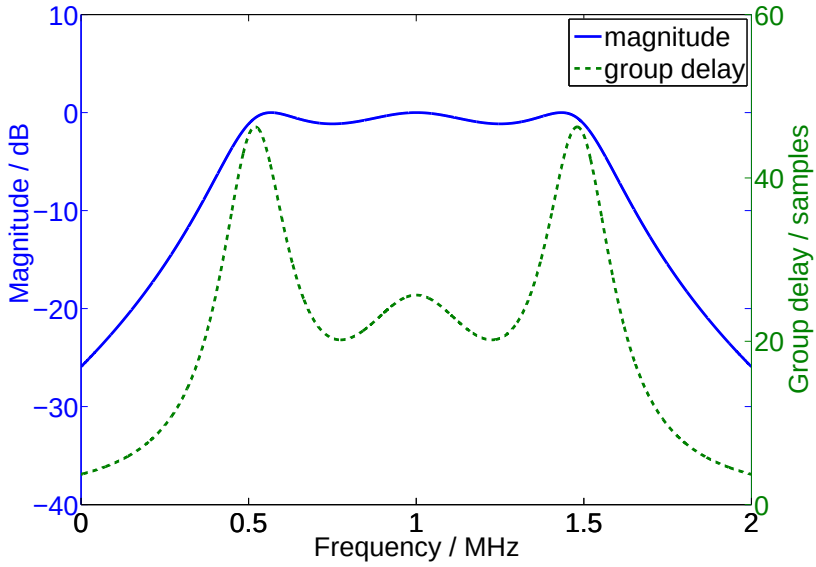


Figure 5.6: Magnitude and group delay response of the complex bandpass chebyshev filter.

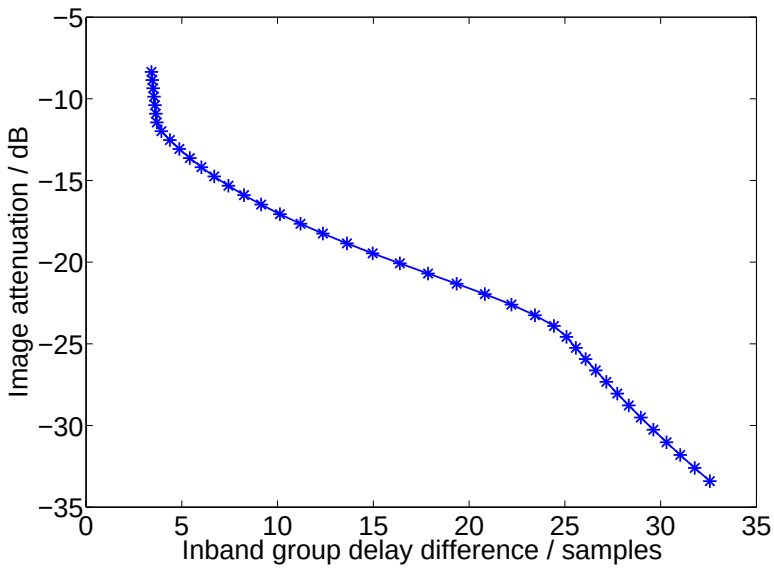


Figure 5.7: Group delay VS. image rejection.

the digitalized IF signal $I_{adc} + jQ_{adc}$ and its image $I_{adc} - jQ_{adc}$ to the baseband as the desired signal D_{base} and the reference signal R_{base} respectively. A look-up-table (LUT) generates the $\cos \omega_{IF} t$ and $\sin \omega_{IF} t$ signals. In the following stage, the desired and reference signals are decimated by 4 (D_{cic} and R_{cic}), low pass filtered (D_{fir} and R_{fir}), and flow into the LMS adaptive filter. In the decimation design, Cascaded Integrator–Comb (CIC) structure is applied without multipliers. It consists of an integration section and a comb section, which are separated by a decimator. The 8th-order FIR LPF filter has 20 dB attenuation at cut off frequency with 8 MHz sampling frequency. After separating the interference components from the wanted signal, the recursive filter is inserted to compensate the group delay deviation in order to obtain the wanted signals (I_{sig} and Q_{sig}). Finally the demodulated signals are differentially discriminated and compared with the adaptive threshold, which is determined by the preamble bits in each burst.

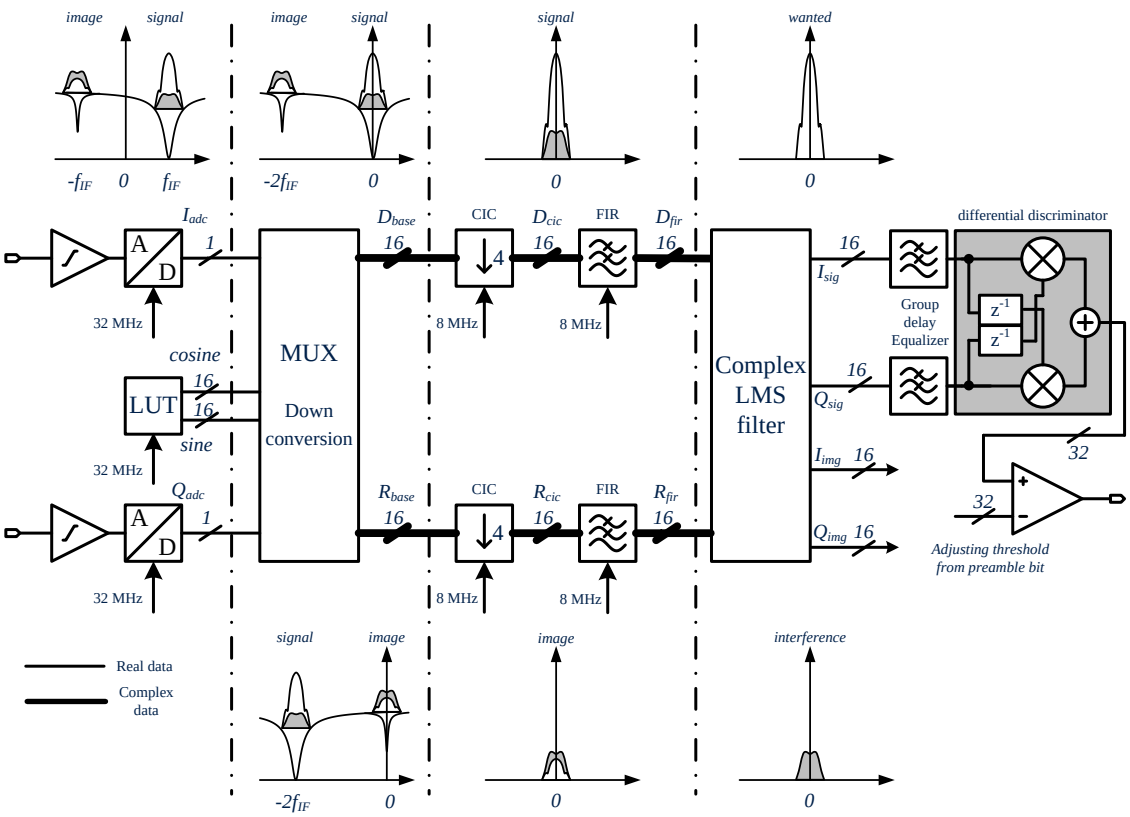


Figure 5.8: Digital demodulator architecture.

The main target of the proposed demodulation is to realize a low-cost low-power but high-efficiency hardware. Firstly, bringing the IF signal to the baseband at the first

stage removes the implementation of complex bandpass filter designs. The complex bandpass filter is very expensive and difficult to be implemented. It works at high speed and consists of four lowpass filters. Secondly, CIC based decimation filters are implemented following the down converter so that all the complicated computations are operated with the decimated sampling frequency. Besides, the CIC filter has very simple structure only with logic circuits and effectively reduces the sampling frequency without distorting the baseband signal. The key building blocks are illustrated in the later sections.

5.3.1 Multiplexer Based Down Converter

In digital circuit design, the power consumption is highly dependent on the operation frequency and computation complexity. In order to achieve the low power performance, the more complicated algorithms are highly desired to be placed after decimation and clocked by the lower sampling frequency. The down conversion circuits are located at the very beginning stage of the whole signal process chain. If down conversion computation complexity can be reduced without scarifying the performance, it can tremendously save the whole system power consumption.

In a conventional down converter circuit, the digitized ΣΔ modulator outputs are multiplied with the LUT generated cosine and sine signals to obtain the baseband signals, shown as Fig. 5.9.

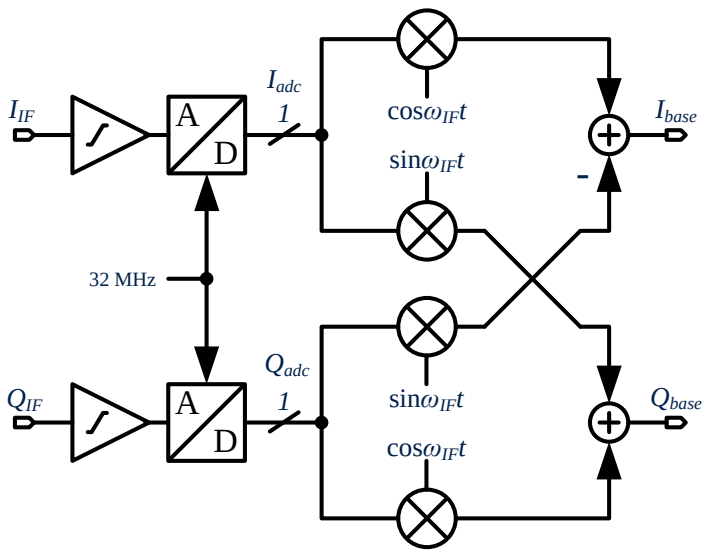


Figure 5.9: Conventional down conversion circuit.

Hence, the down converted baseband desired signal $D_{base}(t)$ and the reference signal $R_{base}(t)$ are expressed as:

$$
\begin{aligned}
D_{base}(t) &= (I_{adc}(t) + jQ_{adc}(t))e^{-j\omega_{IF}t} \\
&= I_{adc}(t)\cos(\omega_{IF}t) + Q_{adc}(t)\sin(\omega_{IF}t) \\
&+ j[-I_{adc}(t)\sin(\omega_{IF}t) + jQ_{adc}(t)\cos(\omega_{IF}t)] \\
R_{base}(t) &= (I_{adc}(t) - jQ_{adc}(t))e^{j\omega_{IF}t} \\
&= I_{adc}(t)\cos(\omega_{IF}t) - Q_{adc}(t)\sin(\omega_{IF}t) \\
&+ j[-I_{adc}(t)\sin(\omega_{IF}t) - jQ_{adc}(t)\cos(\omega_{IF}t)]
\end{aligned}
\tag{5.20}
$$

In this process, four multipliers are required. Multiplier is a common building block for digital process which consumes significant power and area, because two binary numbers of its inputs need to come down to calculating partial products, shift to left, and then add together, requiring a lot of shifters and accumulators to sum each partial product.

An easier approach for the down converter circuit without multipliers can be realized, since the quantized ΣΔADC output generates single-bit sequence: $I_{adc}(t), Q_{adc}(t) \in \{\pm 1\}$. One can notice that:

$$
\begin{aligned}
\pm(\cos(\omega_{IF}t) + \sin(\omega_{IF}t)) &= \pm\sqrt{2}\sin(\omega_{IF}t + \frac{\pi}{4}) \\
\pm(\cos(\omega_{IF}t) - \sin(\omega_{IF}t)) &= \pm\sqrt{2}\cos(\omega_{IF}t + \frac{\pi}{4})
\end{aligned}
\tag{5.21}
$$

In result, the complex signals from desired and reference paths can be rewritten in a very simple way. Only with *cos* and *sin* functions, ignoring the common phase delay of $\frac{\pi}{4}$, the four baseband output signals can be simplified shown as the truth table in Tab. 5.1.

Table 5.1: Truth table of down conversion process.

I_{adc}	1	−1	−1	1
Q_{adc}	1	1	−1	−1
$Re(R_{base})$	sin	− cos	− sin	cos
$Im(R_{base})$	cos	sin	− cos	− sin
$Re(D_{base})$	cos	− sin	− cos	sin
$Im(D_{base})$	− sin	− cos	sin	cos

The implementation of the proposed down conversion logics is shown in Fig. 5.10. Two Multiplexers and a few logic circuits can replace the multiplication functions. It results in much less power consumption and lower complexity compared to the

conventional implementation. Besides, the output bits length is the same as the length of the LUT generated sine and cosine signals. Overflow issues are not necessary to be considered, which are often encountered in the multiplications process. The constant common phase delay of $\frac{\pi}{4}$ is also harmless. This phase delay can be considered as the constant phase offset θ from (5.18). The differential discrimination method can eliminate this common phase delay.

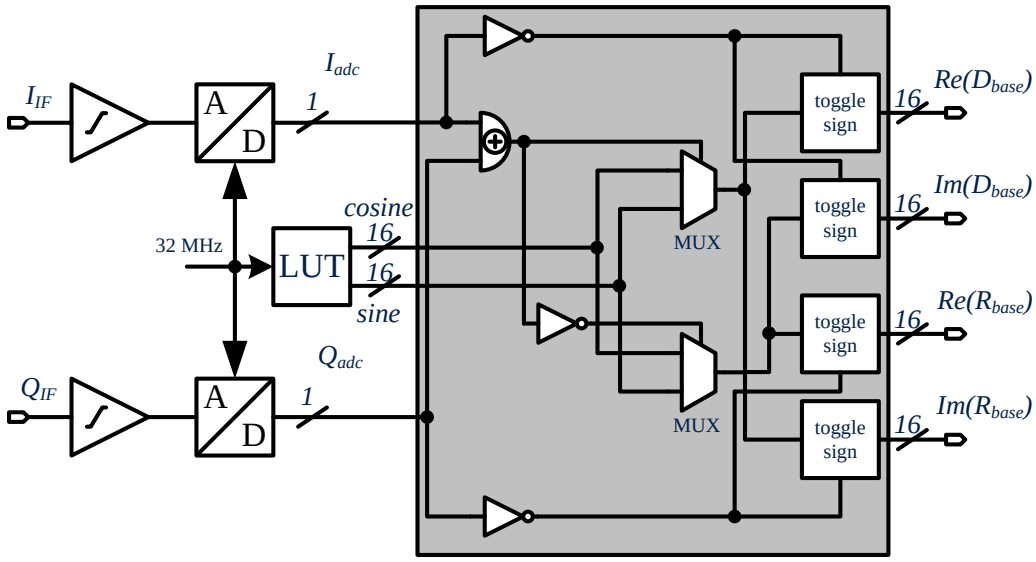


Figure 5.10: Multiplexer based down conversion circuit.

5.3.2 Decimation Filter

Cascaded Integrator Comb (CIC) filter is very efficient in multi rate processing for performing decimation and interpolation because it is multiplier free filter. The CIC decimator filter is composed of N cascaded stages, and each stage consists of an integrator, decimator and a comb, as shown in Fig. 5.11.

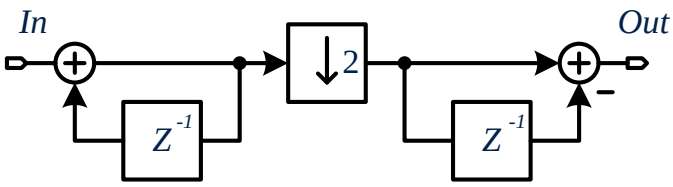


Figure 5.11: CIC decimation circuit stage.

A CIC decimator could have N cascaded integrator stages clocked at sampling rate of f_s, followed by a rate change by a factor of R. So that the circuits running at later stages are operated at f_s/R. The transfer function of the composite CIC filter is:

$$\begin{aligned} H(z) =& [\sum_{k=0}^{R-1} z^{-k}]^N \\ =& (\frac{1-z^{-R}}{1-z^{-1}})^N \end{aligned} \tag{5.22}$$

The CIC filter shows a linear phase response. It utilizes only delay and adder cells, so it requires no multiplication operations. Concerning the orders of CIC filter, the higher order CIC filter is implemented, the less power consumption for later stages. However, higher decimation rate will result in performance degradation. The choice of decimation rate shall be a trade off between lower sampling rate and system performance. The CIC filter can be used to reduce the sampling rate to as low as 4 times the Nyquist sampling rate with negligible SNR degradation. Further reduction in the sampling rate using the CIC will degrade the SNR performance at the band of interest significantly.

5.3.3 Channel Selecting Filter

Since the $\Sigma\Delta$ modulator has a noise shaping of high pass property. The low pass filter following CIC decimator is used to attenuate the high frequency quantization noise generated by $\Sigma\Delta$ modulator. The proposed 32-order filter is designed to have 40 dB attenuation at 1 MHz and the passband is set as 500 kHz. Because the sampling frequency is decimated to 8 MHz, the complexity of this filter is significantly reduced.

5.3.4 One-Tap LMS Algorithm

In general, adaptive interference cancellation methods use the idea of subtracting an interference estimate from the desired signal observation, which contains a wanted signal component and an interference component. The typical setup for interference cancellation uses the symmetric adaptive decorrelation (SAD) LMS filters [VV95]. As shown in Fig. 5.12, the reference input $r(n)$ contains parts of the desired signal and the desired input $d(n)$ also contains parts of the reference signal. The I/Q mismatch can be corrected using a symmetric signal separation by decorrelating $w_1(n)$ and $w_2(n)$, which is applied symmetrically to the signal and the image paths.

The signal estimated value $sig(n)$ and the interference estimated value $img(n)$ can be calculated as:

$$\begin{aligned} sig(n) &= d(n) - w_1^T(n) \otimes img^*(n) \\ img(n) &= r(n) - w_2^T(n) \otimes sig^*(n) \end{aligned} \tag{5.23}$$

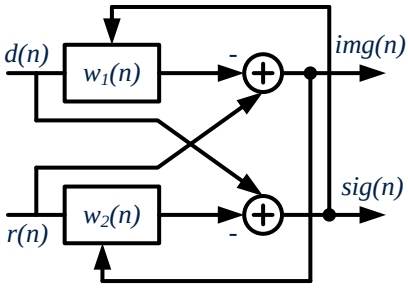


Figure 5.12: Symmetric adaptive decorrelation LMS filter process.

Where $w_i = (w_i[1], w_i[2], w_i[3], ..., w_i[L])^T$, $i = 1, 2$ is the coefficient of L-tap adaptive filter.

In the convergence process, the filters tend to adapt towards the output, while trying the minimize the error signal. The coefficient factors are updated as:

$$\begin{aligned} w_1(n+1) &= w_1(n) + 2\mu \cdot sig(n) \cdot img^*(n) \\ w_2(n+1) &= w_2(n) + 2\mu \cdot img(n) \cdot sig^*(n) \end{aligned} \tag{5.24}$$

Where μ denotes the learning step size, which controls the convergence speed and stability. μ is chosen as a power of 2 so that the multiplication by μ can be achieved using arithmetic shift operations. The adaptive filter coefficient factor $w(n)$ is adapted according to the error signal, which is also the output of the LMS. When $w_1(n)$ and $w_2(n)$ gets convergence, $sig(n)$ and $img(n)$ are decorrelated:

$$\Phi_{sig \cdot img} = \Phi_{img \cdot sig} = 0 \tag{5.25}$$

The multi-tap coefficient adaptive system gains more degrees of freedom. For example, it may be adjusted to the frequency dependent multi-tone signals. Since the proposed I/Q mismatch has no relevant to the frequency variations, the multi-tap approach is not necessary. In addition, for multi-tap filters, the phantom solutions are unstable [VV95], which runs against the purpose of the image rejection. The one-tap signal decorrelation does not require any specific signal conditions. Because the leakage is much smaller than the desired signal, LMS one-tap adjustment starts from the zero initial condition helping to resolve the phantom solution problem and the stability concern. In addition, it requires well defined signal and image evenly distributed over the channel bandwidth for the multi-tap coefficient adaptive filter. Hence, one-tap signal decorrelation technique is more suitable .

The ratio of image leakage compared to the signal is weighted by $w_2(n)$. Similarly, the signal leaking into the image is weighted by $w_1(n)$. These two complex taps can be

exactly conjugated if the two leakage paths have identical gain. One can calculate from Equation (5.12), the signal to interference ratio (SIR) in signal band and interference to signal ratio (ISR) in image are:

$$SIR_{sig} = ISR_{img} = \frac{STF\beta 1}{ISTF\beta 2} \tag{5.26}$$

The leakage gain from signal band to the image band is the same as the leakage gain from the image band to the signal band. These two complex taps are conjugated, so only one complex $w(n)$ is necessary. Totally, 12 multipliers and 12 adders are required, while the classical SAD LMS filter needs 16 multipliers and 16 adders.

5.3.5 Differential Discriminator with Adaptive Threshold

By sending the L period training sequence from (5.19), the discriminator output $\epsilon'(t)$ is expressed as:

$$\epsilon'(t) = \frac{E_b}{2T_b}[2\pi\Delta f + \frac{2\pi}{T_b}\sum_{k=0}^{L-1} a_k h(t - kT_b - T_d)] \tag{5.27}$$

The discriminator output is sampled by the period of T_s, the sampled output $\epsilon'(n)$ is:

$$\epsilon'(n) = \frac{E_b}{2T_b}[2\pi\Delta f + \frac{2\pi}{T_b}\sum_{k=0}^{L-1} a_k h(n - \frac{kT_b}{T_s} - T_d)] \tag{5.28}$$

If the L period training sequence a_k [1,-1,1,-1,1,-1...] is sent, whose average value is zero, the second term of $\epsilon'(n)$ remains zero. The frequency offset Δf can be estimated by:

$$\hat{\Delta f} = \frac{T_b}{\pi E_b}\epsilon'(n) \tag{5.29}$$

The BER under frequency offset errors is due to its influence to the DC offset introduced into the demodulated signal. The DC offset should be detected and used to correct the LO frequency or to add a constant correction term into the recovered message signal, as the feedback or feedfoward compensation path shown in Fig. 5.13.

The advantage of the feedforward approach is its simplicity and stability. Offset calculation only requires that a running sum is taken from the samples of the preamble symbols in order to calculate their mean value, which is then added to the default threshold value (zero) in the comparator circuits. This approach does not require additional analog circuits, has no stability issues, which may occur in feedback system. In addition, the IF offset compensation settling time can be precisely controlled by the length of preamble sequence. The differential discriminator circuit consists of two multipliers and one adder, generating 32-bit output from two 16-bit input signals. This configuration can calibrate the frequency offset with the resolution of 16 Hz.

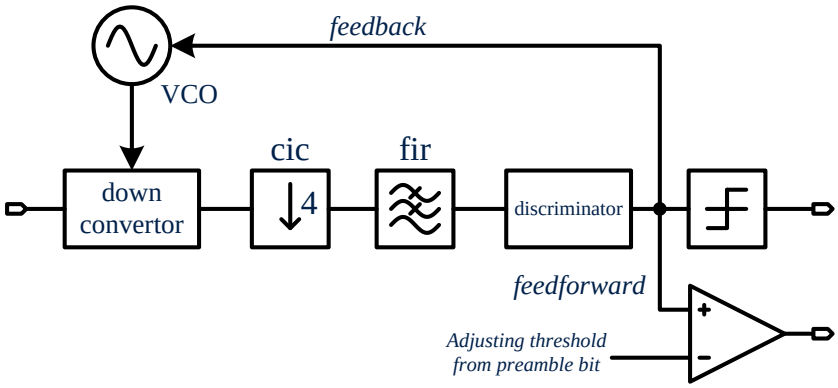


Figure 5.13: IF offset compensation block diagram.

5.3.6 Group Delay Equalizer

The position of the group delay equalizer needs to be optimized. The phase response of the polyphase filter is symmetric to its center frequency. The down converter circuit shifts its group delay performance linearly to the baseband. In the non-recursive circuits such as decimator and FIR filters, the phase response is constant. But for the differential discriminator, where the input signals from I and Q paths need to be multiplied with each other, the phase response is nonlinear. Hence, the appropriate position to insert the group delay equalizer is between the LPF and the discriminator. Since it is operated at baseband and sampled by decimated frequency, the complex IIR filter is also not required, both power and area are saved.

In Fig. 5.8, two group delay equalizer filters from I_{sig} and Q_{sig} are inserted between the FIR filters and the discriminator, whose sampling frequency is $\frac{f_s}{4}$. As discussed before, the group delay response before the equalizer remains the same as the group delay response generated by the polyphase filter, but shifting from IF frequency to DC. Between the polyphase filter and the equalizer, the phase response of the down converter is linear, and the phase responses of the CIC based decimator, FIR filter and LMS filter are constant, since they do not provide any feedback paths to implement recursive circuits.

Therefore, only the transfer function of the polyphase filter needs to be considered. From the analog filter specifications, its corresponding baseband digitized Chebyshev type I filter transfer function $H_{base}(z)$ is modeled as:

$$H_{base}(z) = \frac{0.0031z^3 + 0.0093z^2 + 0.0093z + 0.0031}{z^3 - 2.51z^2 + 2.2138z - 0.6791} \tag{5.30}$$

Its poles are located at $P_1 = 0.9526, P_{2,3} = 0.9717 \pm j0.0924$, and three zeros are all located at $Z_{1,2,3} = -1$.

A 4th-order recursive IIR all pass filter $H_{eq}(z)$ is applied to equalize the group delay response in the passband. Its pole positions are optimized to insert between the poles of $H_{base}(z)$, linearizing the phase response inband; Its zeros are located around the poles out of the unity cycle to make its magnitude response constant. The zero and pole plane of the down converted polyphase filter and equalizer is shown in Fig. 5.14. Its pole and zero positions are located in:

$$\begin{aligned} P_{1,2} &= 0.9604 \pm j0.1389 \\ P_{3,4} &= 0.9609 \pm j0.0408 \\ Z_{1,2} &= 1.0199 \pm j0.1474 \\ Z_{3,4} &= 1.0389 \pm j0.0441 \end{aligned} \tag{5.31}$$

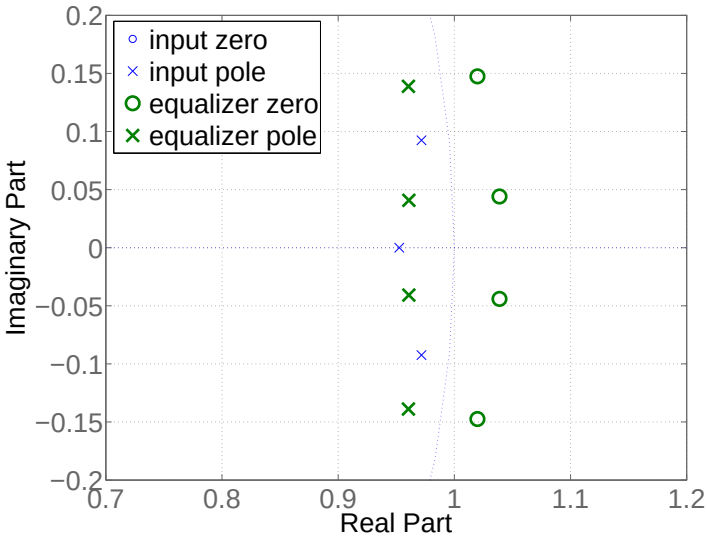


Figure 5.14: Zero pole plane of the group delay equalizer.

The allpass equalizer transfer function $H_{eq}(z)$ is:

$$H_{eq}(z) = \frac{0.5796z^4 - 2.4273z^3 + 4.0404z^2 - 3.1793z + 1}{z^4 - 3.1793z^3 + 4.0404z^2 - 2.4273z + 0.5796} \tag{5.32}$$

The group delay equalizer compensation performance is shown in Fig. 5.15. Since z-transformation represents the coefficients between numerator and denumerator, it keeps constant during decimation or interpolation process with the updated sampling frequency. The samples used as the group delay unit are still counted from the non-decimated sampling clock. It can be seen that in the desired band, the group delay deviation is less than 5 samples. Hence, the rippled group delay curves from the equalizer are utilized to suppress the ripples in the delay curves of Chebyshev filters.

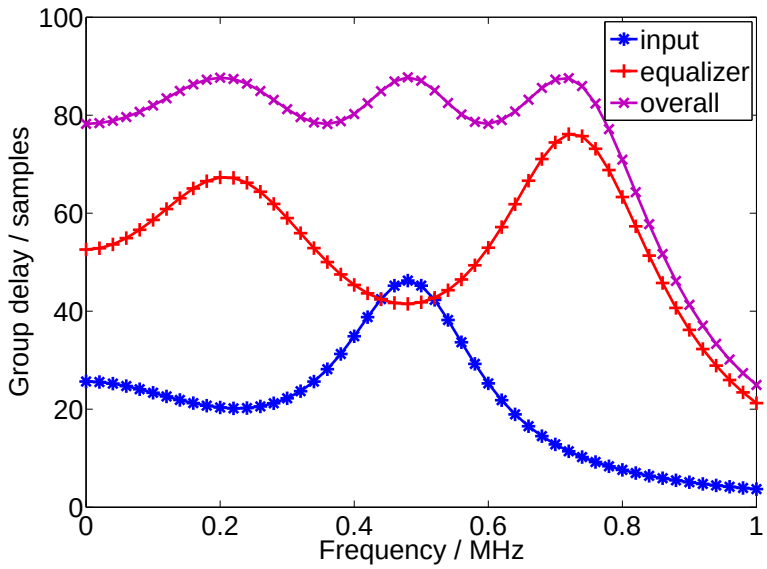


Figure 5.15: Group delay equalizer performance.

5.4 Performance Analysis

5.4.1 Simulation Setup

The performance of the proposed architecture is analyzed with GFSK modulated signals of 1 Mbit/s bit rate. The wanted signal is located at 2.402 GHz and the interference signal generated from an adjacent channel is located at 2.404 GHz. LO signal is generated at 2.403 GHz by quadrature mixer. Additional White Gaussian Noise (AWGN) is considered in the channel modeling, while the fading channel effect is neglected. Since in the Bluetooth application, communication distance is short, Rayleigh fading modeling from multiple paths is not necessary.

All the discussed imperfection issues from the analog parts are considered and modeled in the simulation. In the receiver chain, all analog devices are modeled with reasonable parameters, while the digital demodulator is fully synthesized. So the quantization errors from digital signals are also considered. But there are still several ideal assumptions for the modeling: LNA has a wide bandwidth, so its voltage gain and noise figure inband is assumed as constant over the desired band; All the mismatch parameters are independent from the frequency variation; In the $\Sigma\Delta$ modulator, only the coefficient mismatches are considered. The detailed specifications of the analog components are listed in Tab.5.2.

The proposed digital demodulator was synthesized in 130 µm process with the standard digital cells. It consists of 20700 instances in the die size of 620 µm x 600 µm.

Table 5.2: Specifications of the analog components for simulation setup.

LNA	
Bandwidth	2.1 GHz − 2.7 GHz
Voltage Gain	20 dB
Noise Figure	3 dB
Mixer	
Conversion gain	−2 dB
Amplitude mismatch	2%
Phase mismatch	1°
Polyphase filter	
Center frequency	1 MHz
Bandwidth	1 MHz
Inband ripples	< 1 dB
Out of band attenuation	25 dB
Gain mismatch	5 dB
Bandpass ΣΔADC	
Oversampling ratio	32
Sampling frequency	32 MHz
f_{IF}	1 MHz
SNR@f_{IF}	50 dB
SNR@$-f_{IF}$	20 dB
coefficient mismatch	20%

Power consumption is about 4 mW if the full function is activated. The pie chart of each subcircuit area contribution is shown in Fig. 5.16.

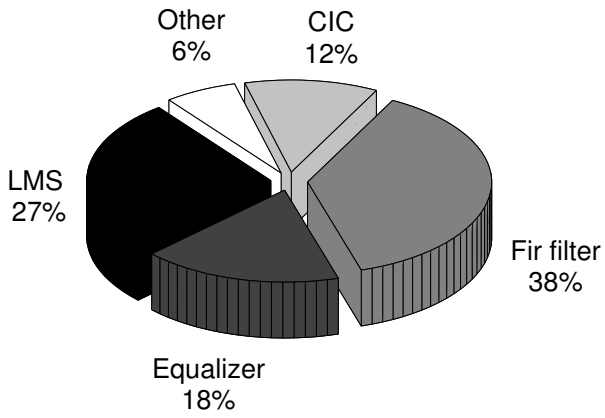
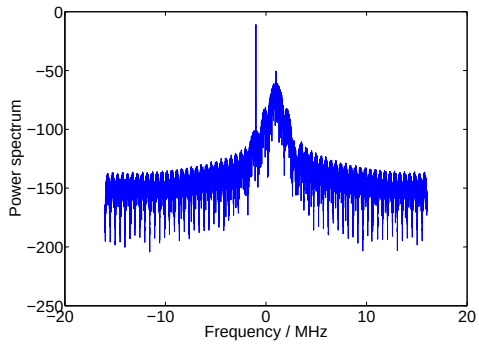


Figure 5.16: Pie chart of the digital demodulator.

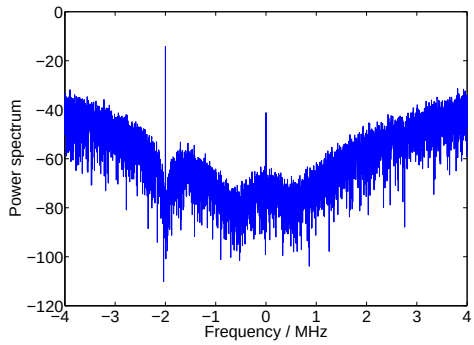
5.4.2 Interference Rejection Performance

Fig. 5.17 shows the spectrals at several demodulator stages. The wanted signal is modulated by a GFSK random source while the interference signal is a single tone signal, in order to verify the LMS function more clearly, as shown in Fig. 5.17(a). The baseband desired signal D_{base} shown in Fig. 5.17(b) has two components: the wanted signal at DC and the interference signal at $-2f_{IF}$. It can be seen that the image interference has already aliased into the baseband. The leakage has already taken place at this stage. The baseband reference signal R_{base} shown in Fig. 5.17(c) contains the signal at $-2f_{IF}$ and the single frequency image at DC, which is symmetric to the desired signal. After decimation and filtering, they are applied for the adaptive mismatch cancellation system, as shown in Fig. 5.17(d) and Fig. 5.17(e). It can be seen that the signals and images are totally separated from each other, since there is no more spur at the desired signal band. The image rejection ratio is increased by 40 dB compared to the original case. The convergence curves of the adaptive filter coefficients are shown at Fig. 5.17(f). Both real part and image part of the coefficient tap can get converged after 10000 samples.

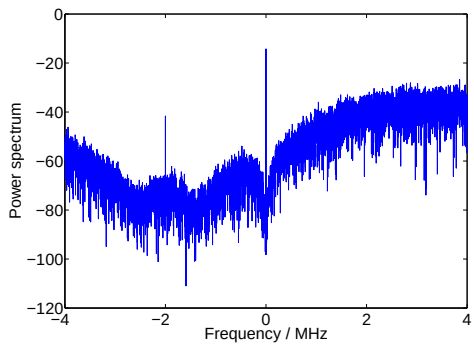
The BER performance comparison over the image signal power ratio is shown in Fig. 5.18. The bottom curve shows the ideal case that all the mismatches from I and Q paths are ignored. No leakage between signals and images occurs in this case. The BER still increases over the image signal power ratio just because the image power is too high, even its side lobes can disturbe the signals. One can observe that the



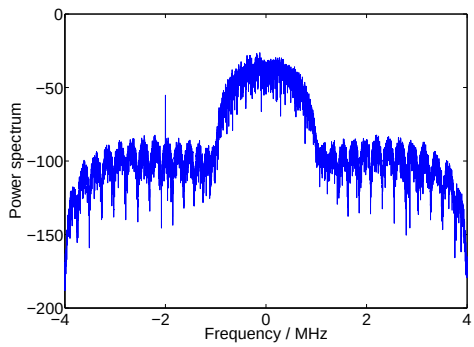
(a) Input signal from $\Sigma\Delta$ modulator.



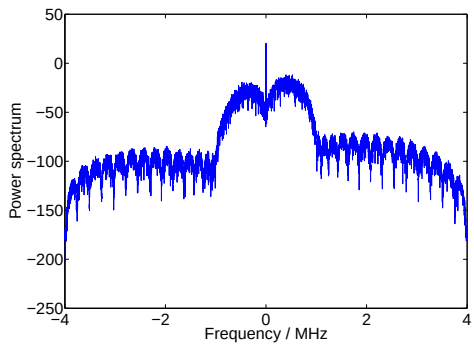
(b) Desired baseband signal D_{base}.



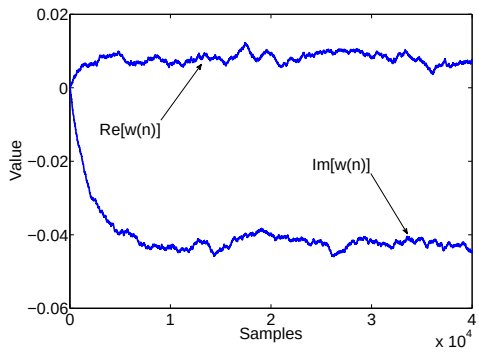
(c) Reference baseband signal R_{base}.



(d) LMS output signals $I_{sig} + jQ_{sig}$.



(e) LMS output images $I_{img} + jQ_{img}$.



(f) LMS coefficient update value $w(n)$.

Figure 5.17: Simulated spectrums of each stage.

BER performance of proposed receiver gets closed to the ideal situation, and it has a significant improvement compared to the receiver without LMS filter. 8 dB SNR is improved when obtaining the same BER performance of 10^{-3}, which is the standard for Bluetooth communication.

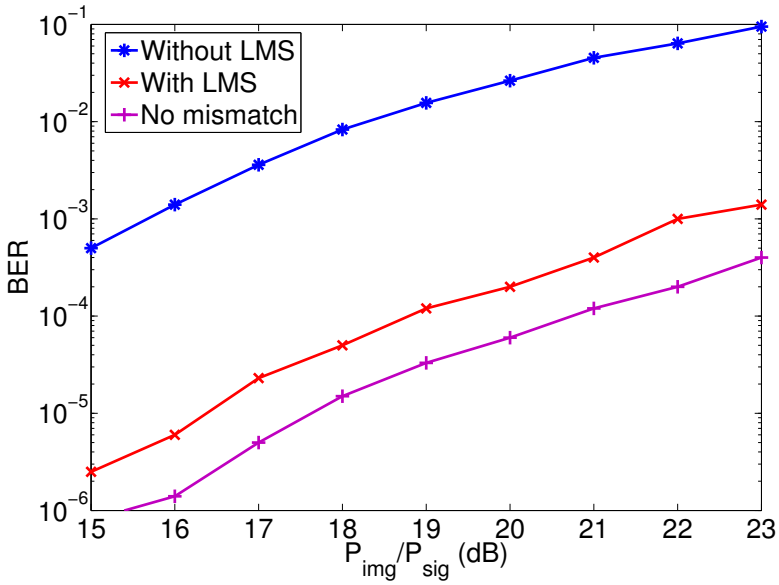


Figure 5.18: BER versus image-signal power ratio.

5.4.3 Timing Acquisition Performance

Timing acquisition with the frequency offset estimation algorithm performance in a single burst is shown in Fig. 5.19. With 32 preamble bits, the error of frequency offset estimation can achieve as small as 0.2%. Hnece, the frequency offset estimation error is about 2 kHz. It is acceptable since it is much less than the operation bandwidth of the discriminator. More sophisticated carrier frequency offset calibration mechanism with clock data recovery system is introduced in the next chapter.

5.4.4 Group Delay Equalizer Performance

The eye patterns comparison with and without the group delay equalizer is shown in Fig. 5.20. The SNR of the transmitted signal is set to 12 dB. The inconstant group delay influence in Fig. 5.20(a) is obvious. All the phase traces can not reach their peaks at the same time, since they have different propagation delays over the different baseband frequencies. This would easily lead to a sampling error and degrade the BER performance. With the equalizer filter, as shown in Fig. 5.20(b), the inconstant signal

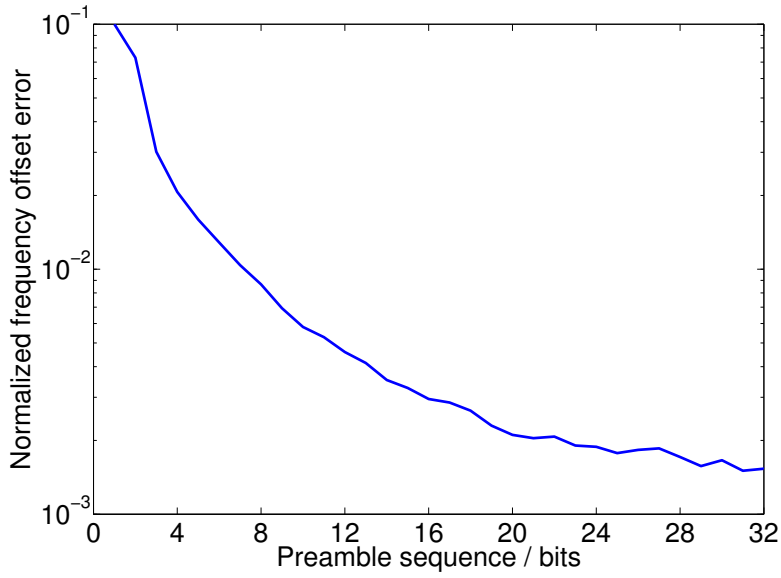


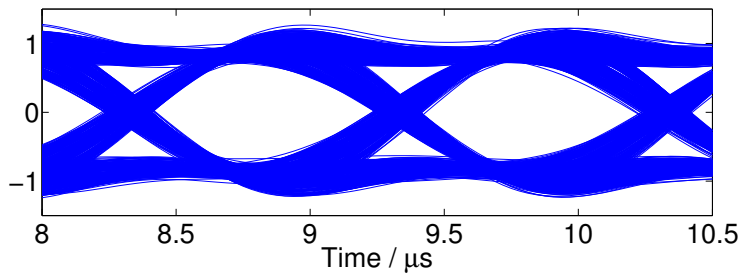
Figure 5.19: Frequency offset estimation with a single burst.

propogation delay is calibrated. The peaks of all the phase traces happen at the same time, so the eye pattern is more clearly and widely opened.

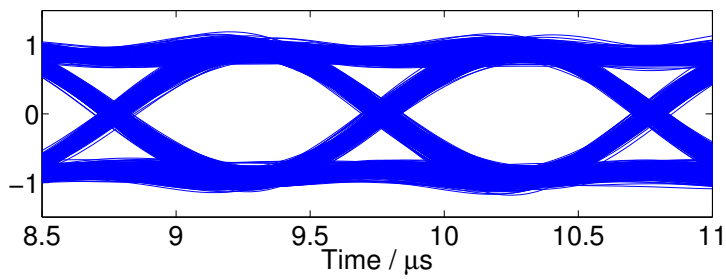
Fig. 5.21 shows the BER performance comparison over the signal to noise ratio of transmitted signals. It can be seen that the proposed demodulator with group delay equalizer yields about 2 dB better performance compared to the demodulator without equalizer, while achieving the Bluetooth standard, 10^{-3}. BER can be further improved if more order recursive filter is applied, or anti-alias filter is implemented to compensate the passband ripples instead of allpass. However, it requires much more effort and complexity while achieving the limited improvments.

5.5 Conclusion

A low-power low-effort digital GFSK demodulator architecture for low-IF receivers has been proposed. The demodulator can compensate the I/Q mismatch due to the impairment within the receiver frontend and thus improve the robustness against interference present at the image frequency. The single bit quantization results in an hardware and power efficient implementation. Additional reasons are: At first no complex bandpass filters are needed since all the signal processing is done at baseband. Secondly, the multiplexer based frequency downconversion circuity saves numerical operation and consumes therefore only the lowest possible power. Moreover it allows that the power hungry signal processing can be performed at the minimum required



(a) Eyes diagram before group delay equalizer



(b) Eyes diagram after group delay equalizer

Figure 5.20: Eyes diagrams performance comparison.

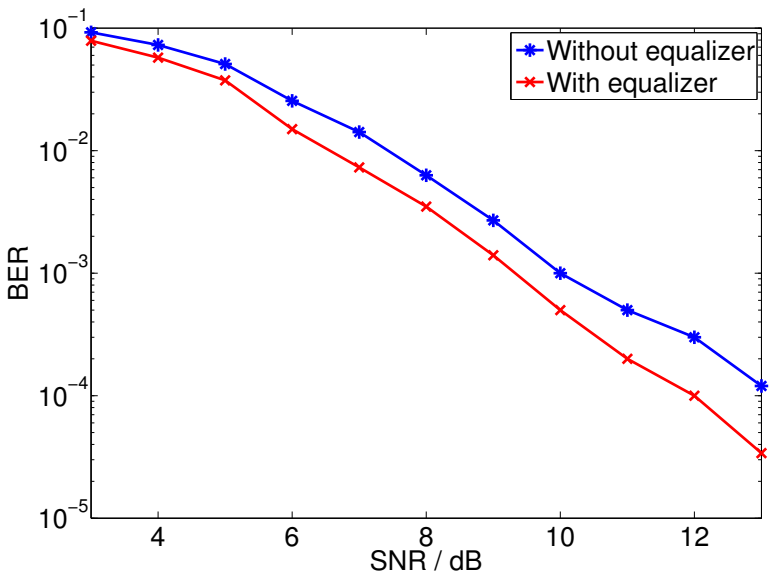


Figure 5.21: BER comparison over SNR.

rate after decimation. This applies as well to the LMS based adaptive filter, which generates only one gain coefficient in order to eliminate the image before demodulation. Simulation results show that the BER performance using the proposed I/Q imbalance scheme is satisfactory for short-range standard.

On the other hand, group delay equalization and frequency offset compensation algorithms are implemented as well. From the simulation results one can see that the demodulator with an IIR based equalizer improves the BER performance significantly compared to the original case. The scheme for carrier frequency offset compensation is effective and accurate, and it achieves the reduction of the circuit complexity.

Hence, it can be demonstrated that the proposed architecture not only greatly enhances the demodulation performance with respect to multiple problems causes by impairments, but also provides an easy and feasible solution for the fully integrated implementation.

Chapter 6

Clock Data Recovery and Carrier Frequency Offset Calibration System

6.1 Background

Short range wireless systems are commonly used recently, ranging from PC peripherals over health and life style to sensor networks. Continuous Phase Modulation (CPM) with constant envelope is widely employed in these relevant standards such as wireless LANs, Bluetooth, SUN, ZigBee and Wireless body area network (802.15.6). The variety of their applications generates the demand of co-integration of a low-power, low-cost and sufficient receiver in moderately scaled CMOS technology, which supports multiple standards for the applications e.g. in the field of smart lighting, smart home and medical care. The complexity and chip area of receivers grow rapidly as the number of covered standards increases. As shown in Fig. 6.1, multiple standards with different frequency bands, data rates and modulation schemes are supported in the proposed low-IF receiver. It features multiple RF frontends and shared IF band signal processing circuits. Sliding IF technique can realize the signals from multi-frequency bands downconversion with a single LO generator in two steps [Cho+04; Zha+13]. The center frequency and bandwidth of image rejection filter and ADC are configurable to meet the different data rates and modulation schemes. The IF frequency selection is optimized according to the bandwidth of the modulated baseband signal.

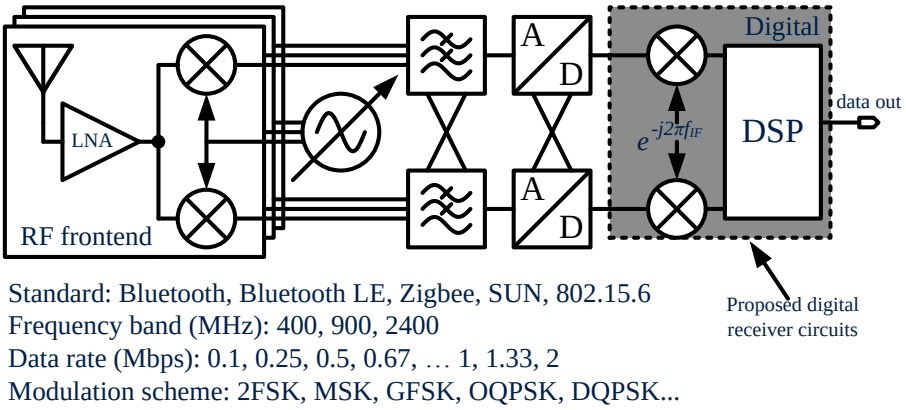
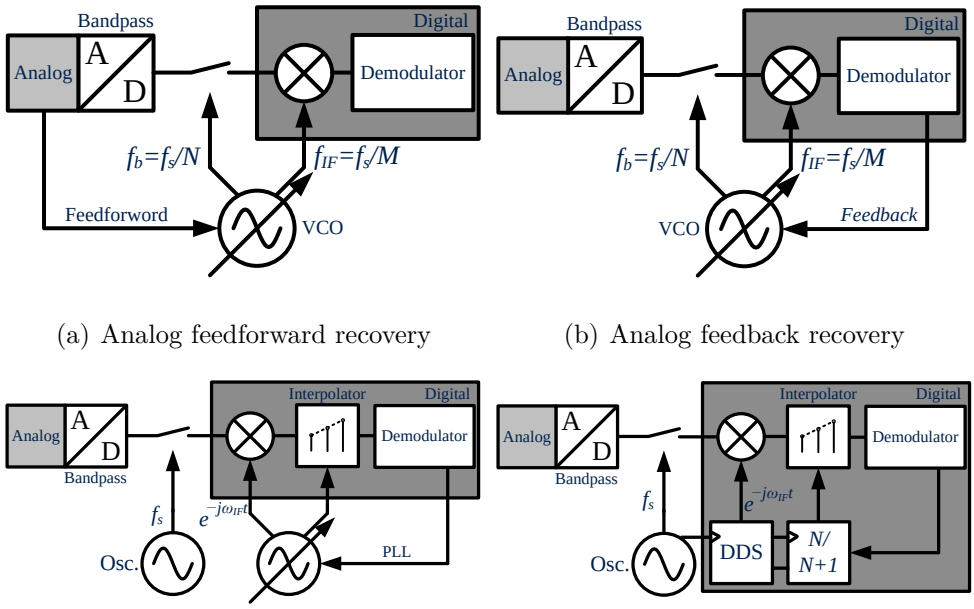


Figure 6.1: Block diagram of the proposed multi-standard low-IF receiver.

Image rejection problem of the relatively close-in image frequency is introduced in low-IF architectures. During the IF frequency mixing, image signals leak easily into wanted signals because of the I/Q path gain and phase mismatches [Y Z+13c]. By implementing an adaptive LMS based equalizer, the interference component from the desired signal observation can be estimated and subtracted [GKL07; YWH13a]. The IF signal needs to be further down converted to the baseband by a sampling clock. Due to the clock misalignment, the sampling frequency at the receiver side is not related to the transmitter carrier frequency. Thus, a Carrier Frequency Offset (CFO) will be contained in the baseband digital signal processing. On the other hand, the receiver must recreate the symbol rate timing information to ensure that the sampling time is optimal for symbol decisions. Symbol timing recovery is essentially resampling of the waveform at different phases and rates. Usually a training sequence is packed before a unique word to estimate the ratio between the original sampling rate and the desired sampling rate for frame synchronization purposes [HW11]. However, any approximation will eventually cause significant problems as the rounding error accumulates [HFH00]. In addition, given the distortions caused by the communication channel, it is not realistic to expect that the original sampling rate and carrier frequency stay constant [Liu+11]. Hence, the frequency offset and symbol timing recovery problem must be solved through a time varying or an adaptive system.

The analog low-IF receiver block diagram is shown in Fig. 6.2(a) and (b). The sampling clock is synchronized to the incoming signal symbol rate either in feedforward or feedback manner [Y Z+13c]. The sampling frequency is typically chosen to be an integer multiple of the symbol frequency, and it is also desired to be multiple of the incoming IF frequency. Therefore, an IF frequency is generated by a look-up table to obtain an oversampled baseband signal. A very clean crystal oscillator is needed for frequency tuning and synchronization. Besides, the irrational clock rate can not be

recovered.



(a) Analog feedforward recovery (b) Analog feedback recovery

(c) Digital recovery (d) Proposed revovery

Figure 6.2: Methodologies of clock and f_{IF} recovery in low-IF receiver.

In the digital processing of unsynchronized frequency multiplexed signals, the sampling clock for data and frequency conversion is independent of the symbol rate [Asc+89; EGH93]. As shown in Fig. 6.2(c), the data is firstly digitized to an IF signal with an unsynchronized clock and adjusted by interpolation. In order to resample a modulated digital waveform according to symbol timing information, the digital PLL generates a clock signal operating at symbol frequency based on the symbol timing error detection and estimation, either in Data-Aided (DA) [MM99] or Non-Data-Aided (NDA) [BLS04] scheme. Afterward the interpolator converts the signal to the symbol rate with a phase that aligns the sample for the optimum decision. Simultaneously the carrier frequency offset is corrected by a complex multiplier. However, the PLL based clock recovery brings issues: The VCO can only operate in a limited frequency band, so the data rate and IF frequency are restricted to a certain range. It is not possible to realize the wide range arbitrary symbol rate clock recovery with single VCO. Besides, the sampling clock frequency and VCO frequency are asynchronous, data conversion between the two irrelative clock domains needs additional buffers. Further more, the symbol rate clock is generated by the VCO, meanwhile the VCO is controlled according to the symbol timing error detector, operating at symbol rate clock. The circuits interaction and verification makes the mixed-signal design much more complicated than the pure digital circuits.

In this chapter, a novel low-IF multi-standard digital receiver with joint synchronized clock recovery and carrier frequency offset calibration is proposed. As shown in Fig. 6.2(d), instead of conventional PLL for clock and frequency offset recovery, the proposed receiver produces the multi-rate clock by modulating the sampling clock with a Fractional Frequency Divider (FFD) to recover different clock rates. The optimal sampling phase is obtained simultaneously by adjusting the fractional delay from a polynomial interpolator. Direct Digital Synthesizer (DDS) with $\Sigma\Delta$ noise shaping [Dai+06] are implemented to generate an arbitrary intermediate frequency. Without additional VCOs, all the generated clocks are synchronized to the existing sampling clock. Thus, the backend circuits of the proposed architecture can be fully synthesized in integrated circuits.

In the beginning of this chapter, the analyzes the general signal flow and the system model are analyzed. Subsequently the proposed circuits for clock synchronization and offset calibration is explained in details. Finally through the measurement results in FPGA, the performance of proposed circuit is verified.

6.2 Signal and System Analysis

The digital part block diagram of the proposed receiver for general signal modulation is shown in Fig. 6.3. The received IF signal $r_{IF}(t)$ is digitized by a fixed but random phase sampling clock, converted to the baseband and low passed. The baseband digital signal is generated by the sampling clock $r(kT_s)$. The interpolator provides the fractional time delay to align the independent phase. The Clock Data Recovery (CDR) control unit determines the sampling phase $kT_s + \mu_n T_s$ for interpolation and the symbol rate m_n for decimation from the estimated timing error $\hat{\varepsilon}$. The carrier phase error $\hat{\theta}$ is simultaneously estimated and calibrated through the phase rotator. When the error detection depends not only on the decimated signal but also on the data decision, the DA manner is utilized. Otherwise it is implemented in NDA scheme.

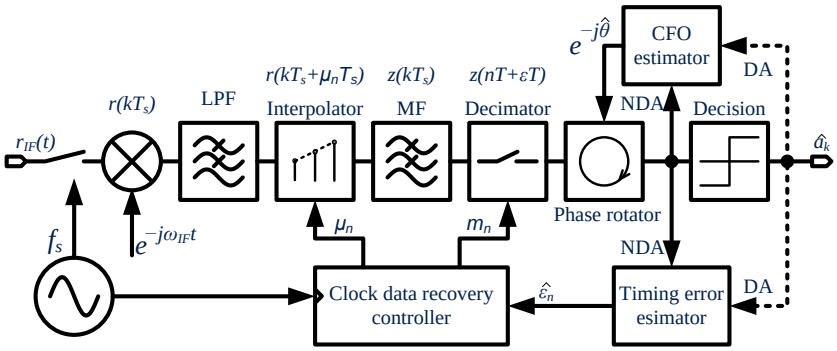


Figure 6.3: Digital part block diagram of the proposed receiver.

The received IF signal $r_{IF}(t)$ in complex envelope notation is expressed as:

$$r_{IF}(t) = \sqrt{2}\mathrm{Re}[u(t)e^{j(\omega_{IF}t+\theta_{IF})}]. \tag{6.1}$$

Where ω_{IF} and θ_{IF} denote carrier intermediate frequency and phase, $u(t)$ denotes the general modulated baseband signal:

$$u(t) = \sum_{n=0}^{\infty} a_n g(t - nT - \varepsilon T). \tag{6.2}$$

Where ε denotes the time delay, and $g(t)$ denotes the pulse shaping filter in the signal modulation. $r_{IF}(t)$ is downconverted to the baseband $r(t)$ and sampled by the free running clock with T_s period. Because the sampling frequency is much higher than the symbol rate, $r(kT_s)$ is a sufficient statistic for the continuous time observation of $r(t)$:

$$\begin{aligned} r(t) &= \sum_{n=0}^{\infty} a_n g(t - nT - \varepsilon T)e^{j\theta_t} + n(t), \\ r(kT_s) &= \sum_{n=0}^{\infty} a_n g(kT_s - nT - \varepsilon T)e^{j\theta_t} + n(kT_s). \end{aligned} \tag{6.3}$$

Where θ_t denotes the remaining long time varying phase offset, n denotes the independent Gaussian noise. From the previous samples, the value at fractional time delay $kT_s + \mu_n T_s$ is predicted from the previous integer values through a polynomial interpolation. A matched filter g_{MF} is implemented to achieve the maximum SNR ($g_{MF}(t) = g^*(-t)$). From the samples $r(kT_s)$, the value $z(nT + \varepsilon T)$ is obtained at the matched filter output. The decimator generates one value per symbol duration depending on the estimated timing shift:

$$\begin{aligned} z(nT + \varepsilon T) &= \sum_{k=-\infty}^{\infty} r(kT_s)g_{MF}(nT + \varepsilon T - kT_s) \\ &= \sum_{k=-\infty}^{\infty} r(kT_s)g^*(kT_s - nT - \varepsilon T) \\ &= \sum_{k=-\infty}^{\infty} a_n e^{j\theta_t} h(kT_s + \varepsilon T) + w(n). \end{aligned} \tag{6.4}$$

The ML criterion for the symbol decision $\hat{a_n}$ extracted from the matched filter output $z(nT + \varepsilon T)$ is expressed as:

$$\hat{a_n} = \frac{p(z(nT+\varepsilon T)|a_n=1)}{p(z(nT+\varepsilon T)|a_n=-1)} \underset{-1}{\overset{1}{\gtrless}} 1. \tag{6.5}$$

The derivative function from LMS algorithm defines an error-detector algorithm, which can iteratively solve the value of ε which satisfies the condition $\frac{\partial e}{\partial \varepsilon} = 0$. The timing error in NDA scheme is estimated from:

$$\begin{aligned} e_{NDA}(nT,\hat{\varepsilon}) =& \frac{1}{2}\frac{\partial |z(nT+\varepsilon T)|^2}{\partial \varepsilon} \\ =& z(nT+\varepsilon T)\frac{\partial z(nT+\varepsilon T)}{\partial \varepsilon} \\ \approx& z(nT+\varepsilon T)\{z[(n+\frac{1}{2})T+\varepsilon T] \\ & - z[(n-\frac{1}{2})T+\varepsilon T]\}. \end{aligned} \tag{6.6}$$

Eq. (6.6) represents the Garner Timing Error Detector (TED) algorithm. The idea is to search for the zero-crossing point. If the current timing estimation is too early from the correct timing, the offset is positive, indicating that the timing should be advanced. Similarly when the offset is negative, timing should be delayed. For a fixed offset, the timing error is independent of carrier phase rotation. However, Gadner's solution needs at least two samples per symbol. The sampled data needs to be further decimated to obtain the symbol rate. Gardner TED is a typical NDA algorithm which does not require any extra information except the current samples.

In the DA scheme, the decision $\hat{a_n}$ is also used for timing error detection, so the Garner algorithm is modified to:

$$e_{DA}(nT,\hat{\varepsilon}) = \hat{a_n}\{z[(n+\frac{1}{2})T+\varepsilon T] - z[(n-\frac{1}{2})T+\varepsilon T]\}. \tag{6.7}$$

By introducing half symbol time delay and previous decision, (6.7) can be improved to Mueller and Muller (M&M) algorithm:

$$e_{MM}(nT,\hat{\varepsilon}) = \hat{a_n} z[(n-1)T+\varepsilon T] - \hat{a_n}(n-1)z(nT+\varepsilon T). \tag{6.8}$$

The M&M Algorithm is a decision-directed, data-aided feedback method, which requires only one sample per symbol.

When the timing error ε and symbol value a_n are both correctly estimated, phase offset can be directly derived from:

$$\hat{\theta} = \arg[\sum_{k=-\infty}^{\infty} \hat{a_n} z(\hat{\varepsilon})]. \tag{6.9}$$

Eq. (6.9) gives a general solution for carrier phase offset estimation. However, the arg function requires a huge Read-Only Memory (ROM) to achieve an appropriate phase resolution. In the next section, a new phase offset estimation approach for CPM signals is realized in hardware, which saves large area in hardware by utilizing the decision output.

Based on the LMS algorithm, the timing and phase recovery is iteratively updated based on the previous value and the current detection:

$$\begin{aligned} \hat{\varepsilon_{n+1}} &= \hat{\varepsilon_n} + \mu_\varepsilon e(nT, \hat{\varepsilon}), \\ \hat{\theta_{n+1}} &= \hat{\theta_n} + \mu_\theta e(nT, \hat{\theta}). \end{aligned} \tag{6.10}$$

Where μ denotes the learning step size for LMS error update, which controls the convergence speed and stability.

6.3 Circuits Implementation

Fig. 6.4 shows the toplevel circuits of the proposed digital backend for CPM signal demodulation. The down-conversion, CIC based decimator, low pass filter, interpolator and DDS circuits are operated at the sampling clock, and they are depicted in light gray region; Other circuits including decimator, discriminator, Viterbi decision and feedback control logics are operated at symbol clock. In the frontend, the incoming multi-band RF signals are connected to LNAs, mixed down with quadrature LO signals from PLL through mixers, and filtered to generate the IF signals. A complex bandpass $\Sigma\Delta$ ADC at IF frequency pushes its quantization noise to the higher frequency offset and provides a single-bit digitized sequence at I and Q paths.

During the digital signal processing, the Digital Down Converter (DDC) shifts the digitalized IF signals to the quasi baseband. However, a small frequency offset ($f_{\Delta IF}$) still exists. A sine wave close to IF frequency is generated by the DDS circuits for the first down conversion. Then the down converted signals are decimated by a tunable bank of cascaded integrator comb filters (CIC), whose decimation ratio is determined by the input data rate. Hence, the output sampling rate becomes relatively low but still much higher (around eight times) than the symbol rate. Before steering into the 24th-order narrow band filter to obtain raw digital data, the second DDS circuits provide $\Sigma\Delta$ noise shaped $\cos\omega_{\Delta IF}t$ and $\sin\omega_{\Delta IF}t$ signals to compensate the remaining frequency error with small stepsize. Therefore, the oversampled raw digital signal is obtained exactly at DC frequency. After its fractional delay is adjusted by the

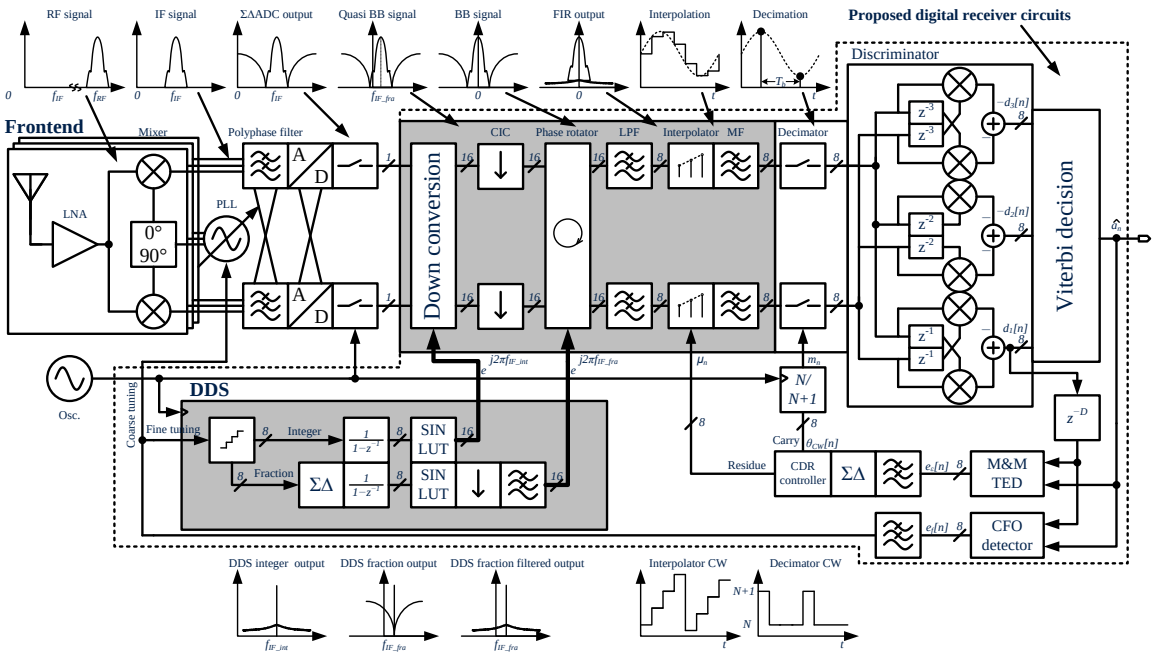


Figure 6.4: Toplevel circuits of the proposed digital receiver.

interpolator, a matched filter with the pulse shaping function is used to achieve the best SNR performance. Finally, the signals at I and Q path are respectively decimated to the symbol rate when the optimum phase is reached.

Multi-order discriminators are implemented to generate the convolution data for Viterbi decoding. When the Viterbi decision determines the output data $\hat{a_n}$, it connects to the feedback control loop for the error calibration. Through the M&M TED, the symbol timing error e_ε is estimated. Afterward it is truncated by a ΣΔ quantizer and flows into the CDR control unit to calculate the corresponding fractional delay and the decimation rate. Comparing the values from D-tap delayed discriminator output and the decision, the carrier frequency error e_f can be estimated. When the CFO error is too large, the coarse frequency tuning is enabled to adjust the LO frequency, guaranteeing that the IF signal can successfully pass through the polyphase filter and ΣΔ ADC. The fine frequency tuning is implemented in two DDS circuits. The first one with straightforward ROM generates the frequency close to f_{IF} so that high bandwidth CIC based decimation banks do not influence on the wanted signal SNR performance. The second DDS with ΣΔ modulator gains higher frequency resolution, so the decimated signals are shifted to the exact zero frequency. In this way the low pass filter can work efficiently to suppress the ΣΔ noise shaping.

The main target of the proposed demodulation is to realize a low-cost low-power, high-efficient hardware supporting a wide range of data rates and IF frequencies. There

are several considerations for the circuit complexity reduction: 1). Complex bandpass filter implementation is avoided both in signal processing chain and DDS circuits. Complex bandpass filters are expensive, as each consists of four equivalent lowpass filters and works at higher speed. 2). Three ΣΔ techniques are implemented for different applications. The second ΣΔ modulated DDS is matched with the ΣΔ ADC so that they can share the same decimator and low-pass filter. The ΣΔ quantizer in the clock recovery is implemented in a MASH structure due to its simplicity and stability. All the coefficients are chosen as a combination of power of two to replace multiplication by arithmetic shift and add operations. 3). According to the different data rates, the CIC based decimation ratio is adjusted so that the sampling clock and bandwidth in the following filter are changed according to the input data rate. Hence, with reasonable orders, the low pass filter can efficiently attenuate the out of band noise for different data rate signals. 4). All source intensive computations such as Viterbi and CDR controller are operated at symbol frequency. The key building blocks are illustrated in the following subsections.

6.3.1 ΣΔ ADC

A 3rd-order single-bit output bandpass ΣΔ ADC in the feedforward structure is implemented in the frontend. As shown in Fig. 6.5, with the feedforward and feedback coefficients k_1, k_2, k_3 and b_f, the pole positions of the noise transfer function (NTF) are optimized to achieve the required bandwidth. When the oversampling ratio (OSR) is chosen as 16, larger than 50dB SNR performance is achieved. The detailed circuits design is presented in [Ata+13]. The coefficients are adjustable by binary-weighted capacitors to extend the loop filter bandwidth and center frequency. The loop filter is designed to achieve excellent noise shaping at the target frequency band. NTF and STF are derived from the loop filter transfer function $H(s)$:

$$\begin{aligned} H(s) &= \frac{k_1 a_1 (s - j\omega_{IF})^2 + k_2 a_1 a_2 (s - j\omega_{IF}) + a_1 a_2 a_3}{(s - j\omega_{IF})[a_2 a_3 b_f + (s - j\omega_{IF})^2]}, \\ NTF(s) &= \frac{1}{1 + H(s)}, \\ STF(s) &= \frac{H(s)}{1 + H(s)}. \end{aligned} \tag{6.11}$$

These imperfections become the bottle neck for the adaptive wide range data rate and IF frequency receiver design in the whole system. The chain of integrators with capacitive summation offers a suitable solution for low power applications, and the feedforward capacitors are tuned to ensure stability of the modulator. And the tunable capacitors both from polyphase filter and ADC are simultaneously controlled by the master digital calibration circuits to achieve the same center frequency and bandwidth.

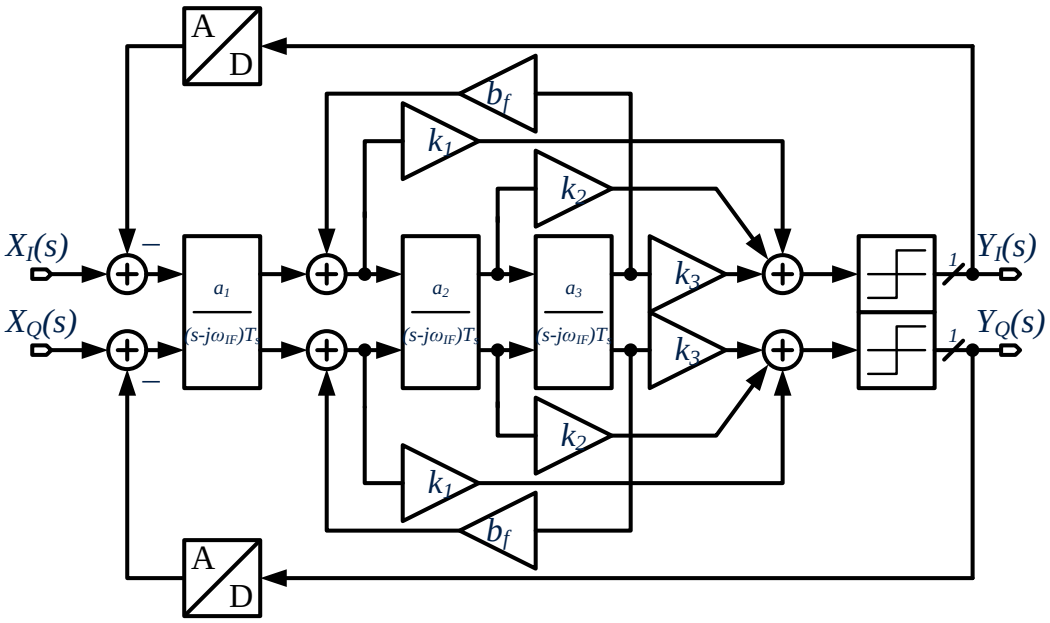


Figure 6.5: Block diagram of ΣΔ ADC.

6.3.2 Direct Digital Synthesizer

As shown in Fig. 6.6, a basic DDS circuit includes a phase accumulator and a look up table that converts the frequency control word to a sinusoidal amplitude information. The input frequency control word $f_{CW}[n]$ is continuously added to the last sampled phase value by N-bit accumulator to generate the phase control signal $\varphi[n]$. DDS output frequency is $f_{DDS} = f_{ref}\frac{f_{CW}}{2^N}$, where f_{ref} denotes the DDS reference clock frequency.

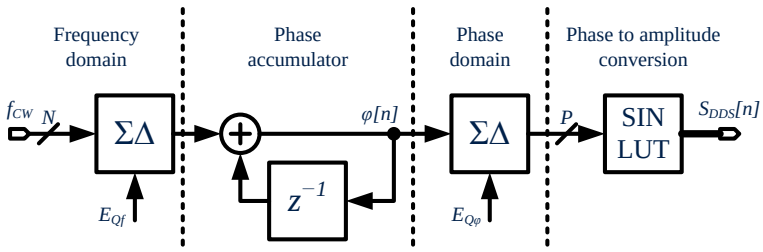


Figure 6.6: Block diagram of the direct digital synthesizer.

In the phase accumulator, the N-bit phase word at the phase accumulator output is updated as:

$$\varphi[n+1] = [\varphi[n] + f_{CW}] \bmod 2^N. \tag{6.12}$$

To reduce the LUT ROM size while keeping the fine step size, the phase word needs to be truncated prior to P-bit of the ROM input. A quantization error $E_Q(n)$ is generated, whose sequence is periodic and causes unwanted noises and spurs. Therefore, the output sequence of DDS is changed to:

$$S_{DDS_{sin}}[n] = \sin(2\pi \frac{\varphi[n] + E_Q}{2^N}) \tag{6.13}$$

Since $E_Q << 2^N$, $\cos(2\pi \frac{E_Q}{2^N}) \approx 1$,$\sin(2\pi \frac{E_Q}{2^N}) \approx 2\pi \frac{E_Q}{2^N}$, it can be simplified as:

$$\begin{aligned} S_{DDS_{sin}}[n] \approx & \sin(2\pi \frac{\varphi[n]}{2^N}) + \cos(2\pi \frac{\varphi[n]}{2^N})(2\pi \frac{E_Q}{2^N}) \\ = & \sin(2\pi \frac{f_{CW}}{2^N} n) + \cos(2\pi \frac{f_{CW}}{2^N} n)(2\pi \frac{E_Q}{2^N}). \end{aligned} \tag{6.14}$$

Similarly, the cosine wave at the DDS output is:

$$S_{DDS_{cos}}[n] = \cos(2\pi \frac{f_{CW}}{2^N} n) - \sin(2\pi \frac{f_{CW}}{2^N} n)(2\pi \frac{E_Q}{2^N}). \tag{6.15}$$

Hence, the complex DDS output is expressed as:

$$\begin{aligned} S_{DDS}[n] = & S_{DDS_{cos}}[n] + jS_{DDS_{sin}}[n] \\ = & \cos(2\pi \frac{f_{CW}}{2^N} n) + j\sin(2\pi \frac{f_{CW}}{2^N} n) \\ & + [j\cos(2\pi \frac{f_{CW}}{2^N} n) - \sin(2\pi \frac{f_{CW}}{2^N} n)] \frac{2\pi E_Q}{2^N} \\ = & e^{j2\pi \frac{f_{CW}}{2^N} n}(1 + e^{j\frac{\pi}{2}} \frac{2\pi E_Q}{2^N}) \end{aligned} \tag{6.16}$$

The first term in (6.16) shows the desired sinusoidal output, and the second term shows that the quantization noise is moved to the IF frequency with 90° phase shift.

Although $\Sigma\Delta$ modulators with different structures can move the truncated quantization noise in the band of interest to the higher frequency band, their noise shaping behaviors are not identical. MASH has much sharper noise shaping effect in band but more quantization noise out of band, which requires a high order filter to suppress. The feedforward modulator provides a flatter out of band noise compared to the MASH type. Besides, it has an advantage of flexibly placing poles inside the unit circle in the

z-domain by changing its feed-forward coefficients. Therefore, feedforward structure is more suitable for this design.

As shown in Fig. 6.7, the ΣΔ modulator in DDS can be implemented in frequency or phase domain. The frequency domain ΣΔ modulator gains advantage of increased dynamic range due to its constant input, and reduced accumulator size from frequency control word truncation. However, the truncated frequency error needs to be accumulated in the phase domain, which degrades the noise shaping performance by one order. The phase domain ΣΔ noise shaping can remove the total phase truncation error to the higher frequency offset with a full size accumulator. On the other hand, the implemented ΣΔ modulator must be stable over the whole dynamic input range, since the accumulator output gives a rail-to-rail phase signal. In the proposed applications, sufficient performance with low-effort design is desired. A 4th-order feedforward ΣΔ modulator with multi-bit quantizer is implemented in the frequency domain. It is modified from the ΣΔ ADC by adding one more integrator. Thus, the identical noise shaping with the same bandwidth can be observed at ADC and DDS outputs, as shown in Fig. 6.8.

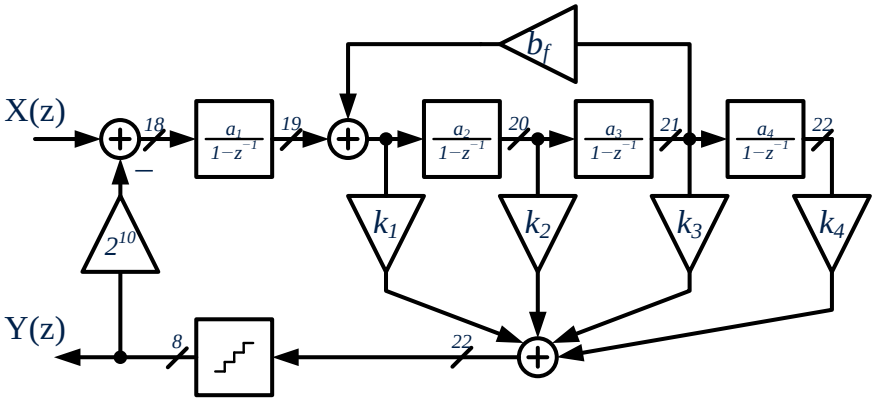


Figure 6.7: Block diagram of ΣΔ modulators in DDS.

Fig. 6.9 shows the comparison of the DDS output spectrum. Since the accumulator output experiences the period of the IF signal, the phase domain ΣΔ modulator generates spurs at its harmonic frequencies. Although the proposed modulator implemented in frequency domain has a dead band due to the limited input range of the quantizer, it gains a flatter noise shaping. Furthermore, its LUT output spectrum has lower in band noise. And it shows an identical bandwidth as the previous ΣΔ ADC.

If the DDS circuits are directly applied to the down convertor, a complex bandpass filter is needed to suppress the ΣΔ shaped quantization noise, which requires enormous high orders. As shown in Fig. 6.4, the proposed DDS circuits are divided into two parts. The integer part is directly accumulated and addressed for the first downconversion, so that the wanted signal can successfully pass through the decimation banks. For

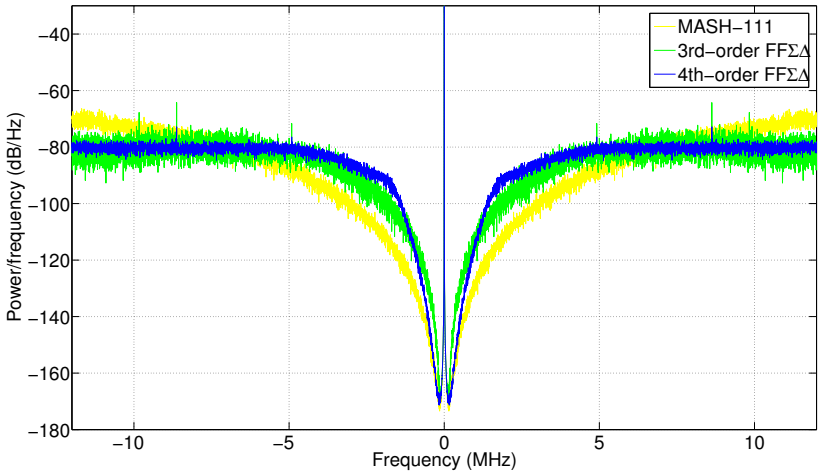


Figure 6.8: Comparison of baseband ΣΔ noise shaping.

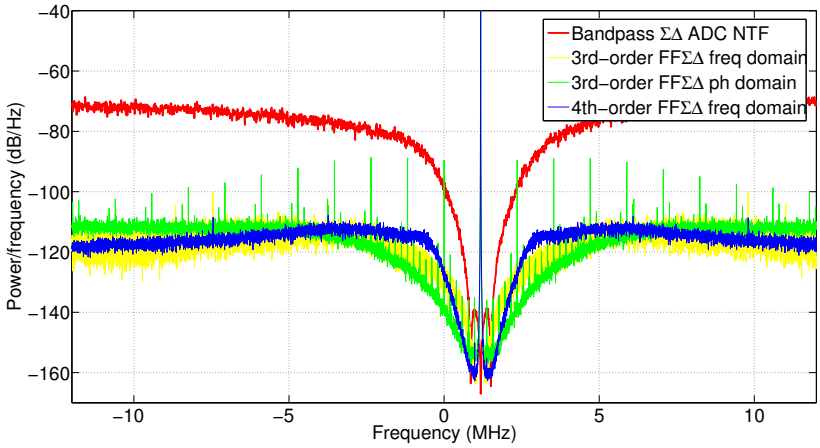


Figure 6.9: Comparison of DDS output spectrum S_{DDS} at IF frequency.

the smaller stepsize frequency tuning, the fractional part of the IF control word is quantized by the proposed modulator, and a ΣΔ noise shaped sine wave is generated at the remaining IF frequency offset. Subsequently it is decimated and low passed by the baseband filter before steering to the second downconversion circuits. The IF wanted signal flows through the two DDS circuits in series. The frequency tuning between the integer part and fractional part will cause a timing mismatch. So 2-bit overlap is reserved between the integer and fractional bits. As long as the wanted signal can pass through the decimator and be detected, the integer control word is fixed. The remaining CFO error is only calibrated through the fractional part.

6.3.3 Fractional Interpolator and Decimator

Fig. 6.10(a) shows the basic mechanism of a VCO, where the oscillated frequency varies linearly proportional to the control voltage. To replace the VCO function, the accumulated phase needs to be controlled continuously to realize the same mechanism as VCO with the help of fractional delay interpolator and the fractional frequency divider, as shown in Fig. 6.10(b). The VCO and FFD output in phase domain is expressed as:

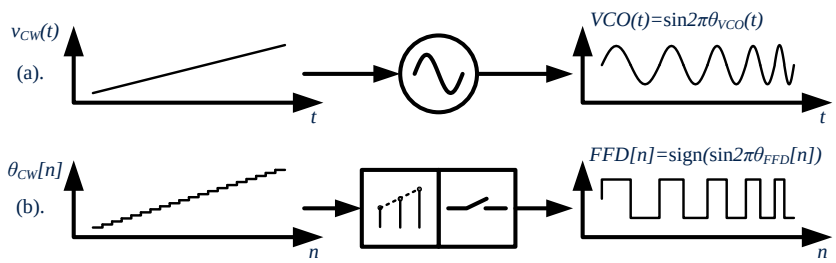


Figure 6.10: Comparison of VCO and fractional frequency divider.

The phase control word $\theta_{CW}[n]$ is updated as:

$$\begin{aligned}\theta_{CW}[n] =& \theta_{CW}[n-1] + k_{CW} e_\theta[n] \\ =& \sum_{k=0}^{n} k_{CW} e_\theta[n].\end{aligned} \tag{6.17}$$

Therefore, in the frequency domain the phase is continuously accumulated according to the control voltage:

$$\begin{aligned}\theta_{VCO}(t) &= \int_0^t f_{VCO}(\tau)d\tau \\ &= \int_0^t k_{VCO}v_{CW}(\tau)d\tau, \\ \theta_{FFD}[n] &= \sum_{k=0}^{n} k_{FFD}\theta_{CW}[k].\end{aligned} \tag{6.18}$$

Where k denotes the frequency gain. Fig. 6.11 illustrates one example of the resampling waveforms under steady-state conditions with the division ratio $\frac{T}{T_s}$ of 4.25. It can be seen that the recovered clock is loaded at every positive edge of sampling clock, while the recovered data is interpolated in time in a periodic manner according to the accumulated fractional delay at the output clock. When the accumulated fractional timing error is larger than the symbol time, the decimation ratio in $\Sigma\Delta$ modulated FFD is incremented by one.

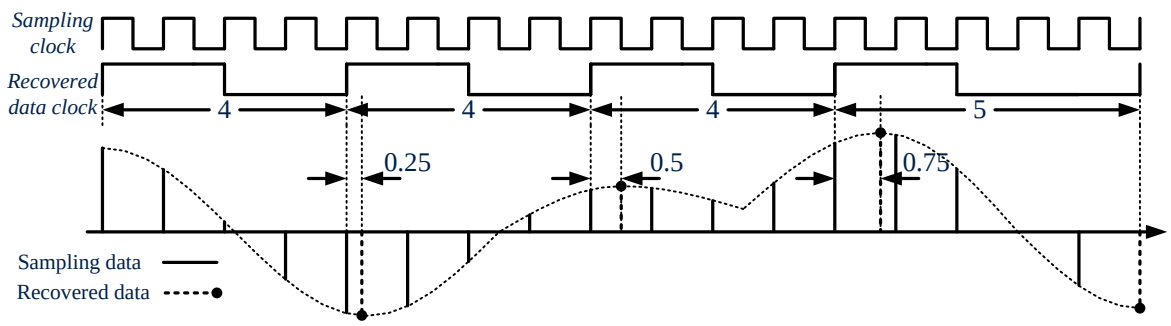


Figure 6.11: Fractional interpolation example: $\frac{T}{T_s} = 4.25$.

As shown in Fig. 6.4, the CDR controller generates the fractional interval μ_n and the output interpolation index m_n. The base point index m_n is determined by μ_n and the control word $\theta_{CW}[n]$ from the detected timing error information e_ε. In hardware, μ_n is produced by incrementing the content of the register and m_n can be generated by an accumulator:

$$\begin{aligned}\mu_n =& [\theta_{CW}[n] + \mu_{n-1}] \bmod 1, \\ m_n =& m_{n-1} + \mathrm{int}[\theta_{CW}[n] + \mu_{n-1}].\end{aligned} \tag{6.19}$$

The hardware structure of polynomial interpolation filters can be effectively implemented by the Farrow structure [Far88]. A 3rd-order cubic polynomial Lagrange interpolator is employed in Farrow structure for clock recovery in this case, as shown in Fig. 6.12. It is performed by a cascade of 3 multipliers. Each multiplier has the

fractional interval μ_k for each interpolation. As all the coefficients are fixed, they are scaled up 6 times. In this way, coefficients $c_l(i)$ become 0, ±1, ±2, ±3 and ±6. Only shifters and adders are used to realize the multiplication functions.

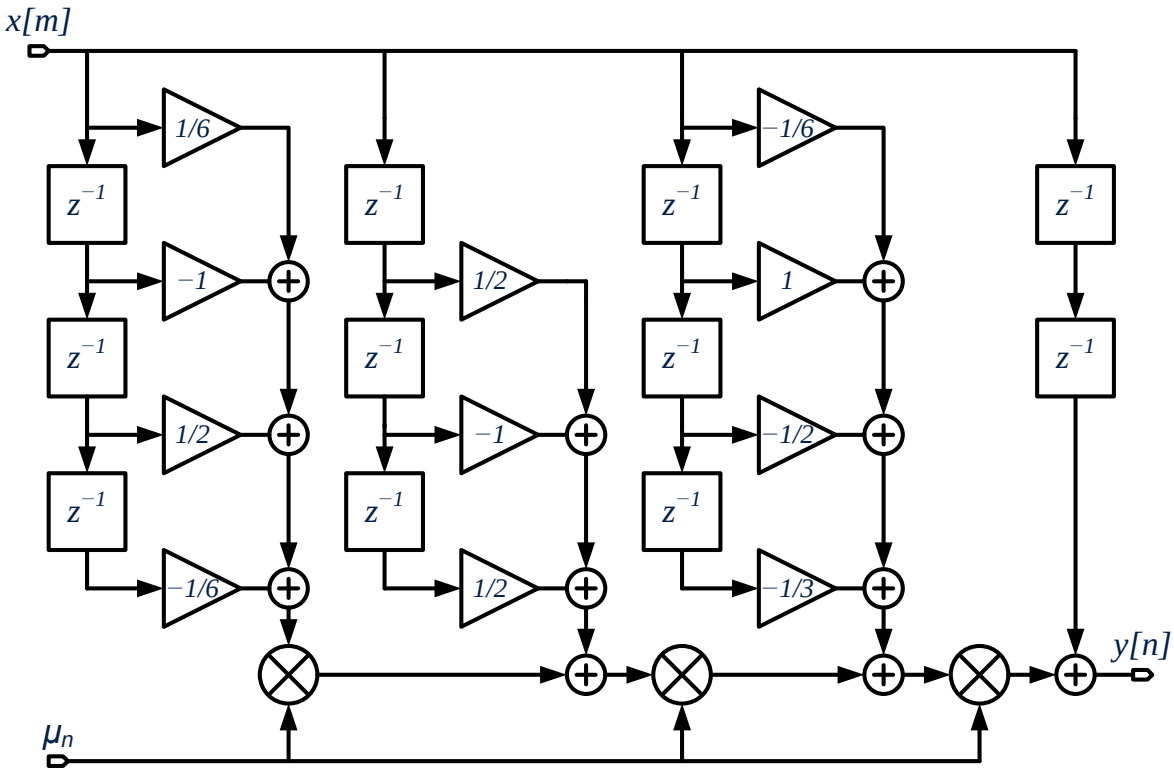


Figure 6.12: Farrow structure of cubic Lagrange interpolator.

6.3.4 Viterbi Decision

For CPM signal modulation, a differential encoded rectangular data stream $a_n \in \{\pm1\}$ is filtered by a pulse shaping filter as premodulation. For example, the GFSK modulated Bluetooth signal is shaped by a Gaussian low pass filter. Due to this premodulation filter, the current symbol suffers Inter-Symbol Interference (ISI) from the pulse shaping of its adjacent symbol. (6.2) with ISI effect consideration is modified to:

$$u(t) = \sum_{n=0}^{\infty} \sum_{i=-k}^{k} a_{n-i} g_i(t - nT - \varepsilon T). \tag{6.20}$$

Where g_i denotes the impulse response of premodulation filter at different symbol periods, and k denotes the number of adjacent symbol periods influenced by the ISI

effect. When the phase is integrated, the phase modulated baseband signal $\phi(t)$ is $\phi(t) = \frac{2\pi}{T}\int_0^t u(\tau)d\tau$.

At the receiver side, the down converted baseband signals at I and Q paths are:

$$\begin{aligned} I(t) =& \cos(\phi(t) + \Delta\omega t + \theta_t) + n_I(t), \\ Q(t) =& \sin(\phi(t) + \Delta\omega t + \theta_t) + n_Q(t). \end{aligned} \tag{6.21}$$

Where $\Delta\omega$ is the frequency offset, θ_t is the phase offset, and n_I and n_Q are uncorrelated zero mean Gaussian noises. Differential discrimination is a typical non-coherent demodulation scheme for CPM signals because of its immunity against fast fading and center frequency drift. Carrier phase recovery is not necessary. The received baseband signal is directly demodulated by the 1st-order derivatives of I and Q signals:

$$\begin{aligned} d_1(t) =& I(t)\frac{dQ(t)}{dt} - Q(t)\frac{dI(t)}{dt} \\ =& \dot{\phi}(t) + \Delta\omega + n_{1t} \\ =& \sum_{n=0}^{\infty}\sum_{i=-k}^{k} a_{n-i}g_i(t - nT - \varepsilon T) + \Delta\omega + n_{1t}. \end{aligned} \tag{6.22}$$

The carrier frequency offset can be calibrated through the phase rotator, and the optimum sampling phase can be achieved by the clock recovery in the following signal processing. When decimating at the optimum time $t = nT + \varepsilon T$, the discriminator output at symbol rate is simplified as:

$$\begin{aligned} d_1[n] =& I[n]Q[n-1] - Q[n]I[n-1] \\ =& \sum_{i=-k}^{k} a_{n-i}g_i + \Delta\omega + n_{1n}. \end{aligned} \tag{6.23}$$

A Decision Feedback Equalizer (DFE) is an easy way to overcome ISI, as it considers previous sequence information into the current state decision [SCP00]. However, DFE only works properly when the prior bit decision is correct. And the previous decision is also influenced by its prior bit. The optimal decision depends not only on current bit and previous decisions, but also on the history of the received signal. By implementing multi-order differential discriminators, it is possible to find the information containing previous states. The m-order differential discriminator output is:

$$d_m(t) = \begin{cases} I(t)\frac{d^mQ(t)}{dt^m} - Q(t)\frac{d^mI(t)}{dt^m} & \text{m is odd} \\ I(t)\frac{d^mI(t)}{dt^m} + Q(t)\frac{d^mQ(t)}{dt^m} & \text{m is even} \end{cases} \tag{6.24}$$

$$
\begin{aligned}
d_m[n] &= \begin{cases} I[n]Q[n-m] - Q[n]I[n-m] & \text{m is odd} \\ I[n]I[n-m] + Q[n]Q[n-m] & \text{m is even} \end{cases} \\
&= -\prod_{j=0}^{m}\Big(\sum_{i=-k}^{k} a_{n-i-j}g_i + \Delta\omega + n_{jn}\Big).
\end{aligned} \tag{6.25}
$$

$d_m[n]$ contains the information about current input a_n and also the previous sequence. Therefore, the optimum maximum likelihood for a_n is estimated from:

$$
\hat{a_n} = \frac{p(d_1[n], ...d_m[n]|a_n = 1, \hat{a_{n-1}}, ...\hat{a_{n-m+1}})}{p(d_1[n], ...d_m[n]|a_n = -1, \hat{a_{n-1}}, ...\hat{a_{n-m+1}})} \underset{-1}{\overset{1}{\gtrless}} 1. \tag{6.26}
$$

The baseband signals are differentially discriminated, integrated and dumped filtered (IDF), and decoded by the Viterbi decision. Viterbi is an algorithm which uses the convolution encoded data to make an optimum decision. Decision a_n can be reconstructed based on the received symbols $d_m[n]$ [Y Z+13a]. With the 1st, 2nd and 3rd-order differential discriminators, an 8 states and 3 branches per state $d_1[n]$, $-d_2[n]$ and $-d_3[n]$, a Trellis diagram is constructed for the Viterbi decoding with 1/3 decoding rate, as shown in Fig. 6.13. The decoding rate is 1/3. It can be seen that the transitions in all Trellis are uniquely determined, so that a_n can be correctly estimated by traceback. Because of the redundancy, it is possible that the data are correctly obtained even though the received symbols are different from the transmitted ones.

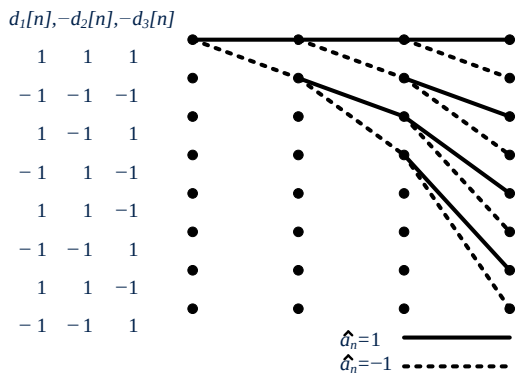


Figure 6.13: Trellis diagram of Viterbi decoder.

Therefore, the maximum likelihood sequence estimation method is to find the symbol sequence which is closest to the received signals by minimizing the cost function $C(L)$:

$$C(L) = \min\{\sum_{k=0}^{L}[(a_n - d_1[n])^2 + (a_n a_{n-1} + d_2[n])^2 + (a_n a_{n-1} a_{n-2} + d_3[n])^2]\}. \tag{6.27}$$

Where L denotes the recursive trace back length. The simplified hardware implementation of the Viterbi decoder is shown in Fig. 6.14. In the proposed receiver, the Viterbi decoder circuit with 32 recursive length is implemented, consisting of a branch metric calculator (BMC), an add-compare-selector (ACS) and a trackback decoder (TBD). The BMC unit calculates the distance of received data to a corresponding branch output. Based on the previous metric and branch metric, a new state is updated in the metric memory. From all the branches coming to a node, only one branch is selected as the survivor. Based on the selected survivors, the decoding result is decided in the TBD circuit. The pipeline registers are inserted in the traceback decoder for branch updating. The result indicating the selected path is stored on the survivor memory.

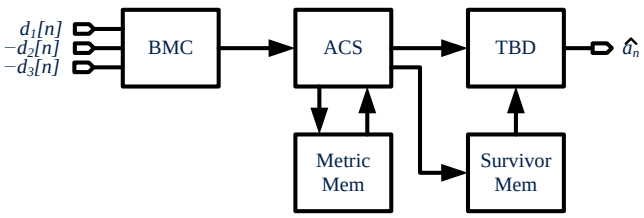


Figure 6.14: Hardware implementation of Viterbi decoder.

6.3.5 Carrier Frequency Offset Calibration

As described from the previous section, the timing error is detected by the M&M algorithm:

$$e_\varepsilon[n] = \hat{a}_n d[n-1] - \hat{a_{n-1}} d[n] \tag{6.28}$$

In (6.23), the output waveform consists of a DC term $\Delta\omega$ and the demodulated signal. As long as the demodulated signal is correctly decided, its mean value can be determined for frequency offset estimation. For Bluetooth GFSK signal with 0.5 BT, more than 99% of the signal energy is contained within 3 times of the symbol period. Other symbol period values can be neglected for the current decision ($k = 1$). As long as the decisions of two adjacent symbols are determined, from (6.23) the carrier frequency offset can be simultaneously estimated in DA scheme:

$$\begin{aligned} e_f[n] = E(d_1[n] - g_1(\hat{a_{n-1}} + \hat{a_{n+1}})|\hat{a_n} = 1, \hat{a_{n-1}}, \hat{a_{n+1}}) \\ +E(d_1[n] - g_1(\hat{a_{n-1}} + \hat{a_{n+1}})|\hat{a_n} = -1, \hat{a_{n-1}}, \hat{a_{n+1}}). \end{aligned} \tag{6.29}$$

Loop filter designs for clock data recovery and frequency offset calibration are both adapted from a classical DPLL. The TED output signal is filtered first before feeding to the CDR control unit. It determines the bandwidth of the timing recovery loop and its ability to track frequency and phase error steps. A zero-order loop filter is required to track the frequency steps which only contains a scaling constant α in its transfer function. To track the phase step, 1st-order loop filter is used with coefficient of β. α and β are programmable according to the different clock frequency mismatches.

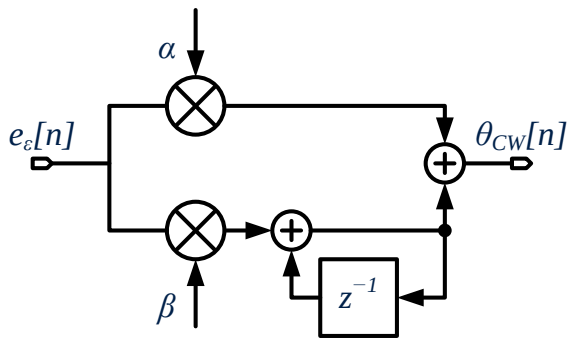


Figure 6.15: Loop filter structure.

Recoverd clock jitter is one of the most important specifications in the receiver design. In the classical clock recovery circuit, the jitter is mainly determined by VCO phase noise, phase error detector linearity, and the loop filter bandwidth. In the proposed architecture, the recovered clock is directly divided from the sampling clock. So its jitter performance fully depends on the oversampling ratio of sampling rate to symbol rate. In steady state, the recovered clock frequency varies from $\{\frac{f_s}{N+1}, \frac{f_s}{N}\}$. For example, in Bluetooth communication, when the sampling clock is larger than 32 MHz and the modulated signal data rate is 1 Mbps ($N > 32$), the frequency deviation of the recovered data clock is smaller than 3%. This is fully acceptable in Bluetooth standard. Fig. 6.16 shows the simulated transient response of joint symbol timing and frequency offset recovery for 1 Mbps GFSK Bluetooth signal. Ideally the receiver is expected to provide 1 MHz IF frequency and 32 MHz sampling clock. In simulation, the clock at the receiver side is 33.25 MHz, and IF frequency is 1.062 MHz. It can be seen that clock frequency error information gets converged after 50 cycles as it is immune to the frequency offset. When the phase is tracked, the normalized frequency error becomes smaller and gets converged in 80 cycles. Finally the CFO is also correctly estimated after 100 cycles.

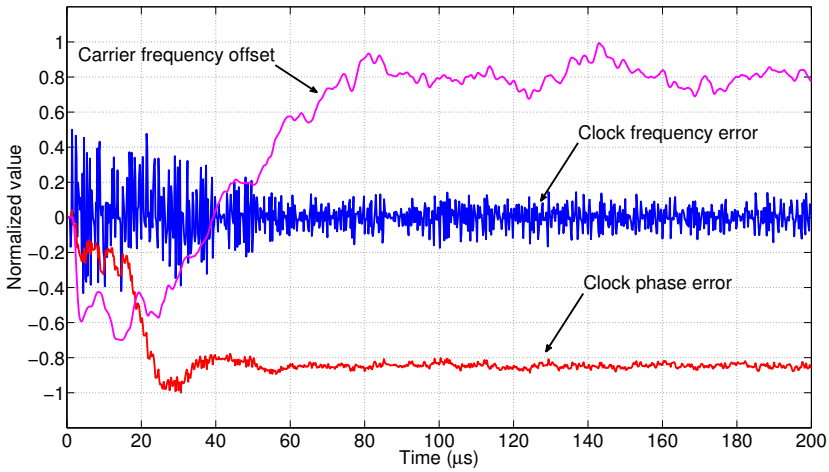


Figure 6.16: Simulation of joint clock recovery with 4% clock mismatch and 6% IF frequency mismatch.

6.4 Measurement Results

6.4.1 Measurement Setup

The proposed digital circuit was fully synthesized in a 130 nm CMOS process with standard digital cells. It consists of 35400 cells in a total die size of 0.83 mm^2. Power consumption is about 4.5 mW when full function is activated. The pie chart of each subcircuit area contribution is shown in Fig. 6.17. It can be seen that the CIC, FIR and DDS circuits occupy most of the area, because they contain the 24th-order low pass filters to suppress the $\Sigma\Delta$ noise. The clock data recover circuit including Farrow interpolator and the Viterbi decision circuits are relatively small. Compared to the Viterbi soft decision in [Y Z+13a], the proposed Viterbi hard decision takes significantly small area.

For the performance verification, the proposed digital receiver is synthesized using Xilinx Virtex-5 FPGA. The frontend devices from the Bluetooth LE receiver chip including the LNA, mixer, poly phase filter, $\Sigma\Delta$ ADC and fractional-N synthesizer are modeled from a fabricated integrated Bluetooth receiver chip [Y Z+13b; Lia+14; Ata+13]. The Bluetooth chip micrograph is shown in Fig 6.18. Only important parameters in the frontend system such as frontend gain, noise figure, total frontend bandwidth are modeled. Moreover, several mismatch and non-ideality issues such as I/Q path mismatch, $\Sigma\Delta$ ADC coefficient mismatch and center frequency shift are also considered [Mar10]. A 1 Mbps GFSK modulated Bluetooth signal is generated at 1 MHz IF frequency from a signal generator. The FPGA is operated by an external crystal

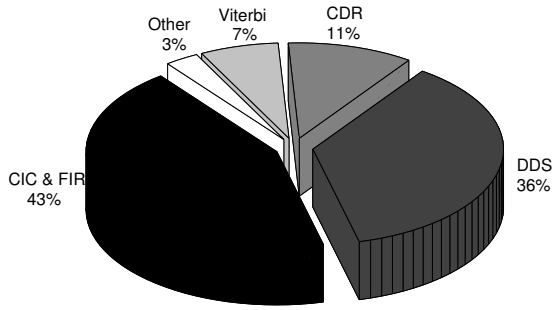


Figure 6.17: Pie chart of the proposed digital receiver area.

clock, whose resonance frequency is around 30.6 MHz.

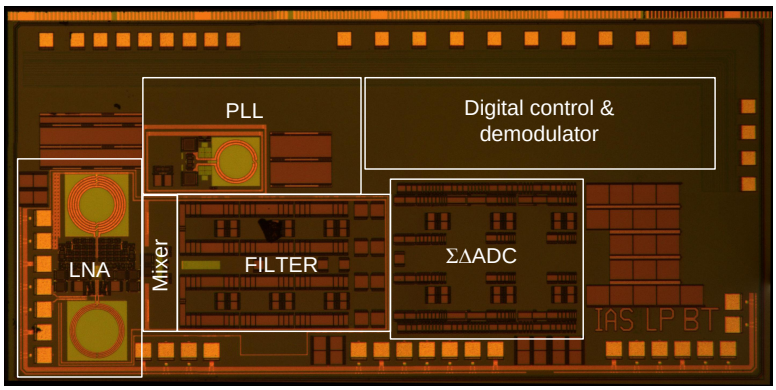


Figure 6.18: Bluetooth receiver chip micrograph.

6.4.2 Clock Recovery Performance

Fig. 6.19 shows the oscilloscope waveforms. The upper waveform presents the input signal, the middle waveform presents the recovered clock signal and the bottom waveform presents the output signal with direct decision. It can be seen that the proposed receiver architecture can successfully demodulate and decode the Bluetooth signal. The symbol clock is also properly recovered, synchronizing with the output data.

The recovered clock frequency is fully determined by the oversampling ratio. In this case the recovered clock is always switched between 30.6/31 MHz and 30.6/30 MHz.

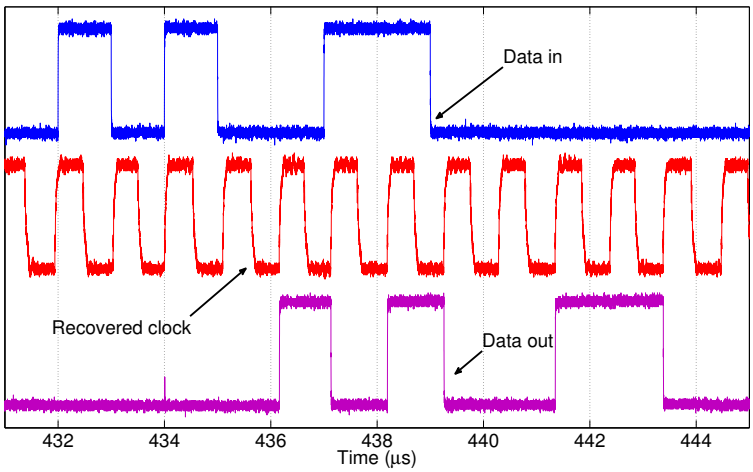


Figure 6.19: Input, output and recovered clock waveforms from oscilloscope.

Hence, about 30 kHz frequency deviation of the recovered clock is seen in the frequency analyzer, as shown in Fig. 6.20.

6.4.3 Fractional Interpolator and Decimator

By using the Xilinx Chipscope Cores tool, the internal register contents can be monitored. Fig. 6.21 shows the comparison of oversampled discriminator output and symbol rate discriminator output. The timing delay caused by the clock recovery circuits is not shown. In Fig. 6.21(a), when an incoming signal with 667 kbps data rate is received, two stages of CIC decimator with decimation factor of 4 are activated. So the data oversampling ratio at discriminator output is about 11.5. In Fig. 6.21(b), when a 2 Mbps incoming signal is received, only one stage of CIC based decimator with decimation factor of 2 is connected to the receiver. So the data oversampling ratio at discriminator output is about 7.7. It can be seen that in both cases the optimum phase can be successfully aligned by the proposed fractional interpolator and $\Sigma\Delta$ modulated decimator.

6.4.4 Direct Digital Synthesizer Performance

A dual channel 16-bit high speed DAC chip TI-DAC5682Z is used to monitor the content of internal registers. It is also connected to the same external clock as the digital receiver. Since high pass filters in the high speed DAC are implemented after the dual channel signals are interleaved, the DC information of the input signal is distorted. Fig. 6.22(a) shows the FFT plot of the IF frequency $\Sigma\Delta$ ADC output from a spectrum analyzer. More than 22 dB inband SNR is achieved when the received power

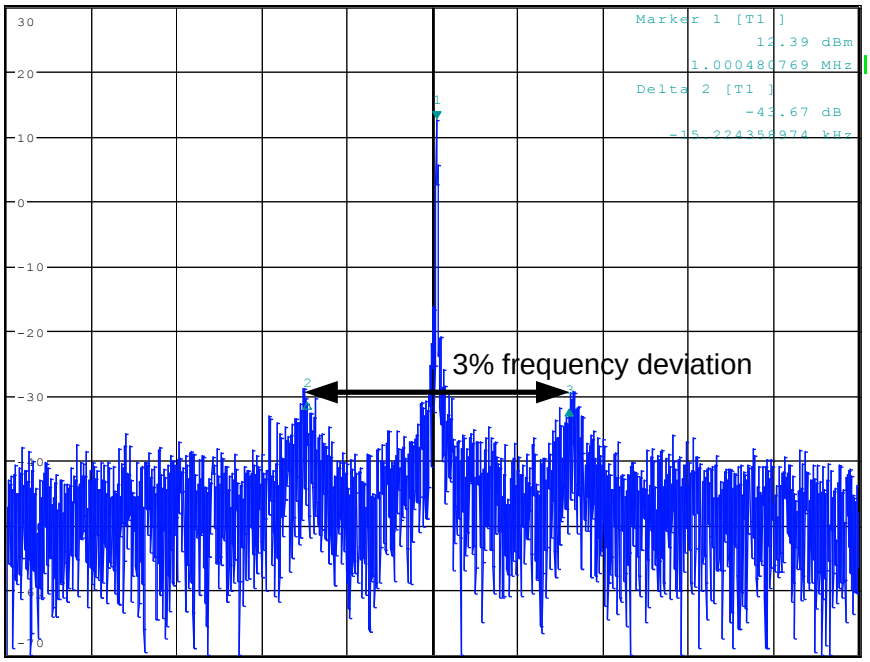


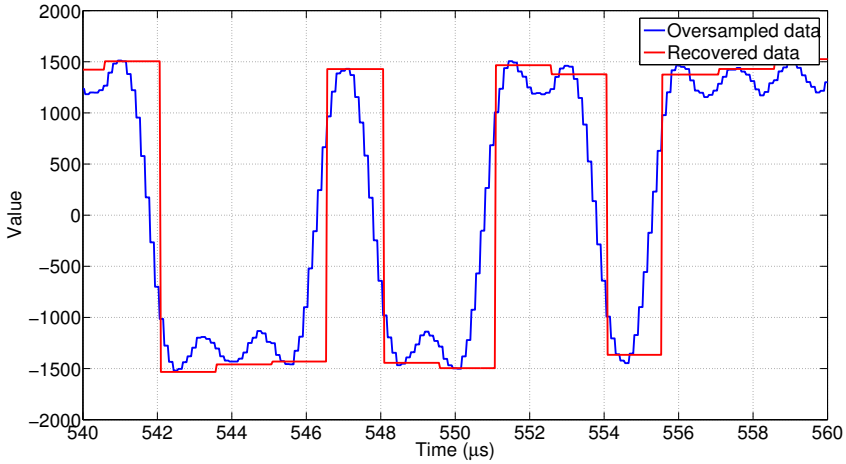
Figure 6.20: Recovered clock spectrum.

is −75 dBm. The DC spur can be neglected. When it is shifted to baseband, as shown in Fig. 6.22(b), the inband SNR and noise shaping performance remains.

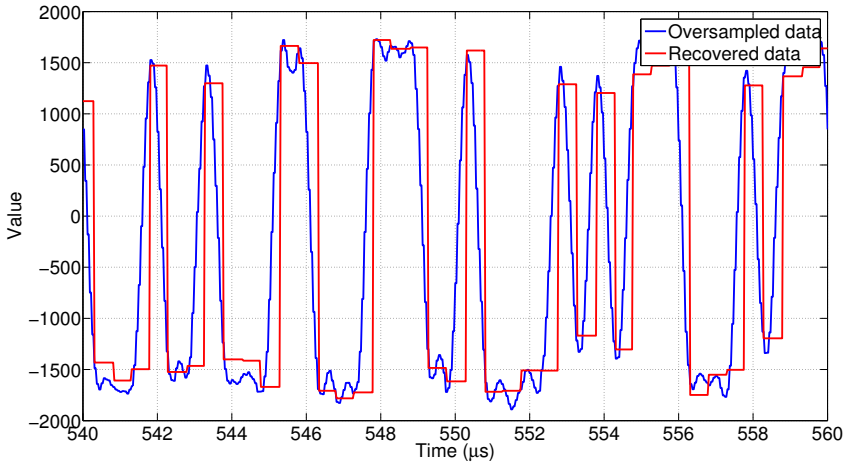
The whole complex DDS generated IF signals spectrum without low pass filtering is shown in Fig. 6.23. Ignoring the same DC spur generated by the DAC high pass filters, the proposed DDS circuits are able to achieve larger than 95 dB SNR in 2.3 MHz bandwidth over the frequency tuning range from 0.5 MHz to 5 MHz. The inband spurs are less than −80 dBc. Compared to the ADC output spectrum in Fig. 6.22, it gains a significant lower noise floor, due to the multi-bit quantizer. Hence, using the proposed DDS generated sine signal will not degrade the receiver performance.

6.4.5 Carrier Frequency Offset Calibration

Fig. 6.24 demonstrates the effectiveness of the frequency offset estimation and calibration for 1 MHz IF frequency when −75 dBm Bluetooth signal is received. A dramatic degradation in BER performance can be seen when original frequency offset varies over 5%. One can observe that the proposed receiver with CFO calibration gains a significant improvement. More than 30% bandwidth is extended when obtaining the BER performance of 10^{-3}. Further frequency offset pushes a large part of the desired signal out of the passband of the receiver filter, which should be coarsly calibrated in the frontend circuits. Table. 6.1 shows the performance comparison with other published

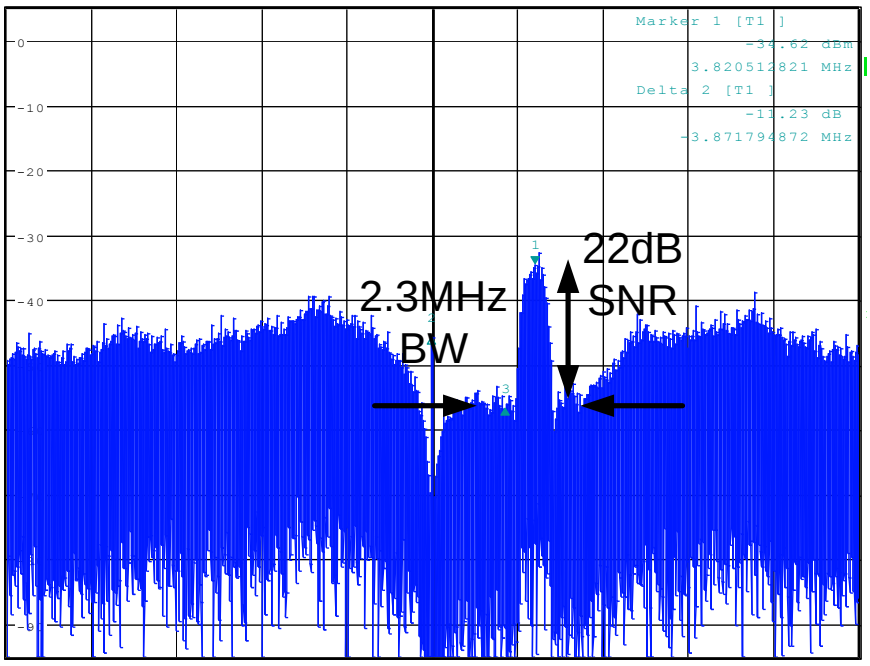


(a) 667 kbps data rate recovery

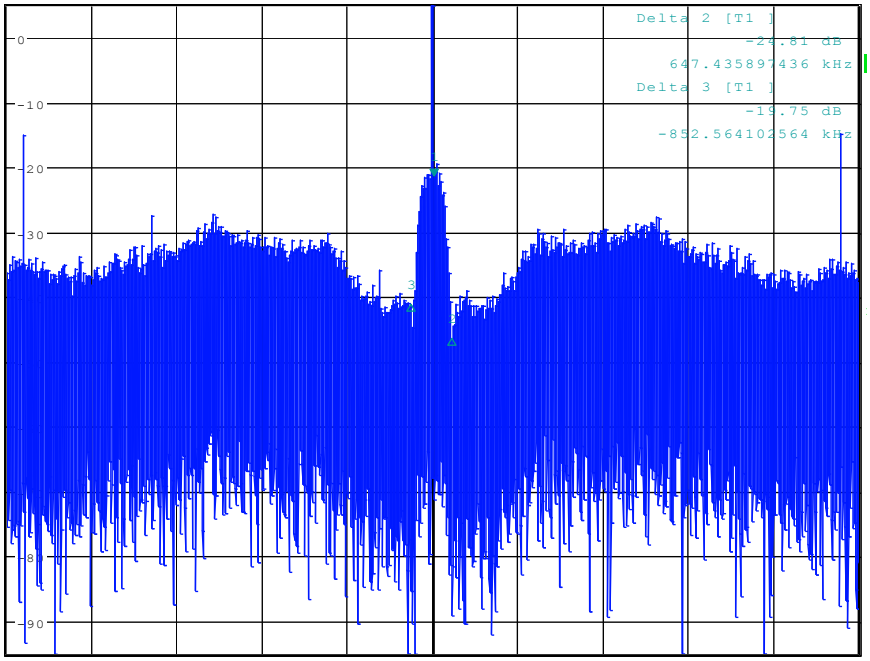


(b) 2 Mbps data rate recovery

Figure 6.21: Comparison of oversampled and data rate waveform from Chipscope.

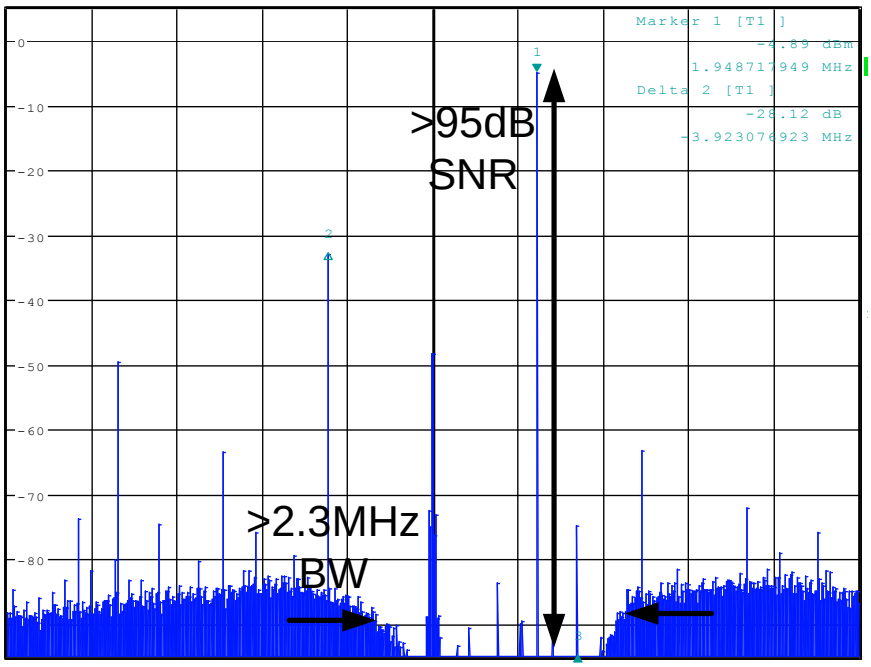


(a) IF frequency signal

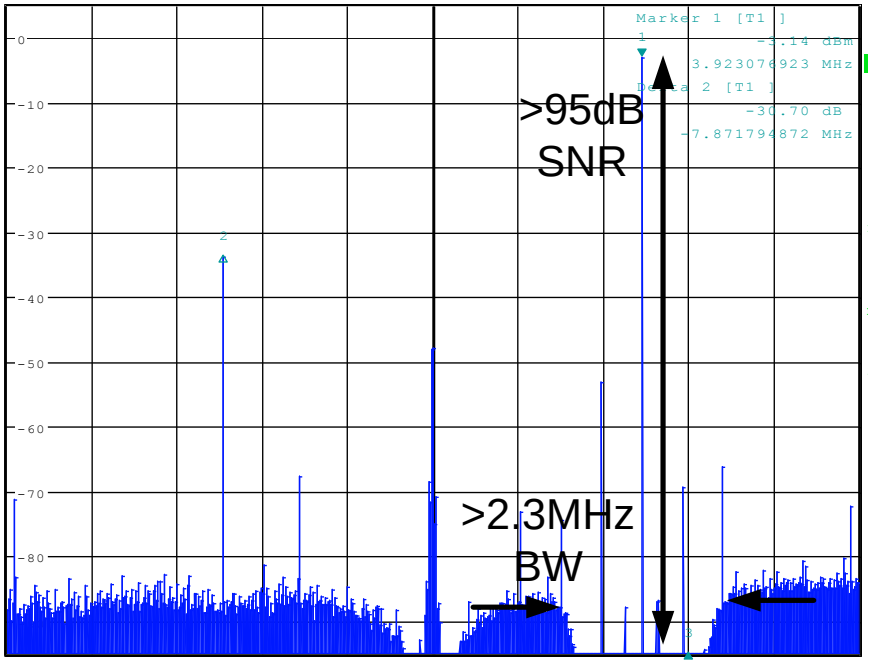


(b) Baseband signal

Figure 6.22: ΣΔ modulated signal performance.



(a) 2 MHz f_{IF}



(b) 4 MHz f_{IF}

Figure 6.23: ΣΔ modulated DDS performance.

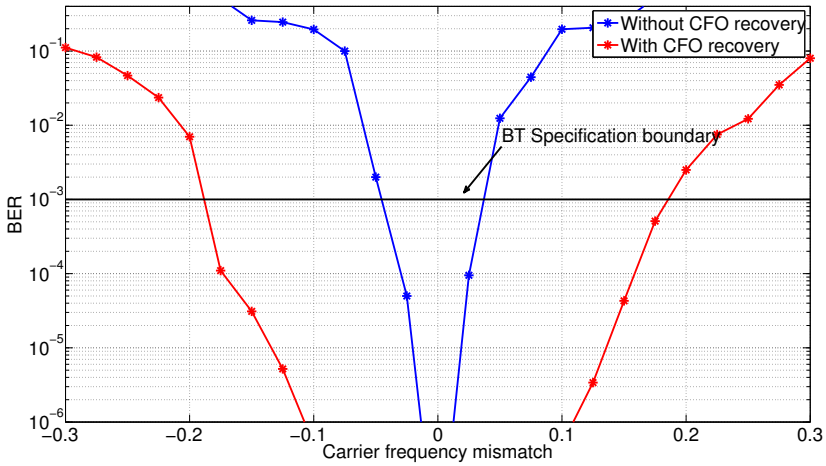


Figure 6.24: BER performance comparison over CFO offset.

works. The proposed receiver gains better flexible performance with various data rates and IF frequencies, which is able to support multi-standard. This error is expected to be acceptable because it is much less than the operation bandwidth of the discriminator.

Table 6.1: Performance comparison with prior works.

Parameter	[Xia+03]	[KYL07]	[HZ09]	This work
Technology (nm)	350	180	180	130
Architecture	Mixed	Delay line	Analog	Digital
IF frequency (MHz)	2	5	2	0.5-1.5
Data rate (Mbps)	1	0.25, 1	0-2	0-2
CDR	No	Yes	Yes	Yes
CFO	Preamble	Yes	Yes	Yes
Area (mm^2)	0.7	0.26	0.23	0.83
Power (mW)	9	3.6	0.74	4.5

6.5 Conclusion

A low-IF digital receiver architecture is presented with low effort and low computation complexity design. Typical synchronization problems including symbol timing recovery and carrier frequency offset calibration are investigated and solved based on a simplified

DA scheme. $\Sigma\Delta$ based DDS circuits provide IF signals with high resolution and SNR. A Viterbi decoder which uses multiple-order differential discriminators provides a better decoding performance, which improves the error calibration efficiency. Hence, it can be demonstrated that the proposed multi-standard receiver architecture not only greatly enhances the performance with wide range data rate and IF frequency, but also provides an easy, feasible and flexible solution for the fully integrated implementation.

Chapter 7

Conclusion and Outlooks

7.1 Conclusion

In this thesis effective novel techniques for short-range wireless communications in the transceiver design are investigated, which aim to achieve low-effort and low-power performance. At the same time, in order to support the multiple short-range standards, issues encountered in the multi-standard transceiver design are analyzed and solved.

Starting from the general introduction of the flexible transceiver architecture, the performance tradeoffs based on different standards are analyzed and compared. Low-IF architecture is chosen for IoT receivers. Compared to the zero-IF architecture, it gains higher inherent immunity to DC offsets and 1/f noise. The PLL based polar transmitter is chosen due to its high efficiency, where the input power is dynamically controlled by the envelop signal and the power amplifier is always operating in the saturation mode.

A current-reuse VCO and symmetric charge pump based synthesizer is presented for low power PLL design, which shows excellent phase noise and reference spur attenuation performance. The current-reuse techniques steer the current from one negative conductance branch to the other branch, so that half the current is saved compared to a conventional differential LC-VCO. The amplitude mismatch issues in current-reuse VCO are discussed and solved. The pre-tuning system uses external memory to store the initial VCO alignment and reuses it in further implementation to calibrate against the large frequency deviation and save the settling time. The

symmetric charge pump makes use of the equalized loads of the control signals, leading to perfect compensation for each switch, and further attenuating the reference spurs in PLLs.

Another novel low power low complexity architecture for frequency/phase modulation PLL system is presented. Based on the proposed RC MASH and differentiator in the signal modulator and quantizer, approximately 50% area and power consumption is saved in digital circuits. And at the same time using the error masking methodology, the proposed PLL shows the same excellent spectral performance as the conventional PLL.

In the transmitter design, a low effort adaptive calibration technique for phase noise cancellation based on the modified classical loop filter structure is proposed. This calibration technique demonstrates fast settling time, low spurs and excellent phase noise performance with low power consumption and small area. Comparing to the previous work, the proposed technique provides a straightforward solution for wideband PLL designs, where the quantization noise is successfully canceled with smaller area and lower power consumption. It is able to transmit constant envelop baseband data with direct modulation for multiple IoT standards. Due to its simplicity and flexibility, it can be directly added as a straightforward phase noise enhancement for any wideband PLL structures, and it also provides an easy and feasible solution of direct frequency/phase modulation for short-range wireless standards.

In the low-IF receiver design, the imperfection from the analog circuits leads to I/Q path mismatch, which degrades the image rejection performance of the receiver. By implementing an adaptive LMS based equalizer, the interference component from the desired signal observation can be estimated and subtracted. The proposed demodulator compensates the I/Q mismatch by the adaptive LMS filter and thus improves the robustness against interference located at the image frequency. The inconstant group delay response of the polyphase filter is another issue, especially in the vicinity of the band-edge, which leads to a phase offset error when the data is recovered to the Nyquist frequency. By inserting a recursive IIR all-pass filter at the baseband, whose poles are located between the poles of equivalent baseband polyphase filter, the ripples in the group delay curves are greatly suppressed. It improves the BER performance significantly.

In the mobile communication environments, the carrier phase offset and the symbol timing errors are often encountered due to the clock misalignment between the transmitter and receiver. And the clocks from different blocks must be synchronized. The typical synchronization problems including symbol timing recovery and carrier frequency offset calibration. A novel low-IF multi-standard digital receiver with joint synchronized clock recovery and carrier frequency offset calibration is proposed in this thesis. By modulating the sampling clock with a fractional frequency divider, the multi-rate clock data can be recovered, and the optimal sampling phase is obtained simultaneously by adjusting the fractional delay from a polynomial interpolator. Direct digital synthesizers with $\Sigma\Delta$ noise shaping are implemented to generate arbitrary

frequencies for offset frequency calibration. With the fully digital implementation, the proposed backend circuit can successfully recover the clock data within a wide frequency range.

In this thesis, the novel low-power low-effort architecture for IoT transceivers has been proposed. Due to its flexibility and simplicity, it shows a great potential for the low cost short range wireless communication applications in the future. Based on the transceiver key performance evaluation, the proposed techniques not only greatly enhance the low power transceiver function with respect to the multiple impairment issues, but also provide an easy and feasible solution for the fully integrated implementation for IoT applications.

7.2 Outlook

Several innovative techniques for low power short distance wireless communications are worthy to be investigated in the future.

7.2.1 RTWO Based Wideband Transmitter

For narrow band as well as short range wireless standards, the wideband phase modulation capability of the architecture can be used to realize a polar transmitter mode. However, the power efficient highly integrated transmitters suitable for broadband OFDM modulated signals are the fundamental challenge for the implementation of wireless systems. Numerous efforts have been made to solve this fundamental quest. Concepts based on polar modulation are capable for the lower end of the bandwidth requirements, but for an RF bandwidth above 20 MHz the increased bandwidth for the polar components namely the amplitude and the phase will become too large and therefore limit the achievable bandwidth. Compared to the polar based close-loop modulation, the open-loop transmitter based on Rotary Traveling Wave Oscillator (RTWO) and phase interpolator can easily extend the modulation bandwidth without suffering from $\Sigma\Delta$ quantization noise, since the phase and amplitude modulation is implemented outside of the PLL dynamical loop.

Rotary Traveling Wave Oscillator

The RTWO was originally developed by J. Wood as a clock generator for digital circuits, which is able to provide quasi-square signals with low phase noise [WEL01]. As shown in Fig. 7.1, a typical circuit topology of the RTWO is composed of a cross connected differential transmission line which forms a closed loop feedback. Distributed cross coupled inverters compensate for the loss of the transmission line to sustain the oscillation. Due to the transmission line delay, the multiphase information is naturally converted into the digital domain at each tap of the RTWO. RTWO relies

on the resonance of the distributed LC tank. Hence, the similar excellent phase noise performance to the LC-VCO can be achieved.

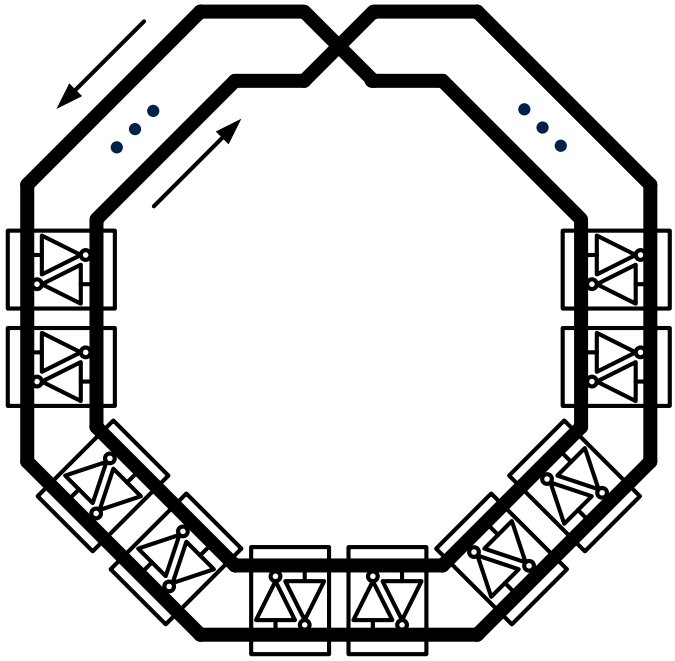


Figure 7.1: RTWO schematic

In a RTWO circuit, the wave propagates only in one direction. Unlike LC-tank oscillators, it is not susceptible to mismatching effects. In addition, the distributed nature of this oscillator alleviates the effects of the transistor parasitic and therefore enables lower phase-noise spectral density. Another advantage is that accurate quadrature outputs or multiphase outputs needed for I/Q modulation and demodulation can be obtained at its fundamental oscillation frequency.

Phase Interpolator

Due to the geometry property of the RTWO, the phase shift between each neighbor taps cannot be exactly equalized, because the inner and out transmission line lengths are not equal. Till now only up to 5-bit phase resolution with the RTWO topology has been reported [Tak+11], which is applied only for enhancing the fractional frequency divider resolution in the close-loop.

The phase quantization noise can be suppressed either by increasing the phase switching speed or by enhancing the phase resolution. However, fast switching among the various taps causes undesired glitches and increases circuit complexity and power consumption. The smallest achievable phase step is limited by technology and fabrication mismatches. The solution to enhance the phase resolution in RTWO is shown in Fig. 7.2.

A linear phase interpolator circuit can straightforward increase the phase resolution by summarizing two neighbor tap vectors φ_M and φ_{M+1} to generate a new vector φ_{out} [Non+13]. The weights of input vectors are digitally controlled by the tail currents I_1 and I_2. Phase interpolation is an attractive method to increase the time resolution in the continuous time domain. It can be seen as a form of digital-to-time conversion, where digital information is converted to a voltage pulse at a specific instant.

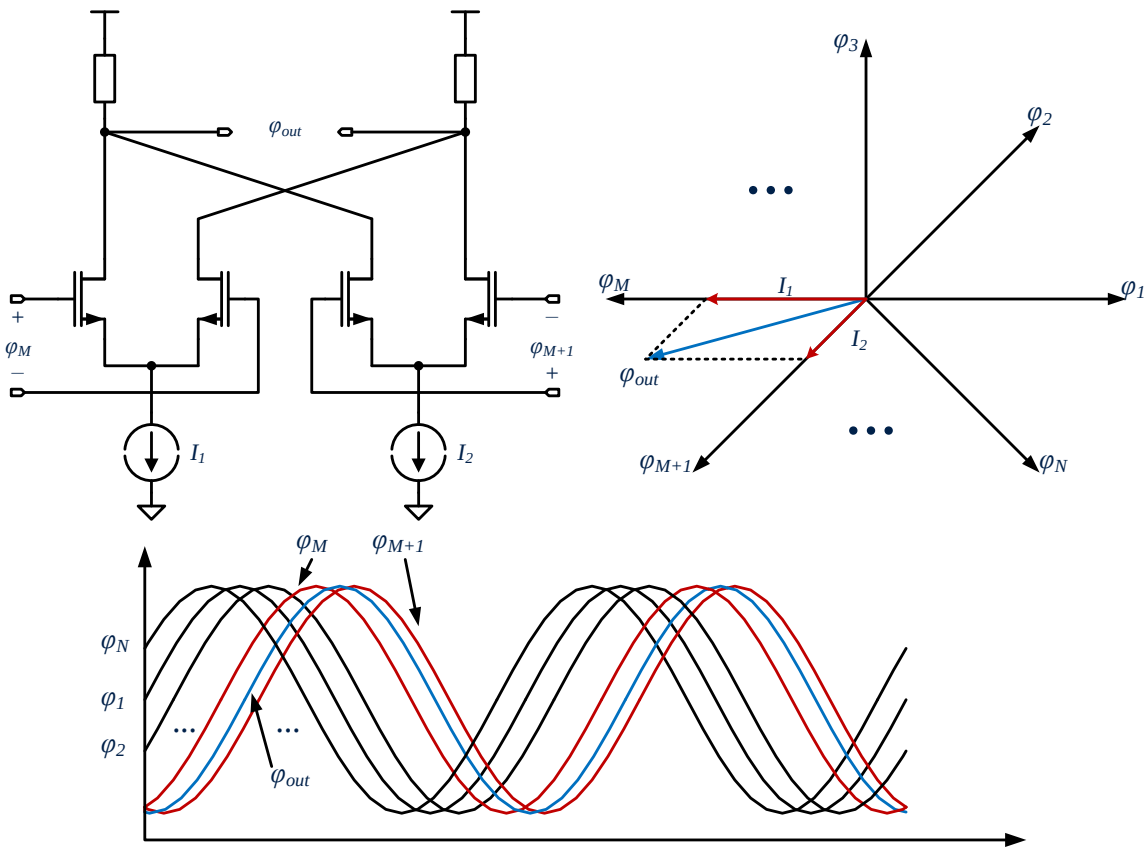


Figure 7.2: Phase interpolator

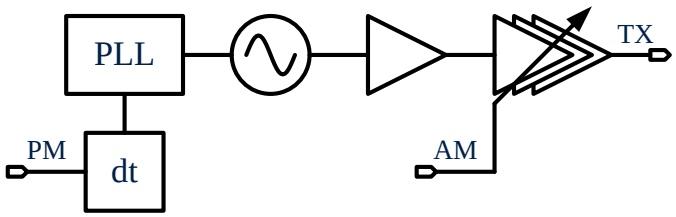
Since the phase interpolation is a linear process, the close-in phase noise maintains as good as the original RTWO circuit. On the other hand, as long as the static phase mismatch caused by the unequal transmission line in RTWO circuit is detected, the digital controlled bias current can calibrate this existing static mismatch to obtain higher resolution multiphase signals.

Wideband Open-Loop Modulation

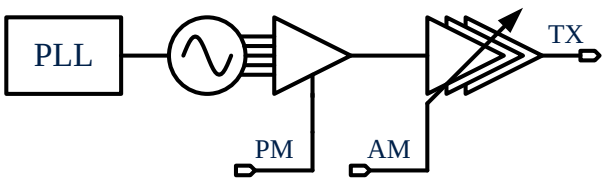
Wideband phase modulators are fundamental building blocks of efficient switching power amplifier architectures. A phase modulation transmitter suitable for such switching

power amplifier transmitters needs to be wideband, preferably digital in architecture and obtain low close in and far out phase noise. Wide bandwidth is required because the PM signal bandwidth can span more than 10 times the original modulation signal bandwidth [Rav+12]. Digital phase modulator architecture is preferred as it can introduce fine and well-controlled phase offsets required to compensate for inevitable delay mismatches. Low phase noise is critical to keep spurious emission low and excellent modulation accuracy.

In the conventional close-loop polar transmitter, the phase domain modulation is differentiated to frequency domain and then implemented in baseband, as shown in Fig. 7.3(a). Another transmitter architecture utilizes the polar modulation architecture and digital controlled high efficiency power amplifier [Gro07]. It works by splitting the amplitude and phase modulations. The general block diagram is shown in Fig. 7.3(b), the polar transmitter is operated in open-loop. By switching on only one transmitting path, the carrier frequency signal is modulated in the phase domain, and its power is controlled by the linear power amplifier separately.



(a) Close-loop transmitter



(b) Open-loop transmitter

Figure 7.3: Comparison of polar transmitter architectures

High Speed Open-Loop Transmitter Architecture

As shown in Fig. 7.4, the proposed transmitter uses open-loop phase switching technique to realize frequency/phase and amplitude modulation in both polar mode and outphasing mode. With fine phase selection resolution that dynamically selects from a bank of periodic signals from RTWO, carrier frequency signals with different but fixed phase offsets are generated from 8 taps. Following the phase selectors, two phase interpolators

can further improve the phase resolution to 12-bit. 6-bit digital power amplifiers are used to control the output power. The modulation data is injected to control the VCO output phase directly instead of frequency divider, which is free from the PLL bandwidth constraint.

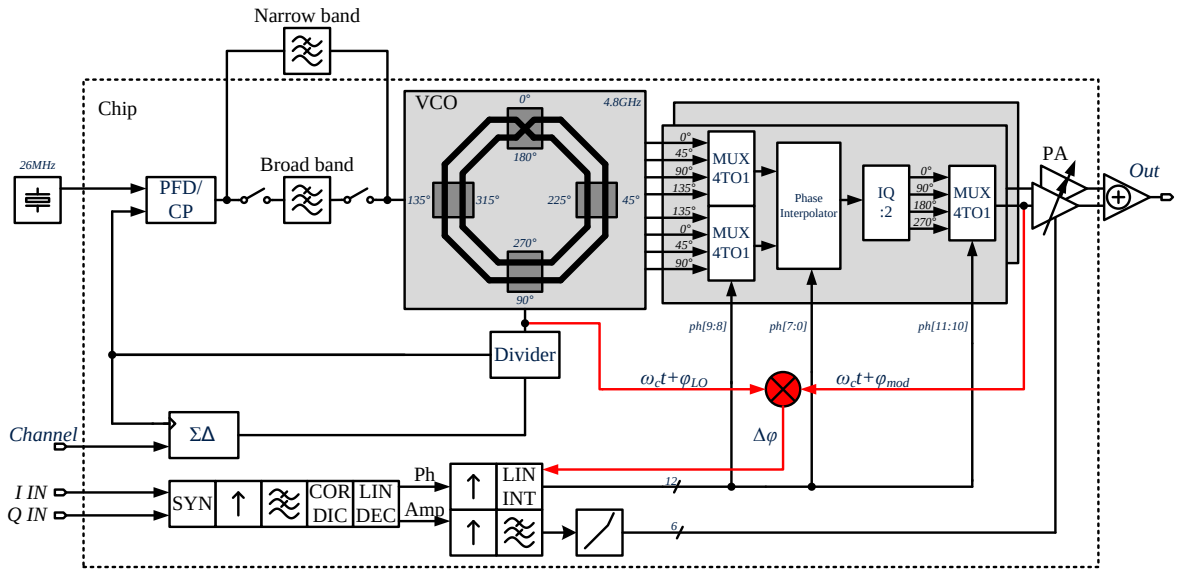


Figure 7.4: RTWO based transmitter

Since the modulation signal path is isolated from the ΣΔ modulator and frequency divider, a narrowband off-chip loop filter is used to sufficiently suppress the ΣΔ highpass shaped quantization noise without influencing the baseband data transmission. And another wideband loop filter is integrated to operate fast frequency hopping mode. The proposed transmitter consists of a conventional PLL system, digital control systems for phase and amplitude modulations, and two banks of phase selectors, interpolators, I/Q dividers and power amplifiers. Only the channel selection value is given to the frequency divider. As long as the correct channel is selected, the fractional ΣΔ noise will be effectively attenuated by the narrow band loop filter. The phase modulation signal is synthesized by combining and rotating the multiphase signals by the proposed phase selector and interpolator. In contrary to the conventional close-loop topology, the VCO remains locked by the PLL continuously regardless of the input data rate or modulation schemes. Since the frequency modulation is performed outside the loop, the data rate is no longer limited by the loop bandwidth. The phase selector takes multi-phase input signals, by properly combining two neighbor phases to generate the desired phase. It can synthesize a frequency/phase modulated output signal. No LO feed through issue would take place since all the processes behind VCO are implemented in the same frequency.

Meanwhile, the constant carrier phase is obtained for LO generator in close-loop.

By mixing this constant phase $\omega t + \varphi_{LO}$ and the modulation phase $\omega t + \varphi_{mod}$ down to the baseband, the static mismatch caused by RTWO circuit can be detected. As shown in the red signal flows in Fig. 7.4, this phase error is fed back to the digital block to generate a calibrated bias current. To further increase the phase resolution, a $\Sigma\Delta$ modulator is used in the bias current generator to quantize phase noise in highpass power spectral density over the band. This architecture is appropriate for highly reconfigurable multi-mode, multi-band, low-cost, and power-efficient mobile communications.

7.2.2 Wake-up Receiver

Large power is consumed to monitor the radio channel for the incoming data packets in the IoT applications, since the wireless network has to remain in an active channel monitoring mode. Especially when the low traffic rate is received, most of the energy is wasted by channel monitoring. The common way to save the energy is to implement a duty-cycled receiver, where the receiver periodically turns from active mode into sleep mode during the monitoring period. In the awake mode, the transmitter sends the request packages until a response is obtained from the receiver. Low traffic network allows low duty-cycling rate, whereby the energy consumption is heavily reduced. However, another issue needed to be taken into account is that the receiving latency will increase dramatically when the low duty cycle rate takes place.

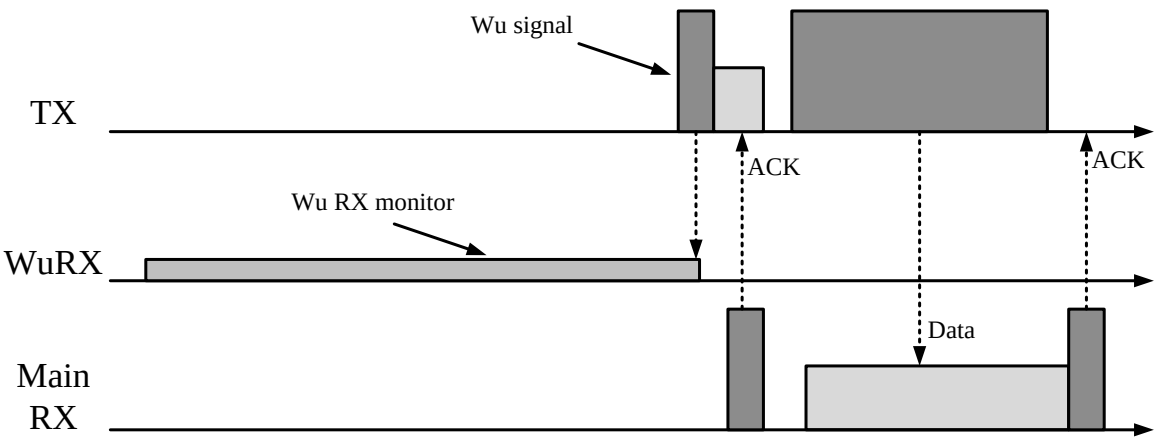


Figure 7.5: Wak-up receiver duty cycling operation process

In order to break this trade-off, a fully asynchronous protocol can be implemented using a dedicated auxiliary receiver called Wake-up Receiver (WuRX). It continuously monitors the channel for requests and activates the main receiver from the sleep mode. The operation process is shown in Fig. 7.5. Because the WuRX is listening to the radio channel continuously, latency is substantially reduced [Yoo+12]. Besides, its active power consumption is very low, not dominating the overall average power of the link.

The block diagram of a typical WuRX is shown in Fig. 7.6. Its analog frontend is directly connected to the digital baseband to generate the wake-up signal. It can be simply implemented with RF amplification and an envelope detector, similar to the AM receivers. The power-hungry LO generator can be eliminated. Because its analog frontend does not require clock signals and the timing constraint in its digital baseband is far below the clock frequency at the main receiver, significant power can be saved from this WuRX architecture.

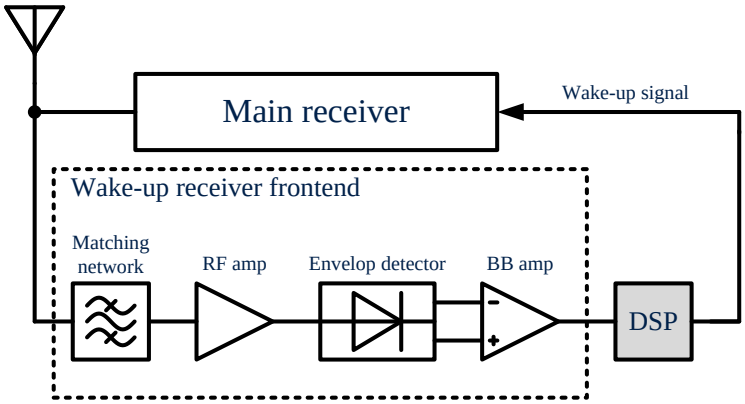


Figure 7.6: Block diagram of the wake-up receiver

The other critical requirement for WuRX is sensitivity. However, the self-mixing operation is insensitive to phase and frequency, so the selectivity must be provided through narrowband filtering directly at RF channel. And high RF gain is required to overcome the sensitivity limitations of the envelop detector, usually implemented with a nonlinear element like a diode. Although the RF amplifier consumes most of the receiver's total power, the available RF gain is limited and ultimately results in poor receiver sensitivity.

7.2.3 Energy Harvesting

Another approach of power saving communication technique is to deploy a network comprising self-powered nodes that can harvest ambient energy from a variety of sources for sustained network operation. This instrument can potentially lead to significant reduction in the costs associated with replacing batteries. This technique becomes a promising solution to power energy-constrained wireless networks [GWZ13]. An RF energy harvesting network has a sustainable power supply from a radio environment. Therefore, the RF energy harvesting capability allows the wireless devices to harvest energy from RF signals for their information processing and transmission.

Fig. 7.7 shows the general block diagram of an energy harvester. The matching networks, composed of inductive and capacitive elements, ensure the maximum power delivery from antenna to voltage multiplier. Subsequently the incident RF power is

converted into DC power by the voltage multiplier. The energy storage ensures smooth power delivery to the load, and as a reserve for durations when external energy is unavailable.

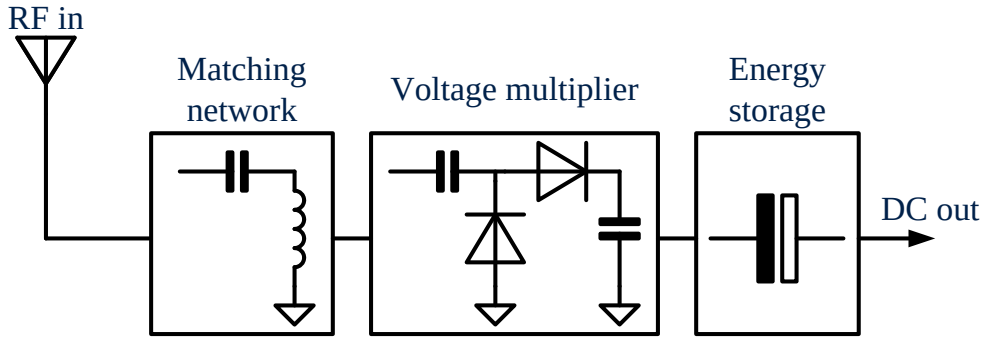


Figure 7.7: RF energy harvester

Several challenges in the RF energy harvester need to be carefully considered. One of the crucial requirements is to be able to operate with weak input RF power. As the peak voltage of the AC signal obtained at the antenna is generally much smaller than the diode threshold, diodes with lowest possible turn on voltage are preferable. Moreover, since the energy harvesting circuit is operating at high frequencies, diodes with fast switching time need to be used. Increasing the number of multiplier stages gives higher voltage at the load, and yet reduces the current through the final load branch, which may result in unacceptable charging delays for the energy storage capacitor. Conversely, fewer stages of the multiplier will ensure quick charging of the capacitor, but the voltage generated across it may be insufficient to drive the sensor mote. Finally, the load impedance must be carefully selected for a specific energy harvesting circuit to achieve its optimal efficiency.

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