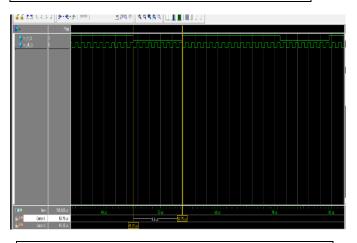
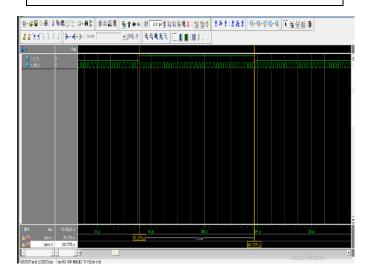
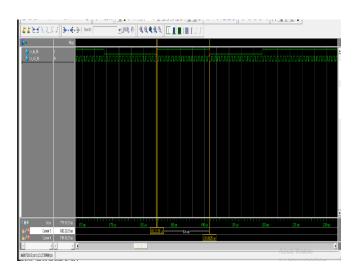
## snippet that shows that f\_rx is 8 of f\_tx



## snippet that shows that f\_rx is 32 of f\_tx

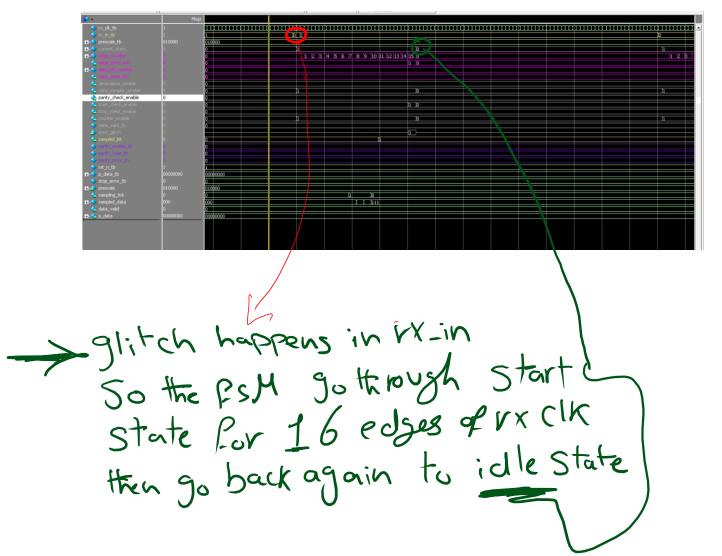


## snippet that shows that f\_rx is 16 of f\_tx



SNIPPETS THAT SHOWS THE WAVE FORM OF THE TEST CASES IN CASE OF PRESCALE EQUALS 16:

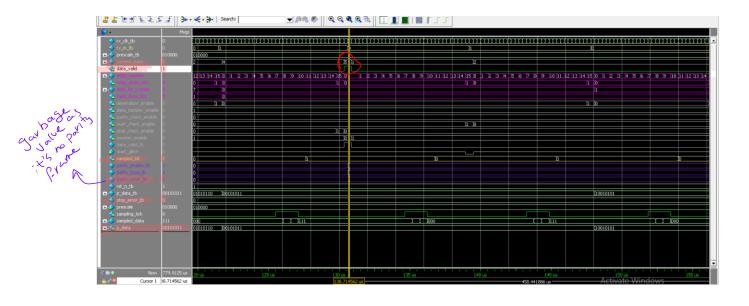
GLITCH\_STATE (rx\_in is zero for a very short time which means it is a glitch)



\* note: we only look at data valid & parity error & stoperror Signals in the check error State only as the frame will be completely recieved.

bit is 1) >>110101001

o frame 1 (without parity bit and stop bit is 1) >>110101001



though State we go

through State 5 which is

check error State that Checks

for stop bit and Since

the Prame is recieved Correctly

then data valid signal is high

in Check error state which means

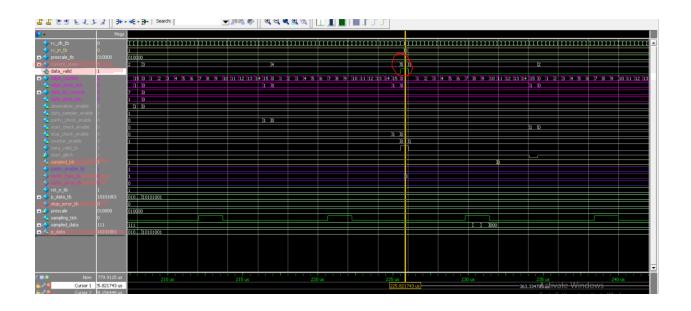
that the Prame is Correct

Same thing in all other

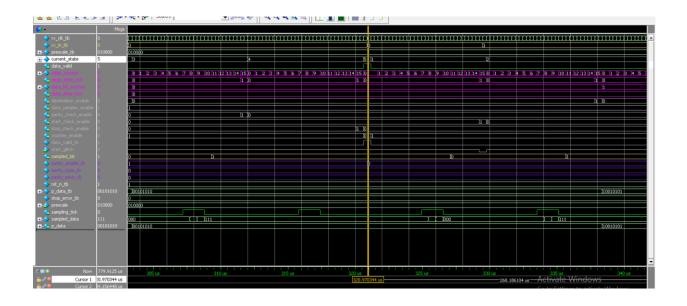
Correct Prames.

1) >>1001010111

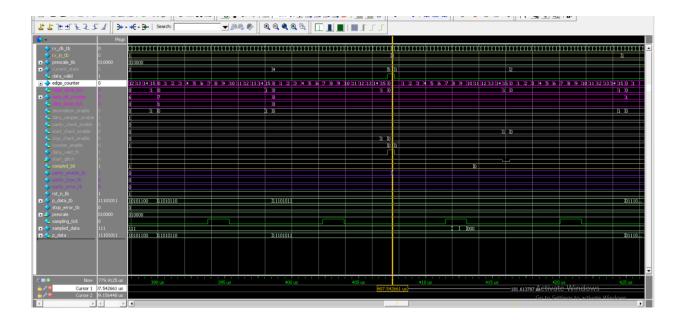
o frame 2 (with correct odd parity bit and stop bit is 1) >>1001010111



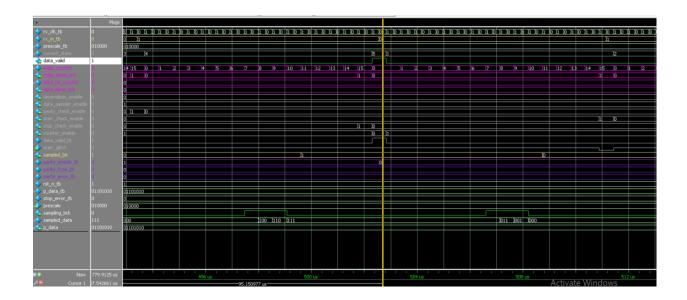
o frame 3 (with correct even parity bit and stop bit is 1) >>0101010011



## o frame 4 (without parity bit and stop bit is 1) >>110101111



o frame 5 (with correct even parity bit and stop bit is 1) >>0101011001



Last three frames are wrong in parity and stop bits in case of parity frames and wrong in stop bit only in case of no parity frame  $\frac{1}{2}$ 

- o frame 6 (without parity bit and stop bit is 0 and parity bit is 0) >>110101000
- o frame 7 (with even parity bit and stop bit is 0 and parity bit is 0) >>01010100000
- o frame 8 (with odd parity bit and stop bit is 0 and parity bit is 0) >>1001010100

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So Data Volid is Tero.

Log window in case of prescale is 32

```
# frame is recieved successfully
# frame is not recieved successfully
# Break in Module RX_TOP_MODULE_TB_P32 at TOP_MODULE_TB_P32.v line 94
# Simulation Breakpoint: Break in Module RX_TOP_MODULE_TB_P32 at TOP_MODULE_TB_P32.v line 94
```

Log window in case of prescale is 16

```
# frame is recieved successfully
# frame is not recieved successfully
# Break in Module RX_TOP_MODULE_TB_Pl6 at TOP_MODULE_TB_Pl6.v line 94
# Simulation Breakpoint: Break in Module RX_TOP_MODULE_TB_Pl6 at TOP_MODULE_TB_Pl6.v line 94
```

Log window in case of prescale is 8

```
# frame is recieved successfully
# frame is not recieved successfully
# Sereak in Module RX_TOP_MODULE_TB_P8 at TOP_MODULE_TB_P8.v line 94
# Simulation Breakpoint: Break in Module RX_TOP_MODULE_TB_P8 at TOP_MODULE_TB_P8.v line 94
```