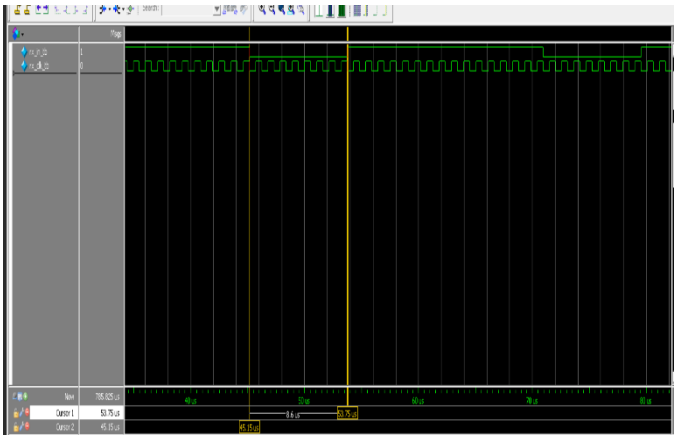
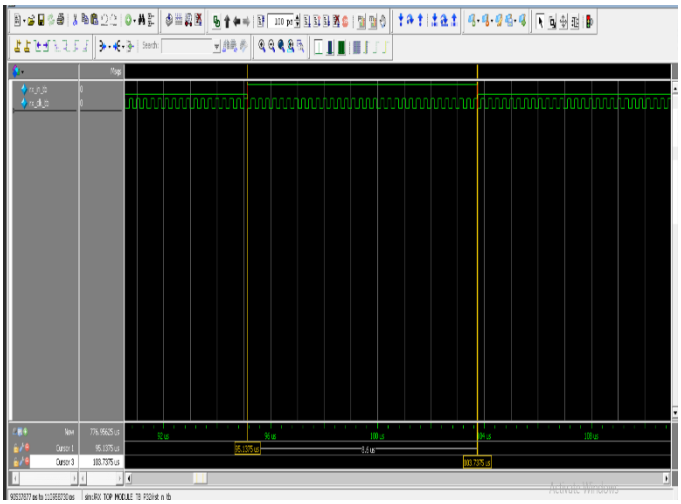
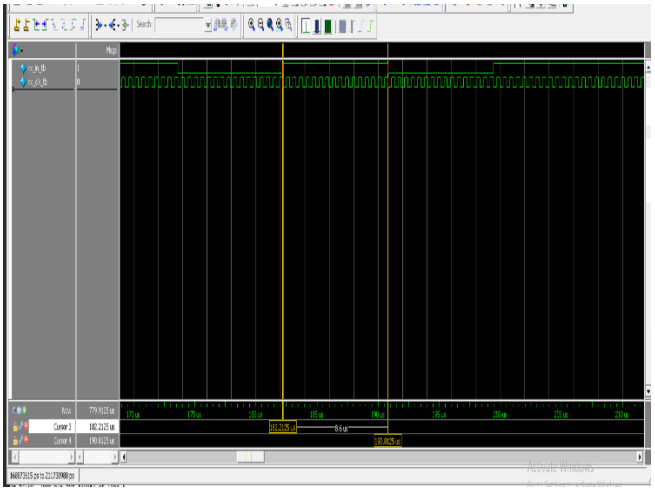
snippet that shows that f_rx is 8 of f_tx



snippet that shows that f_rx is 32 of f_tx

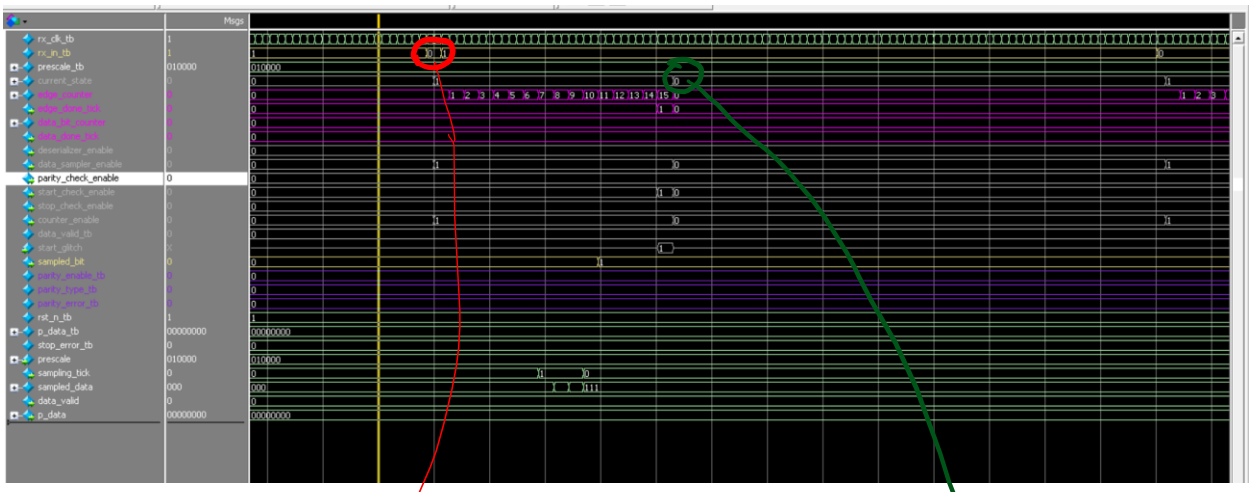


snippet that shows that f_rx is 16 of f_tx



SNIPPETS THAT SHOWS THE WAVE FORM OF THE TEST CASES IN CASE OF PRESCALE EQUALS 16:

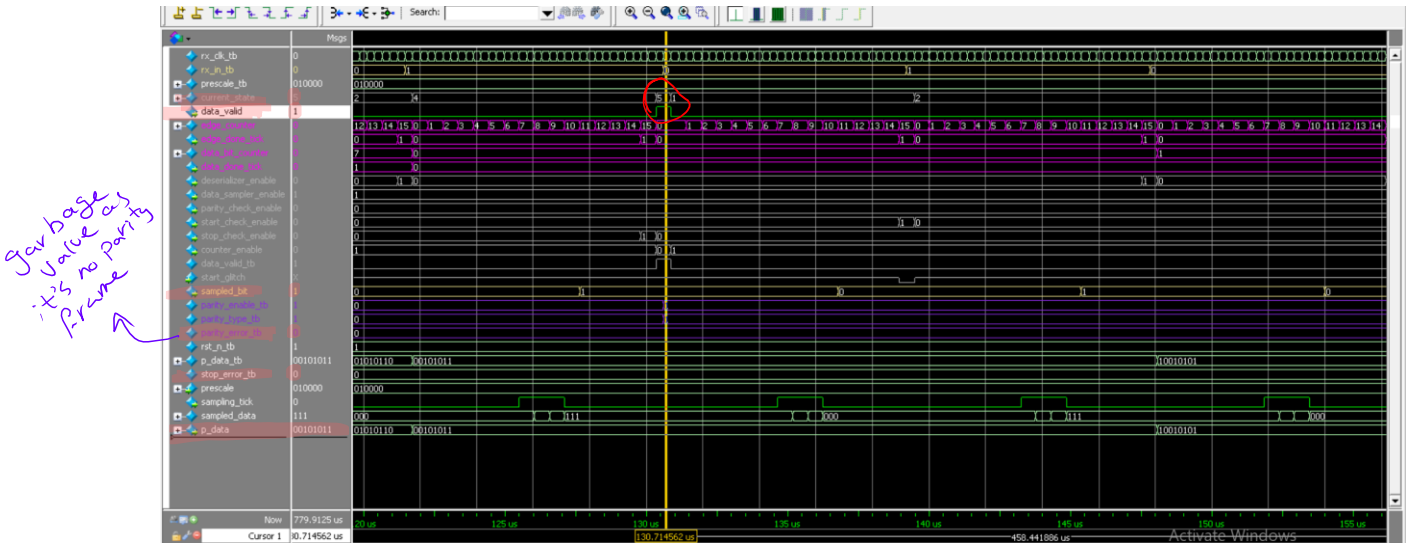
- **GLITCH_STATE (rx_in is zero for a very short time which means it is a glitch)**



glitch happens in rx_in
So the FSM go through start state for 16 edges of rx clk then go back again to idle state

*note: we only look at data valid & parity error & stop error signals in the check error state only as the frame will be completely recieved.

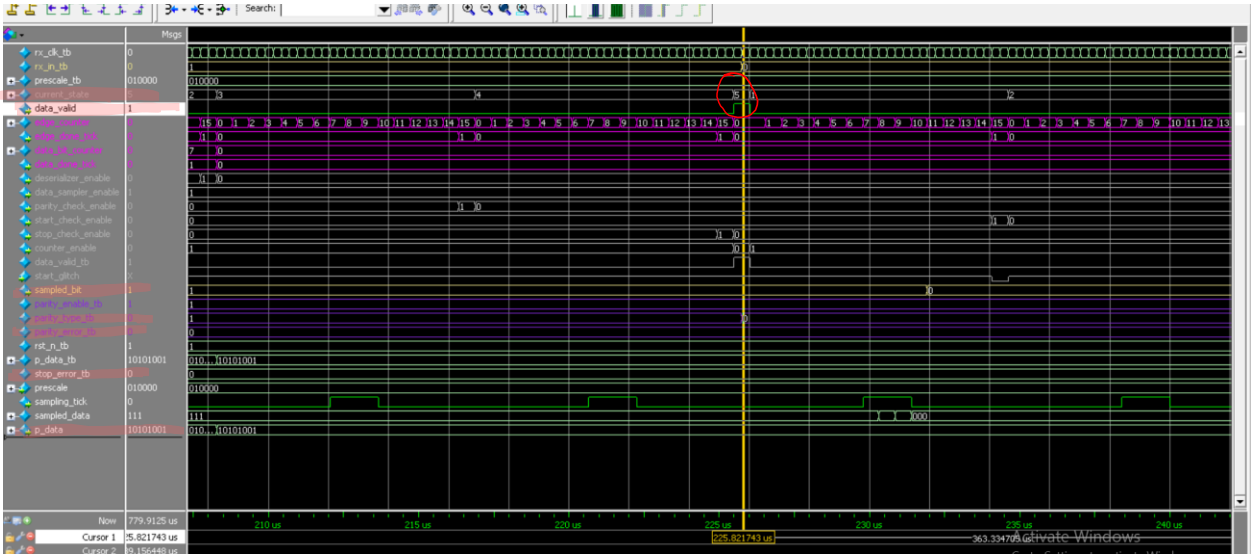
- **frame 1 (without parity bit and stop bit is 1)** `>>110101001`



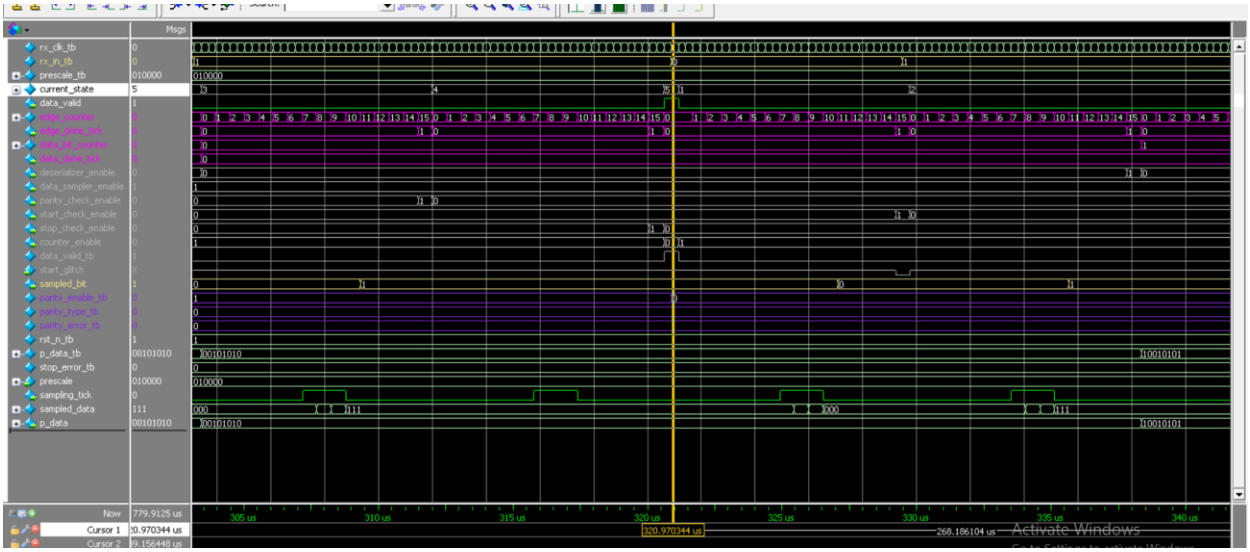
→ after stop state we go through state 5 which is check error state that checks for stop bit and since the frame is recieved correctly then **data valid signal** is high in check error state which means that the frame is correct

- Same thing in all other correct frames.

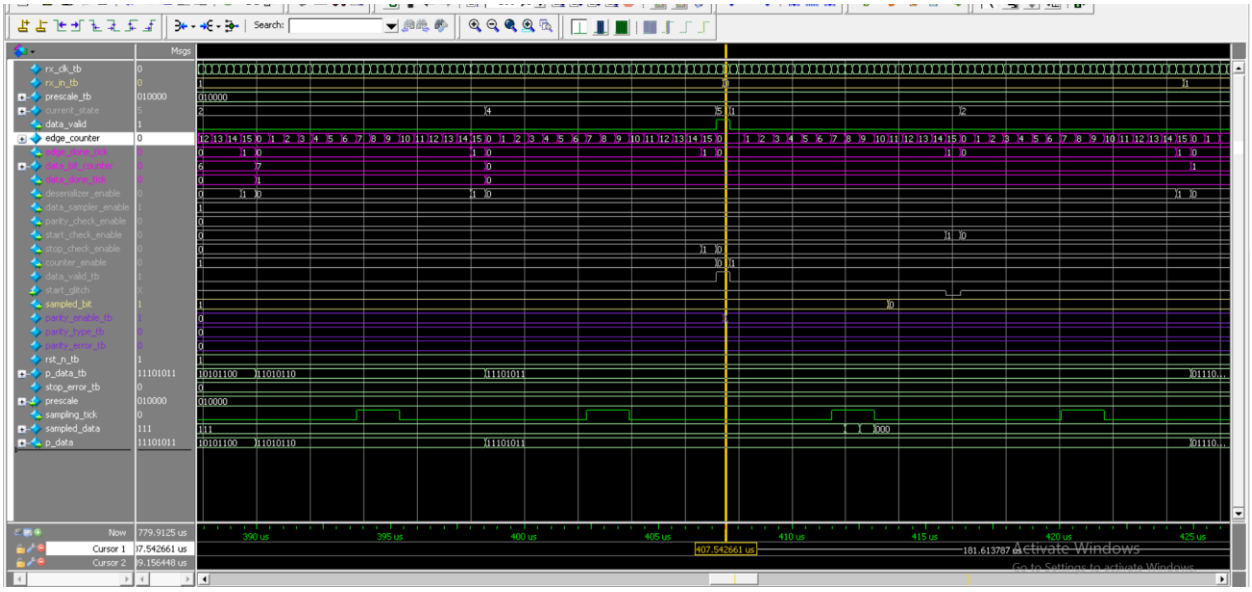
- **frame 2 (with correct odd parity bit and stop bit is 1) >>1001010111**



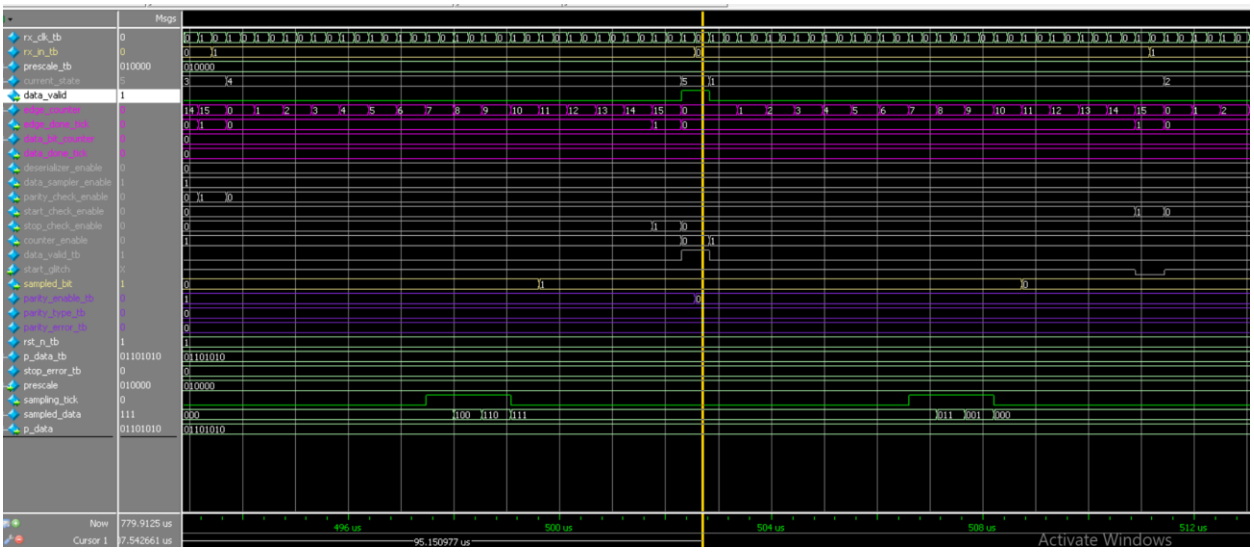
- **frame 3 (with correct even parity bit and stop bit is 1) >>0101010011**



- **frame 4 (without parity bit and stop bit is 1) >>110101111**

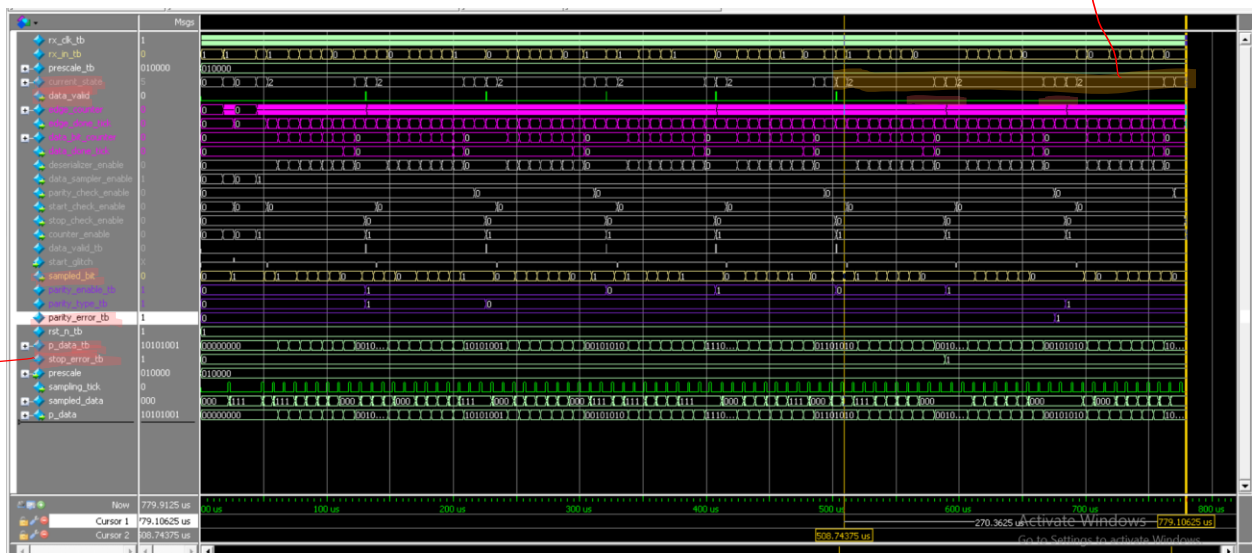


- **frame 5 (with correct even parity bit and stop bit is 1) >>0101011001**



Last three frames are wrong in parity and stop bits in case of parity frames and wrong in stop bit only in case of no parity frame

- frame 6 (without parity bit and stop bit is 0 and parity bit is 0) >>110101000
- frame 7 (with even parity bit and stop bit is 0 and parity bit is 0) >>0101010000
- frame 8 (with odd parity bit and stop bit is 0 and parity bit is 0) >>1001010100



stop error is high in the last 3 frames as well as parity error

So data valid is zero.

- **Log window in case of prescale is 32**

```
# frame is recieved successfully
# frame is recieved successfully
# frame is recieved successfully
# frame is recieved successfully
# frame is recieved successfully
# frame is not recieved successfully
# frame is not recieved successfully
# frame is not recieved successfully
# Break in Module RX_TOP_MODULE_TB_P32 at TOP_MODULE_TB_P32.v line 94
# Simulation Breakpoint: Break in Module RX_TOP_MODULE_TB_P32 at TOP_MODULE_TB_P32.v line 94
```

- **Log window in case of prescale is 16**

```
# frame is recieved successfully
# frame is recieved successfully
# frame is recieved successfully
# frame is recieved successfully
# frame is recieved successfully
# frame is not recieved successfully
# frame is not recieved successfully
# frame is not recieved successfully
# Break in Module RX_TOP_MODULE_TB_P16 at TOP_MODULE_TB_P16.v line 94
# Simulation Breakpoint: Break in Module RX_TOP_MODULE_TB_P16 at TOP_MODULE_TB_P16.v line 94
```

- **Log window in case of prescale is 8**

```
# frame is recieved successfully
# frame is recieved successfully
# frame is recieved successfully
# frame is recieved successfully
# frame is recieved successfully
# frame is not recieved successfully
# frame is not recieved successfully
# frame is not recieved successfully
# Break in Module RX_TOP_MODULE_TB_P8 at TOP_MODULE_TB_P8.v line 94
# Simulation Breakpoint: Break in Module RX_TOP_MODULE_TB_P8 at TOP_MODULE_TB_P8.v line 94
```