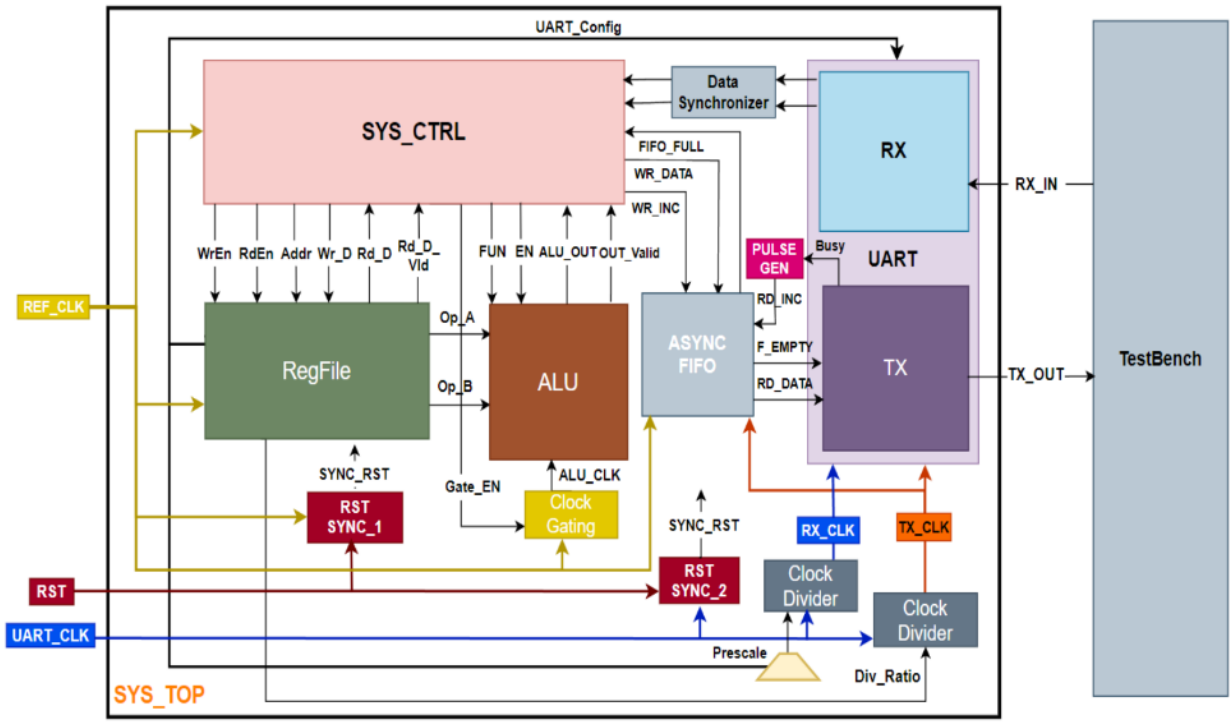
MULTIPLE CLOCK LOW POWER SYSTEM RTL TO GDS

System specs



- **Reserved Registers Description: -**

1) REG0 (Address: 0x0) | ALU Operand A |

2) REG1 (Address: 0x1) | ALU Operand B |

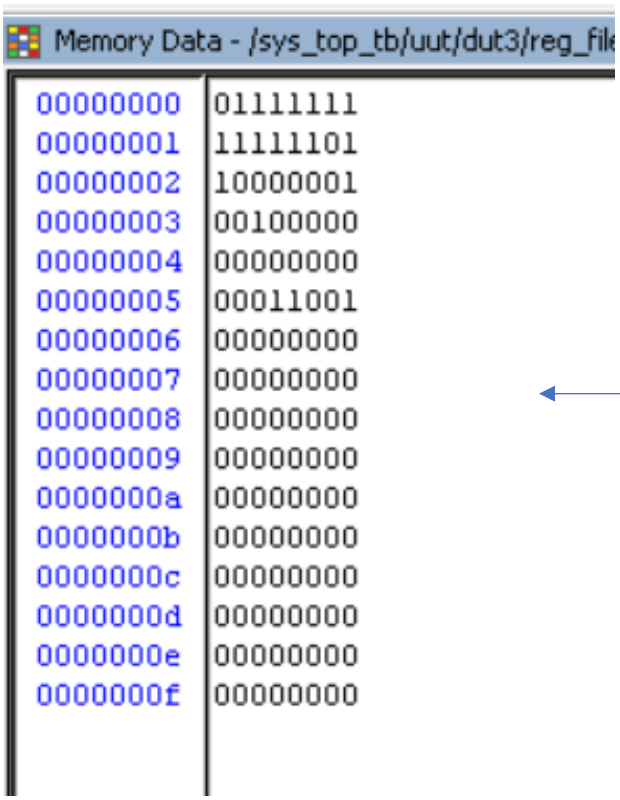
3) REG2 (Address: 0x2) | UART Config |

REG2[0]: Parity Enable
(Default = 1)
REG2[1]: Parity Type
(Default = 0)
REG2[7:2]: Prescale
(Default = 32)

4) REG3 (Address: 0x3) | Div Ratio |

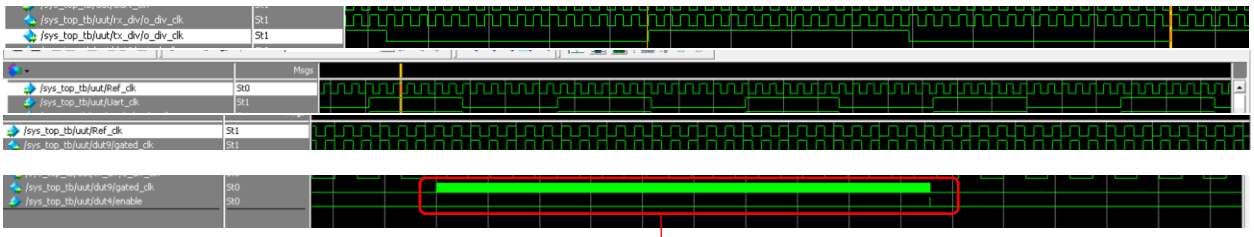
REG3[7:0]: Division ratio
(Default = 32)

Test bench snippets for some of the test cases



Reserved registers data is saved correctly as mentioned in the specs

Clock relations



Gated clk is on when the alu is doing its operation but it is turned on before the alu calulates the result to be stable and ready

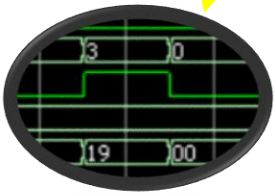
1. Register File Write command (3 frames)

Output of data synchronizer between the uart rx and system control :

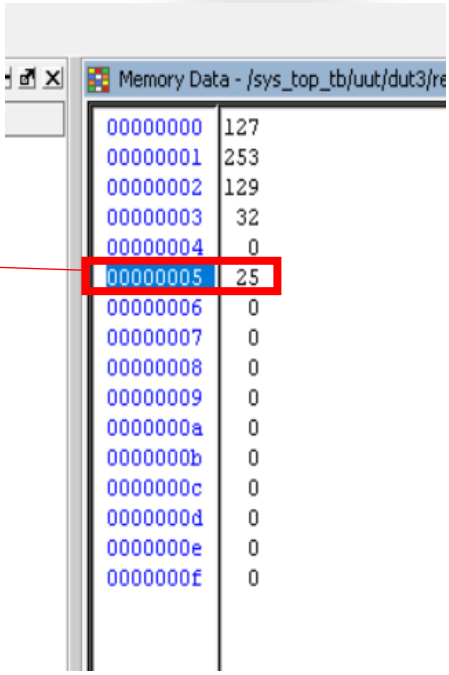
Command code = 0xaa in this state the RF_WR_CMD_FLAG is set to high

write address = 0x05 in this state the address is registered until the write data arrives in the next data

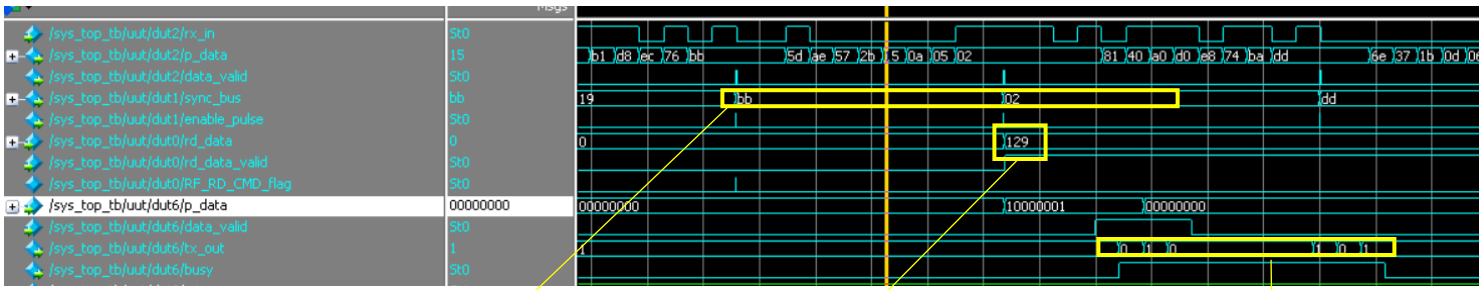
write data = 0x19 (8'd25) in this state the sys_ctrl set the w_en of the reg file to high then stores the data in address 5 in the reg_file



Data is stored in address 5 in reg file as expected



2. Register File Read command (2 frames)

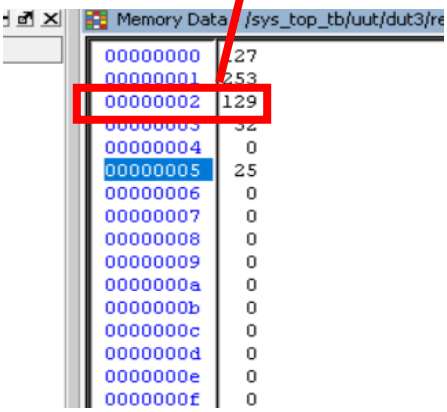


Output of data synchronizer between the uart rx and system control :

Command code = 0xbb in this state the RF_RD_CMD_FLAG is set to high

read address = 0x02

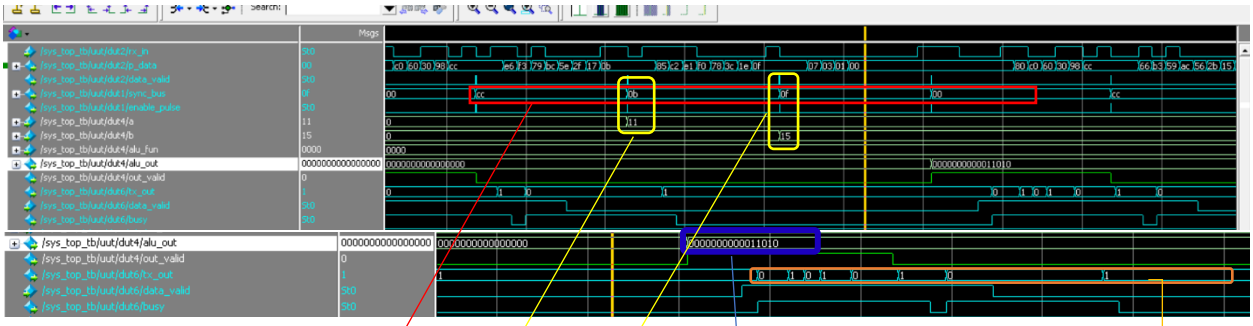
Readed data from the register file is as expected (8'd129)



- ✓ The readed data is then stored in the fifo until the uart tx read it and transmit it as follows :start bit , data bits , even parity bit , stop bit and the busy signal is high as long as the frame is being sent
- ✓ the data valid signal of the tx is set to high when there is any data stored in the fifo

3. ALU Operation command with operand (4 frames)

Frame 3	Frame 2	Frame 1	Frame 0
ALU FUN	Operand B	Operand A	ALU_OPER_W_OP_CMD (0xCC)



Output of data synchronizer between the uart rx and system control :

Command code = 0xcc

Operand a value = 0x0b (stored in address 0 in reg file by default)

Operand b value = 0x0f (stored in address 1 in reg file by default)

Alu_fun value = 0x00 (do addition)

Output of alu is as expected

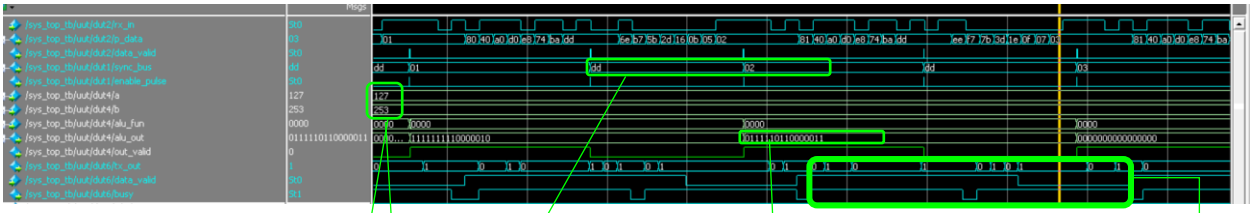
(11 +15 = 25)

- ✓ The output of the alu is 16 bits and the fifo data width is 8 bits so the fifo stores any data comes from the alu in two 8-bits locations then the the uart tx transmits the 8-LSB first in a single frame then transmits the 8-MSB in another single frame (each frame of them has start , data , parity and stop bits)

- ✓ Busy signal is high from the start state to the stop state and then goes low in idle state

4. ALU Operation command with No operand (2 frames)

Frame 1	Frame 0
ALU FUN	ALU_OPER_W_NOP_CMD (0xDD)



Output of data synchronizer between the uart rx and system control :

Command code = 0xdd

Operand a value = this command reads the value stored in address 0 in the reg file which is 8'd127

Operand b value = this command reads the value stored in address 1 in the reg file which is 8'd253

Alu_fun value = 0x02 (do multiply)

Output of alu is as expected

(127*253 = 32131)

- ✓ The output of the alu is 16 bits and the fifo data width is 8 bits so the fifo stores any data comes from the alu in two 8-bits locations then the the uart tx transmits the 8-LSB first in a single frame then transmits the 8-MSB in another single frame (each frame of them has start , data , parity and stop bits)

- ✓ Busy signal is high from the start state to the stop state and then goes low in idle state

synthesis

Worst setup path

```
Operating Conditions: scmetro_tsmc_cl013g_rvt_ss_1p08v_125c   Library: scmetro_tsmc_cl013g_rvt_ss_1p08v_125c
Wire Load Model Mode: top

  Startpoint: dut3/reg_file_reg[1][6]
              (rising edge-triggered flip-flop clocked by Ref_clk)
  Endpoint: dut4/alu_out_reg[0]
            (rising edge-triggered flip-flop clocked by ALU_CLK)
  Path Group: ALU_CLK
  Path Type: max
data arrival time                                                       9.66

clock ALU_CLK (rise edge)                                  10.00       10.00
clock network delay (ideal)                                 0.00       10.00
clock uncertainty                                          -0.20        9.80
dut4/alu_out_reg[0]/CK (DFFRQX1M)                           0.00        9.80 r
library setup time                                         -0.13        9.67
data required time                                                      9.67
--------------------------------------------------------------------------------
data required time                                                      9.67
data arrival time                                                      -9.66
--------------------------------------------------------------------------------
slack (MET)                                                             0.01
```

Worst hold path

```
  Startpoint: dut4/alu_out_reg[8]
              (rising edge-triggered flip-flop clocked by ALU_CLK)
  Endpoint: dut4/alu_out_reg[8]
            (rising edge-triggered flip-flop clocked by ALU_CLK)
  Path Group: ALU_CLK
  Path Type: min

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock ALU_CLK (rise edge)                0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dut4/alu_out_reg[8]/CK (DFFRQX2M)        0.00       0.00 r
  dut4/alu_out_reg[8]/Q (DFFRQX2M)         0.46       0.46 f
  dut4/U123/Y (OAI2B11X2M)                 0.20       0.66 f
  dut4/alu_out_reg[8]/D (DFFRQX2M)         0.00       0.66 f
  data arrival time                                   0.66

  clock ALU_CLK (rise edge)                0.00       0.00
  clock network delay (ideal)              0.00       0.00
  clock uncertainty                        0.10       0.10
  dut4/alu_out_reg[8]/CK (DFFRQX2M)        0.00       0.10 r
  library hold time                       -0.03       0.07
  data required time                                  0.07
  -----------------------------------------------------------
  data required time                                  0.07
  data arrival time                                  -0.66
  -----------------------------------------------------------
  slack (MET)                                         0.59
```

Master and generated clocks

```
 8
 9 Attributes:
10     d - dont_touch_network
11     f - fix_hold
12     p - propagated_clock
13     G - generated_clock
14     g - lib_generated_clock
15
16 Clock          Period   Waveform            Attrs     Sources
17 ---------------------------------------------------------------------------
18 ALU_CLK         10.00   {0 5}               G         {dut9/gated_clk}
19 Ref_clk         10.00   {0 5}                         {Ref_clk}
20 UART_CLK       271.00   {0 135}                       {Uart_clk}
21 UART_RX_CLK    271.00   {0 135}             G         {rx_div/o_div_clk}
22 UART_TX_CLK   8672.00   {0 4336}            G         {tx_div/o_div_clk}
23 ---------------------------------------------------------------------------
24
25 Generated     Master         Generated      Master         Waveform
26 Clock         Source         Source         Clock          Modification
27 ---------------------------------------------------------------------------
28 ALU_CLK       Ref_clk        {dut9/gated_clk}
29                                             Ref_clk        divide_by(1)
30 UART_RX_CLK   Uart_clk       {rx_div/o_div_clk}
31                                             UART_CLK       divide_by(1)
32 UART_TX_CLK   Uart_clk       {tx_div/o_div_clk}
33                                             UART_CLK       divide_by(32)
34 ---------------------------------------------------------------------------
35 1
```

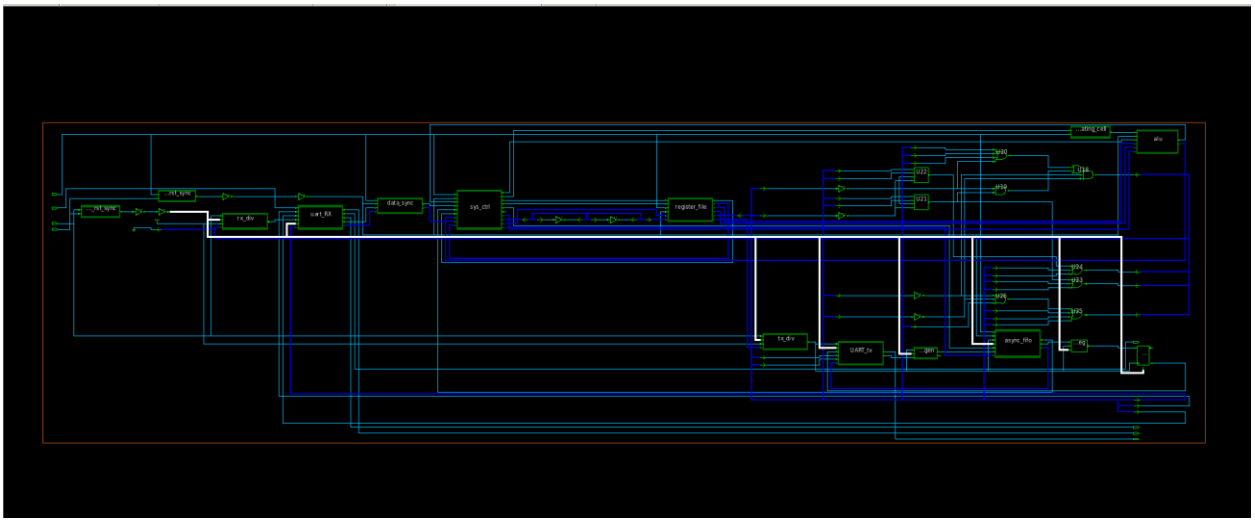
Total area

```
 5
 6 Number of ports:                          745
 7 Number of nets:                          2814
 8 Number of cells:                         2027
 9 Number of combinational cells:           1563
10 Number of sequential cells:               423
11 Number of macros/black boxes:               0
12 Number of buf/inv:                        286
13 Number of references:                      24
14
15 Combinational area:              15683.057873
16 Buf/Inv area:                     1139.045623
17 Noncombinational area:           10699.732988
18 Macro/Black Box area:                0.000000
19 Net Interconnect area:      undefined  (No wire load specified)
20
21 Total cell area:                 26382.790861
```

Total power

```
4 ---------------------------------------------------------------------------
5                                    Switch   Int      Leak     Total
6 Hierarchy                          Power    Power    Power    Power
7 ---------------------------------------------------------------------------
8 sys_top                            1.37e-02    0.493 1.63e+07    0.524
```

Synthesis gate level netlist snippets



Post synthesis formality

```
****************************** Verification Results ******************************
Verification SUCCEEDED
```

```
****************************************

This design has no violated constraints.

1
```

```
********************************

No aborted compare points.

1
```

```
****************************************

No failing compare points.

1
```

```
****************************************

No unverified compare points.

1
```

```
************************************************

413 Passing compare points:
```

DFT

Calculate number of chains

```
1
################################################################################
# DFT Preparation Section
################################################################################
set flops_per_chain 100
100
set num_flops [sizeof_collection [all_registers -edge_triggered]]
409
set num_chains [expr $num_flops / $flops_per_chain + 1 ]
5
################################################################################
```

Worst setup path

```
3 Wire Load Model Mode: top
4
5   Startpoint: alu/alu_out_reg[1]
6               (rising edge-triggered flip-flop clocked by ALU_CLK)
7   Endpoint: alu/alu_out_reg[1]
8             (rising edge-triggered flip-flop clocked by ALU_CLK)
9   Path Group: ALU_CLK
0   Path Type: max
1
2   Point                                   Incr       Path
3   -----------------------------------------------------------
4   clock ALU_CLK (rise edge)               0.00       0.00
5   clock network delay (ideal)             0.00       0.00
6   alu/alu_out_reg[1]/CK (SDFFRQX2M)       0.00       0.00 r
7   alu/alu_out_reg[1]/Q (SDFFRQX2M)        0.43       0.43 f
8   alu/U88/Y (AOI222X1M)                   0.26       0.69 r
9   alu/U49/Y (NAND4X2M)                    0.14       0.84 f
0   alu/alu_out_reg[1]/D (SDFFRQX2M)        0.00       0.84 f
1   data arrival time                                  0.84
2
3   clock ALU_CLK (rise edge)              10.00      10.00
4   clock network delay (ideal)             0.00      10.00
5   clock uncertainty                      -0.20       9.80
6   alu/alu_out_reg[1]/CK (SDFFRQX2M)       0.00       9.80 r
7   library setup time                     -0.43       9.37
8   data required time                                 9.37
9   -----------------------------------------------------------
0   data required time                                 9.37
1   data arrival time                                 -0.84
2   -----------------------------------------------------------
3   slack (MET)                                        8.54
4
```

Worst hold path

```
Wire Load Model Mode: top

  Startpoint: alu/alu_out_reg[6]
              (rising edge-triggered flip-flop clocked by ALU_CLK)
  Endpoint: alu/alu_out_reg[7]
            (rising edge-triggered flip-flop clocked by ALU_CLK)
  Path Group: ALU_CLK
  Path Type: min

  Point                                     Incr       Path
  -----------------------------------------------------------
  clock ALU_CLK (rise edge)                 0.00       0.00
  clock network delay (ideal)               0.00       0.00
  alu/alu_out_reg[6]/CK (SDFFRQX2M)         0.00       0.00 r
  alu/alu_out_reg[6]/Q (SDFFRQX2M)          0.37       0.37 r
  alu/alu_out_reg[7]/SI (SDFFRQX2M)         0.00       0.37 r
  data arrival time                                    0.37

  clock ALU_CLK (rise edge)                 0.00       0.00
  clock network delay (ideal)               0.00       0.00
  clock uncertainty                         0.10       0.10
  alu/alu_out_reg[7]/CK (SDFFRQX2M)         0.00       0.10 r
  library hold time                        -0.18      -0.08
  data required time                                  -0.08
  -----------------------------------------------------------
  data required time                                  -0.08
  data arrival time                                   -0.37
  -----------------------------------------------------------
  slack (MET)                                          0.45

```

Master and generated clocks

```

Clock          Period   Waveform            Attrs     Sources
------------------------------------------------------------------------------
ALU_CLK         10.00   {0 5}               G         {clock_gating_cell/gated_clk}
REF_CLK         10.00   {0 5}                         {Ref_clk}
SCAN_CLK       100.00   {0 50}                        {SCAN_CLK}
UART_CLK       271.00   {0 135}                       {Uart_clk}
UART_RX_CLK    271.00   {0 135}             G         {rx_div/o_div_clk}
UART_TX_CLK   8672.00   {0 4336}            G         {tx_div/o_div_clk}
------------------------------------------------------------------------------

Generated     Master         Generated      Master         Waveform
Clock         Source         Source         Clock          Modification
------------------------------------------------------------------------------
ALU_CLK       Ref_clk        {clock_gating_cell/gated_clk}
                                            REF_CLK        divide_by(1)
UART_RX_CLK   Uart_clk       {rx_div/o_div_clk}
                                            UART_CLK       divide_by(1)
UART_TX_CLK   Uart_clk       {tx_div/o_div_clk}
                                            UART_CLK       divide_by(32)
------------------------------------------------------------------------------
1
```

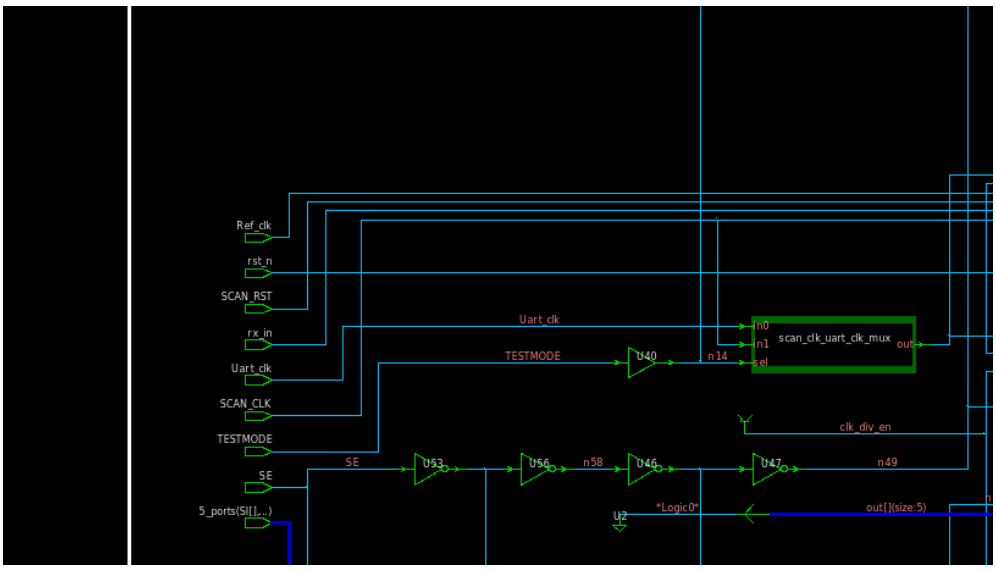
Total area

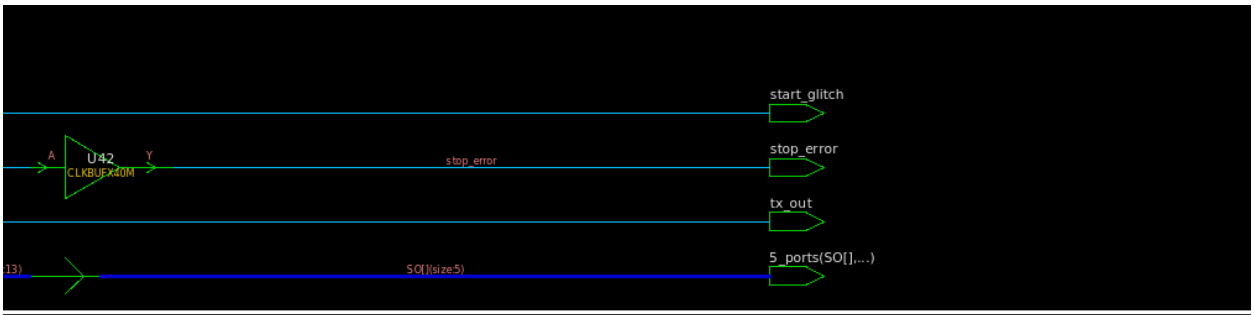
```
14     scmetro_tsmc_cl013g_rvt_ss_1p08v_125c (File: /home/IC/FINAL_PROJ
15
16 Number of ports:                          877
17 Number of nets:                         2910
18 Number of cells:                        2012
19 Number of combinational cells:          1543
20 Number of sequential cells:              421
21 Number of macros/black boxes:              0
22 Number of buf/inv:                       300
23 Number of references:                     35
24
25 Combinational area:              14725.224061
26 Buf/Inv area:                     1227.298124
27 Noncombinational area:           13537.933994
28 Macro/Black Box area:               0.000000
29 Net Interconnect area:      undefined  (No wire load specified)
30
31 Total cell area:                 28263.158055
```

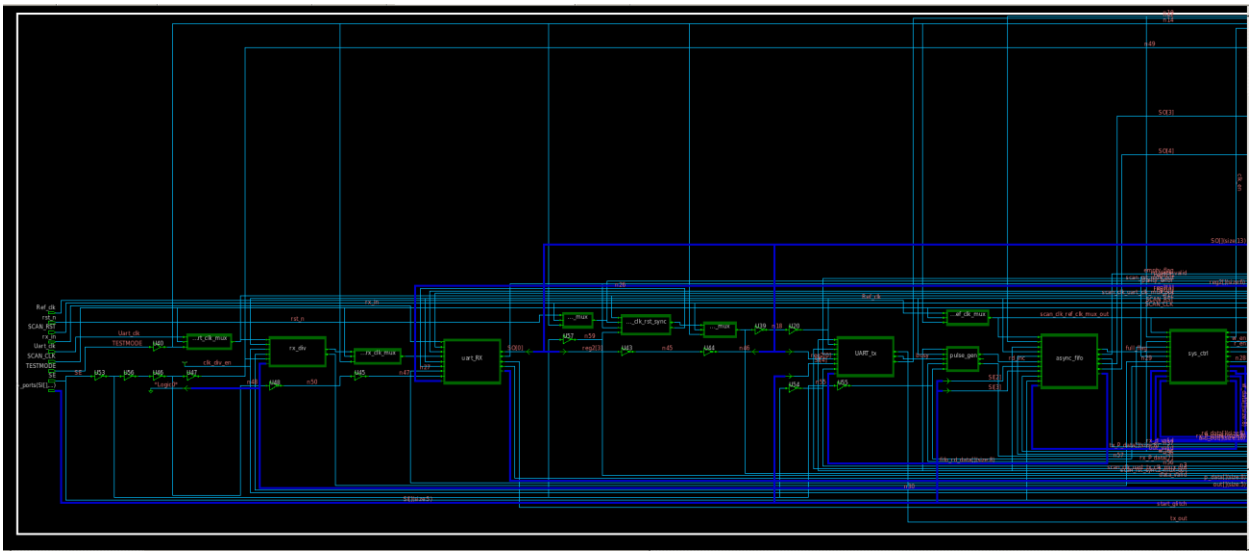
Total power

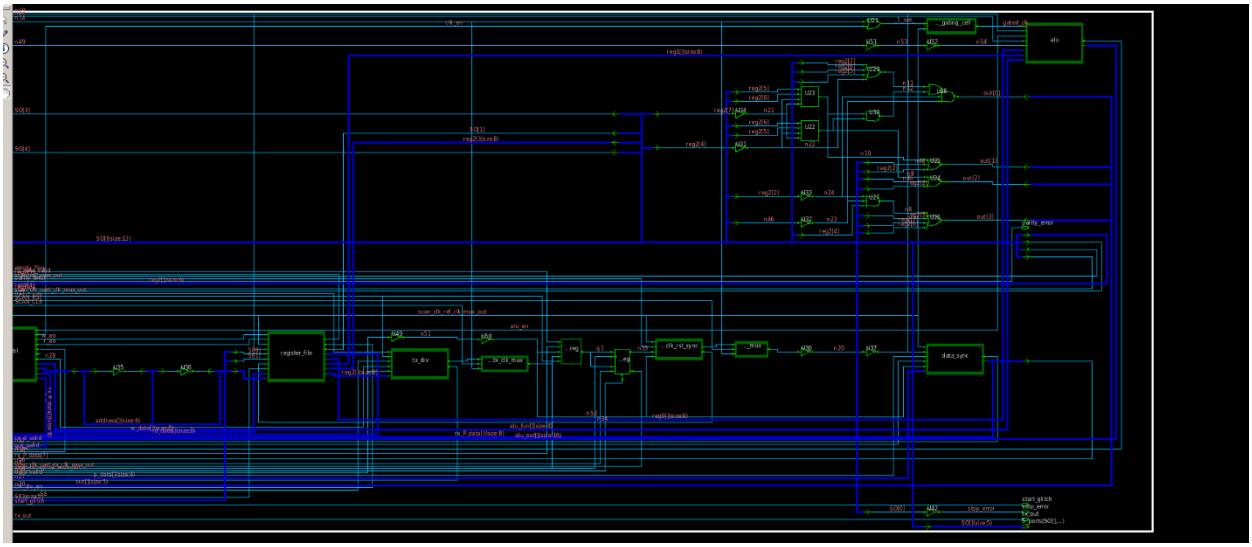
```
3 ----------------------------------------------------------------------------------
4                                      Switch   Int      Leak     Total
5 Hierarchy                            Power    Power    Power    Power    %
6 ----------------------------------------------------------------------------------
7 system_TOP                           3.75e-02    0.150 1.65e+07    0.204 100.0
```

DFT gate level netlist snippets




start_glitch
stop_error
tx_out
5_ports(SO[],...)
A
U42
CLKBUFX40M
Y
stop_error
SO[](size:5)





Scan chain distribution

```
9
0 Number of chains: 5
1 Scan methodology: full_scan
2 Scan style: multiplexed_flip_flop
3 Clock domain: no_mix
4
5 Chain      Scan Ports (si --> so)        # of Cells   Inst/Chain               Clock (port, time, edge)
6 -----      ----------------------        ----------   ----------               ------------------------
7 S 1        SI[4] -->  SO[4]                     82   UART_tx/uut0/current_state_reg[0]
8                             (SCAN_CLK, 30.0, rising)
9 S 2        SI[3] -->  SO[3]                     82   async_fifo/dut2/fifo_reg[5][1]
0                             (SCAN_CLK, 30.0, rising)
1 S 3        SI[2] -->  SO[2]                     82   async_fifo/dut2/fifo_reg[15][3]
2                             (SCAN_CLK, 30.0, rising)
3 S 4        SI[1] -->  SO[1]                     82   register_file/reg_file_reg[2][4]
4                             (SCAN_CLK, 30.0, rising)
5 S 5        SI[0] -->  SO[0]                     81   register_file/reg_file_reg[12][6]
6                             (SCAN_CLK, 30.0, rising)
7 1
```

Coverage percentage

```
    Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class                     code   #faults
------------------------------  ----  ---------
Detected                         DT      16829
Possibly detected                PT          0
Undetectable                     UD         86
ATPG untestable                  AU         70
Not detected                     ND         21
-----------------------------------------------
total faults                             17006
test coverage                            99.46%
-----------------------------------------------
 Information: The test coverage above may be inferior
              than the real test coverage with customized
              protocol and test simulation library.
1
```

Post dft formality

```
********************************** Verification Results **********************************
Verification SUCCEEDED
```

```
 8 ****************************************      3 ************************************************
 9                                                 9
10 This design has no violated constraints.       0 No aborted compare points.
11                                                1
12 1                                              2 1
```

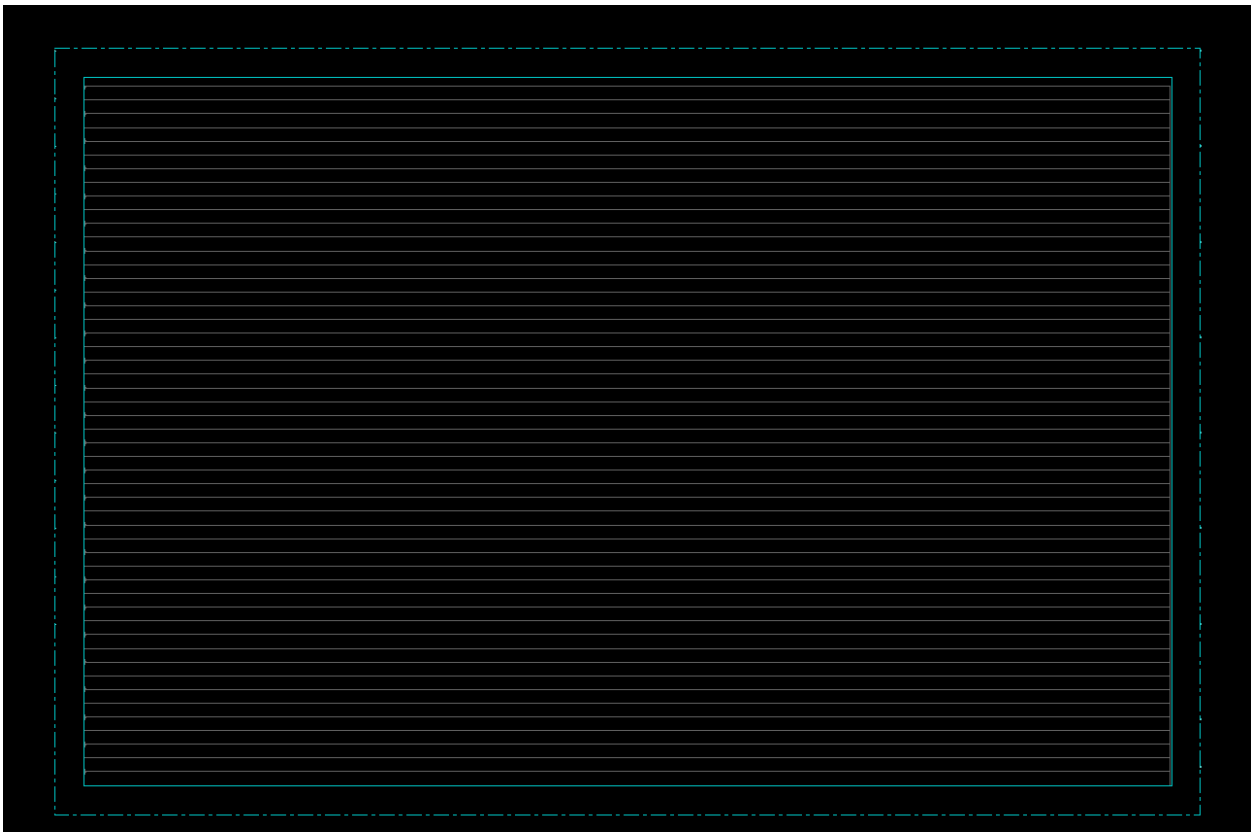
```
 7 Date           : Thu Aug 29 00:38:41 2024
 8 ************************************************
 9
10 No failing compare points.
11
12 1
```

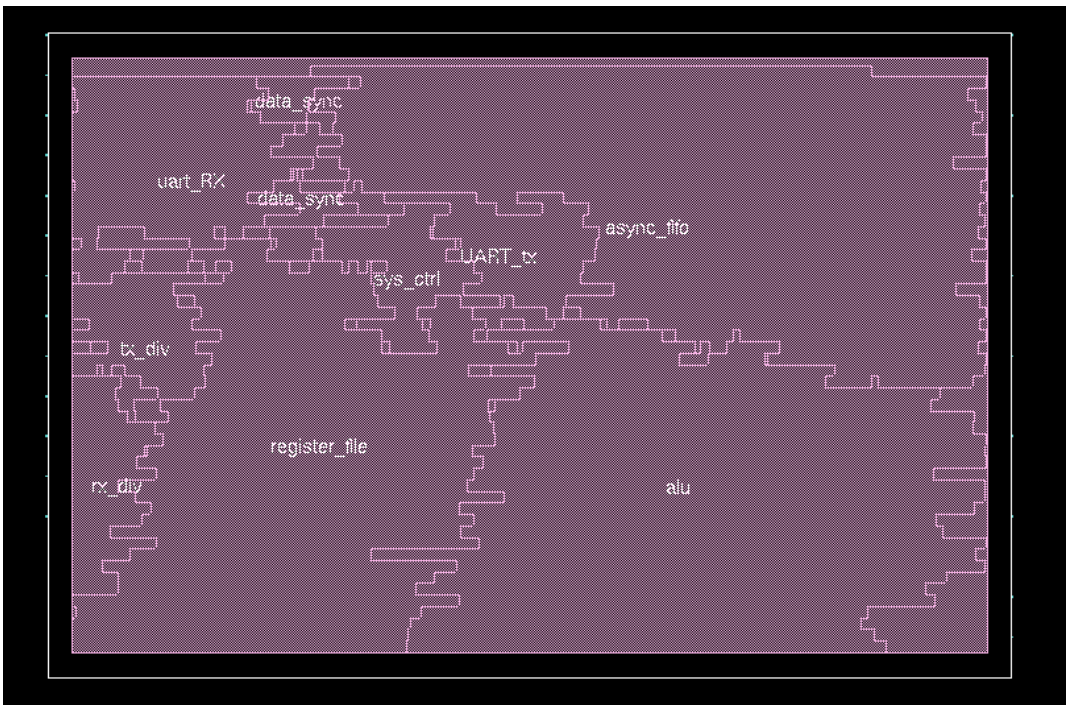
```
7 Date           : Thu Aug 29 00:38:41 2024
8 ************************************************
9
0 No unverified compare points.
1
2 1
```

```
************************************************

413 Passing compare points:

Date           : Thu Aug 29 00:38:41 2024
************************************************

No failing compare points.

1
```

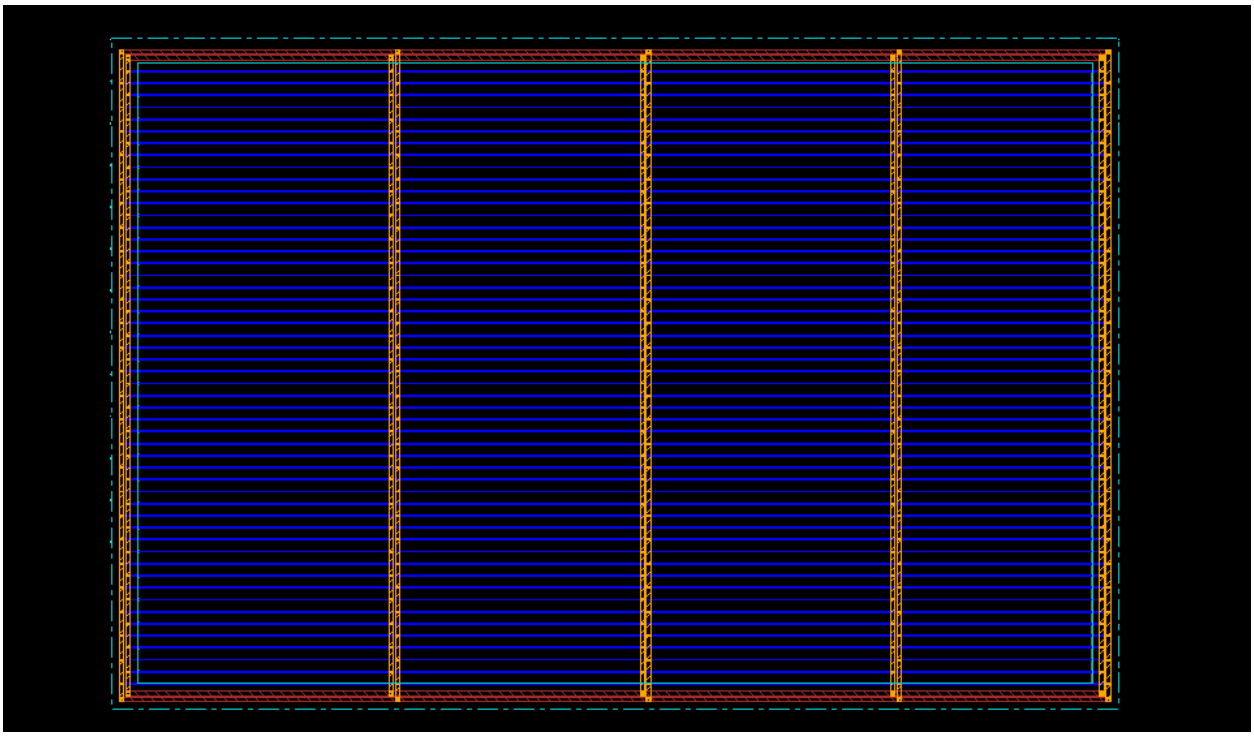
PNR

Floor planning

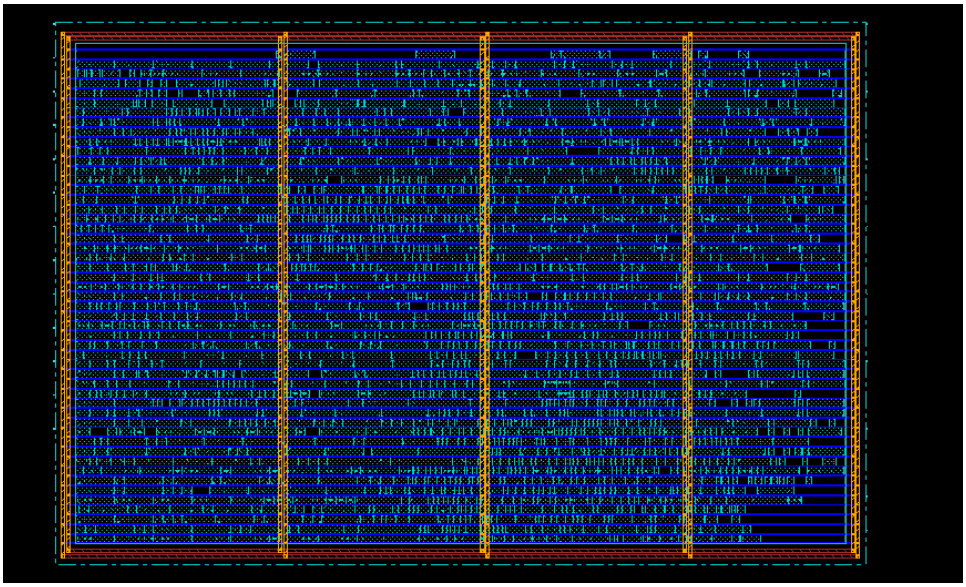




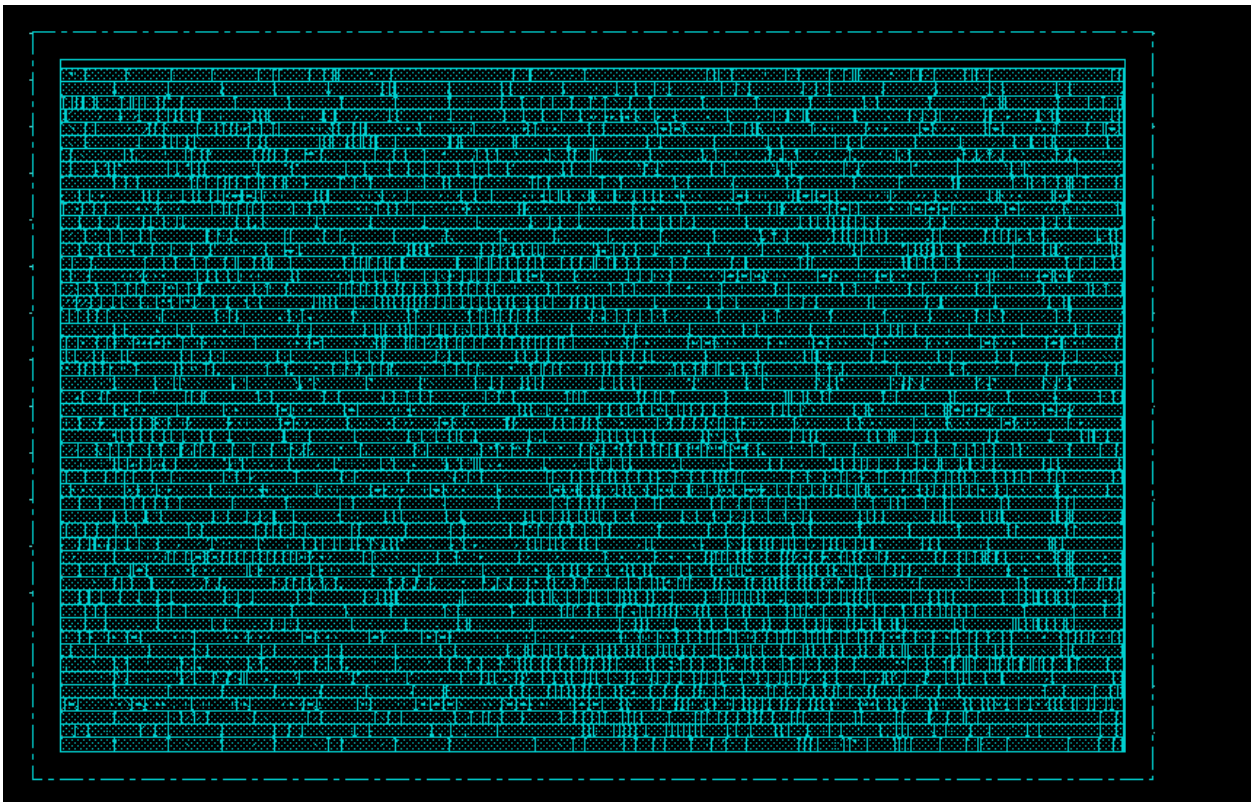
Power planning



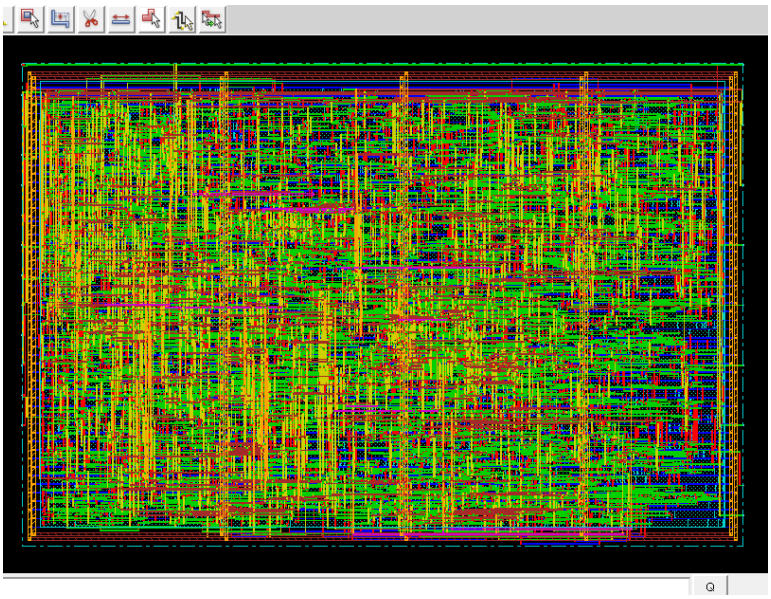
Placement



Add filler cells



Routing (post route)



Check connectivity

```
End Time: Wed Aug 28 22:08:05 2024
******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.1  MEM: 0.000M)
```

Check geometry

```
Verification Complete : 0 Viols.  0 Wrngs.

********End: VERIFY GEOMETRY**********
```

Check if there are any gaps after adding filler cells

```
O: Total number of gaps found: 0
```

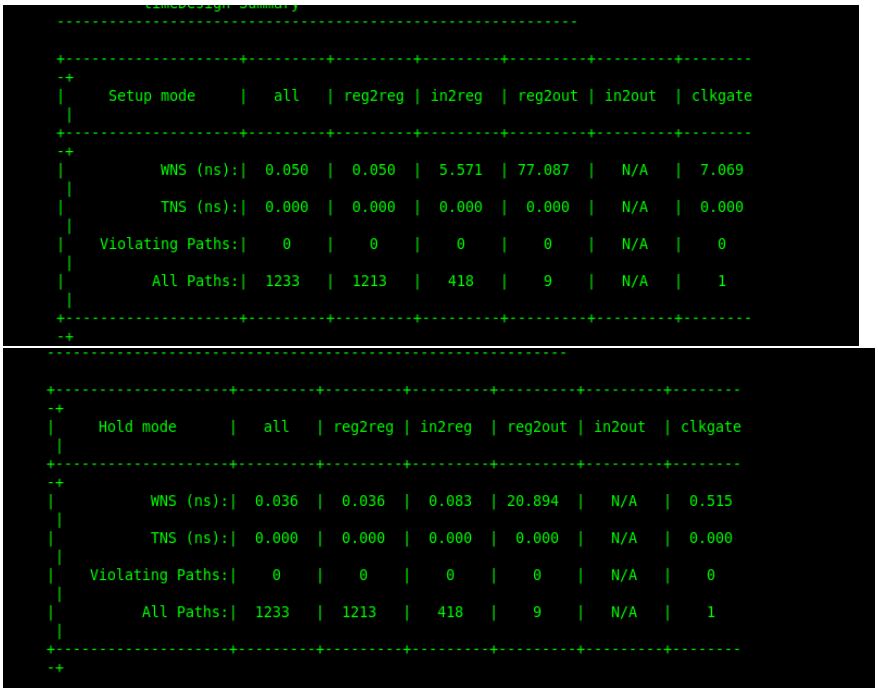
Check drc violations

```
#               24401
#
#Total number of DRC violations = 0
#Total number of net violated process antenna rule = 0
#Total number of violations on LAYER METAL1 = 0
#Total number of violations on LAYER METAL2 = 0
#Total number of violations on LAYER METAL3 = 0
#Total number of violations on LAYER METAL4 = 0
#Total number of violations on LAYER METAL5 = 0
#Total number of violations on LAYER METAL6 = 0
#Total number of violations on LAYER METAL7 = 0
#
```

Check process antenna

```
******* START VERIFY ANTENNA ********
Report File: system_TOP.antenna.rpt
LEF Macro File: system_TOP.antenna.lef
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
```

Setup and hold timing analysis (post route)



Setup mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.050	0.050	5.571	77.087	N/A	7.069
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1233	1213	418	9	N/A	1

Hold mode	all	reg2reg	in2reg	reg2out	in2out	clkgate
WNS (ns):	0.036	0.036	0.083	20.894	N/A	0.515
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1233	1213	418	9	N/A	1

- **Link for the rtl code of the system and all backend scripts and files : github link**
- **Link for the rtl code and functional verification of each block :github link**