Lecture Notes 2: PLD

Contents

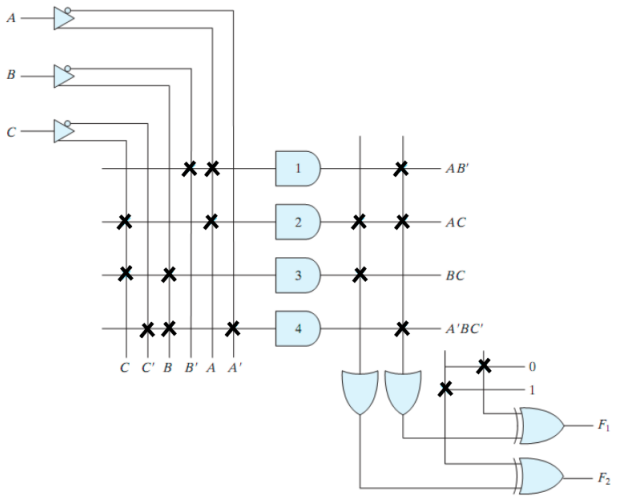
1 Overview

PLD stands for Programmable Logic Device, and it can be classified into:

- **ROM:**
  - Consists of OR gates and a decoder
  - Programmable OR gates and fixed AND gates
  - if I have n inputs, then I need 2^n AND gates
  - OR gates are programmed using fuses.
- **PLA (Programmable Logic Array):**
  - Programmable AND gates
  - Programmable OR gates (using fues)
  - Slower compared to PAL
- **PAL (Programmable Array Logic):**
  - Programmable AND gates
  - Fixed OR gates
- **FPGA (Field Programmable Gate Array)**

2 Implement using PLA

$f_1 = AB' + AC + A'BC'$
$f_2 = (AC + AB)'$



Using XOR at the end to allow a complement output

3 PAL

3.1 PAL chips

Examples

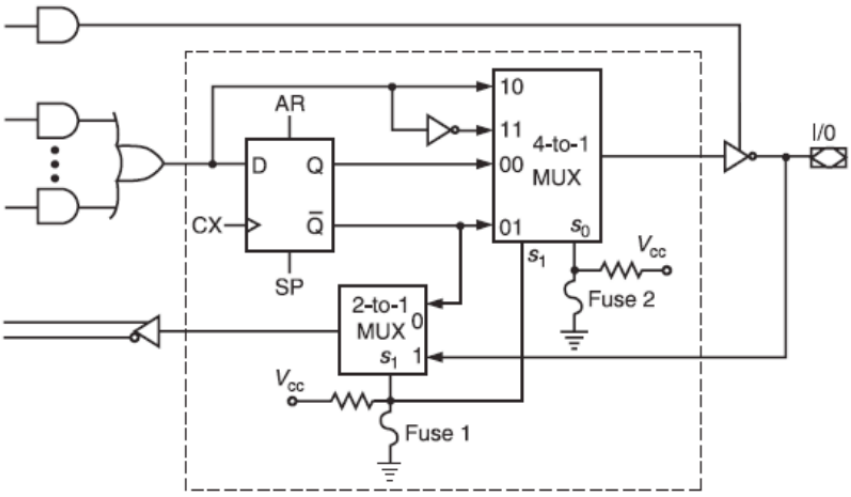
- **16L8:**
  - up to 16 inputs
  - up to 8 outputs
  - active low
- **16H8:** active high
- **16R8:** uses register
- **16A8:** arithmetic (uses XOR)

Note 1

16 and 8 aren't constants, they are just used as examples

3.2 GAL chips

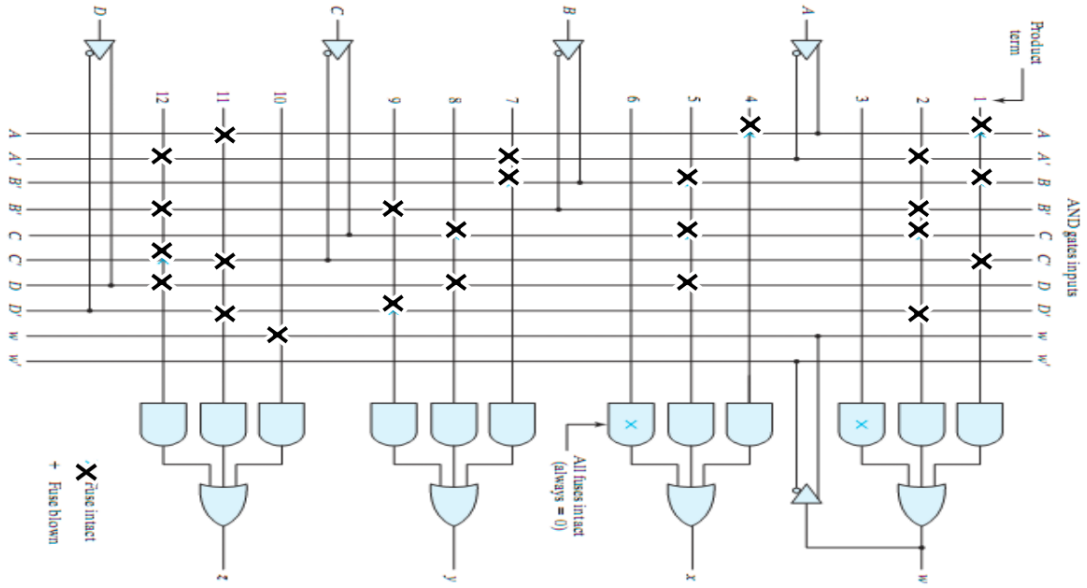
GAL (Generic Array Logic): It contains a macro-cell, which allows you to control whether your PAL should act as (L),(H),(R),(A)



- **To act as R:** using the D flip-flop
- **To act as L or H:** using (10), (11) in the 4 to 1 MUX
- **The 2 to 1 MUX**: To allow a feedback from the function, or to use the output as an input

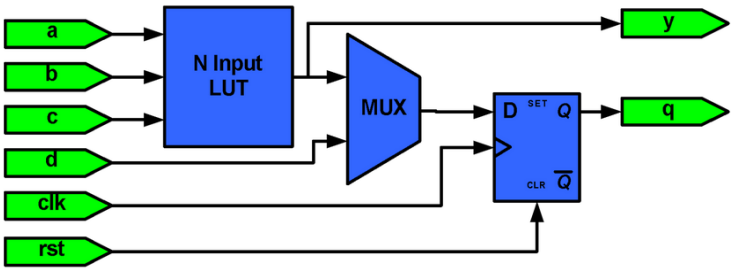
3.3 Implement using PAL

$W = ABC' + A'B'CD'$
$X = A + BCD$
$Y = A'B + CD + B'D'$
$Z = W + AC'D' + A'B'C'D$



4 FPGA

- **CLB (Configurable Logic Block):** Implement combinatorial and sequential logic Based on LUT and DFF

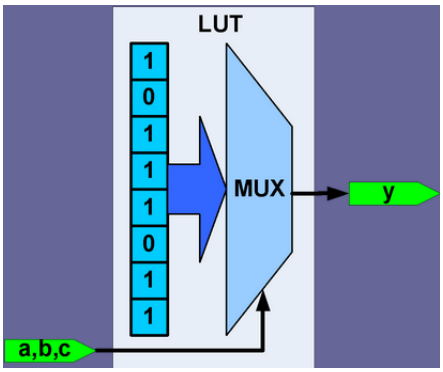


- **Programmable I/O blocks (IOB):**
  - Configurable I/Os for external connections.
  - Supports various voltages and tri-states
- **Programmable Interconnects**

- Switches
- Horizontal/vertical lines
- allow logic blocks to be connected to each other and to the I/O pins

LUT

LUT: A ram with width of 1 bit



- **Block of bits entering the MUX:**It's a register that contains the truth table of each function
- **Number of functions:** It can represent 2^n functions, where n is the number of bits in each register.