A 212.5 Gbps-PAM4 Chip-to-Module Channel for "Universal Port" and Its Characteristics: Design B

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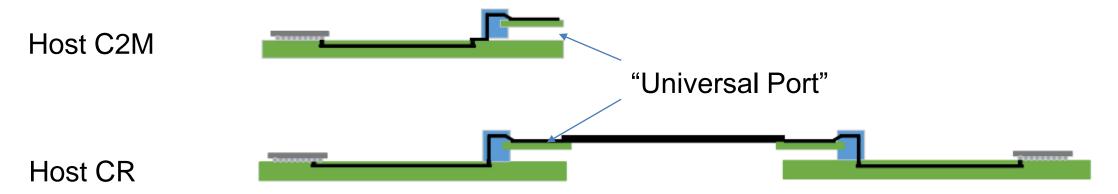
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Background and Introduction (I)

• An important and common Chip-to-Module (C2M) Channel is the so-called "Universal Port" C2M, as shown in the following diagram



• The loss of the C2M channel (TPO-TP1A) budge is determined/bounded by the bump-to-bump, ref PKG, and DAC loss budget, which are trending <=40 dB, ~6 dB, and ~16 dB for 212.5 Gbps-PAM4 signaling.

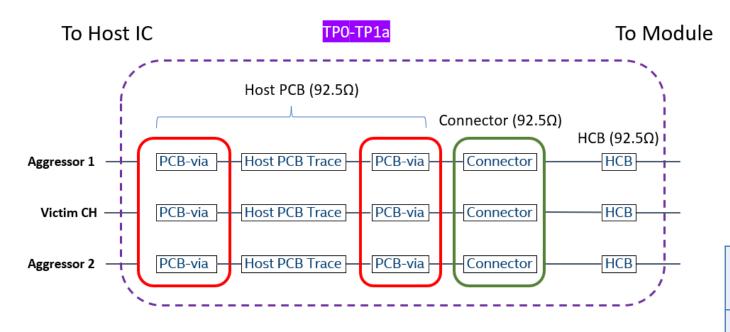
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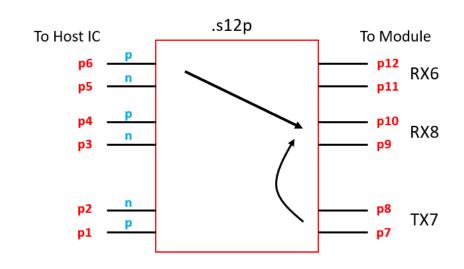
Background and Introduction (II)

• We leveraged our established/validated C2M channel design tool-flow-methodology (TFM) (e.g., oif2022.355.00, oif2022.498.00, oif2023.032.00) to create this C2M channel design B to support 212.5 Gbps-PAM4 "Universal Port".



C2M Channel Design B for "Universal Port"





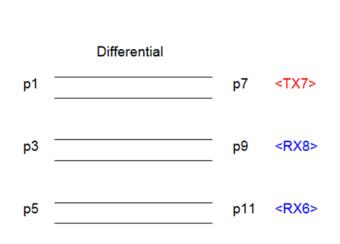
Component	Insertion Loss TP0-TP1a (dB) @ 53.125GHz
	Design B
Host PCB via	0.75 dB
Host PCB Trace	3.75 inch (1.27 dB/inch)
Connector	2.10 dB
НСВ	3.42 dB
Total *	11.6 dB

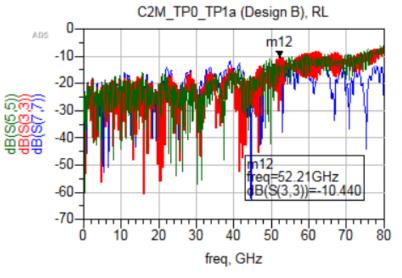
^{*} Not lineally added

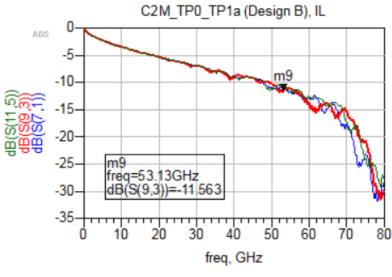


P802.3dj June 2023 4

C2M Channel Design B Characteristics (I)

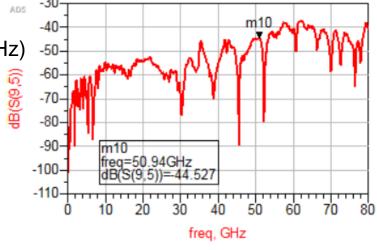




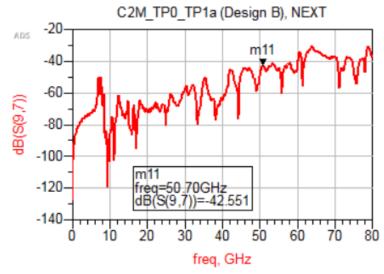


TP0-TP1a Characteristics (DC-53.125GHz)

- IL: 11.56dB @ 53.125GHz
- RL < ~10.4dB (<53.125GHz)
- FEXT < 44.5dB (<53.125GHz)
- NEXT < 42.5dB (<53.125GHz)

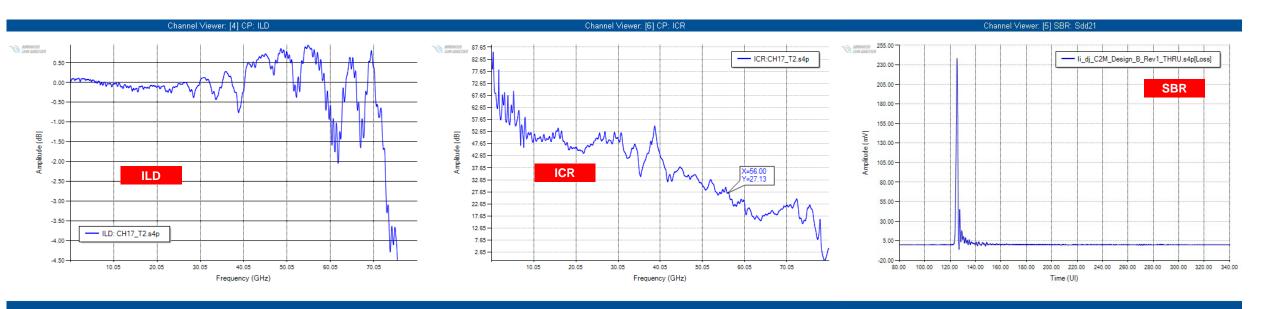


C2M TP0 TP1a (Design B), FEXT





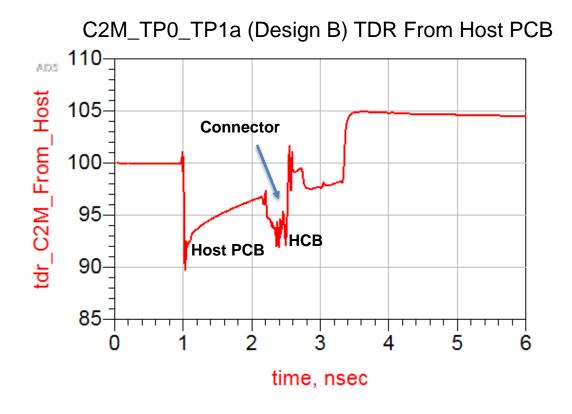
C2M Channel Design B Characteristics (II)

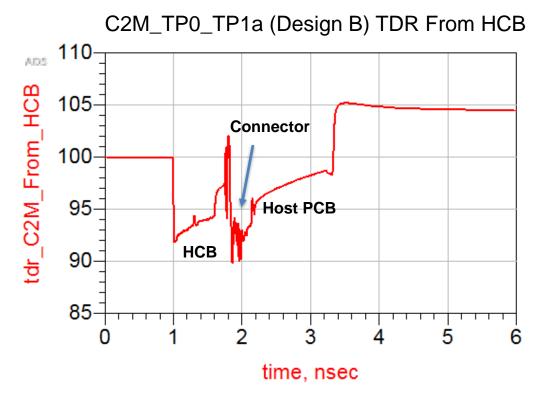


- ILD < +- 1 dB (<53.125 GHz)
- ICR > 27.13 dB (<53.125 GHz)



C2M Channel Design B Characteristics (III)





[S] parameter BW DC-80GHz



Summary

- We have created a C2M channel Design B supporting "Universal Port" at 212.5 Gbps-PAM4
- This C2M channel includes PCB-Via, PCB, connector, and HCB
- This C2M channel has:
 - An IL (TP0-TP1A) of ~11.6 dB at 53.125 GHz
 - $RL <^{\sim} 10.4 dB at <= 53.125 GHz$
 - FEXT < 44.5dB, NEXT < 42.5dB, at <= 53.125 GHz</p>
 - PCB IL of 4.8 dB/reach of 3.75 inch (with 1.27 dB/inch) at 53.125 GHz

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