ELEC 204 Digital System Design
Laboratory Manual

Experiment #2
Introduction to Logic Circuits: 4-bit Comparator

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1 Objectives

The purpose of this experiment is to make you familiar with the elementary logic gates while designing 4-bit comparator circuits for unsigned and 2's complement systems. During the laboratory session, you will be referring to combinational logic design and optimization methodologies.

You will design your circuit using Xilinx ISE software as performed in the first experiment. Then you will simulate your circuit behavior and deploy your design to the Prometheus board.

2 Equipment & Software

- IBM compatible PC with Windows operating system,
- Xilinx ISE v14.7 & Prometheus software packages,
- Prometheus FPGA board,
- USB cable for programming.

3 Procedure

1. Read the **Background Information** section.
2. Do your preliminary work before coming to lab and upload it to the blackboard web page.
3. Having your designs from the preliminary work, follow the digital design procedure from experiment 1 with the following steps.

    - **Design Entry:** Enter gates and blocks to build your design using hardware description language in to the software tool.
    - **Design Simulation:** Test your design in computer simulation. Revise your design if necessary by turning back to the design task.
    - **Synthesize and Map Design:** After a successful simulation, map inputs and outputs of the design to I/O pins of the hardware.
    - **Program Hardware:** Upload the final synthesized bit file to the hardware using a USB cable.
    - **Test Hardware:** Verify the hardware functionality for your design. Revise your design if necessary by turning back to the design task.

4 Background Information

Binary comparators are combinational logic circuits, which are used for testing whether the value represented by one binary number is greater than, less than, or equal to the value represented by another binary number. We can define two types of comparators: i) Equality comparator and ii) Magnitude comparator.

The equality comparator checks bitwise equality of two binary numbers, and outputs logic 1 for equality and logic 0 otherwise.

The magnitude comparator computes three output logic bits for the given two binary numbers A and B. The first output is the equality comparator, which is logic 1 when A equals B, the second logic output is logic 1 when A is greater than B, and the third logic output is logic 1 when A is less than B.

Note that magnitude comparators are fundamental decision making blocks in logic circuits. Any logical problem can be reduced to one or more comparator decisions for a pair of binary numbers.

5 Preliminary Work

Question 5.1 Design an equality comparator circuit for 4-bit binary numbers. We can define functionality of the equality comparator with logic variable E as following,

$$E = \begin{cases} 1 & \text{if } A = B, \\ 0 & \text{otherwise,} \end{cases}$$

where $A = a_3a_2a_1a_0$ and $B = b_3b_2b_1b_0$ are the two 4-bit binary inputs.

Question 5.2 Extend your design in 5.1 to build a magnitude comparator for 4-bit unsigned binary numbers, A and B. Find the three outputs of the magnitude comparator as,

$$E = \begin{cases} 1 & \text{if } A = B, \\ 0 & \text{otherwise.} \end{cases}$$

$$G_{AB} = \begin{cases} 1 & \text{if } A > B, \\ 0 & \text{otherwise.} \end{cases}$$

$$G_{BA} = \begin{cases} 1 & \text{if } A < B, \\ 0 & \text{otherwise.} \end{cases}$$

Question 5.3 Extend your design in 5.2 to build a comparator for 4-bit signed binary numbers in 2's complement system, $C = c_3c_2c_1c_0$ and $D = d_3d_2d_1d_0$. For this signed comparator, find the three outputs as,

$$E = \begin{cases} 1 & \text{if } C = D, \\ 0 & \text{otherwise.} \end{cases}$$

$$G_{CD} = \begin{cases} 1 & \text{if } C > D, \\ 0 & \text{otherwise.} \end{cases}$$

$$G_{DC} = \begin{cases} 1 & \text{if } C < D, \\ 0 & \text{otherwise.} \end{cases}$$

Note that, you can use the magnitude comparator in 5.2 to design the signed comparator.

6 Experimental Work

6.1 Part 1

- Create a new "MComparator" VHDL file. Implement your design in Question 5.2 and simulate the magnitude comparator circuit for three sample input pairs to observe proper functionality of the E, G_{AB}, and G_{BA} outputs. Then download your design to the Prometheus FPGA board for further testing.
- Use switches S7, S6, S5 and S4 for input A and S3, S2, S1 and S0 for input B. For outputs G_{AB}, E and G_{BA} respectively use LEDs LD2, LD1, and LD0.
- Test your deployed magnitude comparator circuit by verifying truth table.
- Demonstrate performance of your circuit to the teaching assistants.

6.2 Part 2

- Create a new "SComparator" VHDL file. Implement your design in Question 5.3 and simulate the magnitude comparator circuit for three sample input pairs to observe proper functionality of the E, G_{CD}, and G_{DC} outputs. Then download your design to the Prometheus FPGA board for further testing.
- Use switches S7, S6, S5 and S4 for input C and S3, S2, S1 and S0 for input D. For outputs G_{CD}, E and G_{DC} respectively use LEDs LD7, LD6, and LD5.
- Test your deployed magnitude comparator circuit by verifying truth table.
- Demonstrate performance of your circuit to the teaching assistants.

6.3 Bonus

Use your creativity to display outputs of the previous two parts on the 7-segment displays using the delivered VHDL code under the resources section of the lab web-page.

7 Assessment

Provide the lab report as described in the *Lab Report Guidelines* document, which is available online on the blackboard web-page.