



ELEC 204 Digital System Design  
Laboratory Manual

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**Experiment #4**  
**Design and Implementation of LED Ping Pong**

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DEPARTMENT OF ELECTRICAL & ELECTRONICS  
ENGINEERING  
COLLEGE OF ENGINEERING  
KOÇ UNIVERSITY

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# 1 Objectives

- To design a sequential circuit for LED pattern animations with control inputs and status output functions,
- To implement the sequential circuit on FPGA,
- To experimentally check functionality of the sequential circuit.

This laboratory session will be your first sequential circuit design and implementation experience. So the main objective of the lab is to get familiar with sequential circuit design and to learn implementation of them in VHDL. Preliminary work will be critical to gain a knowledge on sequential circuit implementation in VHDL.

# 2 Equipment & Software

- IBM compatible PC with Windows operating system,
- Xilinx ISE v14.7 & Prometheus software packages,
- Prometheus FPGA board,
- USB cable for programming.

# 3 Procedure

1. Read the **Problem Statement** section.
2. Do your preliminary work before coming to lab and upload it to the blackboard web page.
3. Having your designs from the preliminary work, follow the digital design procedure from the Experiment 1 with the following steps.
  - **Design Entry:** Enter gates and blocks to build your design using hardware description language in to the software tool.
  - **Design Simulation:** Test your design in computer simulation. Revise your design if necessary by turning back to the design task.
  - **Synthesize and Map Design:** After a successful simulation, map inputs and outputs of the design to I/O pins of the hardware.
  - **Program Hardware:** Upload the final synthesized bit file to the hardware using a USB cable.
  - **Test Hardware:** Verify the hardware functionality for your design. Revise your design if necessary by turning back to the design task.

## 4 Problem Statement

LED Ping Pong experiment will consist of several functional blocks:

1. N-bit LED display, which continuously displays a light pattern using a clock synchronous sequential circuit. For example, a 4-bit LED pattern will be  $1000 \rightarrow 0100 \rightarrow 0010 \rightarrow 0001 \rightarrow 0010 \rightarrow 0100 \rightarrow 1000 \rightarrow 0100 \dots$
2. Ball catching interface: Using two push button switches, respectively assigned for the leftmost and rightmost LEDs, a time synchronized ball detection is to be executed with push button event occurring only in the clock cycle of LED pattern 1000 and 0001.
3. A score counter, which counts number of successful ball/LED catches with timely push button events. Score counter is to be displayed on the seven-segment display in decimal.

## 5 Preliminary Work

Do the following tasks beforehand. Write the answers to all questions in your preliminary report prior to coming to the laboratory.

**Question 5.1** *Build knowledge on implementing sequential circuits with VHDL.* Watch [the video lecture 16 on making sequential circuits](#). Study, implement and discuss the sample sequential circuit code provided in Listing 1.

**Question 5.2** *Design of the LED display.* Design a synchronous sequential circuit that can output the 4-bit LED pattern  $1000 \rightarrow 0100 \rightarrow 0010 \rightarrow 0001 \rightarrow 0010 \rightarrow 0100 \rightarrow 1000 \rightarrow 0100 \dots$ . Briefly justify your design methodology. Explain the design procedure, give the logic diagram, the flip-flop input equations and output equations.

**Question 5.3** *Design of the ball catching interface.* Introduce two push button events as inputs to the LED display circuit and define output function for the ball catching event. Briefly justify your design methodology.

**Question 5.4** *Design of the score counter.* Design 4-bit counter to monitor the number of successful ball/LED catches.

## 6 Experimental Work

### 6.1 Task 1: LED Display

Extend your LED display design in preliminary work to 10-bits and implement LED ping pong pattern animation on the LEDs of the Prometheus FPGA board. Divide the clock frequency to a level that is suitable for visual screening and ball catching task. Make sure the LED display is working properly and demonstrate it in the laboratory.

## 6.2 Task 2: Ball Catching Game

Implement the ball catching interface on top of the LED display in Task 1. Display score counter on the 7-segment display in decimal.

Simulate the full design and demonstrate the full functionality in the laboratory.

## 7 Assessment

Provide the lab report as described in the *Lab Report Guidelines* document, which is available online on the blackboard webpage. Do not forget to include a clear description of your design approach and the overall schematic with simulation waveforms.

## 8 Appendix

Listing 1: Sample VHDL code: Outputs 1 if the number of 1s in the clock synchronous input sequence is odd.

```
-----  
--Company:  
--Engineer:  
--  
--Create Date: 09:53:23 03/09/2018  
--Design Name:  
--Module Name: Lab4TutorialCode -Behavioral  
--Project Name:  
--Target Devices:  
--Tool versions:  
--Description:  
--  
--Dependencies:  
--  
--Revision:  
--Revision 0.01 -File Created  
--Additional Comments:  
--  
-----  
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;  
  
entity Lab4TutorialCode is  
    Generic (N : INTEGER:=50*10**6); --50*10^6 Hz Clock  
    Port (MCLK : in STD_LOGIC;  
          X : in STD_LOGIC; --Push button input  
          Z : out STD_LOGIC; --Output for the odd number of 1s  
          CL : out STD_LOGIC; --Output for clock low  
          CH : out STD_LOGIC); --Output for clock high  
end Lab4TutorialCode;
```

```

architecture Behavioral of Lab4TutorialCode is
    signal CLK_DIV : STD_LOGIC;
    signal State: STD_LOGIC;

begin
    --Transfer state vector into LEDS
    Z <= State xor X;
    CH <= CLK_DIV;
    CL <= not CLK_DIV;

    --Clock divider
    process(MCLK)
        variable Counter : INTEGER range 0 to N;
    begin
        if rising_edge(MCLK) then
            Counter := Counter + 1;
            if (Counter = N/1-1) then
                Counter := 0;
                CLK_DIV <= not CLK_DIV;
            end if;
        end if;
    end process;

    --LED shifter
    process(CLK_DIV)
    begin
        if rising_edge(CLK_DIV) then
            State <= State xor X;
        end if;
    end process;
end Behavioral;

```

Listing 2: Pin connections for the sample VHDL code

```

NET "MCLK" LOC = "P40" ;

NET "X" LOC = "P32" ;
NET "Z" LOC = "P16" ;
NET "CH" LOC = "P77" ;
NET "CL" LOC = "P83" ;

```