# INSTRUCTION SET / KOMUT SETİ

# ( ENGLISH MNEMONICS / TÜRKÇE KISALTMALAR)

Transfer/Aktarma	
MOV	AKT
LDA	YÜK
STA	YAZ
EXC	TKS
CHN	DĞŞ

Shift-Rotate/		
Öteleme-		
Döndürme		
LSL	SOL	
LSR	SAĞ	
ASR	SAĞİ	
ROL	SOLD	
ROR	SAĞD	

Logic/Mantıksal		
AND	VE	
OR	VEYA	
XOR	YADA	
CLR	SİL	
SET	KUR	
COM	TÜM	
NEG	EKS	

Dii	Directives/	
Direktifler		
ORG	BAŞ	
EQU	EŞT	
RMB	YER	
DAT	VER	
END	SON	

Arithmetic/			
Α	Aritmetik		
ADD	TOP		
ADC	TOPE		
SUB	ÇIK		
SUE	ÇIKE		
MUL	ÇAR		
DIV	BÖL		
INC	ART		
DEC	AZT		

Ор	erational/
Ор	erasyonel
DAA	ONA
PSH	YIĞ
PUL	ÇEK
EIN	KİZ
DIN	KEN
NOP	GEÇ
INT	KES
RTS	DÖN
RTI	DÖNK

Bran	ich-Compare/
	Dallanma -
Ka	arşılaştırma
CMP	KAR
BIT	SIN
BRA	DAL
JMP	BAĞ
JMC	BAĞK
BEQ	DEE
BNE	DED
BGT	DEB
BGE	DBE
BLT	DEK
ВНІ	DEI
BHE	DİE

Brand	ch-Compare/	
D	Dallanma -	
Ka	rşılaştırma	
BLO	DEU	
BIO	DTV	
BNO	DTY	
BIC	DEV	
BNC	DEY	
BIH	DYV	
BNH	DYY	
BSR	ALT	
JSR	ALTD	
BSC	ALTK	
JSC	ALTDK	
DBNZ	ADED	

## EDU-CPU INSTRUCTION SET

-	Transfer
MOV	Move
LDA	Load
STA	Store
EXC	Exchange
CHN	Change

Shift/Rotate		
LSL	Logical shift	
	left	
LSR	Logical shift	
	right	
ASR	Arithmetic	
	shift right	
ROL	Rotate left	
ROR	Rotate right	

Logic	
AND	And
OR	Or
XOR	Exclusive or
CLR	Clear
SET	Set
сом	Complement
NEG	Negate

#### First Operands Ri Rii V

Directives	
ORG	Origin
EQU	Equal
RMB	Reserve
	memory
	bytes
DAT	Data
END	End

Arithmetic		
ADD	Add	
ADC	Add with	
	carry	
SUB	Subtract	
SUE	Subtract	
	with carry	
MUL	Multiply	
DIV	Divide	
INC	Incremenet	
DEC	Decrement	

Second	
Operands	
Rj	
Rjj	
V	
VV	
<address></address>	
<cd></cd>	
<sk+s></sk+s>	
<sk+s> + - R</sk+s>	
<sk+cd+s></sk+cd+s>	
<yg+s></yg+s>	

Operational	
DAA	Decimal
	adjust
	accumulator
PSH	Push
PUL	Pull
EIN	Enable
	interrupt
DIN	Disable
	interrupt
NOP	No
	operation
INT	Interrupt
RTS	Return from
	subroutine
RTI	Return from
	interrupt

data)
VV : 16-bit data
Ri, Rj : 8-bit register
Rii, Rjj : 16-bit register
S : Sıra (Index)
R: Range (incr/decr SK)

Operand Symbols V : Veri (8-bit

Bran	ch - Compare
CMP	Compare
BIT	Bit test
BRA	Branch
	(unconditional)
JMP	Jump
	(unconditional)
JMC	Jump
	conditionally
BEQ	Branch if equal
BNE	Branch if not
	equal
BGT	Branch if
	greater than
BGE	Branch if
	greater or
	equal
BLT	Branch if less
	than
BHI	Branch if
	higher
BHE	Branch if
	higher or equal

8-bit Re	egisters
A, B, C, D	
DK : Durum	ı Kütüğü
	•
16-bit R	egisters
AB, CD	•
SK : Sıralam	na Kütüğü
(Index Regi	Ū
,	<b>,</b>
YG : Yığın G	östergesi
(Stack Poin	ter)

Brand	ch - Compare
BLO	Branch if
	lower
BIO	Branch if
	overflow
BNO	Branch if not
	overflow
BIC	Branch if carry
BNC	Branch if not
	carry
BIH	Branch if half
	carry
BNH	Branch if not
	half carry
BSR	Branch to
	subroutine
JSR	Jump to
	subroutine
BSC	Branch to
	subroutine
	conditionally
JSC	Jump to
	subroutine
	conditionally
DBNZ	Decrease,
	branch if not
	zero

# Status Flags (DK) E: Carry Y: Half carry S: Zero N: Negative T: Overflow K: Interrupt

## ÖRNEK-MİB KOMUT SETİ

	Aktarma
AKT	Aktar
YÜK	Yükle
YAZ	Yaz
TKS	Takas
DĞŞ	Değiştir

Direktifler	
BAŞ	Başlangıç
EŞT	Eşit
YER	Yer ayır
VER	Veri
SON	Son

D	irektifier
BAŞ	Başlangıç
EŞT	Eşit
YER	Yer ayır
VER	Veri
SON	Son

Ar	itmetik
TOP	Topla
TOPE	Elde ile
	topla
ÇIK	Çıkart
ÇIKE	Elde ile
	çıkart
ÇAR	Çarp
BÖL	Böl
ΛDT	Δrtır

Operasyonel	
ONA	Ondalık
	akümülatör
	ayarla
YIĞ	Yığ
ÇEK	Çek
KİZ	Kesmeye
	izin ver
KEN	Kesmeyi
	engelle
GEÇ	Geç
KES	Kesme
DÖN	Geri dön
DÖNK	Kesmeden
	geri dön

Dallanma -		
Karşılaştırma		
DEU	Dallan eğer	
	mutlak ufaksa	
DTV	Dallan eğer	
	taşma varsa	
DTY	Dallan eğer	
	taşma yoksa	
DEV	Dallan elde	
	varsa	
DEY	Dallan elde	
	yoksa	
DYV	Dallan yarım	
	elde varsa	
DYY	Dallan yarım	
	elde yoksa	
ALT	Alt rutini çağır	
ALTD	Alt rutine	
	bağlan	
ALTK	Alt rutini	
	koşullu çağır	
ALTDK	Alt rutine	
	koşullu bağlan	
ADED	Azalt, dallan	
	eşit değilse	

Döndürme		
SOL	Sola ötele	
SAĞ	Sağa ötele	
SAĞİ	Sağa	
	aritmetik	
	ötele	
SOLD	Sola döndür	
SAĞD	Sağa döndür	

Mantıksal

Ve

Veya

Yada

Sil

Kur

Eksi

Tümleyen

VE

VEYA

YADA

SİL

KUR

TÜM

EKS

Öteleme /

Ar	itmetik
TOP	Topla
TOPE	Elde ile
	topla
ÇIK	Çıkart
ÇIKE	Elde ile
	çıkart
ÇAR	Çarp
BÖL	Böl
ART	Artır
AZT	Azalt

<YG+S>

İkinci	
İşlenenler	
Rj	
Rjj	
V	
VV	
<adres></adres>	
<cd></cd>	
<sk+s></sk+s>	
<sk+s> + - R</sk+s>	
<sk+cd+s></sk+cd+s>	
AVC . Cs	

İşlenen Sembolleri

mutlak büyük
veya eşitse
8-bit Registerler
A, B, C, D
DK : Durum Kütüğü
16-bit Registerler
AB, CD
SK : Sıralama Kütüğü (Index Register)
YG : Yığın Göstergesi

(Stack Pointer)

Dallanma -

Karşılaştırma

Bit sına

Dallan

Bağlan

BAĞK Bağlan koşullu Dallan eğer

eşitse

Karşılaştır

(koşulsuz)

(koşulsuz)

Dallan eşit değilse

Dallan eğer

büyükse Dallan büyük

eşitse Dallan eğer

küçükse

mutlak

büyükse

Dallan eğer

Dallan eğer

KAR

SIN

DAL

BAĞ

DEE

DED

DEB

DBE

DEK

DEI

DİE

Durum Registeri Bayrakları E : Elde Y: Yarım elde S : Sıfır N: Negatif T : Taşma K : Kesme

#### Birinci İşlenenler Ri Rii ٧

	8 Bit Registers Accumulator A Accumulator B AUX Register C AUX Register D	А В С	16 Bit Registers Accumulator pair AUX register pair Index register Stack pointer	AB CD SK YG	
Trogram country	Status Register D	DK	Program counter	PS	_

Status Flags (DK)

- 0 Becomes 0 after the execution.
- 1 Becomes 1 after the execution.
- No changes after the execution.
- Becomes 1 or 0 after the execution.

Status Flag	<u>s(DK)</u>
Carry	Е
Half Carry	Υ
Zero	S
Negative	Ν
Overflow	T
Interrupt	K

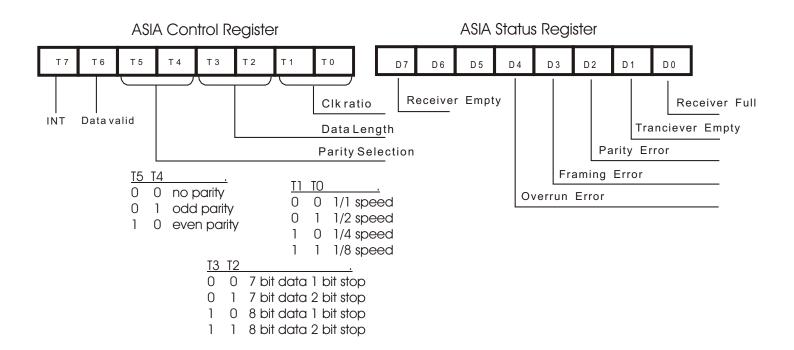
Addressing Methods **Immediate** Immediate memory Υ Register L Direct D Indirect Κ Relative В S Indexed (SK) Incremental SK R Decremental SK 7 Indirect SK U Υ Indexed (YG)

KTSNYE

	Initialization of PIA for Ready Input				
D1	D0	Read	dy Input	Interrupt Output	
0	0	From 1 to 0	D7 flag becomes 1	not genaretes interrupt	
0	1	From 0 to 1	D7 flag becomes 1	not genaretes interrupt	
1	0	From 1 to 0	D7 flag becomes 1	genaretes interrupt	
1	1	From 0 to 1	D7 flag becomes 1	genaretes interrupt	

	Initialization of PIA for ACK Input			
D3	D2	ACK	Input	Interrupt Output
0	0	From 1 to 0	D7 flag becomes 1	not genaretes interrupt
0	1	From 0 to 1	D7 flag becomes 1	not genaretes interrupt
1	0	From 1 to 0	D7 flag becomes 1	genaretes interrupt
1	1	From 0 to 1	D7 flag becomes 1	genaretes interrupt

	Initialization of PIA for Data Valid output			
D5	D4	Data Valid output		
0	0	Becomes 0		
0	1	Becomes 1		
1	0	Becomes 0 after data writen to port.		
1	1	Becomes 1 after data writen to port.		



				ARITHM	ETIC INS	TRUCTION	S	- (8	bit )			
Oper	Op Code	Adr met	1. Byte	Instruction 2. Byte	Format 3. Byte	4. Byte	St		Reg.	ΙE	А	Explanation
	Ai,V	V	00000011	0 0 0 0 Ai	Data	,			<b>* *</b>	_	3	Ai <b>←</b> Ai +V
	Ai,Ki	L	01000011	0 0 Ai Ki			\$	<b>\$</b>	<b>* *</b>		3	Ai ← Ai + Ki
	Ai, <adr></adr>	D	00000011	0 0 1 0 0 Ai	Adr (H)	Adr (L)	<b>\$</b>	<b>\$</b>	<b>* *</b>	<b>\$</b>	4	Ai ← Ai + <adr></adr>
	Ai, <cd></cd>	К	00000011	0 1 0 0 0 Ai			<b>\$</b>	<b>\$</b>	<b>* *</b>		6	Ai ← Ai + < <cd>&gt;</cd>
ADD	Ai, <sk+s></sk+s>	S	00000011	0 1 1 0 0 Ai	S		\$	<b>\$</b>	<b>* *</b>	<b>\$</b>	7	Ai ← Ai + <sk+s></sk+s>
ADD	Ai, $<$ $SK+S$ $>$ $+R$	R	00000011	1 0 0 0 0 Ai	S	R	<b>\$</b>	<b>\$</b>	<b>\$ \$</b>	<b>\$</b>	7	Ai ← Ai + <\$K+\$> +R
	Ai, <sk+s>-R</sk+s>	Z	00000011	1 0 1 0 0 Ai	S	R	\$	<b>\$</b>	<b>\$ \$</b>	<b>\$</b>	7	Ai ← Ai + <sk+s> - R</sk+s>
	Ai, <sk+cd+s></sk+cd+s>	U	00000011	1 1 0 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>\$</b>	<b>\$</b>	8	Ai ← Ai + <\$K+CD+\$>
	Ai, <yg+\$></yg+\$>	Υ	00000011	1 1 1 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>* *</b>		7	Ai ← Ai + <yg+\$></yg+\$>
	Ai,V	٧	00000100	0 0 0 0 0 Ai	Data		\$	<b>\$</b>	<b>\$ \$</b>	<b>\$</b>	3	Ai ← Ai +V + E
	Ai,Ki	L	01000100	0 0 Ai Ki			\$	<b>\$</b>	<b>\$ \$</b>	<b>\$</b>	3	Ai ← Ai + Ki + E
	Ai, <adr></adr>	D	00000100	0 0 1 0 0 Ai	Adr (H)	Adr (L)	\$	<b>\$</b>	<b>\$ \$</b>	<b>\$</b>	4	Ai ← Ai + <adr> + E</adr>
ADC	Ai, <cd></cd>	K	00000100	0 1 0 0 0 Ai			\$	<b>\$</b>	<b>\$ \$</b>	<b>\$</b>	6	Ai ← Ai + < <cd>&gt; + E</cd>
ADC	Ai, <sk+s></sk+s>	S	00000100	0 1 1 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>* *</b>	<b>\$</b>	7	Ai ← Ai + <\$K+\$> + E
	Ai, <sk+s>+R</sk+s>	R	00000100	1 0 0 0 0 Ai	S	R	<b>\$</b>	<b>\$</b>	<b>\$ \$</b>	<b>\$</b>	7	Ai ← Ai + <\$K+\$> + E +R
	Ai, $<$ $SK+S>-R$	Z	00000100	1 0 1 0 0 Ai	S	R	<b>\$</b>	<b>\$</b>	<b>\$ \$</b>	<b>\$</b>	7	Ai ← Ai + <\$K+\$> + E - R
	Ai, <sk+cd+s></sk+cd+s>	U	00000100	1 1 0 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>\$</b>	<b>\$</b>	8	Ai ← Ai + <\$K+CD+\$> + E
	Ai, <yg+\$></yg+\$>	Υ	00000100	1 1 1 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>\$ \$</b>	•	7	Ai ← Ai + <yg+\$> + E</yg+\$>
	Ai,V	٧	00000101	0 0 0 0 0 Ai	Data		\$	<b>\$</b>	<b>\$</b> -	• ♦	3	Ai ← Ai - V
	Ai,Ki	L	01000101	0 0 Ai Ki			\$	<b>\$</b>	<b>* -</b>	• 🛊	3	Ai ← Ai - Ki
	Ai, <adr></adr>	D	00000101	0 0 1 0 0 Ai	Adr (H)	Adr (L)	<b>\$</b>	<b>♦</b>	<b>* -</b>	• ♦	4	Ai ← Ai - <adr></adr>
SUB	Ai, <cd></cd>	K	00000101	0 1 0 0 0 Ai			<b>\$</b>	<b>\$</b>	<b>+</b> -	• 🛊	6	Ai ← Ai - < <cd>&gt;</cd>
306	Ai, <sk+s></sk+s>	S	00000101	0 1 1 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>* -</b>	• ♦	7	Ai ← Ai - <sk+s></sk+s>
	Ai, <sk+s>+R</sk+s>	R	00000101	1 0 0 0 0 Ai	Ş	R	<b>\$</b>	<b>\$</b>	<b>\$</b> -	• 🛊	7	Ai ← Ai - <sk+s> +R</sk+s>
	Ai, <sk+s>-R</sk+s>	Z	00000101	1 0 1 0 0 Ai	S	R	<b>\$</b>	<b>\$</b>	<b>\$</b> -	• 🛊	7	Ai ← Ai - <sk+s> - R</sk+s>
	Ai, <sk+cd+s></sk+cd+s>	U	00000101	1 1 0 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>\$</b> -	• 🛊	8	Ai ← Ai - <sk+cd+\$></sk+cd+\$>
	Ai, <yg+\$></yg+\$>	Υ	00000101	1 1 1 0 0 Ai	S		\$	<b>\$</b>	<b>\$</b> -	• 🛊	7	Ai ← Ai - <yg+\$></yg+\$>
	Ai,V	٧	00000110	0 0 0 0 0 Ai	Data		\$	<b>\$</b>	<b>♦</b> -	• 🛊	3	Ai ← Ai -V - E
	Ai,Ki	L	01000110	0 0 Ai Ki			<b>\$</b>	<b>\$</b>	<b>\$</b> -	• 🛊	3	Ai ← Ai - Ki - E
	Ai, <adr></adr>	D	00000110	0 0 1 0 0 Ai	Adr (Y)	Adr (L)	<b>\$</b>	<b>\$</b>	<b>♦</b> -	• 🛊	4	Ai ← Ai - <adr> - E</adr>
	Ai, <cd></cd>	K	00000110	0 1 0 0 0 Ai			<b>\$</b>	<b>\$</b>	<b>\$</b> -	• 🛊	6	Ai ← Ai - < <cd>&gt; - E</cd>
SUE	Ai, <sk+s></sk+s>	S	00000110	0 1 1 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>\$</b> -	• 🛊	7	Ai ← Ai - <sk+s> - E</sk+s>
	Ai, <sk+s>+R</sk+s>	R	00000110	1 0 0 0 0 Ai	S	R	\$	<b>\$</b>	<b>\$</b> -	• 🛊	7	Ai ← Ai - <sk+s> - E +R</sk+s>
	Ai, <sk+s>-R</sk+s>		00000110	1 0 1 0 0 Ai	S	R	\$	<b>\$</b>	<b>\$</b> -	• 🛊	7	Ai ← Ai - <sk+s> - E - R</sk+s>
	Ai, <sk+cd+s></sk+cd+s>	U	00000110	1 1 0 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>\$</b> -	• 🛊	8	Ai ← Ai - <sk+cd+s> - E</sk+cd+s>
	Ai, <yg+\$></yg+\$>	Υ	00000110	1 1 1 0 0 Ai	S		<b>\$</b>	<b>\$</b>	<b>\$</b> -	•	7	Ai ← Ai - <yg+\$> - E</yg+\$>

				ARITH	METIC IN	STRUCTIO	N S	-	(16	bit			
Oper	Op Code	Adr		Instruction	Format		St	tatus	Re	g. <u>.</u>	А	1	Explanation
	0,00000	met	11.57.5	2. Byte	3. Byte	4. Byte	T	S	N	_	_		Explanation
	AB,VV	V	00100011		Data(H)	Data(L)	•	<b>*</b>	·	- 4	-	AB◀─	AB +VV
	AB,Kii	L	0 1 1 0 0 0 1 1				<b>♦</b>	_	_	- 4	4	AB◀─	AB + Kii
	AB, <adr></adr>	D	00100011	0 0 1 0 0 AB	Adr (H)	Adr (L)	\$	\$	\$	- 4	5	AB◀─	AB + ( <adr>+<adr+1>)</adr+1></adr>
	AB, <cd></cd>	K	00100011	0 1 0 0 0 AB			\$	\$	\$	- 4	7	AB◀─	AB +(< <cd>&gt;+&lt;<cd+1>&gt;)</cd+1></cd>
ADD.	AB, <sk+s></sk+s>	S	00100011	0 1 1 0 0 AB	S		<b>\$</b>	\$	<b>\$</b>	- 4	-	AB◀─	AB + ( <sk+s>+<sk+s+1>)</sk+s+1></sk+s>
	AB, <sk+s>+R</sk+s>	R	00100011	1 0 0 0 0 AB	S	R	\$	<b>\$</b>	\$	- 4	8	AB <b>←</b>	AB + ( <sk+s> + <sk+s>) + R</sk+s></sk+s>
	AB, <sk+s>-R</sk+s>	Z	00100011	1 0 1 0 0 AB	S	R	<b>\$</b>	\$	<b>\$</b>	- 4	8	AB◀─	AB +( <sk+s>+<sk+s+1>) - R</sk+s+1></sk+s>
	AB, <sk+cd+s></sk+cd+s>	U	00100011	1 1 0 0 0 AB	S		\$	\$	<b>\$</b>	1	9	AB <b>←</b>	AB + ( <sk+cd+s>+<sk+cd+s+< td=""></sk+cd+s+<></sk+cd+s>
	AB, <yg+s></yg+s>	Υ	00100011	1 1 1 0 0 AB	S		<b>\$</b>	<b>\$</b>	<b>\$</b>	1	8	AB◀─	AB +( <yg+\$>+<yg+\$>)</yg+\$></yg+\$>
	AB,VV	٧	00100101	0 0 0 0 0 AB	Data (H)	Data (L)	<b>\$</b>	<b>\$</b>	<b>\$</b>	4	4	AB◀	AB - VV
	AB,Kii	L	01100101	O O AB Kii			\$	<b>\$</b>	<b>\$</b>	-	4	AB◀─	AB - Kii
	AB, <adr></adr>	D	00100101	0 0 1 0 0 AB	Adr (H)	Adr (L)	\$	\$	<b>\$</b>	- 4	5	AB <b>∢</b>	AB - ( <adr>+<adr+1>)</adr+1></adr>
UB	AB, <cd></cd>	К	00100101	0 1 0 0 0 AB			\$	\$	<b>\$</b>	- 4	7	AB◀─	AB -(< <cd>&gt;+&lt;<cd+1>&gt;)</cd+1></cd>
UB	AB, <sk+s></sk+s>	S	00100101	0 1 1 0 0 AB	Š		\$	\$	\$	- 4	8	AB◀─	AB -( <sk+s>+<sk+s+1>)</sk+s+1></sk+s>
	AB, <sk+s>+R</sk+s>	R	00100101	1 0 0 0 0 AB	S	R	\$	\$	<b>\$</b>	- 4	8	AB◀─	AB -( <sk+s>+<sk+s>) +R</sk+s></sk+s>
	AB, <sk+s>-R</sk+s>	Z	00100101	1 0 1 0 0 AB	S	R	\$	<b>\$</b>	\$	- 4	8	AB◀	AB -( <sk+s>+&gt;SK+S+1&gt;) - R</sk+s>
	AB, < SK+CD+S>	U	00100101	1 1 0 0 0 AB	S		<b>\$</b>	•	<b>\$</b>	- 4	9	1	AB -( <sk+cd+s>+<sk+cd+s+1< td=""></sk+cd+s+1<></sk+cd+s>
	AB, <yg+s></yg+s>	Υ	00100101	1 1 1 0 0 AB	S		\$	\$	<b>*</b>	- 4	8	AB◀─	AB -( <yg+s>+<yg+s>)</yg+s></yg+s>
	A,V	V	00000111	00000 A	Data		-	•	•		<b>2</b> /	AB◀─	A * V
	A,Ki	L	01000111	0 0 A Ki			-	\$	•	_	<b>2</b> 4	AB◀─	
	A, <adr></adr>	_	00000111	0 0 1 0 0 A	Adr (H)	Adr (L)	-	•	<b>*</b>	_	20	+	A * <adr></adr>
	A, <cd></cd>	_	00000111				-	<b>*</b>	<b>*</b>	_	28	1 -	A * < <cd>&gt;</cd>
ИUL	A, <sk+s></sk+s>	_	00000111		S		-	<b>*</b>	<b>*</b>	_	-	+	A * <sk+s></sk+s>
	A, < \$K+\$>+R	<del>-</del>	00000111	10000 A	S	R	-	<b>*</b>	<b>*</b>	_	-	+	A * <sk+s> +R</sk+s>
	A, < \$K+\$>-R	- ' '	00000111		S	R	_	<b>*</b>	<b>*</b>	$\vdash$	3	+	A * <sk+s> - R</sk+s>
	A, < SK+CD+S>	_	000000111		Š		-	<b>*</b>	<b>*</b>	-	32	+	A * < SK+CD+S>
	A. <yg+s></yg+s>	_	00000111		S		_	<b>*</b>	<u> </u>	_	1 -	+	A * <yg+\$></yg+\$>
	AB.V	-	00100111		Data			<b>*</b>	<b>*</b>	$\vdash$	32	+	
	AB,Ki	L		0 0 0 0 0 AB				<b>*</b>	<b>*</b>	_	-	+	
	AB, <adr></adr>	-		0 0 1 0 0 AB	Adr (H)	Adr (L)		<b>*</b>	<b>*</b>	$\vdash$	3,	+	AB / <adr></adr>
	AB, <cd></cd>	-	00100111	01000 AB	7 (0.1)	ion (E)		<b>*</b>	<b>*</b>	$\vdash$	30	+	AB / < <cd>&gt;</cd>
n. /	AB, < SK+S>	-	00100111	01100 AB				<b>*</b>	-		100	+	AB / < <cd>&gt;</cd>
ΝV	AB, < SK+S>+R	<u> </u>		1 0 0 0 0 AB		R	E	<b>*</b>	<b>*</b>	$\vdash$	38	+	
	AB, <sk+s>-R</sk+s>	-	00100111		S	, i		<b>▼</b>	<b>▼</b>		+	+	AB / <sk+s></sk+s>
	AB, < SK+CD+S>	_	00100111		S	15	=	+÷	i i		1	+	AB / <sk+s></sk+s>
	AB,<3K+CD+3> AB, <yg+\$></yg+\$>	Y					E	♦	♦			+	AB / <sk+cd+s></sk+cd+s>
	~D, < 10 +3 /	,	00100111	1 1 1 0 0 AB	Ş			-	₹		38	AB◀─	AB / <yg+\$></yg+\$>

				TRANS	FER INSTR	UCTIONS	- ( 8 bit )						
Oper	Op Code	Adr		Ins	truction Format			S	tatus	Reg		Α	Explanation
Орог	op code	met	1. Byte	2. Byte	3. Byte	4. Byte	5. Byte	T	S	N	Y E		· ·
MOV	Ki,Kj	L	01000000	0 0 Ki Kj				_	<b>\$</b>	<b>\$</b> •		1	Ki <b>←</b> Kj
EXC	Ki,Kj	L	01000001	0 0 Ki Kj				_	_	-	_ -	3	Кі← Кј
CHN	Ki	L	01000010	0 1 Ki				_	<b>*</b>	<b>*</b>		5	D3 D2 D1 D0 D7 D6 D5 D4
	Ki,V	٧	0000000	0 0 0 0 0 Ki	Data			_	\$	<b>\$</b>	- -	1	Ki <b>←</b> ─V
	Ki, <adr></adr>	D	0000000	0 0 1 0 0 Ki	Adr (H)	Adr (L)		_	\$	<b>*</b>	_ -	2	Ki <b>←</b> — <adr></adr>
	Ki, <cd></cd>	K	0000000	0 1 0 0 0 Ki				_	<b>\$</b>	<b>\$</b>	_	3	Ki <b>←</b> ─< <cd>&gt;</cd>
LDA	Ki, <sk+s></sk+s>	S	0000000	0 1 1 0 0 Ki	S			_	\$	<b>\$</b>	_ -	4	Ki <b>←</b> —<\$K+\$>
LDA	Ki, $< SK+S > +R$	R	0000000	1 0 0 0 0 Ki	S S	R		_	<b>\$</b>	<b>\$</b>	_ -	5	Ki <b>←</b> <\$K+\$> +R
	Ki, <sk+s>-R</sk+s>	Z	0000000	1 0 1 0 0 Ki	S	R		_	\$		_ -	5	Ki ←—<\$K+\$> -R
	Ki,<\$K+CD+\$>	U	0000000	1 1 0 0 0 Ki	Ś			_	<b>\$</b>	<b>\$</b>		6	Ki ←—<\$K+CD+\$>
	Ki, <yg+\$></yg+\$>	Υ	0000000	1 1 1 0 0 Ki	S			_	<b>\$</b>	<b>\$</b>		5	Ki <b>←</b> <yg+\$></yg+\$>
	V,Adr	٧	0 0 0 0 0 0 0 1	00001	Datai	Adr (H)	Adr (L)	_	_	-		3	Adr← V
	Ki, <adr></adr>	D	0 0 0 0 0 0 0 1	0 0 1 0 0 Ki	Adr (H)	Adr (L)		_	_	-		2	Adr <b>←</b> Ki
	Ki, <cd></cd>	K	0 0 0 0 0 0 0 1	0 1 0 0 0 Ki				_	-	-	- -	3	< <cd>&gt; <b>←</b> Ki</cd>
STR	Ki, <sk+s></sk+s>	S	0 0 0 0 0 0 0 1	0 1 1 0 0 Ki	Ş			_	-	-		4	<\$K+\$> <b>←</b> Ki
JIK	Ki, $< SK + S > + R$	R	0 0 0 0 0 0 0 1	1 0 0 0 0 Ki	S	R		_	-	-		5	<\$K+\$> <b>←</b> Ki + R
	Ki, <sk+s>-R</sk+s>	Z	0 0 0 0 0 0 0 1	1 0 1 0 0 Ki	S	R			_	-	_   _	5	<\$K+\$> <b>←</b> Ki - R
	Ki, <sk+cd+s></sk+cd+s>	U	0 0 0 0 0 0 0 1	1 1 0 0 0 Ki	S			_		-		6	<\$K+CD+\$> <b>←</b> Ki
	Ki, <yg+\$></yg+\$>	Υ	0 0 0 0 0 0 0 1	1 1 1 0 0 Ki	S				_	<b>-</b>	- -	5	<yg+\$> <b>←</b> Ki</yg+\$>

				TRANSF	ER INSTRU	ICTIONS -(	16	bit )					
Oper	On Code	Adr		Instru	uction Format			Sto	atus	Reg.		А	Explanation
Opei	Op Code	met	1. Byte	2. Byte	3. Byte	4. Byte	Т	S	N	Υ	Е		. Diplanation
MOV	Kii,Kjj	L	0 1 1 0 0 0 0 0	o o Kii Kjj			-	\$	\$		-	2	Kii <b>←</b> Kjj
EXC	Kii,Kjj	L	0 1 1 0 0 0 0 1	o o Kii Kjj			_	_	-	ı	_	4	Kii ← Kjj
	Kii,VV	٧	0010000	0 0 0 0 0 Kii	Datai	Data	_	\$	<b>\$</b>	-	_	2	Kii ← W
	Kii, <adr></adr>	D	0010000	0 0 1 0 0 Kii	Adr (H)	Adr (L)	-	\$	\$	_	-	3	Kii <b>←</b> <adr>+<adr+1></adr+1></adr>
	Kii, <cd></cd>	К	0010000	0 1 0 0 0 Kii			_	\$	\$	1	-	4	Kii <b>←</b> < <cd>&gt;+&lt;<cd+1>&gt;</cd+1></cd>
	Kii, < SK+S>	S	0010000	0 1 1 0 0 Kii	S		_	\$	<b>\$</b>	1	_	5	Kii <b>←</b> < SK+S>+ <sk+s+1></sk+s+1>
LDA	Kii, $<$ SK $+$ S $>$ +R	R	0010000	1 0 0 0 0 Kii	S	R	_	\$	\$	_	-	6	Kii <b>←</b> <sk+s>+<sk+s+1> +R</sk+s+1></sk+s>
	Kii, < SK+S>-R	Z	0010000	1 0 1 0 0 Kii	S	R	_	\$	\$	_	-	6	Kii <b>←</b> <sk+s>+<sk+s+1> - R</sk+s+1></sk+s>
	Kii, < SK+CD+S>	U	0010000	1 1 0 0 0 Kii	S		_	\$	<b>\$</b>	ı	_	7	Kii ← <\$K+CD+\$>+<\$K+CD+\$+1>
	Kii, <yg+\$></yg+\$>	Υ	0010000	1 1 1 0 0 Kii	S		_	\$	<b>\$</b>	-	_	6	Kii <b>←</b> <yg+\$>+<yg+\$+1></yg+\$+1></yg+\$>
	Kii, <adr></adr>	D	00100001	0 0 1 0 0 Kii	Adr (H)	Adr (L)	-	_	-	_	-	3	Adr+(Adr+1) ← Kii
	Kii, <cd></cd>	K	0 0 1 0 0 0 0 1	0 1 0 0 0 Kii			_	_	-	ı	_	4	< <cd>&gt;+&lt;<cd+1>&gt;  ← Kii</cd+1></cd>
STR	Kii, < SK+S>	S	0 0 1 0 0 0 0 1	0 1 1 0 0 Kii	S		_	_	_	-	_	5	<\$K+\$>+<\$K+\$+1> <b>←</b> Kii
OIIX	Kii, < SK+S>+R	R	0 0 1 0 0 0 0 1	1 0 0 0 0 Kii	S	R	-	_	-	_	-	6	<\$K+\$>+<\$K+\$+1> <b>←</b> Kii + R
	Kii, < SK+S>-R	Z	0 0 1 0 0 0 0 1	1 0 1 0 0 Kii	S	R	_	_	-	_	-	6	<\$K+\$>+<\$K+\$+1>
	Kii, < SK+CD+S>	U	00100001	1 1 0 0 0 Kii	S		_	_	-	_	-	7	<\$K+CD+\$>+<\$K+CD+\$+1> <b>←</b> K
	Kii, <yg+\$></yg+\$>	Υ	0 0 1 0 0 0 0 1	1 1 1 0 0 Kii	S		_	_			_	6	<yg+\$>+<yg+\$+1><b>◆</b> Kii</yg+\$+1></yg+\$>

				LOGI	C INSTRU	CTIONS -(8	bit )						
Oper	I Ob-Code I	Adr met	1. Byte	Instruction  2. Byte	Format 3. Byte	4. Byte		_	Stat		eg. E	А	Explanation
	Ai,V		00001000	,	,	4. byte	T	\$	-		$\blacksquare$	3	Ai ← Ai • V
	Ai,V Ai,Ki		01001000				-	<del>l ;</del>	<b>*</b>	_	$\vdash$	3	Ai ← Ai • Ki
		-	00001000			Adr (L)		+ :	<b>*</b>	-	_	4	Ai ← Ai • <adr></adr>
	Ai, <adr></adr>		00001000			Adi (E)		+÷	<b>*</b>		_	6	Ai ← Ai • < <cd>&gt;</cd>
	Ai, <cd> Ai,<sk+s></sk+s></cd>	-11	00001000	011000 Ai			E	+:	<del>                                     </del>	=	$\vdash$	-	
AND	Ai, < 5K+5> Ai, < 5K+5>+R	-			3	R	<del>.    -  </del>	+·		-	$\vdash$	7	Ai ← Ai • <sk+s></sk+s>
	,	- 11	00001000		S	I K		+*	<b>*</b>	_	$\vdash$	7	Ai ← Ai • <sk+s>+R</sk+s>
	Ai, <sk+s>-R</sk+s>	-	00001000		S	, K	_	+*	-	-	_	7	Ai ← Ai • <sk+s> - R</sk+s>
	Ai, <sk+cd+s></sk+cd+s>	-	00001000	1 1 0 0 0 Ai	S		-	-	<b>\$</b>	-	_	8	Ai ← Ai • <\$K+CD+\$>
	Ai, <yg+\$></yg+\$>	-	00001000		S	=	-	<b>*</b>	- * ·	_	-	<u> </u>	Ai ← Ai • <yg+\$></yg+\$>
	Ai,V	٧	00001001	0 0 0 0 0 Ai	Data		-	+*	\$	_	_	3	Ai ← Ai + V
	Ai,Ki	L	01001001	0 0 Ai Ki			<b> -</b>	•	\$	_		3	Ai ← Ai + Ki
	Ai, <adr></adr>	D	00001001	0 0 1 0 0 Ai	Adr (H)	Adr (L)	_	♦	\$	_		4	Ai ← Ai + <adr></adr>
OR	Ai, <cd></cd>	K	00001001	0 1 0 0 0 Ai			_	<b>\$</b>	\$	_	_	6	Ai ← Ai + < <cd>&gt;</cd>
OI.	Ai, <sk+s></sk+s>	S	00001001	0 1 1 0 0 Ai	S		-	<b>\$</b>	<b>\$</b>	_	_	7	Ai ← Ai + <\$K+\$>
	Ai, <sk+s>+R</sk+s>	R	00001001	1 0 0 0 0 Ai	S	R	] -	<b>\$</b>	\$	_	_	7	Ai ← Ai + <sk+s>+R</sk+s>
	Ai, <sk+s>-R</sk+s>	Z	00001001	1 0 1 0 0 Ai	S	R	-	<b>\$</b>	\$	ı	_	7	Ai ← Ai + <sk+s> - R</sk+s>
	Ai, <sk+cd+s></sk+cd+s>	U	00001001	1 1 0 0 0 Ai	S		-	<b>\$</b>	\$	_	_	8	Ai ← Ai + <\$K+CD+\$>
	Ai, <yg+\$></yg+\$>	Υ	00001001	1 1 1 0 0 Ai	S		-	\$	\$	_	_	7	Ai ← Ai + <yg+\$></yg+\$>
	Ai,V	٧	00001010	0 0 0 0 0 Ai	Data		-	\$	\$	-	_	3	Ai ← Ai ⊕ V
	Ai,Ki	L	0 1 0 0 1 0 1 0	0 0 Ai Ki			1-	\$	\$	_		3	Ai ← Ai ⊕ Ki
	Ai, <adr></adr>	D	00001010	0 0 1 0 0 Ai	Adr (H)	Adr (L)	1 -		\$	_	_	4	Ai ← Ai ⊕ <adr></adr>
	Ai, <cd></cd>	K	00001010	0 1 0 0 0 Ai			-	•	\$	-	_	6	Ai <b>←</b> Ai ⊕ < <cd>&gt;</cd>
XOR	Ai, <sk+s></sk+s>	s	00001010	0 1 1 0 0 Ai	S		1-	\$	-	_		7	Ai ← Ai ⊕ <sk+s></sk+s>
	Ai, <sk+s>+R</sk+s>	_	00001010			R	1 -	+:	+ ; +		_	-	Ai ← Ai ⊕ <sk+s>+R</sk+s>
	Ai, <sk+s>-R</sk+s>		00001010		S	R	1 -	<b>*</b>	1	_	_	7	Ai ← Ai ⊕ <sk+s> - R</sk+s>
	Ai,<\$K+CD+\$>	_	00001010		S		-	+ :	\$	_		8	Ai ← Ai ⊕ <\$K+CD+\$>
	Ai, <yg+s></yg+s>	-	00001010				-	+;	<b>*</b>	_	$\vdash$	7	Ai ← Ai ⊕ <yg+\$></yg+\$>

						0	PΕ	RΑ	TΤ	0 1	1 -1										
Oper	Op Code	Adr							ln	struc	ction Fo	ormat			S	tatu	s Flo	ags		Α	Explanation
Opei	Op Code	met	1. B	yte			2.	Byte	)		3. Byt	ei	4. Byte		T	S	Ν	Υ	Е		
	Ki	L	0100	1	0 1 1	0	1		Ki						0	1	0	0	0	3	Ki <b>←</b> 0
	<adr></adr>	D	0000	1	0 1 1	0	0 1 0	) [			Adr (\	'ük)	Adr (Dü	ş)	0	1	0	0	0	4	<adr> ← 0</adr>
	<cd></cd>	-	0000	-		0	100	0 1							0	1	0	0	0	6	< <cd>&gt; ← 0</cd>
CLR	<sk+s></sk+s>	-	0000	$\rightarrow$		0	1 1 0	) [							0	1	0	0	0	7	<\$K+\$> <b>←</b> 0
CLIX	<sk+s>+R</sk+s>		0000			1	000	) 1					R		0	1	0	0	0	7	<\$K+\$> <b>←</b> 0, + R
	<\$K+\$>-R	Z	0000	) 1	0 1 1	1	0 1 0	) ]					R		0	1	0	0	0	7	<\$K+\$> <b>←</b> 0, - R
	<sk+cd+s></sk+cd+s>	_	0000	_	0 1 1	1	100	0 1							0	1	0	0	0	8	<\$K+CD+ <b>\$</b> > <b>←</b> 0
	<yg+\$></yg+\$>	Υ	0000	) 1	0 1 1	1	1 1 0	) [							0	1	0	0	0	7	<yg+\$><b>←</b>0</yg+\$>
	Ki	L	0 1 0 1	0	000	0	1		Ki						\$	<b>\$</b>	\$	_	\$	3	Ki ← Ki + 1
	<adr></adr>	D	0001	0	000	0	0 1 0	) [			Adr (\	'ük)	Adr (Dü	ş)	\$	<b>\$</b>	\$	_	\$	4	<adr> ← <adr> + 1</adr></adr>
INC	<cd></cd>	K	0001	0	000	0	100	) [							\$	\$	\$	_	\$	6	< <cd>&gt; ← &lt;<cd>&gt; + 1</cd></cd>
1110	<\$K+\$>	S	0 0 0 1	0	000	0	1 1 0	) [							\$	<b>\$</b>	\$	_	\$	7	<\$K+\$> ← <\$K+\$> + 1
	<\$K+\$>+R	R	0001	0	000	1	000	) [1					R		\$	<b>\$</b>	\$	_	\$	7	<\$K+\$> ← <\$K+\$> + 1, + R
	<\$K+\$>-R	Z	0001	0	000	1	0 1 0	) 1					R		\$	<b>\$</b>	\$	_	\$	7	<\$K+\$> ← <\$K+\$> + 1, - R
	<sk+cd+s></sk+cd+s>	U	0001	0	000	1	100	0 1							\$	\$	\$	-	\$	8	<\$K+CD+\$> <b>←</b> <\$K+CD+\$> + 1
	<yg+\$></yg+\$>	Υ	0001	0	000	1	1 1 0	) [			(				\$	\$	\$	_	\$	7	<yg+\$> ← <yg+\$> + 1</yg+\$></yg+\$>
	Ki	L	0 1 0 1	0	0 0 1	0	1		Ki						<b>\$</b>	\$	\$	_	\$	3	Ki <b>←</b> Ki - 1
	<adr></adr>	D	0001	0	0 0 1	0	0 1 0	) [			Adr (\	'ük)	Adr (Dü	ş)	<b>\$</b>	<b>\$</b>	\$	_	\$	4	<adr> ← <adr> - 1</adr></adr>
DEC	<cd></cd>	K	0001	0	0 0 1	0	100	) ]		<u></u>					<b>\$</b>	\$	\$	_	\$	6	< <cd>&gt; ← &lt;<cd>&gt; - 1</cd></cd>
DLC	<\$K+\$>	S	0001	0	0 0 1	0	1 1 0	)   1			5	;			<b>\$</b>	\$	\$	_	\$	7	<\$K+\$> ← <\$K+\$> - 1
	<sk+s>+R</sk+s>	R	0001	0	0 0 1	1	000	) [			9		R		\$	\$	\$	_	\$	7	<\$K+\$> ← <\$K+\$> - 1, + R
	<\$K+\$>-R	Z	0001	0	0 0 1	1	0 1 0	) 1					R		\$	\$	\$	_	\$	7	<\$K+\$> ← <\$K+\$> - 1, -R
	<sk+cd+s></sk+cd+s>	U	0001	0	0 0 1	1	100	) 1							<b>\$</b>	<b>\$</b>	\$	_	\$	8	<\$K+CD+\$> <b>←</b> <\$K+CD+\$> - 1
	<yg+\$></yg+\$>	Υ	0001	0	0 0 1	1	1 1 0	) 1							<b>\$</b>	\$	\$	_	\$	7	<yg+\$> <b>←</b> <yg+\$> - 1</yg+\$></yg+\$>
	Ki	L	0 1 0 1	0	0 1 0	0	1		Ki						_	\$	\$	_	_	3	Ki ← com <ki></ki>
	<adr></adr>	D	0001	0	0 1 0	0	010	) 1			Adr (\	'ük)	Adr (Dü	ş)	_	\$	\$	_	_	4	<adr> ← com<adr></adr></adr>
	<cd></cd>	K	0001	0	0 1 0	0	100	)		<u></u>					_	\$	\$	_	-	6	< <cd>&gt; ← com&lt;<cd>&gt;</cd></cd>
COM	<\$K+\$>	_	0 0 0 1	=		==	1 1	A/A			3				_	<b>‡</b>	\$	-	_	7	<\$K+\$> ← com<\$K+\$>
	<sk+s>+R</sk+s>	R	0001	0	0 1 0	1	00	111					R		_	<b>\$</b>	\$	-	_	7	<\$K+\$> ← com<\$K+\$>, + R
	<\$K+\$>-R	Z	0001	0	0 1 0	1	01	111			(		R		_	<b>\$</b>	\$	-	_	7	<\$K+\$> <b>←</b> com<\$K+\$>, - R
	<sk+cd+s></sk+cd+s>	U	0001	0	0 1 0	1	100	111							_	\$	\$	-	_	8	<sk+cd+\$>◆ com<sk+cd+\$></sk+cd+\$></sk+cd+\$>
	<yg+s></yg+s>	Υ	0001	0	0 1 0	1	1 1	1			5				_	<b>\$</b>	\$	-		7	<yg+\$></yg+\$>

				OPERATIO	DN - II								
Oper	Op Code	Adr		Inst	ruction Format		S	tatu	is Flo	ags		Α	Explanation
Opei	Op Code	met	1. Byte	2. Byte	3. Bytei	4. Byte	T	S	N	Υ	Е		
	Ki	L	0 1 0 1 0 0 1 1	0 1 Ki			_	\$	\$	_		3	Ki ← neg <ki></ki>
	<adr></adr>	D	00010011	00101	Adr (Yük)	Adr (Düş)	_	\$	\$	_	-	4	<adr> ← neg<adr></adr></adr>
	<cd></cd>	К	00010011	01001			_	\$	\$	_		6	< <cd>&gt;→ neg<cd>&gt;</cd></cd>
NEG	<sk+s></sk+s>	S	00010011	01101	S		_	\$	\$	_		7	<\$K+\$> ← neg<\$K+\$>
NEG	<SK $+$ S $>$ +R	R	00010011	10001	S	R	_	\$	\$	_	-	7	<\$K+\$> ← neg<\$K+\$>, + R
	<\$K+\$>-R	Z	0 0 0 1 0 0 1 1	10101	S	R	_	\$	\$	_	_	7	<\$K+\$> ← neg<\$K+\$>, - R
	<\$K+CD+\$>	U	00010011	1 1 0 0 1	S		-	\$	\$	-	-	8	<\$K+CD+\$>◆ neg<\$K+CD+\$>
	<yg+\$></yg+\$>	Υ	0 0 0 1 0 0 1 1	1 1 1 0 1	S		-	\$	\$	_	-	7	<yg+\$> ← neg<yg+\$></yg+\$></yg+\$>
	N,Ki	L	0 1 0 0 1 1 0 1	1 1 N Ki			-	\$	\$	_	-	3	Ki ← Ki(N=0)
	N, <adr></adr>	D	00001101	0 0 1 1 0 N	Adr (Yük)	Adr (Düş)	-	\$	\$	_	-	4	<adr> ← <adr,n=0></adr,n=0></adr>
CLR	N, <cd></cd>	K	00001101	0 1 0 1 0 N			_	\$	\$	_	-	6	< <cd>&gt; ← <cd,n=0>&gt;</cd,n=0></cd>
CLIK	N, <sk+s></sk+s>	S	00001101	0 1 1 1 0 N	S		-	\$	\$	_		7	<\$K+\$> ← <\$K+\$,N=0>
	N, <sk+s>+R</sk+s>	R	00001101	1 0 0 1 0 N	S	R	_	\$	\$	_	-	7	<\$K+\$> ← <\$K+\$,N=0>, + R
	N, <sk+s>-R</sk+s>	Z	00001101	1 0 1 1 0 N	S	R	-	\$	\$	_		7	<\$K+\$> ← <\$K+\$,N=0>, - R
	N, <sk+cd+s></sk+cd+s>	U	00001101	1 1 0 1 0 N	S		-	\$	\$	_	-	8	<\$K+CD+\$> <b>←</b> <\$K+CD+\$,N=0>
	N, <yg+\$></yg+\$>	Υ	00001101	1 1 1 1 0 N	S		-	\$	\$	_	-	7	<yg+\$> <b>←</b> <yg+\$,n=0></yg+\$,n=0></yg+\$>
	N,Ki	L	0 1 0 0 1 1 1 1	1 1 N Ki			-	\$	\$	-		3	Ki ← Ki(N=1)
	N, <adr></adr>	D	00001111	0 0 1 1 0 N	Adr (Yük)	Adr (Düş)	-	\$	\$	_	-	4	<adr> ← <adr, n="1"></adr,></adr>
SET	N, <cd></cd>	K	0 0 0 0 1 1 1 1	0 1 0 1 0 N			_	\$	\$	_	_	6	< <cd>&gt;→ <cd,n=1>&gt;</cd,n=1></cd>
JLI	N, <sk+s></sk+s>	S	00001111	0 1 1 1 0 N	S		-	\$	\$	-	-	7	<\$K+\$> <b>←</b> <\$K+\$,N=1>
	N, <sk+s>+R</sk+s>	R	00001111	10010 N	S	R	-	\$	\$	_	-	7	<\$K+\$> ← <\$K+\$,N=1>, + R
	N, <sk+s>-R</sk+s>	Z	0 0 0 0 1 1 1 1	<b>1</b> 0 1 1 0 N	S	R	-	\$	\$	_	-	7	<\$K+\$> ← <\$K+\$,N=1>, - R
	N, <sk+cd+s></sk+cd+s>	U	0 0 0 0 1 1 1 1	1 1 0 1 0 N	S		-	\$	\$	_	-	8	<\$K+CD+\$> <b>◆</b> <\$K+CD+\$,N=1>
	N, <yg+\$></yg+\$>	Υ	0 0 0 0 1 1 1 1	1 1 1 1 0 N	S		_	\$	\$	_		7	<yg+\$> ← <yg+\$,n=1></yg+\$,n=1></yg+\$>

			O P E R	ATION I	NSTR	UC	TIC	N S				
Oper	Op Code	Adr	Instruct	on Format			Statu	ıs Reç	j.		А	Explanation
- 1	op code	met	1. Byte	2. Byte		T	S	Ν	Υ	Е		
	Е	L	01001100	10	000	_	_	_	_	0	1	E ← 0
	Υ	L	01001100	10	001	_	_	_	0	-	1	Y <b>←</b> 0
CLR	N	L	01001100	10	0 1 0	_	_	0	_	_	1	N <b>←</b> 0
	S	L	01001100	10	0 1 1	_	0	_	_	_	1	S ← 0
	T	L	01001100	10	100	0	_	_	_	_	1	T ← 1
	E	L	01001110	10	000	_	_	_	_	1	1	E ← 1
	Υ	L	01001110	10	0 0 1	_	_	_	1	_	1	Y← 1
SET	N	L	01001110	10	0 1 0	_	_	1	_	_	1	N <b>←</b> 1
	S	L	01001110	10	0 1 1	-	1	_	_	_	1	S ← 1
	T	L	01001110	1 0	100	1	_	_	_	_	1	T ← 1
INC	Kii	L	01110000	0 1	Kii	\$	\$	<b>‡</b>	_	\$	2	Kii ← Kii + 1
DEC	Kii	L	0 1 1 1 0 0 0 1	0 1	Kii	\$	\$	<b>‡</b>	_	\$	2	Kii ← Kii - 1
DAA	Ai	L	01010100	0 1	Ai	_	_	_	0	0	2	Binary to Decimal
PSH	Ai	L	01010101	0 1	Ai	_	_	_	_	_	2	Push Ai to Stack
PUL	Ai	L	01010110	0 1	Ai	-	\$	\$	_	_	2	Pull Stock to Ai
EIN		L	11000000			_	_	-	_	_	1	Enable Interrupt
DIN		L	11000001			_	_	_	_	_	1	Disable Interrupt
NOP		L	11000010			_	_	_	_	_	1	No Operation
RTS		L	11000100			_	_	_	_	_	5	Return fron subroutine
RTI		L	1 1 0 0 0 1 0 1			_	_	_	_	_	15	Return from interrupt
INT		L	11000011			_	_	_	_	_	15	Software Interrupt

				SHIFT	&ROTATE	INSTRUC	TIC	N	S				
		Adr		Instruction	Format		St	atus	Re	g.		Α	Contamortica
Oper	Op Code	met	1. Byte	2. Byte	3. Byte	4. Byte	Т	S	Ν	Υ	Е	А	Explanation
	Ki	L	01010111	0 1 Ki			-	<b>\$</b>	<b>\$</b>	-	<b>\$</b>	1	
	<adr></adr>	D	00010111	00101	Adr (H)	Adr (L)	_	\$	<b>\$</b>	-	<b>\$</b>	2	
	<cd></cd>	К	00010111	01001			_	<b>\$</b>	<b>\$</b>	_	<b>\$</b>	3	
LSL	<\$K+\$>	S	00010111	01101	S		_	<b>\$</b>	<b>\$</b>	_	<b>\$</b>	4	E V7 V6 V3 V4 V3 V2 VI V0
LOL	<\$K+\$>+R	R	00010111	10001	S	R	_	<b>\$</b>	<b>\$</b>		<b>\$</b>	5	
	<\$K+\$>-R	Z	00010111	10101	S	R	_	<b>\$</b>	<b>\$</b>	_	<b>\$</b>	5	1
	<sk+cd+s></sk+cd+s>	U	00010111	11001	S		_	<b>\$</b>	<b>\$</b>	_	\$	6	
	<yg+\$></yg+\$>	Υ	00010111	1 1 1 0 1	S		_	<b>\$</b>	<b>\$</b>	_	<b>\$</b>	4	
	Ki	L	01011000	0 1 Ki			_	<b>\$</b>	<b>\$</b>	-	<b>\$</b>	1	
	<adr></adr>	D		00101	Adr (H)	Adr (L)	_	<b>\$</b>	<b>\$</b>	-	<b>\$</b>	2	
LSR	<cd></cd>	К	00011000				_	<b>\$</b>	<b>\$</b>	$\rightarrow$	<b>\$</b>	3	
	<\$K+\$>	S	00011000		S		_	-	<b>\$</b>	$\rightarrow$	<b>\$</b>	4	V7 V6 V5 V4 V3 V2 V1 V0 E
	<\$K+\$>+R	R	00011000	10001	S	R	-	<b>\$</b>	<b>♦</b>	-	<b>*</b>	5	
	<sk+s>-R</sk+s>	Z	00011000	10101	S	R	_	\$	<b>\$</b>	-	<b>\$</b>	5	0
	<sk+cd+s></sk+cd+s>	U	00011000	11001	S		_	\$	<b>\$</b>	-	\$	6	
	<yg+\$></yg+\$>	Υ	00011000	11101	S		-	\$	<b>\$</b>	-	\$	4	
	Ki	L	01011001	0 1 Ki			-	\$	<b>\$</b>	-	<b>\$</b>	1	
	<adr></adr>	D	00011001	00101	Adr (H)	Adr (L)	_	\$	<b>\$</b>	$\rightarrow$	<b>\$</b>	2	
ASR	<cd></cd>	K	00011001	01001			_	\$	<b>\$</b>	-	\$	3	
, tort	<sk+s></sk+s>	S	00011001	01101	S		-	-	<b>\$</b>	-	<b>*</b>	4	V7 V6 V5 V4 V3 V2 V1 V0 E
	<\$K+\$>+R	R	00011001	10001	S	R	-		<b>♦</b>	$\rightarrow$	<b>\$</b>	5	
	<sk+s>-R</sk+s>	Z	00011001	10101	S	R	_	\$	<b>\$</b>	$\rightarrow$	<b>\$</b>	5	
	<\$K+CD+\$>	U	00011001	11001	S		-	\$	<b>\$</b>	-	<b>\$</b>	6	
	<yg+\$></yg+\$>	Υ	00011001	1 1 1 0 1	S		_	<b>\$</b>	<b>*</b>	-	<b>\$</b>	4	
	Ki	L	01011010	0 1 Ki			-	<b>\$</b>	<b>♦</b>	-	-	1	
	<adr></adr>	D	00011010	00101	Adr (H)	Adr (L)	-	•	<b>\$</b>	-	-	2	
	<cd></cd>	K		01001			_	\$	<b>\$</b>	-	_	3	
ROL	<\$K+\$>	S		01101	S		-	_	<b>\$</b>	-	-	4	
	<sk+s>+R</sk+s>	R	<del></del>	10001	S	R	_	<del>-</del>	<b>\$</b>	-	-	5	E V7 V6 V5 V4 V3 V2 V1 V0
	<sk+s>-R</sk+s>	+-	00011010		S	R	_	-	<b>\$</b>	-	-	5	
	<sk+cd+s></sk+cd+s>	U		11001	S		-		<b>\$</b>	-	-	6	
	<yg+\$></yg+\$>	Υ	00011010	22000	S		-	<b>\$</b>	<b>\$</b>	-	-	4	
	Ki	L	01011011	0 1 Ki			_		<b>\$</b>	-	-	1	
	<adr></adr>	D	00011011	00101	Adr (H)	Adr (L)	-	-	<b>\$</b>	-	-	2	
	<cd></cd>	K		01001			-		<b>\$</b>	-	-	3	
ROR	<sk+s></sk+s>	S		01101	S		-	_	•	-	-	4	
	<\$K+\$>+R	R	00011011	10001	S	R	_	_	<b>\$</b>	-	-	5	V7 V6 V5 V4 V3 V2 V1 V0 E
	<sk+s>-R</sk+s>	Z	00011011		S	R	-	_	<b>\$</b>	-	-	5	V/ V0 V3 V4 V3 V2 V1 V0 E
	<sk+cd+s></sk+cd+s>	-	00011011		Š		-	$\overline{}$	<b>\$</b>	-	-	6	
	<yg+\$></yg+\$>	Υ	00011011	111101	S S		_	<b>\$</b>	<b>\$</b>	-	-	4	

				COM	1 P <i>A</i>	ARE INSTRU	CTION	S					
Oper	Op Code	Adr				Format	011011		Stat	tus R	eg.	Α	Explanation
Ореі	Op Code	met	1. Byte	2. Byte	9	3. Byte	4. Byte	T	S	N	Y E		
	Ki,V	٧	00011100	00000	Ki	Data		\$	<b>\$</b>	<b>\$</b>	<b>*</b>   <b>*</b>	2	Ki - V
	Ki,Kj	L	0 1 0 1 1 1 0 0	0 0 Ki I	Kj			<b>\$</b>	<b>*</b>	<b>\$</b>	<b>*</b>   <b>*</b>	2	Ki - Kj
	Ki, <adr></adr>	D	00011100	00100	Ki	Adr (H) Ad	dr (L)	\$	<b>\$</b>	<b>\$</b>	<b>*</b>   <b>*</b>	3	Ki - <adr></adr>
	Ki, <cd></cd>	Κ	00011100	01000	Ki			\$	<b>*</b>	<b>\$</b>	<b>*</b>   <b>*</b>	3	Ki - < <cd>&gt;</cd>
CMP	Ki, <sk+s></sk+s>	S	00011100	01100	Ki	S		<b>\$</b>	\$		<b>*</b>   <b>*</b>	4	Ki - <sk+s></sk+s>
CIVIP	Ki, < \$K+\$>+R	R	00011100	10000	Ki	S	R	<b>\$</b>	<b>\$</b>	<b>\$</b>	<b>\$</b>   <b>\$</b>	5	Ki - <\$K+\$>+R
	Ki, <sk+s>-R</sk+s>	Z	0 0 0 1 1 1 0 0	10100	Ki	S	R	#	<b>\$</b>	<b>\$</b>	<b>\$</b>   <b>\$</b>	5	Ki - <\$K+\$> - R
	Ki, <sk+cd+s></sk+cd+s>	С	0 0 0 1 1 1 0 0	11000	Ki	S		<b>\$</b>	<b>*</b>	<b>\$</b>	<b>*</b>   <b>*</b>	6	Ki - <\$K+CD+\$>
	Ki, <yg+\$></yg+\$>	Υ	0 0 0 1 1 1 0 0	111100	Ki	S		<b>\$</b>	<b>\$</b>	<b>\$</b>	<b>* *</b>	5	Ki - <yg+\$></yg+\$>
	Kii,VV	٧	0 0 1 1 1 1 0 0	00000	Kii	Data (H)	ata (L)	\$	\$	<b>\$</b>	- \$	4	Kii - VV
ı	Kii,Kjj	L	0 1 1 1 1 1 0 0	0 0 Kii l	Kjj			<b>\$</b>	<b>\$</b>	<b>\$</b>	- +	4	Kii - Kjj
	Kii, <adr></adr>	D	0 0 1 1 1 1 0 0	00100	Kii	Adr (H) Ad	dr (L)	\$	<b>\$</b>	<b>\$</b>	-   \$	5	Kii - ( <adr>+<adr+1>)</adr+1></adr>
CMP	Kii, <cd></cd>	K	0 0 1 1 1 1 0 0	01000	Kii			\$	<b>\$</b>	<b>\$</b>	- \$	5	Kii - (< <cd>&gt;+&lt;<cd+1>&gt;)</cd+1></cd>
CIVII	Kii, < SK+S>	S	0 0 1 1 1 1 0 0	01100	Kii	S		<b>\$</b>	\$	<b>\$</b>	-   \$	6	Kii - ( <sk+s>+<sk+s+1>)</sk+s+1></sk+s>
	Kii, < SK+S>+R	R	0 0 1 1 1 1 0 0	10000	Kii	S	R	<b>\$</b>	<b>\$</b>	<b>\$</b>	- \$	7	Kii - ( <sk+s>+<sk+s>) +R</sk+s></sk+s>
ı	Kii, < SK+S>-R	Z	0 0 1 1 1 1 0 0	10100	Kii	S	R	<b>\$</b>	<b>\$</b>	<b>\$</b>	- +	7	Kii - ( <sk+s>+&gt;SK+S+1&gt;) - R</sk+s>
ı	Kii, < SK+CD+S>	U	0 0 1 1 1 1 0 0	11000	Kii	S		<b>\$</b>	<b>\$</b>	<b>\$</b>	- \$	8	Kii - ( <sk+cd+\$>+<sk+cd+\$+1></sk+cd+\$+1></sk+cd+\$>
ı	Kii, <yg+\$></yg+\$>	Υ	0 0 1 1 1 1 0 0	11100	Kii	S		\$	<b>\$</b>	<b>\$</b>	- +	7	Kii - ( <yg+\$>+<yg+\$>)</yg+\$></yg+\$>
	Ki,V	٧	0 0 0 1 1 1 0 1	00000	Ki	Data		-	\$	\$		2	Ki • V
	Ki,Kj	L	0 1 0 1 1 1 0 1	0 0 Ki I	Kj				<b>\$</b>	<b>\$</b>		2	Ki • Ki
	Ki, <adr></adr>	D	0 0 0 1 1 1 0 1	00100	Ki	Adr (H) Ad	dr ( L)	-	<b>\$</b>	\$		3	Ki • < Adr>
DIT	Ki, <cd></cd>	K	0 0 0 1 1 1 0 1	01000	Ki			-	<b>\$</b>	<b>\$</b>		3	Ki •< <cd>&gt;</cd>
BIT	Ki, <sk+s></sk+s>	S	0 0 0 1 1 1 0 1	01100	Ki	S		-	<b>\$</b>	<b>\$</b>		4	Ki • < SK+S>
	Ki, <sk+s>+R</sk+s>	R	0 0 0 1 1 1 0 1	10000	Ki	S	R	-	<b>\$</b>	<b>\$</b>		5	Ki • < SK+S> +R
	Ki, <sk+s>-R</sk+s>	Z	0 0 0 1 1 1 0 1	10100	Ki	S	R	-	<b>\$</b>	<b>\$</b>		5	Ki • < SK+S> - R
	Ki,<\$K+CD+\$>	U	0 0 0 1 1 1 0 1	1 1 0 0 0	Ki	S		-	<b>\$</b>	<b>\$</b>		6	Ki • < SK+CD+S>
	Ki, <yg+\$></yg+\$>	Υ	0 0 0 1 1 1 0 1	111100	Ki	S		-	<b>\$</b>	<b>\$</b>		5	Ki • <yg+\$></yg+\$>

		JUMP & BRANCH INSTRUCTIONS		
Op Code	Adr met	Instruction Format  1. Byte 2. Byte 3. Byte 4. Byte	А	Explanation
BRA V	В	1 0 0 0 0 0 0 0 Step count	2	Branch Always (V step)
JMP Adr	D	0 0 0 1 1 1 1 1 0 0 0 1 0 1 Adr (H) Adr (L)	2	Jump Always (To address)
JMC S,Adr	D	0 0 0 1 1 1 1 1 0 0 1 1 1 0 1 1 Adr (H) Adr (L)	3	S=1 => jump to address
JMC N,Adr	D	0 0 0 1 1 1 1 1 0 0 1 1 1 0 1 0 Adr (H) Adr (L)	3	N=1 => jump to address
JMC E,Adr	D	0 0 0 1 1 1 1 1 0 0 1 1 1 0 0 0 Adr (H) Adr (L)	3	E=1 => jump to address
JMC T,Adr	D	0 0 0 1 1 1 1 1 0 0 1 1 1 1 1 0 0 Adr (H) Adr (L)	3	T=1 => jump to address
BEQ	В	1 0 0 0 0 0 0 1 Step count	2	Branch if equal (V step)
BNE	В	1 0 0 0 0 0 1 0 Step count	2	Branch if not equal (V step)
BGT V	В	1 0 0 0 0 0 1 1 Step count	2	Branch if greater (V step)
BGE V	В	1 0 0 0 0 1 0 0 Step count	2	Branch if greater or equal
BLS V	В	1 0 0 0 0 1 0 1 Step count	2	Branch if less than
BHI V	В	1 0 0 0 0 1 1 0 Step count	2	Branch if higher
BHE V	В	1 0 0 0 0 1 1 1 1 Step count	2	Branch if higher or equal
BLO V	В	1 0 0 0 1 0 0 0 Step count	2	Branch if lower
BIO V	В	1 0 0 0 1 0 0 1 Step count	2	T=1 => jump V step
BNO V	В	1 0 0 0 1 0 1 0 Step count	2	T=0 => jump V step
BIC V	В	1 0 0 0 1 0 1 1 Step count	2	E=1 => jump V step
BNC V	В	1 0 0 0 1 1 0 0 Step count	2	E=0 => jump V step
BIH V	В	1 0 0 0 1 1 0 1 Step count	2	Y=1 => jump V step
BNH V	В	1 0 0 0 1 1 1 0 Step count	2	Y=0 => jump V step
BSR V	В	1 0 0 0 1 1 1 1 Step count	2	Branch to subprogram (V step)
JSR Adr	D	0 0 0 1 0 1 0 0 0 0 1 0 1 Adr (H) Adr (L)	5	Branch to subprogram (Address)
BSC S,V	В	1 0 0 1 0 0 1 1 Step count	6	S=1 => jump to subprogram (V step)
BSC N,V	В	1 0 0 1 0 0 1 0 Step count	6	N=1 = > jump to subprogram (V step)
BSC E,V	В	1 0 0 1 0 0 0 0 Step count	6	E=1 => jump to subprogram (V step)
BSC T,V	В	1 0 0 1 0 1 0 0 Step count	6	T=1 => jump to subprogram (V step)
BSC S,Adr	D	0 0 0 1 0 1 0 1 0 0 1 1 1 0 1 1 Adr (H) Adr (L)	6	S=1 => jump to subprogram (Address)
BSC N,Adr	D	0 0 0 1 0 1 0 1 0 0 1 1 1 0 1 0 Adr (H) Adr (L)	6	N=1 => jump to subprogram (Address)
BSC E,Adr	D	0 0 0 1 0 1 0 1 0 0 1 1 1 0 0 0 Adr (H) Adr (L)	6	E=1 => jump to subprogram (Address)
BSC T,Adr	D	0 0 0 1 0 1 0 1 0 0 1 1 1 1 0 0 Adr (H) Adr (L)	6	T=1 => jump to subprogram (Address)
DBNZ Ki,V	В	1 1 0 0 0 1 1 0 0 1 Ki Step count	8	Decrease Ki, branch if not zero (V step)
DBNZ <adr>,V</adr>	В	1 1 0 0 0 1 1 1 1 Step count Adr (H) Adr (L)	9	Decrease M[adr], branch if not zero (V step)