

IN GOD WE TRUST
PRINCIPLES OF ELECTRONICS
1398-1399 SECOND SEMESTER

Project 2
simulation

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1 Introduction

In this project, the circuit is combination of differential amplifier and output stage with feedback. We should check voltage gain, maximum power of a 8 Load and DC power. We also draw frequency response of output and check its 3dB bandwidth. Node numbers and circuit design are like below.

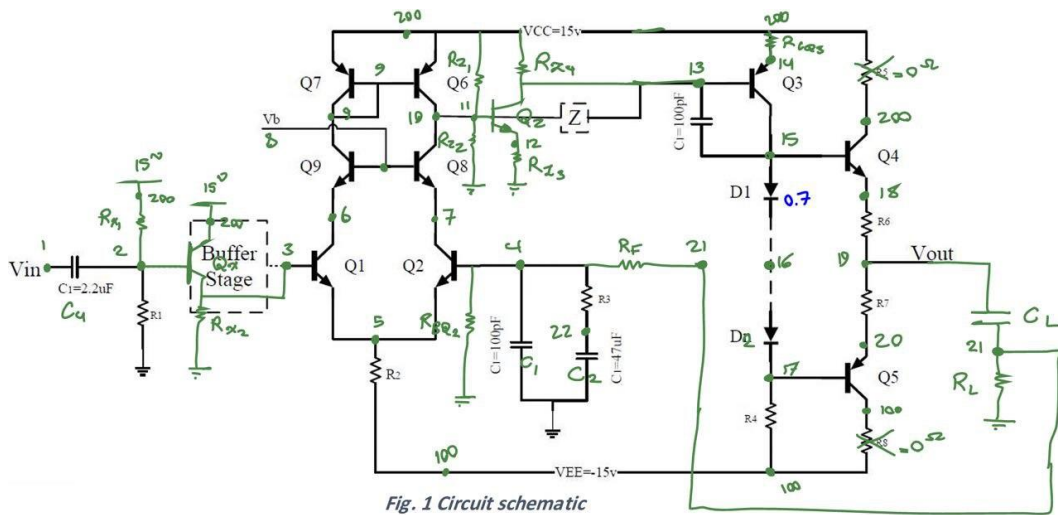


Figure 1: Design and number of the circuit nodes



2 Circuit bias

As we can see, bias of the node's voltages and bias of transistors are similar to our theoretic calculation.

```
*** BEGIN: Saved Operating Point ***
.option
+ gmindc= 1.0000p
.nodeset
+ 1 = 0.
+ 2 = 647.4257m
+ 3 = -87.1183u
+ 4 = -16.7388u
+ 5 = -650.6750m
+ 6 = 1.3521
+ 7 = 1.3491
+ 8 = 2.0000
+ 9 = 14.3494
+ 10 = 2.1777
+ 11 = 2.1777
+ 12 = 1.5173
+ 13 = 7.5397
+ 14 = 8.2293
+ 15 = 316.8204m
+ 16 = -363.3289m
+ 17 = -1.0435
+ 18 = -360.1126m
+ 19 = -363.2199m
+ 20 = -366.3273m
+ 21 = -886.8225n
+ 22 = 0.
+ 100 = -15.0000
+ 200 = 15.0000
*** END: Saved Operating Point ***
```

Figure 2: circuit nodes' voltages

There is just a little difference between collector current of Q_3 based on difference from what we assumed of V_{BEon} and its real values that we can see below.



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**** bipolar junction transistors

| subckt element model | 0:qx1 0:q2n3904 | 0:q1 0:q2n3904 | 0:q2 0:q2n3904 | 0:q8 0:q2n3904 | 0:q9 0:q2n3904 | 0:q6 0:q2n3906 |
|----------------------------|--------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| ib | 2.9224u | 3.2930u | 3.3020u | 3.3296u | 2.9612u | -4.9397u |
| ic | 1.0004m | 998.8092u | 1.0015m | 998.1648u | 995.8480u | -1.1055m |
| vbe | 647.5128m | 650.5878m | 650.6582m | 650.8721m | 647.8517m | -650.6323m |
| vce | 15.0001 | 2.0028 | 1.9998 | 828.5258m | 12.9972 | -12.8223 |
| vbc | -14.3526 | -1.3522 | -1.3491 | -177.6537m | -12.3494 | 12.1717 |
| vs | -14.9999 | -1.3520 | -1.3490 | -2.1776 | -14.3493 | -14.3495 |
| power | 15.0075m | 2.0026m | 2.0049m | 829.1724u | 12.9452m | 14.1779m |
| betad | 342.3090 | 303.3093 | 303.2981 | 299.7861 | 336.3027 | 223.7920 |
| gm | 38.8435m | 38.7713m | 38.8753m | 38.7452m | 38.6669m | 42.9125m |
| rpi | 8.7913k | 7.8019k | 7.7807k | 7.7162k | 8.6763k | 5.2011k |
| rx | 20.0000 | 20.0000 | 20.0000 | 20.0000 | 20.0000 | 20.0000 |
| ro | 114.3108k | 101.4730k | 101.1979k | 100.3618k | 112.8177k | 101.4702k |
| cpi | 23.8770p | 23.8630p | 23.8996p | 23.8549p | 23.8164p | 27.8847p |
| cmu | 1.4851p | 2.8467p | 2.8481p | 3.7290p | 1.5565p | 1.7589p |
| cbx | 0. | 0. | 0. | 0. | 0. | 0. |
| ccs | 0. | 0. | 0. | 0. | 0. | 0. |
| betaac | 341.4867 | 302.4889 | 302.4756 | 298.9662 | 335.4839 | 223.1921 |
| ft | 243.7556x | 231.0264x | 231.3166x | 223.5534x | 242.5437x | 230.3948x |

| subckt element model | 0:q7 0:q2n3906 | 0:qz 0:q2n3904 | 0:q3 0:q2n3906 | 0:q4 0:q2n3904 | 0:q5 0:q2n3906 |
|----------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| ib | -4.9420u | 4.8070u | -21.9074u | 9.0662u | -13.6661u |
| ic | -985.9664u | 1.5140m | -4.6476m | 3.0983m | -3.0937m |
| vbe | -650.6323m | 660.3879m | -689.5961m | 676.9330m | -677.1509m |
| vce | -650.6323m | 6.0224 | -7.9124 | 15.3601 | -14.6337 |
| vbc | 0. | -5.3620 | 7.2228 | -14.6832 | 13.9565 |
| vs | -14.3495 | -7.5395 | -7.5401 | -14.9997 | 1.0432 |
| power | 644.7170u | 9.1209m | 36.7887m | 47.5961m | 45.2812m |
| betad | 199.5082 | 314.9544 | 212.1467 | 341.7410 | 226.3766 |
| gm | 38.2726m | 58.7037m | 178.9349m | 119.7634m | 119.5815m |
| rpi | 5.1987k | 5.3447k | 1.1727k | 2.8338k | 1.8800k |
| rx | 20.0000 | 20.0000 | 20.0000 | 20.0000 | 20.0000 |
| ro | 101.4233k | 69.5929k | 23.0707k | 37.0150k | 36.8352k |
| cpi | 26.2609p | 30.8751p | 75.6735p | 52.3077p | 54.8400p |
| cmu | 4.5000p | 2.0017p | 2.0628p | 1.4745p | 1.6854p |
| cbx | 0. | 0. | 0. | 0. | 0. |
| ccs | 0. | 0. | 0. | 0. | 0. |
| betaac | 198.9676 | 313.7543 | 209.8458 | 339.3871 | 224.8097 |
| ft | 198.0202x | 284.1823x | 366.3460x | 354.4096x | 336.6983x |

Figure 3: bias of transistors



3 Results of simulation

3.1 Maximum output power

In the following picture, the input signal was $100\sqrt{2}mV$. The output signal's pick is $2V$ so the output power is:

$$P_{out} = \frac{V_o^2}{2 * R_L} = \frac{4}{2 * 8} = 0.25w$$

and the differential gain is:

$$20\log_{10}A_v = 20\log_{10}\frac{2000}{100 * \sqrt{2}} = 23dB > 10dB$$

and the power calculated above is somehow the maximum power we can inject to an 8Ω resistor because we have limited our output swing.

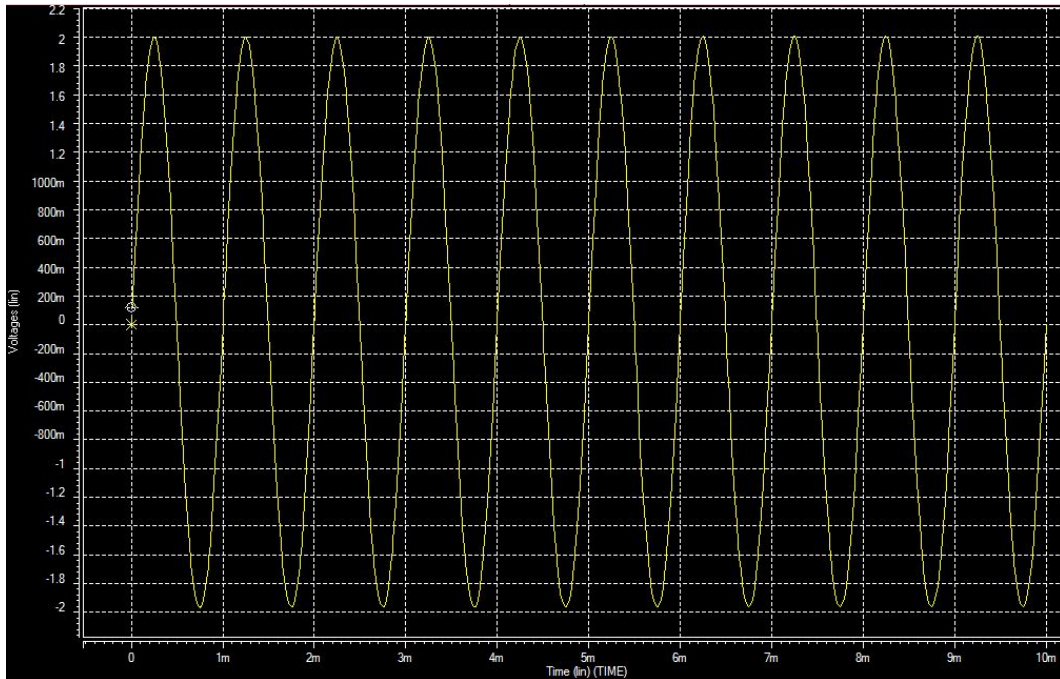


Figure 4: output signal



3.2 DC power

For DC power usage we have :

```
**** voltage sources
subckt
element 0:vcc 0:vee 0:vin1 0:vb
volts 15.0000 -15.0000 0. 2.0000
current -14.3494m 11.7514m 0. -6.2907u
power 215.2406m 176.2703m 0. 12.5815u
total voltage source power dissipation= 391.5235m watts
```

Figure 5: DC power

3.3 Frequency response

As we can see below, our 3dB high frequency band is more than $20kHz$ and 3dB low frequency band is around $10Hz$. So frequency response between $50Hz$ to $20kHz$ is completely flat. Because low band is not clear in first image, we have checked it again with linear command in hSpice.

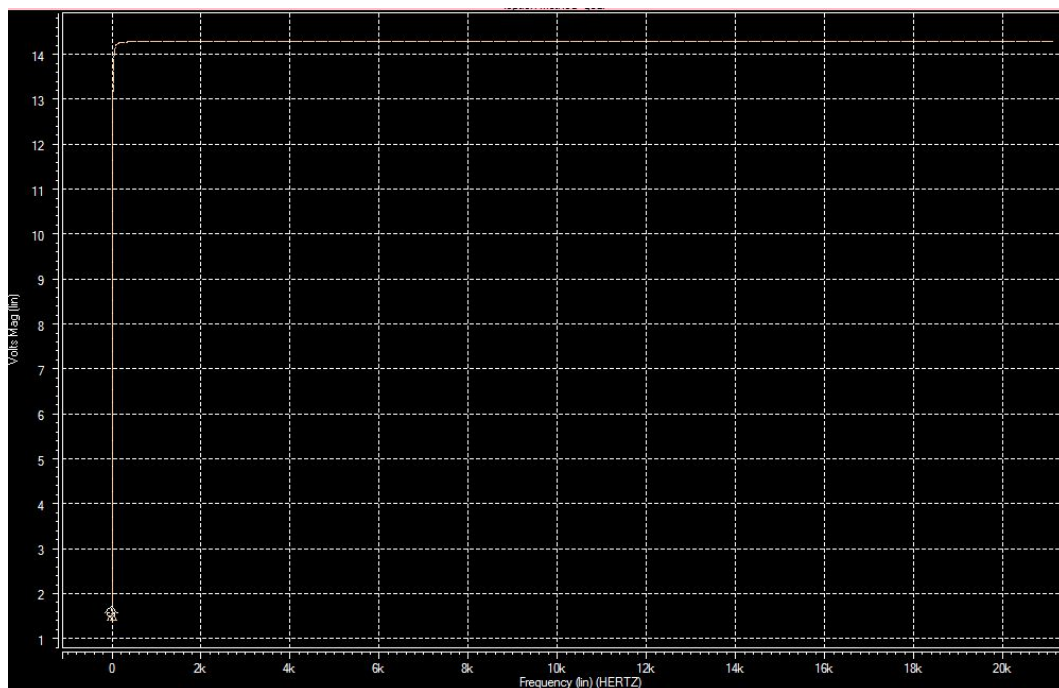


Figure 6: output is completely flat between $50Hz$ to $20kHz$



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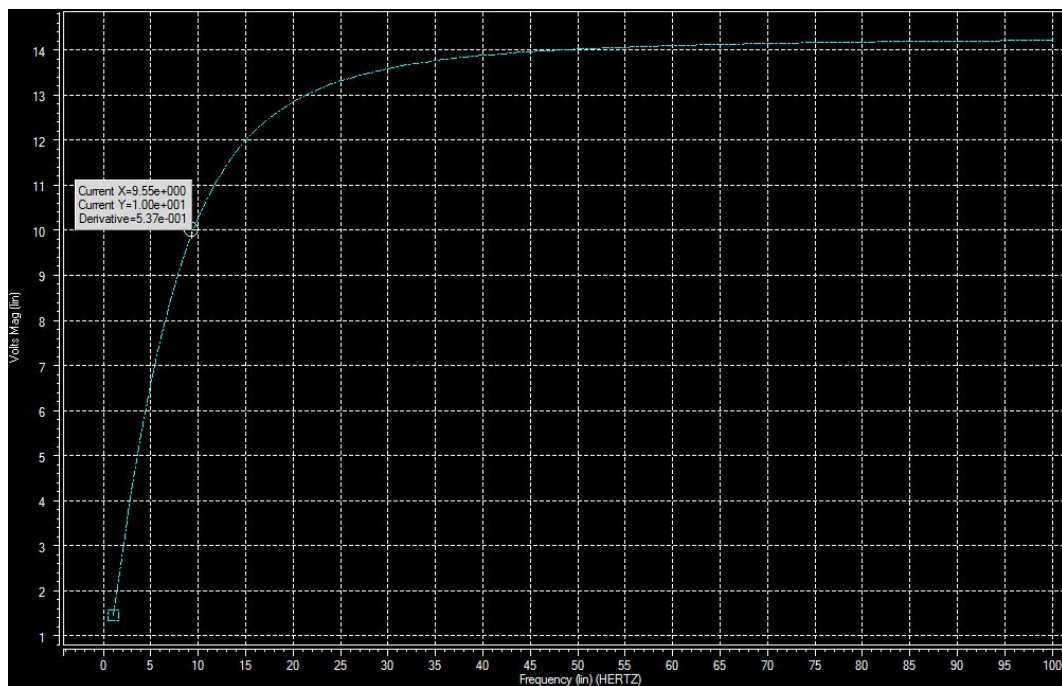


Figure 7: check 3dB low frequency band