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Principles of Electronics

1398-1399 Second Semester

Project

phase 0

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Contents

1 Introduction

The project circuit is differential amplifier and we should check it's differential and common mode gain. We should also check it's CMR. For output swing, the swing is OK and you can see this in the results part. This output swing is because of our output bias in 0 volt using feedback circuit. We made a little change in the gain of feedback because of the orders of input and output signals, the original feedback did not work properly and it diverged.

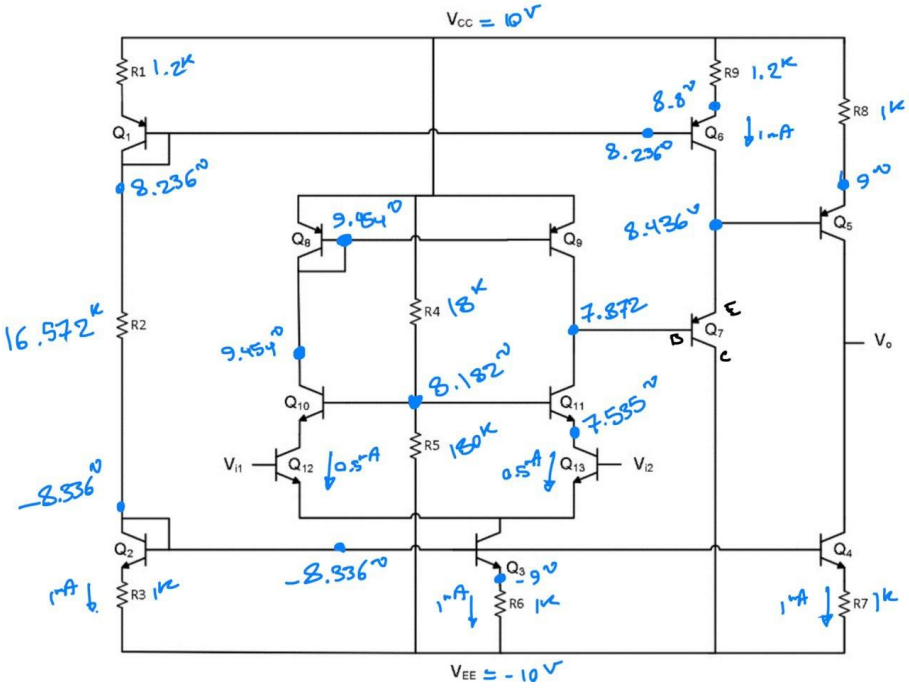

Figure 1: Values of the circuit elements

2 Node names and HSPICE code

You can see node numbers and the feedback's node numbers in the following images.

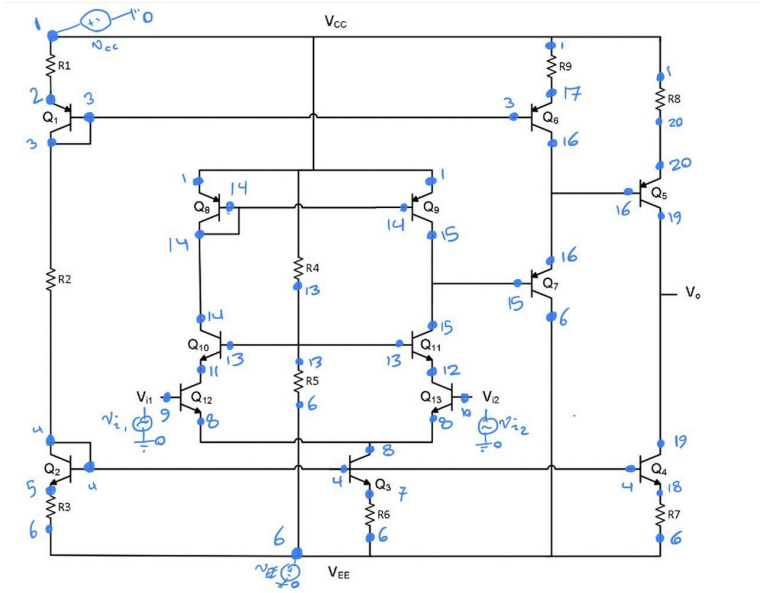

Figure 2: the main circuit node numbers

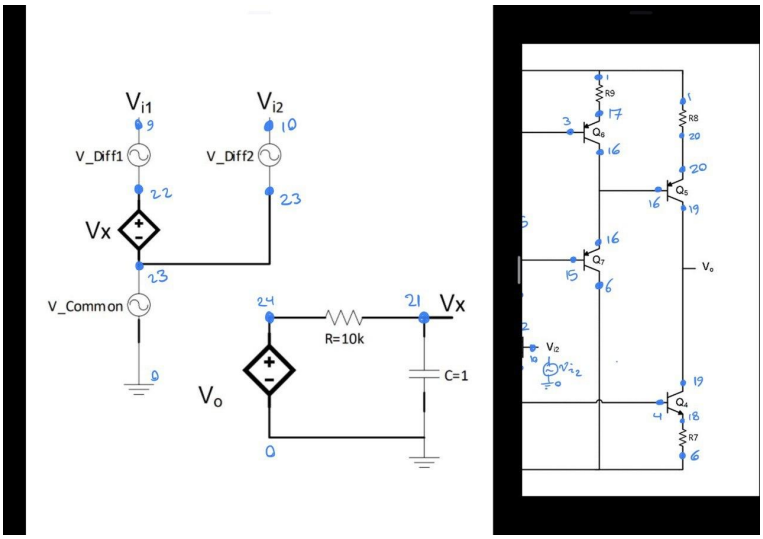

Figure 3: the feedback node numbers

You can also see our HSPICE code in the following image. As you can see, there is little change in the feedback gain to make the circuit converge. There is also four voltage sources. For calculating deferential gain, we should turn Vcmr and Vcom off. Now by giving a value to Vcmr, we put a DC voltage in input and we should increase or decrease this value until we see disorders in output so in this way we will find CMR of input. Finally, to calculate common mode gain, we just turn the Vcom on as our input signal.

```
.option method=GEAR
.option accurate=1

.model NP npn Is=7.049f Bf=150 Vaf=200     *NPN
.model PN pnp Is=336.7f Bf=80 Vaf=150   *PNP
**********************************Netlist**************************
* Sources
Vcc             1               0               10
VEE             0               6               10
Vdif1           9               22              sin(0   -1u     1k    0       0)
Vdif2           10              23              sin(0   1u      1k    0       0)
*Vcom           23              0               sin(0   0       1k    0       0)
Vcmr            23              0               10
E1              24              0               VCCS    19              0       1
E2              22              23              VCCS    21              0       150

* Resistors
R1              1               2               1.2k
R2              3               4               16.572k
R3              5               6               1k
R4              1               13              18k
R5              13              6               180k
R6              7               6               1k
R7              18              6               1k
R8              1               20              1k
R9              1               17              1.2k
R10             21              24              10k

*Capacitors
C1              21              0               10

* Transistors
Q1              3               3               2               PN
Q2              4               4               5               NP
Q3              8               4               7               NP
Q4              19              4               18              NP
Q5              19              16              20              PN
Q6              16              3               17              PN
Q7              6               15              16              PN
Q8              14              14              1               PN
Q9              15              14              1               PN
Q10             14              13              11              NP
Q11             15              13              12              NP
Q12             11              9               8               NP
Q13             12              10              8               NP


**********************************************************************
.op
.tran 1u        15m     start=10m
.end
```

Figure 4: the HSPICE code

3 Results of simulation

3.1 Bias of the circuit

To see bias of the circuit we use .op results and they are as same as our calculated voltages in figure 1.

```
* time =    0.
* temperature =   25.0000
*** BEGIN: Saved Operating Point ***
.option
+ gmindc=   1.0000p
.nodeset
+ 1 =  10.0000
+ 2 =   8.8124
+ 3 =   8.2526
+ 4 =  -8.3514
+ 5 =  -9.0107
+ 6 = -10.0000
+ 7 =  -9.0097
+ 8 =-640.5002m
+ 9 =-216.6329u
+ 10 =   0.
+ 11 =   7.4353
+ 12 =   7.4349
+ 13 =   8.0762
+ 14 =   9.4589
+ 15 =   7.8888
+ 16 =   8.4458
+ 17 =   8.8124
+ 18 =  -9.0097
+ 19 =  -1.4442u
+ 20 =   9.0043
+ 21 =  -1.4442u
+ 22 =-216.6329u
+ 23 =   0.
+ 24 =  -1.4442u
***   END: Saved Operating Point ***
```

Figure 5: bias of the circuit

3.2 The differential gain and output swing

In the following picture, the input signal was 1 μv. The output signal's pick is 7.69 v so the differential gain is :

$$\frac{V_{id}}{2} = 1uv \longrightarrow V_{id} = 2uv \longrightarrow A_d = \frac{7.69 * 10^6}{2} = 3.845 * 10^6$$

As we can see the gain is more than 1M and it's OK. Our calculated gain was less than this maybe because of our estimations and overlooking the effect of the circuit of feedback that is used for output bias. As we can see the output swing is also OK and more than 8.5 v_{p-p}.

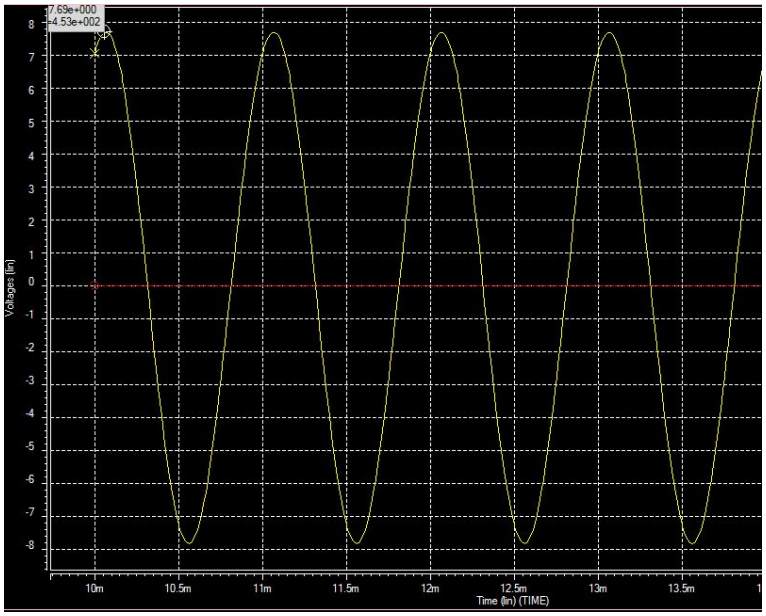

Figure 6: output signal in differential mode

3.3 The common mode gain and CMRR

For common mode gain, we set the input voltage 0.1 v so for common mode gain we have :

$$V_{icm} = 0,1v \longrightarrow A_{vc} = \frac{0.0318}{0.1} = 0.318$$

so that for CMRR we have :

$$CMRR = \frac{A_d}{A_{cm}} > 10^5 (OK)$$

3.4 The CMR

For checking CMR of the circuit, as we can see in the following figures, when we put a 8v DC and -8v DC in input signal, there is not any disorder in the output signal so our CMR is more than 8v.

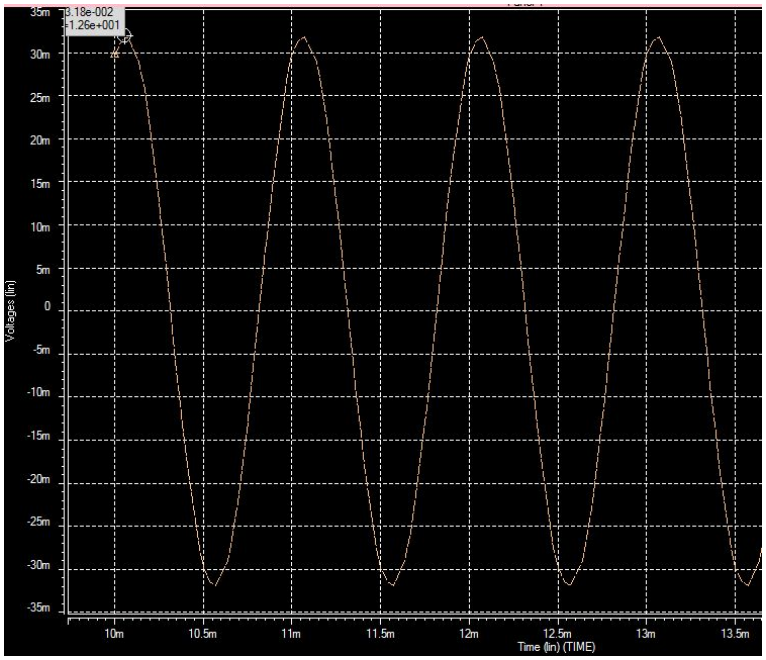

Figure 7: output signal in differential mode

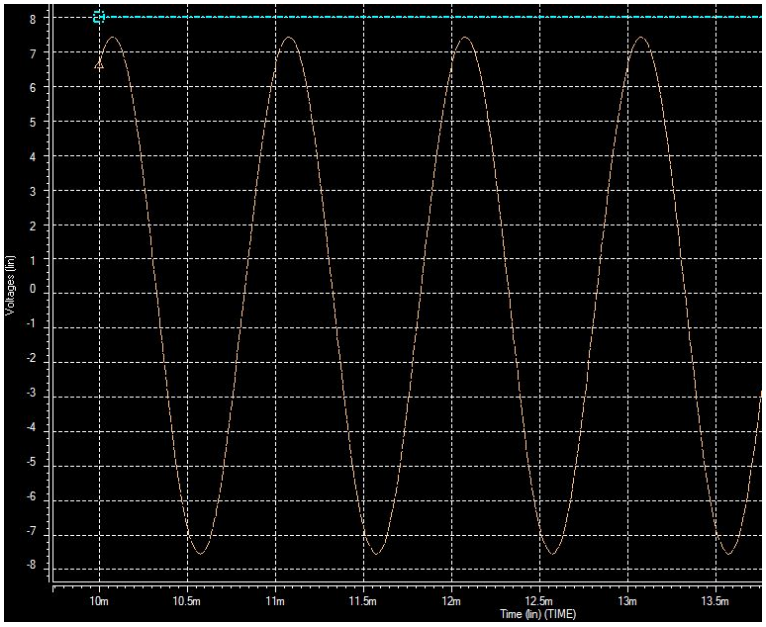

Figure 8: positive CMR is more than 8v

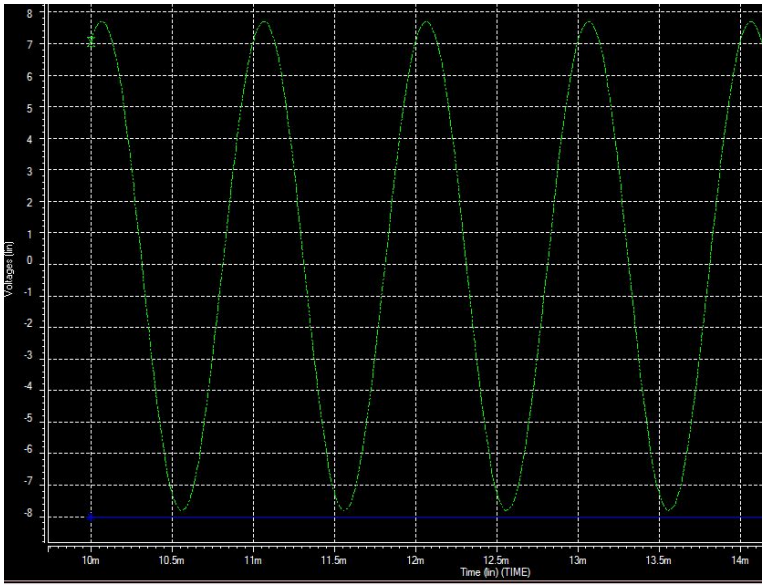

Figure 9: negative CMR is less than -8v