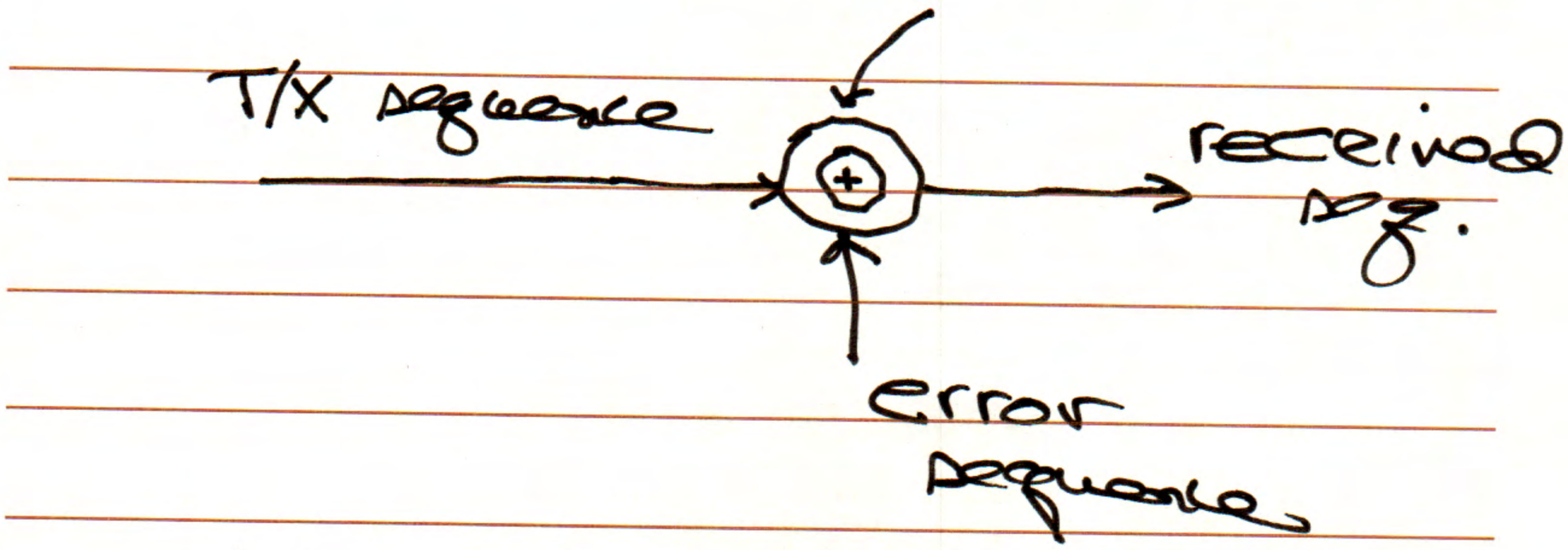
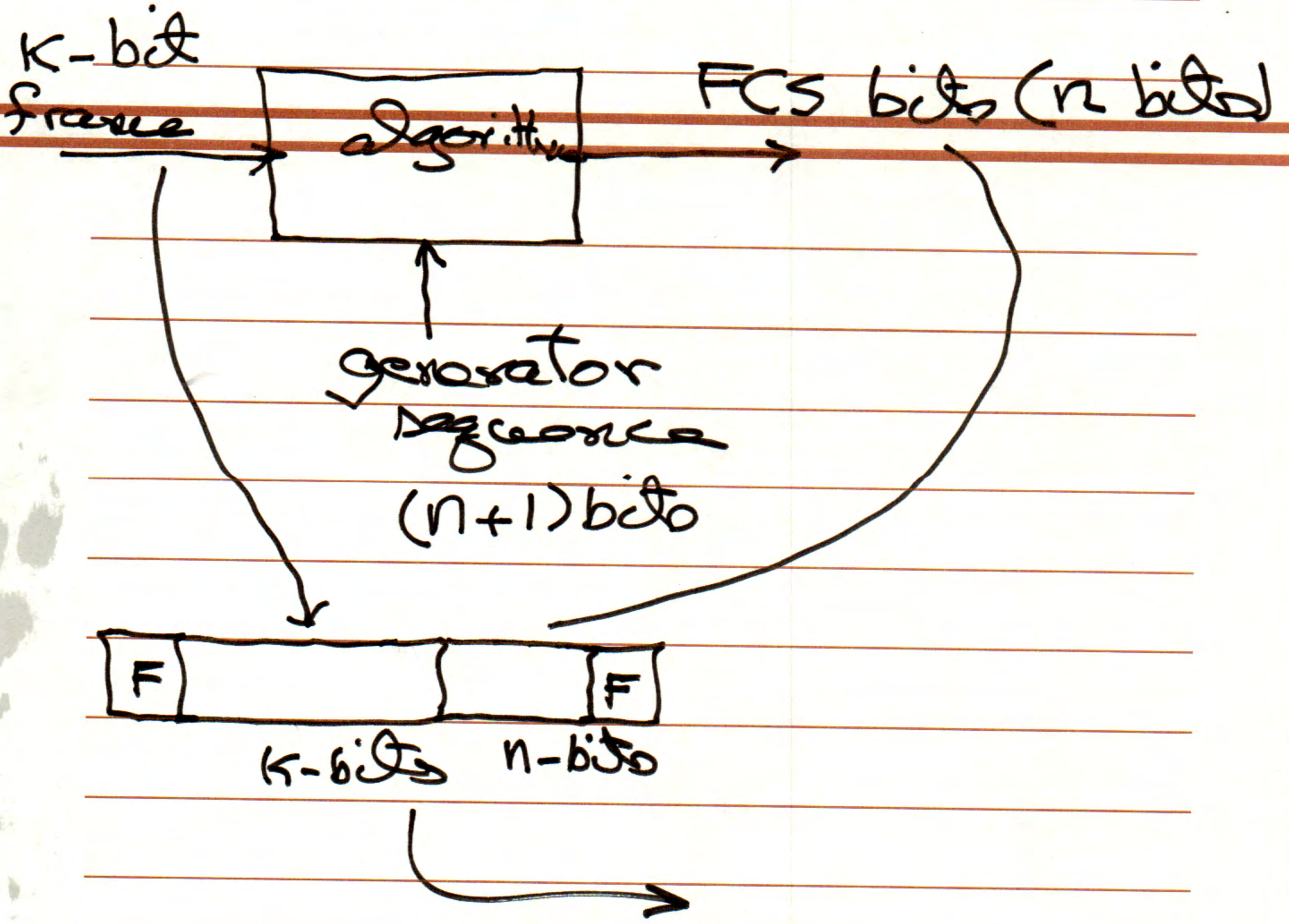
Error Detection: Mod-2 adder



Generation of FCS (frame check sequence) at Sender.



algorithm

Remainder
must be
≤ n bits

↑

FCS bits
(n-bits)

another way of demonstrating the algorithm is by using polynomials

110110 → $x^5 + x^4 + x^2 + x$

101101 → $x^5 + x^3 + x^2 + 1$

$$x^3 + x$$

$$x^3+x+1 \;\overline{)\; x^6 + x^3}$$

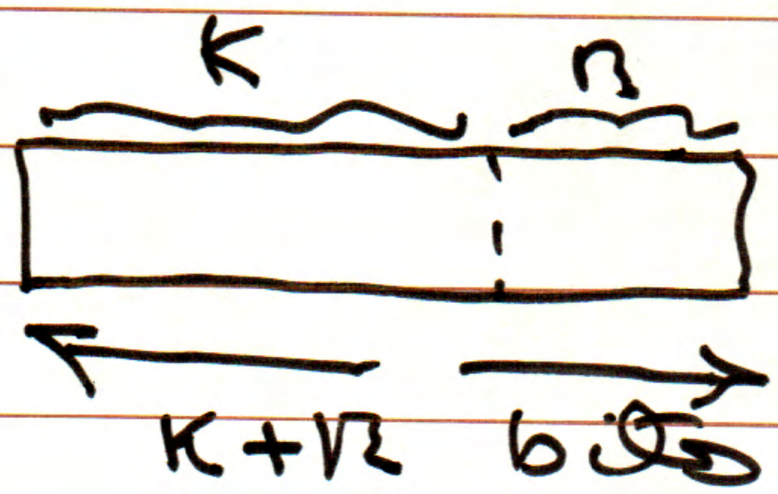
$$x^6 + x^4 + x^3$$

$$x^4$$

$$x^4 + x^2 + x$$

$$x^2 + x$$

@ receiver (after establishing frame Sync. & removing the flags)



n+1 bits

generator

K+n bits (received sequence)

Remainder

if remainder ≠ 0

if remainder is 0

error is detected

rcvr is 100% correct in his decision

rcvr declare no errors are detected.

rcvr could be right or he could be wrong in his decision.

$$x^3+x+1 \overline{)\, x^6+x^2+x \,} \quad x^3+x+1$$

$$x^6+x^4+x^3$$

$$x^4+x^3+x^2+x$$

$$x^4+x^2+x$$

$$x^3$$

$$x^3+x+1$$

$$x+1$$

٥١١

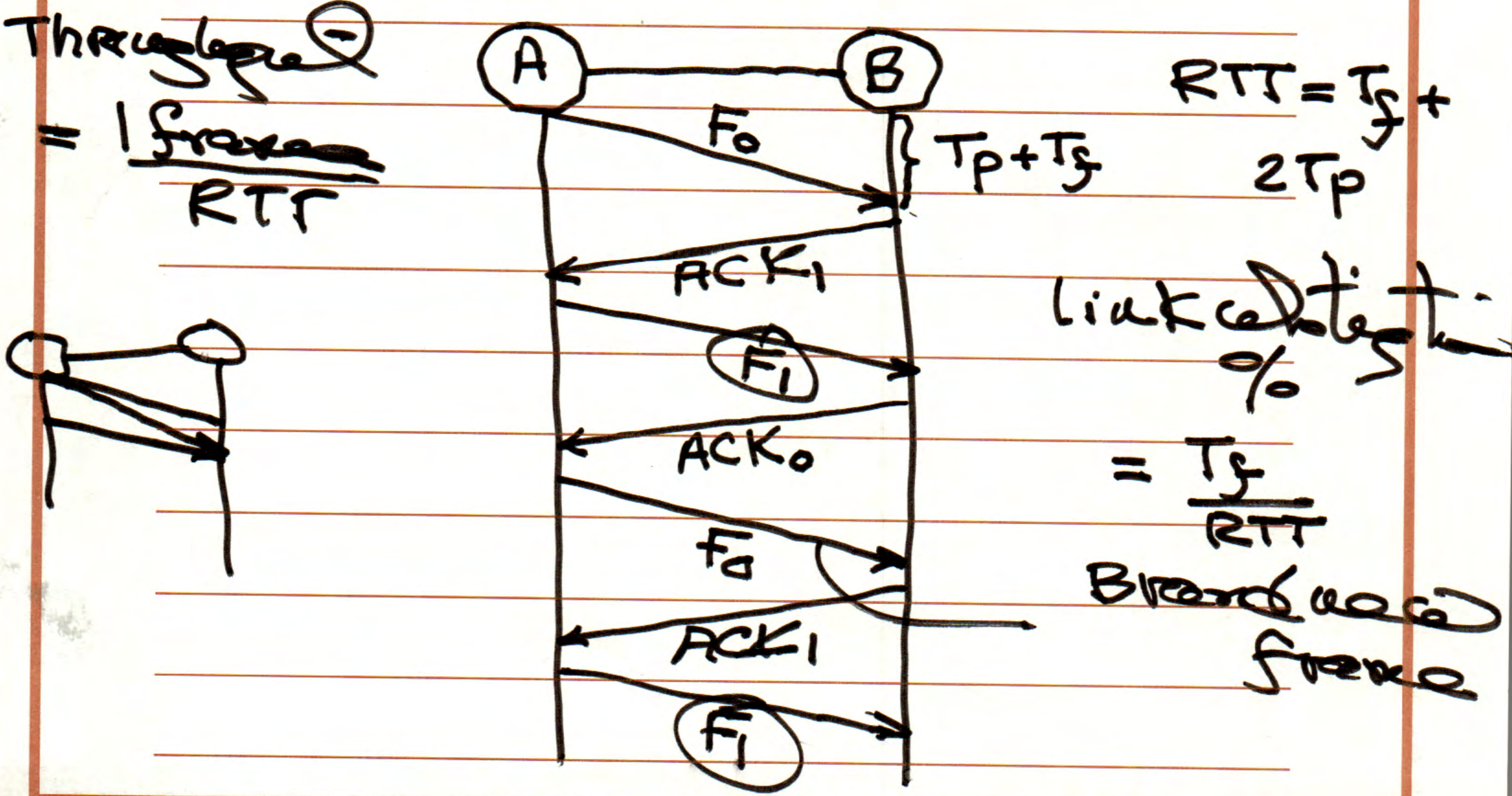
Error Control

ARQ : Automatic Repeat Request

S&W ARQ

Here the sender can send one frame at a time & then have to stop & wait for ACK before he can send another frame.

Throughput = $\frac{1 \text{ frame}}{RTT}$



$RTT = T_f + 2T_p$

link utilization %

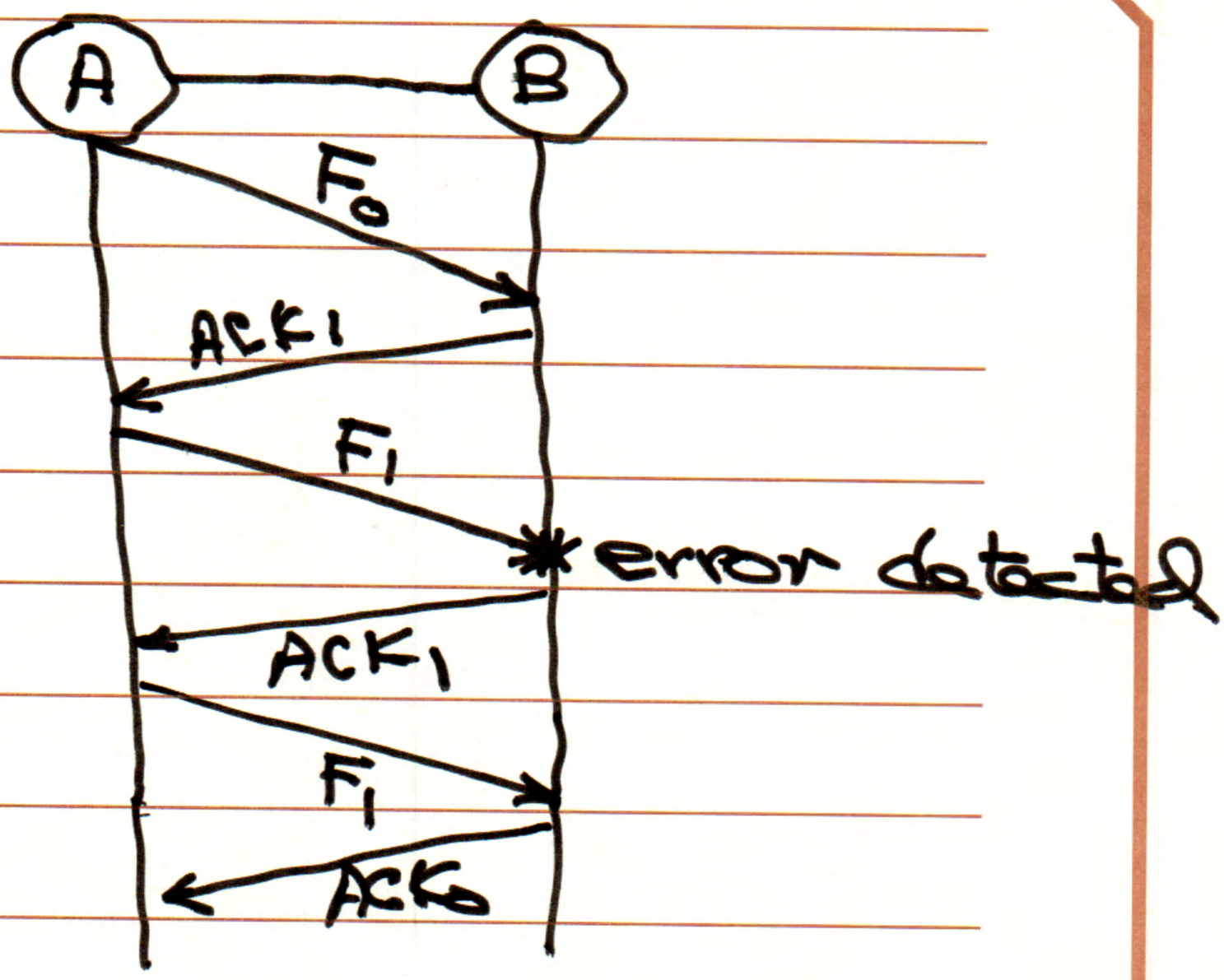
$= \frac{T_f}{RTT}$

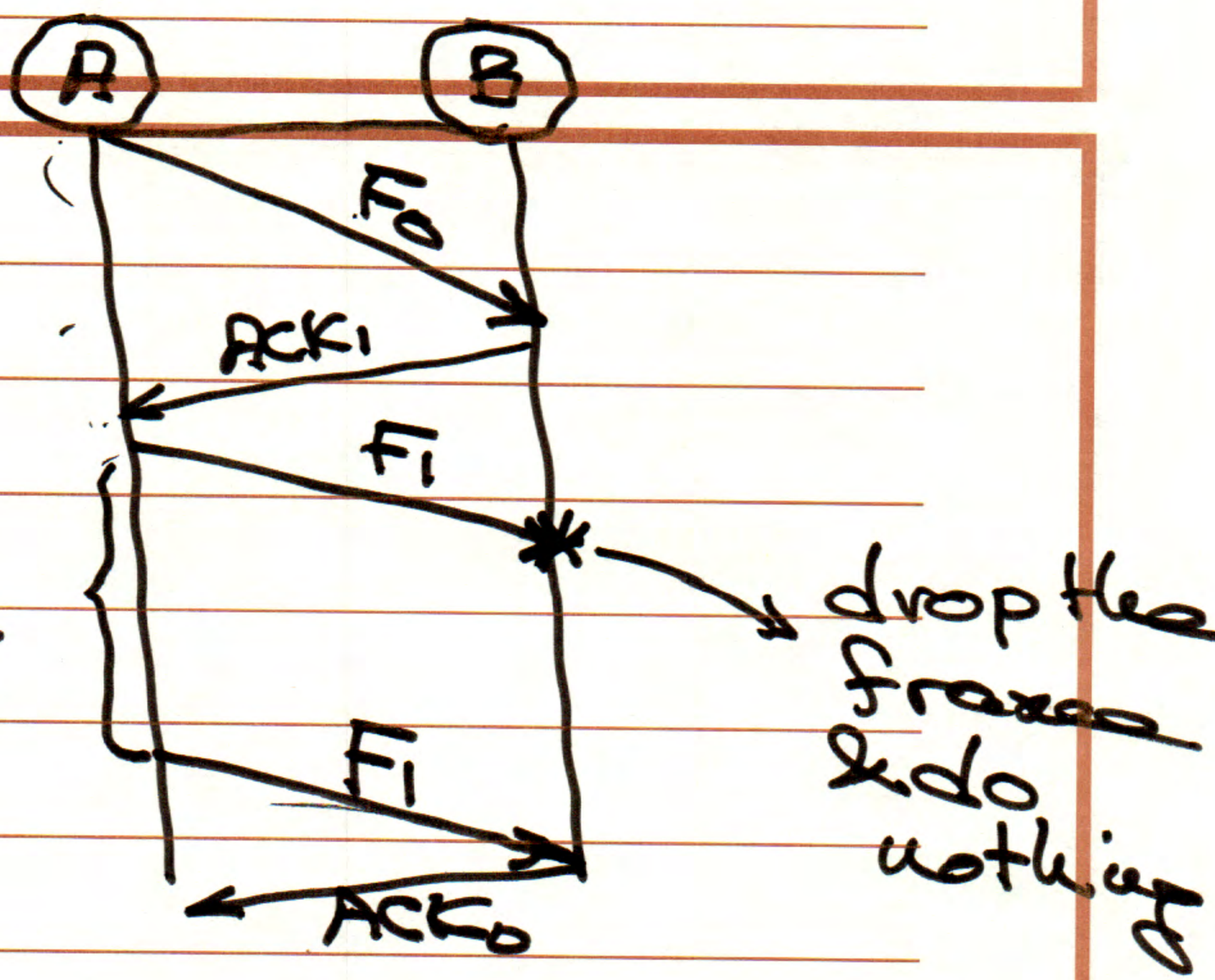
Bandwidth of frame

Throughput

$= \frac{2 \text{ Frames}}{3 RTT}$

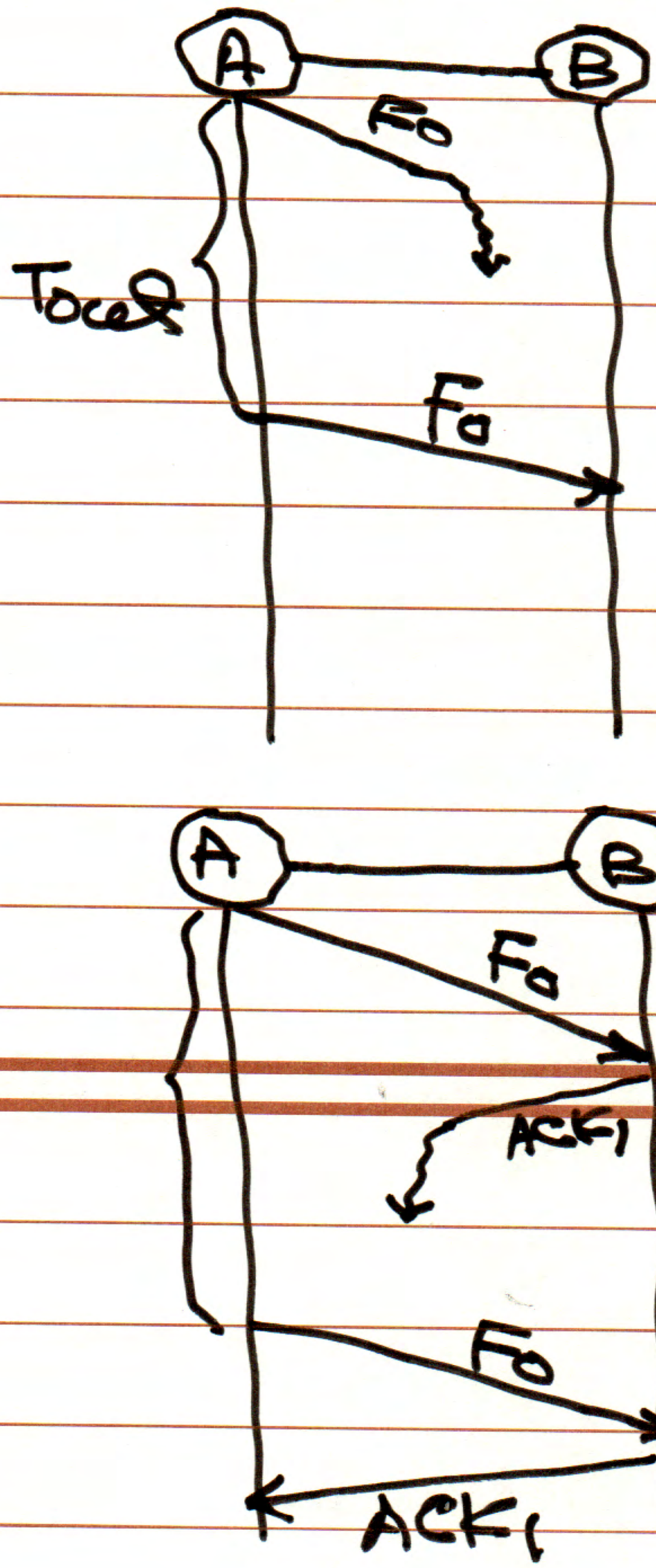
$\eta = \frac{2T_f}{3RTT}$



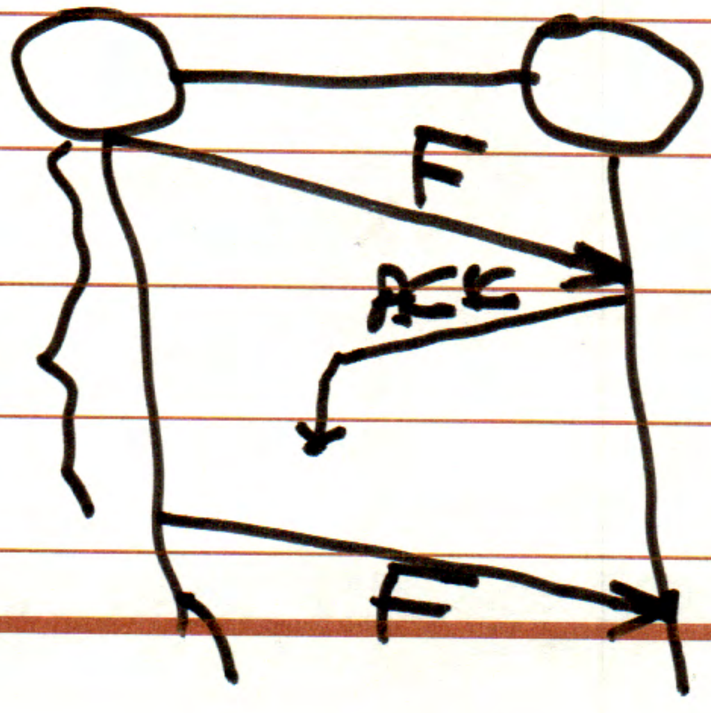


Throughput

$\frac{2 \text{ Frames}}{2 RTT + T_{out}}$


A
B
Fo
Toce
Fo

A
B
Fo
ACK1
Fo
drop
ACK1


F
ACK
F

Continuous (Sliding window) ARQ

- Go-back-N
- Selective Repeat (Reject)

* In continuous ARQ the sender is allowed to transmit multiple frames without having to wait for ACKs (i.e. pipelining).

what determines the Max. # of frames sender can send in one RTT.

- BW x Delay product
- The sequence bits length in the control field.

Max # of un-acknowledged frames the sender can send in one RTT.

let m = # of bits needed for sequencing the frames.

address m = 3

$F_0 F_1 \dots F_7$

For stop & wait ARQ, m = 1

* In Continuous ARQ, Acknowledgment can be cumulative.