

# Multiple Adaptive Current Feedback Technique for Small-Gain Stages in Adaptively Biased Low-Dropout Regulator

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**Abstract**—Adaptive bias scheme, which can be used to provide a current proportional to the current flowing through the power transistor under high current load, avoiding the need for providing additional large fixed bias current to the circuit, has been adopted in many low-dropout regulators (LDO). When an adaptive bias scheme is applied to an LDO with a current mirror buffer, although a low chip area consumption and a better transient response can be achieved, the loop gain of LDO at high-load current and loop bandwidth at low load are still low. In previous works, multiple small-gain stages can effectively improve the gain and bandwidth but may lead to stability problems or even need to consume large currents to ensure stability, thus affecting current efficiency. This article proposes the multiple adaptive current feedbacks technique for small-gain stages in adaptively biased low dropout regulator (AB-LDO) with a current mirror buffer, improving the loop gain and bandwidth and eliminating the need for frequency compensation to meet stability requirements. Moreover, in the case that multiple adaptive bias loops can be introduced after the proposed technique is applied to this design, an intuitive and simple method is adopted to analyze the whole circuit. The designed AB-LDO was fabricated in Semiconductor Manufacturing International Corp (SMIC) 0.18- $\mu\text{m}$  process. The measured results show that the designed LDO realizes 30.75-mV transient performances with a step of 10 ns.

**Index Terms**—Adaptively bias, low-dropout regulator (LDO), small-gain stage, transient response.

## I. INTRODUCTION

LOW-DROPOUT regulator (LDO) has several merits when applied to portable equipment, such as small chip area, high current efficiency, low power consumption, and fast response [1]. The progressive development of portable equipment has also led

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to stricter requirements in the above aspects for LDOs [2] [3]. Therefore, the adaptively biased LDO (AB-LDO) with a current mirror buffer was proposed in prior works, which can provide better support for portable equipment due to its lower silicon area and better transient response [4]. The adaptive bias scheme in AB-LDO, which enhances the loop bandwidth under high-load current and brings about a diminution of overshoot, has been adopted in more and more power management designs [5]–[7] [8]. In addition, a simple current mirror buffer is utilized in front of the gate of the power transistor to reduce the impact of the large parasitic capacitance at power transistor gate on the loop bandwidth and transient response of the regulator [4] [8]–[10]. These advantages have led to an increasing number of choices and designs of AB-LDO.

Despite all this, AB-LDO still has some disadvantages. The insertion of the current mirror buffer leads to the low loop gain at a high current load and affects the accuracy of the regulator, which is reflected in LDO's poor line and load regulations [4]. Furthermore, the adaptive bias scheme limits the loop bandwidth of the regulator at a low current load [11]. The undershoot in the transient response is closely related to the loop bandwidth in the case of low-load current [9], that is, a lower loop bandwidth results in a larger undershoot. Actually, both low gain and low bandwidth can be improved by increasing transconductance. As a structure that is beneficial to transconductance enhancement, the structure of multiple small-gain stages is proposed in [12] and applied in amplifiers [13]–[15] and LDOs [16], [17], which can effectively improve the gain and bandwidth simultaneously.

However, there are some issues when considering the application of small-gain stages to AB-LDO for the purpose of improving the loop gain and loop bandwidth. The multiple small-gain stages directly applied to AB-LDO are defective because of its internal poles or even additional large current consumption. First, under high load, the internal poles of the small-gain stages may be pulled to relatively low frequencies, leading to instability of the regulator. Otherwise, the multiple small-gain stages may need to consume large currents to maintain the high frequency of its internal poles, which causes that the current efficiency  $\eta$  of AB-LDO, especially under low-load current, could be seriously reduced. Therefore, in order to avoid complicated frequency compensation, this article needs to solve the stability problem caused by small-gain stages

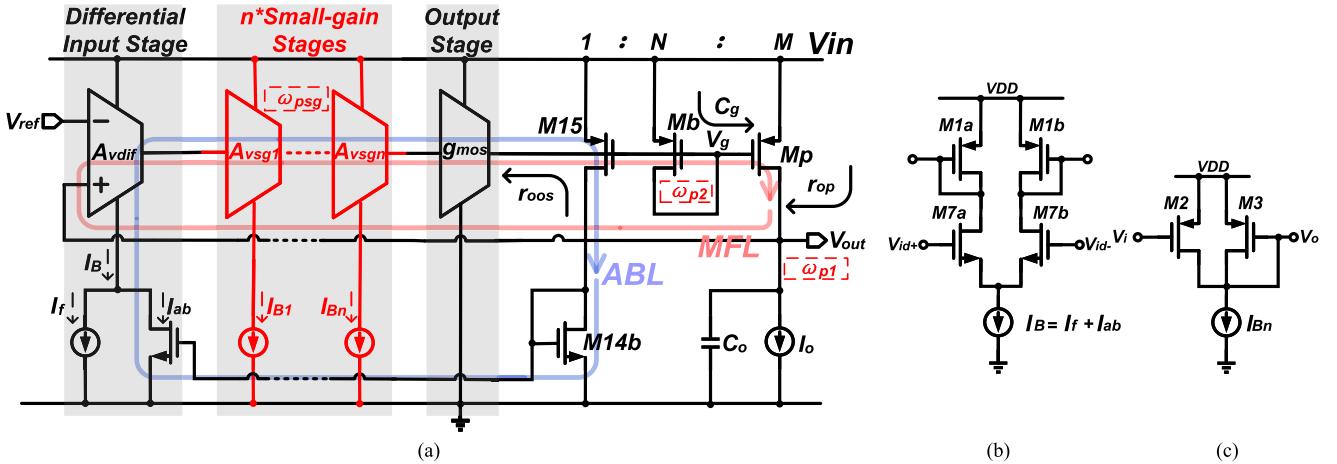


Fig. 1. Structures of (a) AB-LDO with small-gain stages. (b) Differential input stages. (c) Small-gain stage.

on the basis of the first proposal of applying multiple small-gain stages to AB-LDO, as shown in Fig. 1.

To solve the above problems caused by the multiple small-gain stages in AB-LDO, a multiple adaptive current feedbacks technique is adopted to the AB-LDO with multiple small-gain stages in this article. This technique can adaptively feedback the required multiple currents to the small-gain stages, which not only enables their internal poles to track the loop bandwidth and the first nondominant pole to solve the stability problem at high load, but also avoids the possibility that the small-gain stages may need to be supplied with large fixed currents, and thus the current efficiency cannot be greatly affected.

Moreover, based on this technique, the design of AB-LDO proposed in this article introduces multiple adaptive bias loops (ABL). However, there is no analysis method for AB-LDO containing multiple ABLs in prior works on AB-LDO. In [4], [5], [7], and [8] on the design of AB-LDO containing only one MFL and one ABL, the method of closing one loop to study the effect on the other loop is adopted, which is obviously troublesome to analyze the AB-LDO containing multiple ABLs in this article. Hence, an intuitive method is adopted [10], which can not only analyze multiple ABLs simultaneously but also avoid complex simulation and calculation.

The rest of this article is organized as follows. A presentation of the limitations of AB-LDO with multiple small-gain stages is shown in Section II. In Section III, the detailed calculations and analysis about AB-LDO using the multiple adaptive current feedbacks technique for small-gain stages are given on the premise of adopting the convenient method. Section IV displays the postsimulation and testing results. Finally, Section V concludes this article.

## II. PRESENTATION OF THE LIMITATIONS OF AB-LDO WITH MULTIPLE SMALL-GAIN STAGES

In spite of the great transient response of AB-LDO brought from the adaptive bias scheme, the loop gain of AB-LDO at high load is quite low, which affects the line and load regulations of AB-LDO. Similarly, the loop bandwidth is relatively low as

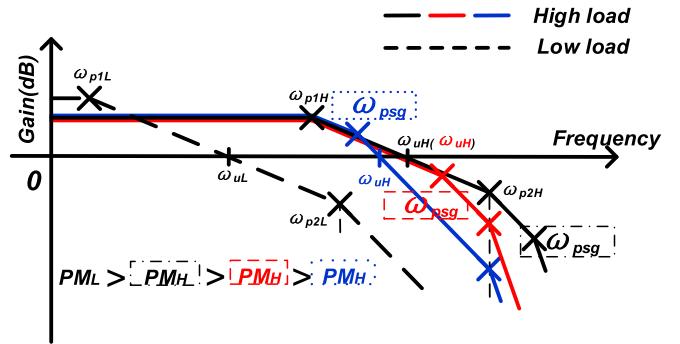


Fig. 2. Presentation on solving problems caused by AB-LDO with multiple small-gain stages in frequency response.

well at low load, resulting in an obvious transient undershoot. To improve the loop gain and bandwidth more, multiple small-gain stages are adopted to this design as Fig. 1. Normally, the dominant pole \$\omega\_{p1}\$ is generated from the output node, and the first nondominant pole \$\omega\_{p2}\$ is introduced from the gate of power transistor \$V\_g\$. However, the structure containing multiple small-gain stages introduces many poles while increasing the loop gain, which may have a serious impact on stability especially under high current load. The following is a specific analysis of the stability problem.

Fig. 2 shows the distribution of poles and loop bandwidth \$\omega\_u\$ of AB-LDO containing multiple small-gain stages with fixed bias current under high-load current and low-load current, respectively, satisfying

$$\omega_{p1} = -\frac{1}{r_{op} C_o} \quad (1)$$

$$\omega_u = -\frac{A_{vdif} \cdot A_{vsg1} \cdots A_{vsgn} \cdot g_{mos} \cdot (r_{oos} // \frac{1}{g_{mb}}) \cdot g_{mp}}{C_o} \quad (2)$$

$$\omega_{p2} = -\frac{1}{(r_{oos} // \frac{1}{g_{mb}}) C_g} \quad (3)$$

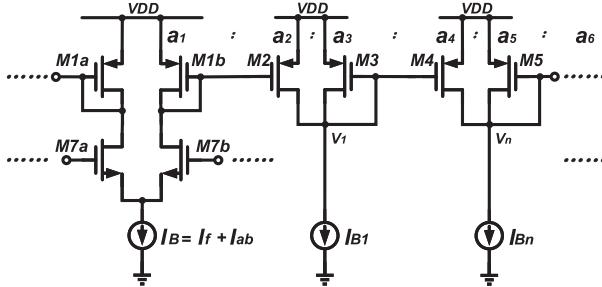


Fig. 3. Connection between a differential input stage and a small-gain stage or between two small-gain stages.

where  $A_{\text{vdf}}$  is the gain of the differential input stage and  $A_{\text{vsg}}$  is the gain of the  $n$ th small-gain stage. Besides,  $\omega_{p1H}$  or  $\omega_{p2H}$  or  $\omega_{uH}$  represents the pole or loop bandwidth in the case of high-load current and  $\omega_{p1L}$  or  $\omega_{p2L}$  or  $\omega_{uL}$  in the case of low-load current. And all the other symbols, such as the output stage resistance  $r_{\text{oos}}$ , the power transistor output resistance  $r_{\text{op}}$ , the load capacitance  $C_o$ , the parasitic capacitance at power transistor gate  $C_g$ , the effective transconductance of  $M_x$  transistor  $g_{\text{mx}}$ , the effective transconductance of output stage  $g_{\text{mos}}$ , and the effective transconductance of  $M_b$  transistor  $g_{\text{mb}}$  are annotated in the corresponding places in Fig. 1. There are  $r_{\text{oos}} \ll \frac{1}{g_{\text{mb}}}$  at low load while  $r_{\text{oos}} \gg \frac{1}{g_{\text{mb}}}$  at high load. Nevertheless, at high-load current condition, the stability needs to be paid more attention since the distance between the loop bandwidth  $\omega_{uH}$  and the first nondominant pole  $\omega_{p2H}$  is much smaller than that under low-load condition [4], although both  $\omega_{p2}$  and  $\omega_u$  are improved at high-load condition due to the adaptive bias scheme, as shown in Fig. 2 by the black solid and black dashed lines. And under high load, when  $\omega_{p2H}$  is increased to high frequencies, it is likely to happen that  $\omega_{p2H}$  is higher than that of poles introduced by small-gain stages, resulting in a pole  $\omega_{\text{psg}}$  from small-gain stages becoming a new first nondominant pole, shown as the red solid line in Fig. 2, or even the loop bandwidth  $\omega_{uH}$  being higher than  $\omega_{\text{psg}}$  at high-load condition, shown as the blue solid line in Fig. 2, which causes the AB-LDO to be unstable.

In the case of a high-load current, in addition to the situation where the poles  $\omega_{p2H}$  generated at  $V_g$  and  $\omega_{uH}$  are increased to high frequencies, the situation where the  $\omega_{\text{psg}}$  is pulled to a low frequency may occur, leading to stability problems as well. Assuming that all PMOS transistors in differential input stage and small-gain stages have the same unit size, the current mirror, such as  $M1a(b)$  and  $M2$  in Fig. 1(b) and (c), can be formed when the above two structures are connected, as shown in Fig. 3. Thus, all PMOS transistors have the same parasitic unit capacitance  $C_i$  at the gate and the proportion of  $M1a(b)$ ,  $M2$ ,  $M3$ ,  $M4$ ,  $M5$ , and so on is  $a_1 : a_2 : a_3 : a_4 : \dots$ . The current  $I_B$  provided to the differential input stage in AB-LDO consists of a fixed current  $I_f$  and an adaptive biasing current  $I_{ab}$  satisfying  $I_{ab} \propto I_o$ . When the load current  $I_o$  is switched to a high current,  $I_{ab}$  plays a dominant role in  $I_B$ . The current flowing through the  $M1a(b)$  transistor, which acts as the load in the differential input stage, starts to increase and can be replicated through the current mirror

structure  $M1a(b) - M2$ , resulting in an increase in the current flowing through  $M2$  of small-gain stage. If  $I_{B1}$  is not large enough, the current that can be provided to  $M3$  in small-gain stage structure is severely reduced. Hence, for the pole in the small-gain stage

$$\omega_{\text{psg}} \approx -\frac{g_{m3}}{(a_3 + a_4)C_i} \quad (4)$$

introduced from the node  $V_1$ , both  $g_{m3}$  and  $\omega_{\text{psg}}$  are decreased sharply, which is more detrimental to stability, whereas  $I_{Bn}$  should not be set too large because consuming much quiescent current seriously reduces the current efficiency

$$\eta = \frac{I_o}{\frac{I_o}{M} + I_{os} + I_B + I_o + (I_{B1} + \dots + I_{Bn})} \quad (5)$$

of AB-LDO, especially under low-current load. Therefore, the specific value selection of the fixed current  $I_{Bn}$  becomes a problem to be considered. Obviously, under the circumstance that the load current may change at any time, the value of  $I_{Bn}$  can neither be too small to affect the stability nor too large to reduce the current efficiency of AB-LDO, which is troublesome to select. The same problem can occur when two small-gain stage structures are connected to form a current mirror. Similarly, the uneven current distribution of the  $M2$  and  $M3$  transistors in the previous small-gain stage can result in the uneven current distribution in the next gain stage, which may cause the same stability problems. The solution to the above problems requires a large area of capacitor for the frequency compensation or a large fixed current  $I_{Bn}$  to be provided so that the current flowing through  $M3$  is large enough to ensure stability. However, the problem of uneven current distribution in the small-gain stage still exists when a large  $I_{Bn}$  is provided.

### III. ANALYSIS OF AB-LDO WITH SMALL-GAIN STAGES USING MULTIPLE ADAPTIVE CURRENT FEEDBACKS TECHNIQUE

#### A. Description of Multiple Adaptive Current Feedbacks Technique and Analysis of the Overall Loop

To solve the problem that these poles introduced by small-gain stages need to be pushed to high frequency under high-load current,  $I_{B1} - I_{Bn}$  needs to be increased adaptively with  $I_B$  according to the requirements of stability and  $\eta$  of AB-LDO. For this solution, the multiple adaptive current feedbacks technique is adopted to increase  $I_{Bn}$  so that  $I_{Bn}$  can vary with  $I_B$ , as shown in Fig. 4. The current  $I_{Bn}$  is divided into two parts. In the case of high load,  $I_{Bn}$  is dominated by an  $I_{abn}$  that can adaptively change with the load current  $I_o$  by utilizing the adaptive bias scheme, enabling the current flowing through  $M3$  in Fig. 3 to be unrestricted and to be increased with the increase of the load current, ultimately improving the pole  $\omega_{\text{psg}}$ . What is more, since both the current flowing through  $M3$  and the current through the diode-connected transistor  $Mb$  in AB-LDO vary proportionally with  $I_o$  through  $M_p$ ,  $\omega_{\text{psg}}$  can track  $\omega_{p2}$  and  $\omega_u$  at high load

$$\omega_{p2H} \approx -\frac{g_{mb}}{C_g} \quad (6)$$

$$\omega_{uH} \approx \frac{g_{m7a}a_2a_4a_6M}{a_1a_3a_5NC_o} \quad (7)$$

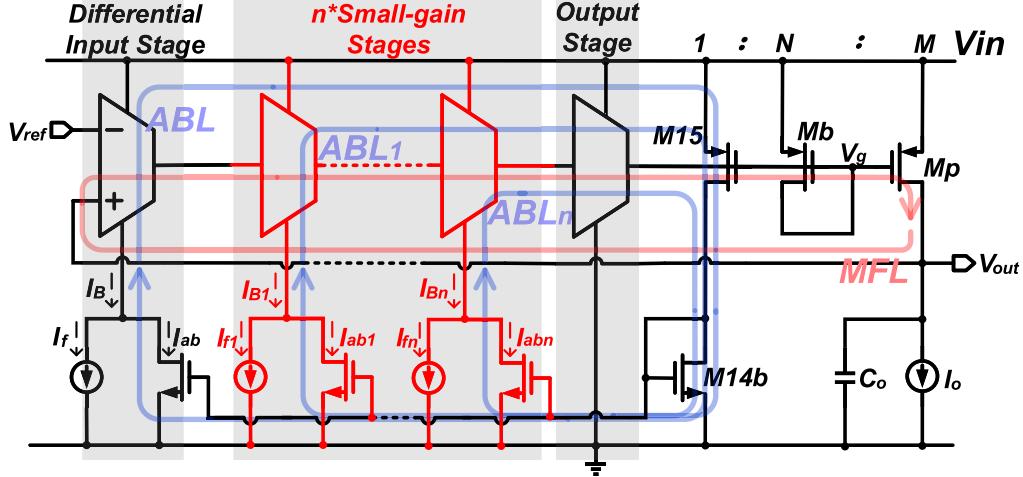


Fig. 4. AB-LDO with small-gain stages using the proposed multiple adaptive current feedback technique.

which makes the whole circuit eliminate the need for large on-chip capacitors for compensation and avoid complex frequency compensation. Conversely, in the case of low load,  $I_{Bn}$  is determined by a small fixed bias current  $I_{fn}$  to ensure the normal operation of the small-gain stage and the high current efficiency of AB-LDO. In the above two cases, when the size ratios between transistors are set to meet the requirement of stability, there is no extra current consumption to affect the current efficiency  $\eta$  of AB-LDO.

The AB-LDO with small-gain stages using multiple adaptive current feedbacks technique is displayed as Fig. 5, which inserts two small-gain stages. Besides the original main feedback loop (MFL) and the adaptive biasing loop (ABL), the complete circuit also contains two extra pairs of ABL due to its symmetrical structure. This article adopts the method of analyzing at the common link  $V_g$  before the gate of the power transistor to get the amplitude-frequency response and phase-frequency of the overall AB-LDO [10], [18], [19]. As can be seen from Fig. 6 about the complete signal structure diagram, on the basis of ABL which is the common-mode, the other ABLs introduced by the multiple adaptive current feedbacks technique form the common mode after superposition as well. Therefore, in order to facilitate

calculation, all ABLs are superposed to form one loop for analysis. MFL consists of  $M7a(b)$ ,  $M1a(b) - M6a(b)$ ,  $Mb$ , and  $Mp$  while ABLs include  $M13b$ ,  $M9a(b)$ ,  $M11a(b)$ ,  $M7a(b)$ ,  $M1a(b) - M6a(b)$ ,  $Mb$ ,  $M15$ , and  $M14b$ , where MFL and ABLs have the same pole  $\omega_{p2} = -1/[(r_{o6b}/r_{o8b}/g_{mb}) \cdot C_g]$  from  $V_g$  at a relatively low frequency and the same mismatch factor  $m = g_{m6a} \cdot g_{m8b} / (g_{m6b} \cdot g_{m8a})$ . In fact, the transfer functions of MFL, ABL, and complete circuit satisfying  $A_{vMFL-ABL}(s) = A_{vMFL}(s) + A_{vABL}(s)$  are presented as (8)–(10), shown at the bottom of this page. The gain responses of two separate loops and the complete circuit at low and high load, respectively, in Fig. 7. prove the correctness of the relationship among the three transfer functions.

Combined with the phase-frequency response in Fig. 8, it can be seen that there is an obvious zero lower than  $\omega_{p2L}$  in low-load current case. The zero is mainly caused by the parallel connection between two loops. When the gain of these ABLs is low enough, the zero generated by the parallel connection of two loops is at a high frequency and it has little effect on stability. In order to avoid the influence of zero on circuit design and stability analysis, the gain of ABLs should be as small as possible. The gain of ABLs is closely related to the value of

$$A_{vMFL}(s) = \frac{g_{m7a}g_{m2a}g_{m4a}g_{m6b}Rg_{mp}r_o(1+m)}{2[g_{m1a} + (a_1 + a_2)C_i s][g_{m3a} + (a_3 + a_4)C_i s][g_{m5a} + (a_5 + a_6)C_i s][1 + C_g R s](1 + C_o r_o s)} \quad (8)$$

$$A_{vABLs}(s) = \frac{[g_{m13b}g_{m2a}g_{m4a} - 2[g_{m1a} + (a_1 + a_2)C_i s][g_{m9a}g_{m4a} - g_{m11a}[g_{m3a} + (a_3 + a_4)C_i s]]]g_{m6b}g_{m15}R(1-m)}{2g_{m14b}[g_{m1a} + (a_1 + a_2)C_i s][g_{m3a} + (a_3 + a_4)C_i s][g_{m5a} + (a_5 + a_6)C_i s][1 + C_g R s]} \\ \approx \frac{(g_{m13b}g_{m2a}g_{m4a} - 2g_{m1a}g_{m9a}g_{m4a} + 2g_{m1a}g_{m11a}g_{m3a})g_{m6b}g_{m15}R(1-m)}{2g_{m14b}g_{m1a}g_{m3a}g_{m5a}(1 + C_g R s)} \quad (9)$$

$$A_{vMFL-ABL}(s) \approx \frac{[g_{m13b}g_{m2a}g_{m4a} - 2[g_{m1a} + (a_1 + a_2)C_i s][g_{m9a}g_{m4a} - g_{m11a}[g_{m3a} + (a_3 + a_4)C_i s]]]}{2g_{m14b}[g_{m1a} + (a_1 + a_2)C_i s][g_{m3a} + (a_3 + a_4)C_i s][g_{m5a} + (a_5 + a_6)C_i s]} \\ *g_{m6b}g_{m15}R(m-1)(1 + C_o r_o s) - 2g_{m14b}g_{m7b}g_{m2b}g_{m4b}g_{m6b}Rg_{mp}r_o \\ [1 + C_g R s](1 + C_o r_o s) \quad (10)$$

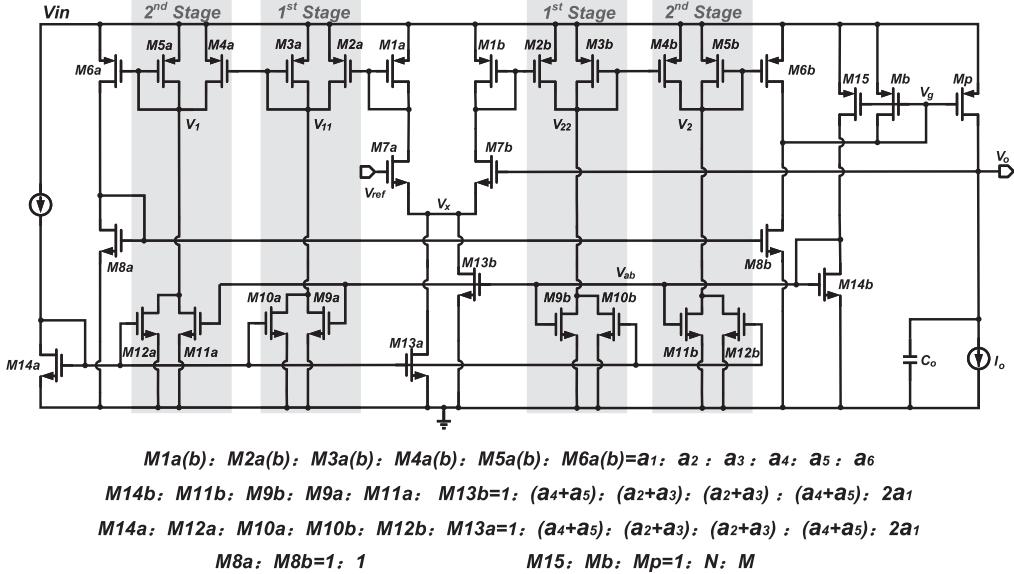


Fig. 5. Complete schematic of AB-LDO.

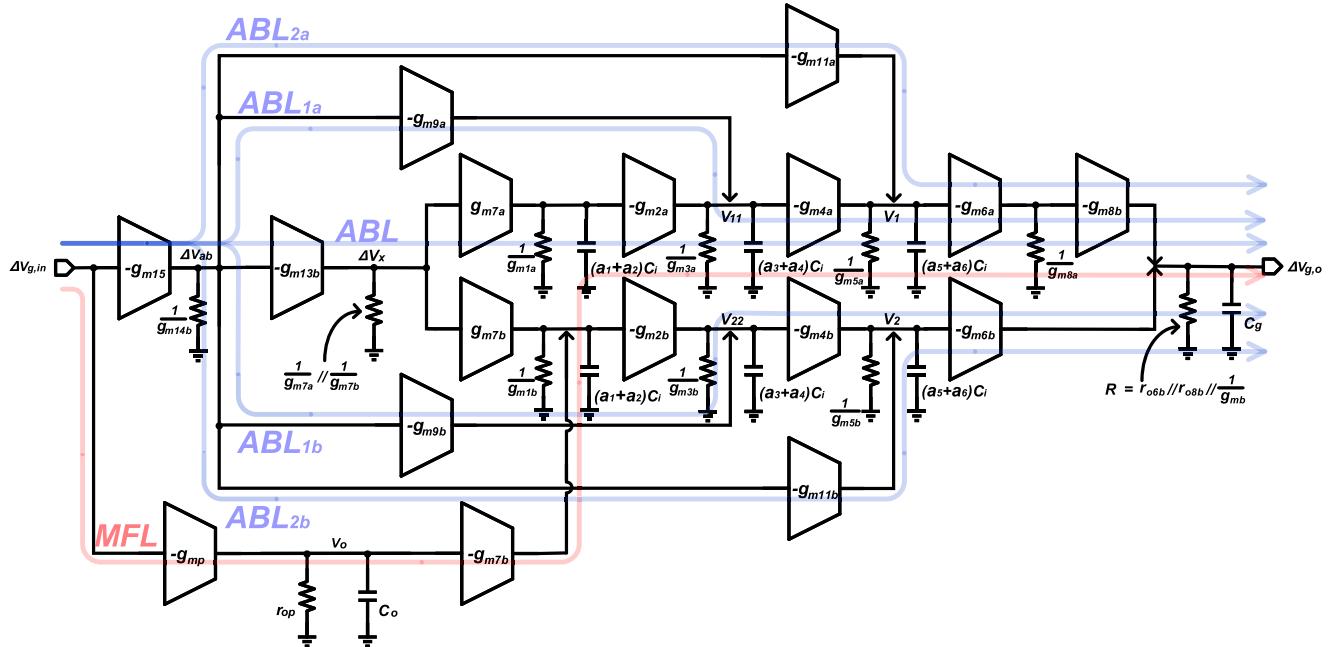


Fig. 6. Block diagram of the small-signal of MFL-ABL.

mismatch factor  $m$ . In the ideal case, since the differential input stage, small-gain stages, and output stages are symmetric, the value of  $1 - m$  is equal to 0, where the gain of ABLs is much less than 0 dB. However, in the complete circuit, due to the existence of  $Mb$ , the circuit is no longer symmetrical, making the value of  $m$  deviate from 1.

When under high current load, the value of  $m$  may deviate more from 1 because of the current  $I_o * N/M$  flowing through  $Mb$ . Hence, more considerations should be given to the selection of a smaller  $N/M$  value. In addition, for AB-LDO, stability under high current load may have the worst results. Hence, the stability at high load needs special attention. When the zero due to parallel connections between loops is not taken into account,

the stability is guaranteed on the condition that  $\omega_{p2H}/\omega_{uH} > 2$ . For the loop bandwidth at high load,

$$\omega_{uH} \approx \frac{g_{m7a} a_2 a_4 a_6 g_{mp} (1+m)}{2a_1 a_3 a_5 g_{mb} C_o} \quad (11)$$

is determined by MFL since the gain of ABL is usually much less than 0 dB. An upper bound on  $M/N$  can be obtained according to the relation between  $\omega_{uH}$  and  $\omega_{p2H} \approx \frac{g_{mb}}{C_g}$  as

$$\frac{M}{N} < \frac{g_{mb} a_1 a_3 a_5 C_o}{g_{m7a} a_2 a_4 a_6 (1+m) C_g}. \quad (12)$$

When considering avoiding the effect of zero due to parallel connection between loops by achieving a low gain of ABLs,

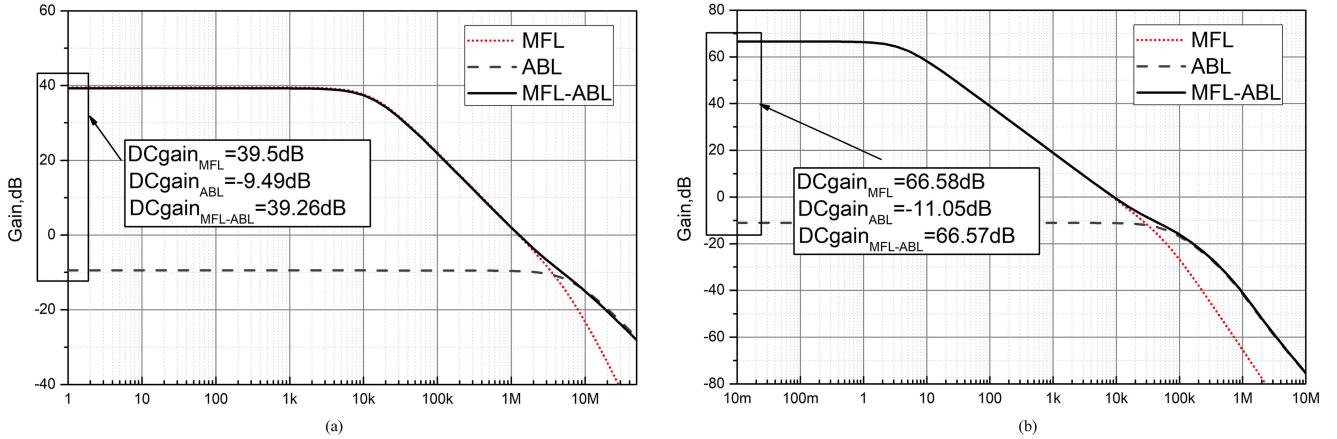


Fig. 7. Gain responses of two separate loops and complete circuit at (a) high load of 50 mA and (b) low load of 10  $\mu$ A, respectively.

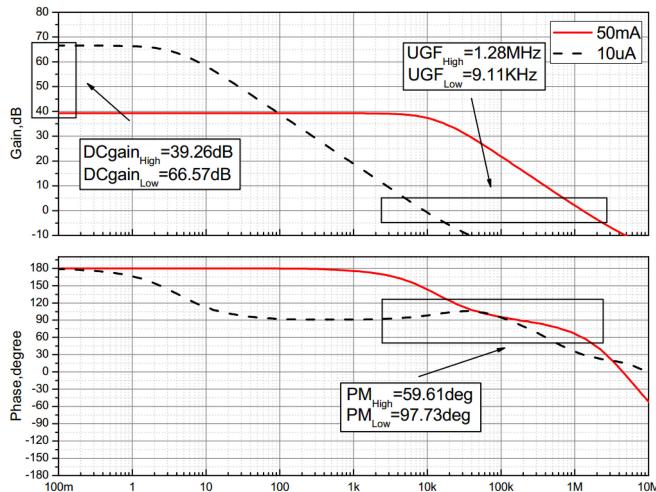


Fig. 8. Simulated frequency response of complete circuit at the load current of 10  $\mu$ A and 50 mA, respectively.

this relationship also provides a lower bound for a small  $N/M$  value. However, the upper bound on  $M/N$  limits  $A_{vMFL-ABL}$  since  $A_{vMFL-ABL}$  under high load satisfies

$$A_{vMFL-ABL} \propto g_{mp}/g_{mb} \propto M/N. \quad (13)$$

Hence, appropriate selection of the values of  $a_1 - a_6$  can simultaneously improve the loop gain and guarantee stability at high load. The above relationship related to  $g_{m7a}$  and  $a_1 - a_6$  limits the selection of  $I_{abn}$  as well. At the same time,  $I_{abn}$  should meet the requirement of low quiescent current.

When under low current load, as the current flowing through  $M_b$  replicating power transistor  $M_p$ 's current is small, the impact of asymmetric structure on ABLs' gain is slight. Therefore, the ABL gain is usually lower at low current loads. Furthermore, it is easier for AB-LDO to achieve stability at low current loads than at high-load currents. Based on the above situation and on the premise that AB-LDO is stable in the case of high-load current, there is no strict condition for stability in the case of the low current load. In this design, after the calculation and simulation of the zero, it is concluded that the zero at 10  $\mu$ A load

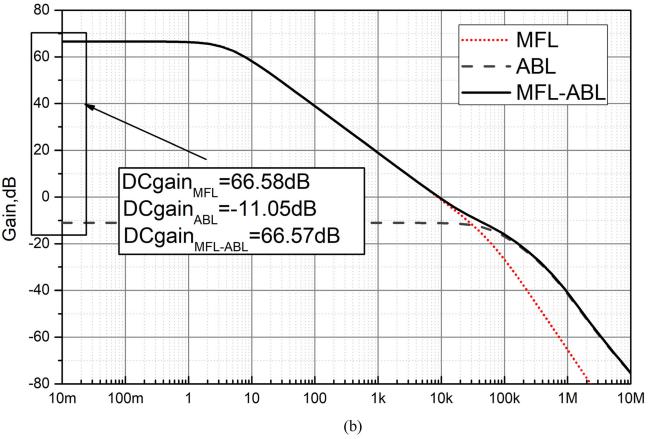


Fig. 9. Simulated quiescent current versus  $I_o$ .

current is on the left-half-plane, which has no significant adverse effect on the stability, as can be seen from the phase-frequency response in Fig. 8.

Fig. 9 gives the variation trend of quiescent current as the load current  $I_o$  changes. Under this trend, the changes in phase margin (PM) and loop bandwidth with the load current  $I_o$  after the design considers the stability from the above aspects are displayed in Fig. 10, indicating that the design can maintain stability when the load current changes from 10  $\mu$ A to 50 mA. Moreover, Monte-Carlo simulation for dc gain and PM at 50 mA load current is carried out at 100°C under the analysis variations of process and mismatch, as shown in Fig. 11. A probabilistic PM result with the 17.52 square deviation (sd) value and 58.24 mean (mu) value indicates that this design needs to be avoided in high-temperature applications.

### B. Contrastive Analysis With Conventional AB-LDO

In order to further prove that of AB-LDO with small-gain stages can improve the loop gain at high load and the loop bandwidth at low load while maintaining stability by using multiple

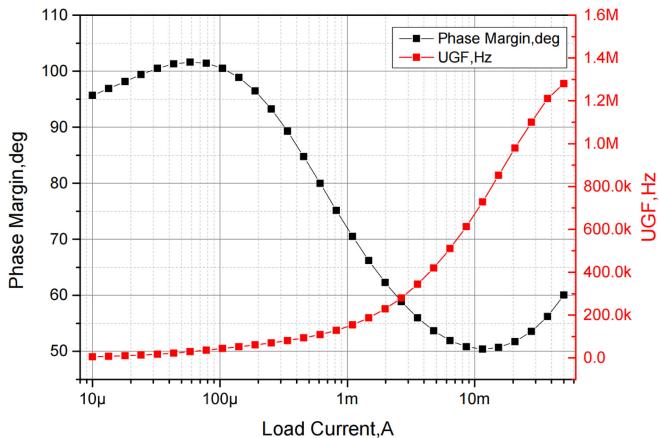


Fig. 10. Phase margin and unity-gain frequency (UGF) versus  $I_o$ , respectively.

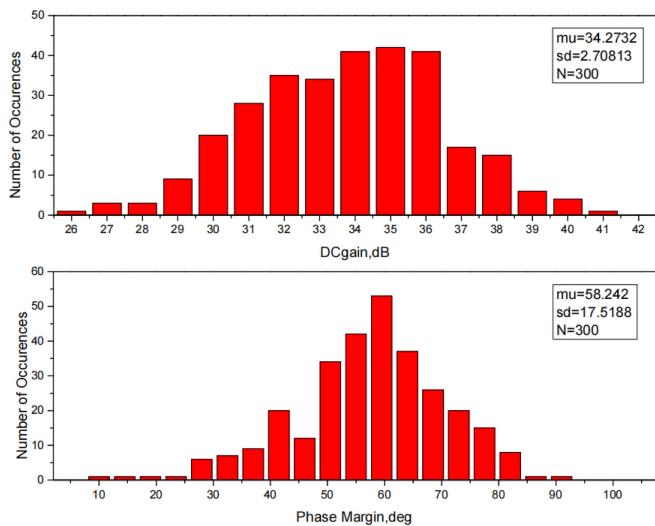


Fig. 11. Monte-Carlo simulations of dc gain and phase margin at 50 mA load current with the analysis variations of process and mismatch at 100 °C.

adaptive current feedbacks technique, this article compares it to a conventional AB-LDO without small-gain stages. Set the unit transconductance of the two AB-LDOs' transistors at the corresponding position to be the same and set the multiplier according to the same quiescent current and area consumed by the two AB-LDOs. The size ratios of all transistors are also marked in Fig. 12. Therefore, the two AB-LDOs differ in the transistor size and current consumption of their output stages. In spite of this, the resulting difference in capacitance and impedance between the two output stages is not more than one order of magnitude. Therefore, the dominant pole  $\omega_{p1}$  and the first nondominant pole  $\omega_{p2}$  generated at  $V_g$  between the two AB-LDOs can be considered to be similar.

As shown in Fig. 13, the frequency responses of this designed AB-LDO and conventional AB-LDO at low and high loads are simulated. From the comparison of gain responses, it can be seen that the loop gain of the proposed AB-LDO is improved under both high and low current loads. At the same time, its loop bandwidth is increased as well. For the phase responses, the PM of the proposed AB-LDO at a high load is approximately

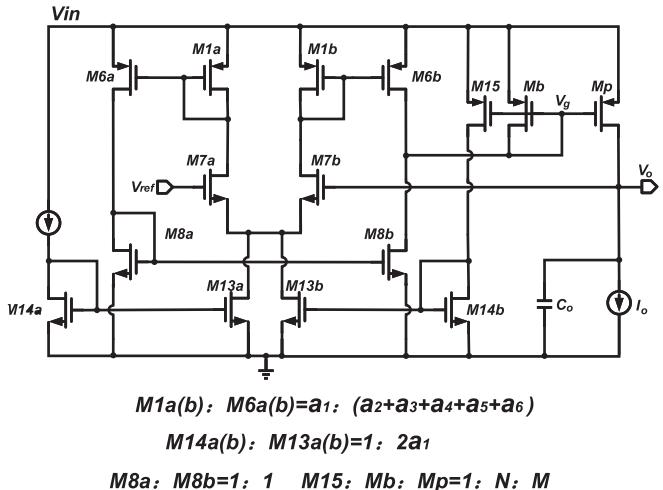
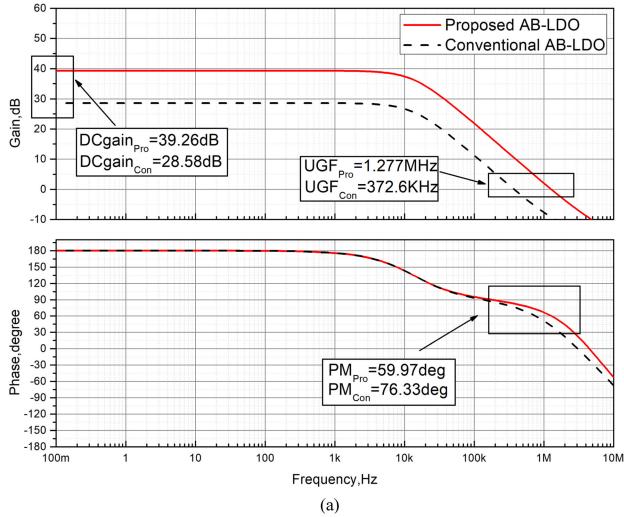


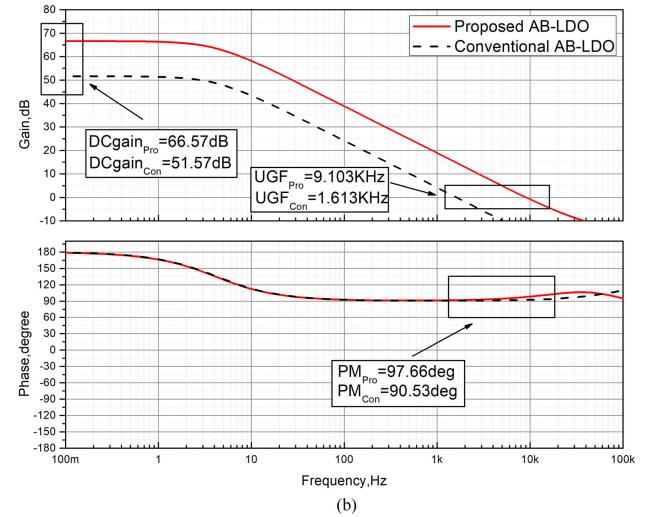
Fig. 12. Conventional AB-LDO without small-gain stages.

60 degrees, which indicates that it is stable. Compared with the proposed AB-LDO, the PM of the conventional AB-LDO is larger due to its lower bandwidth. Moreover, it can also be seen from the phase response that there are some effects caused by zero, partly because the ABL gain is not low enough. And in this design, the zeros do not have much of an adverse effect. Fig. 13 proves that under the same current and area consumption conditions, using multiple adaptive current feedbacks technique for AB-LDO with small-gain stages can improve the loop gain at high load and the loop bandwidth at low load without the need for frequency compensation to ensure stability.

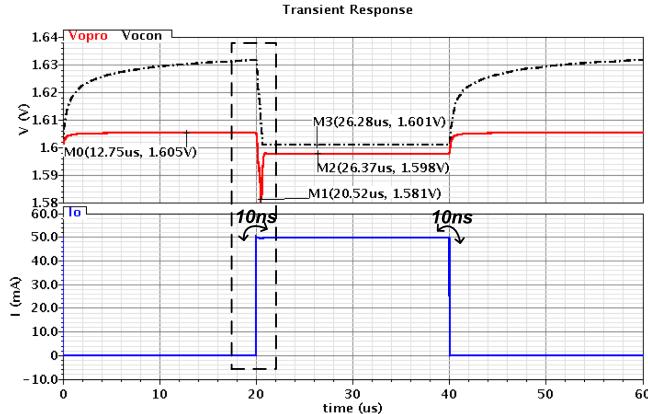
The comparison of the transient responses of the two AB-LDOs for a 10-ns step varying from 10  $\mu$ A to 50 mA in Fig. 14 can further reflect that the loop gain and loop bandwidth of the proposed regulator are effectively improved. Under the same current, area consumption, and guaranteed stability, the proposed AB-LDO can respond more rapidly than the conventional AB-LDO to achieve a stable output voltage, especially in the case of low-load current, indicating that the proposed AB-LDO has higher loop bandwidth than the conventional AB-LDO. Therefore, when the load current is small, the lower loop bandwidth of the conventional AB-LDO also leads to a larger undershoot in general. However, due to the lower loop gain of the conventional AB-LDO in the case of high-load current, the output voltage accuracy is much lower than that of the proposed AB-LDO. As a result, the difference between the output dc voltages at 10  $\mu$ A and 50 mA load current is so large that the undershoot is no longer significant compared to the output voltage difference. Fig. 14 proves that the proposed AB-LDO can obtain a better transient response compared with the conventional AB-LDO on the premise that the loop gain and loop bandwidth are boosted by using multiple small-gain stages to increase the transconductance. More importantly, the small-gain stages after using multiple adaptive current feedbacks technique do not affect the stability so that no ringing occurs in Fig. 14.



(a)



(b)

Fig. 13. Frequency responses of designed AB-LDO and conventional AB-LDO at (a) high load of 50 mA and (b) low load of 10  $\mu$ A, respectively.Fig. 14. Transient response simulations of the proposed and conventional AB-LDOs for a 10-ns step varying from 10  $\mu$ A to 50 mA.

#### IV. POSTSIMULATION AND TESTING RESULTS

The designed AB-LDO with multiple small-gain stages using multiple adaptive current feedbacks technique was fabricated in SMIC 0.18  $\mu$ m CMOS process and its microphotograph is displayed in Fig. 15. In this section, the postsimulation and testing results about line and load regulations and transient response are provided.

Fig. 16 provides the variation trend of measured quiescent current as the load current  $I_o$  changes, which is corresponding to the simulation result in Fig. 9. The line and load regulations that can reflect the loop gain of AB-LDO are simulated and tested. The results are given in Figs. 17 and 18. Fig. 17 shows the postsimulation results of line regulations at 10  $\mu$ A and 50 mA are 1.9 and 6.8 mV/V and the testing results are 4 mV/V and 36.8 mV, respectively, reflecting the decrease of gain of the whole loop under high-load current, which leads to the increase of line regulation. The simulated and tested load

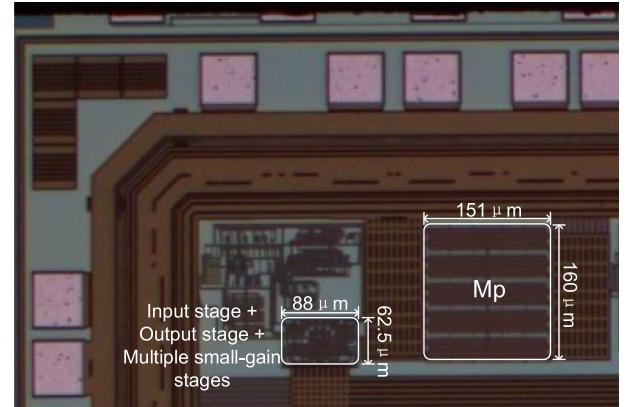


Fig. 15. Microphotograph of the designed AB-LDO.

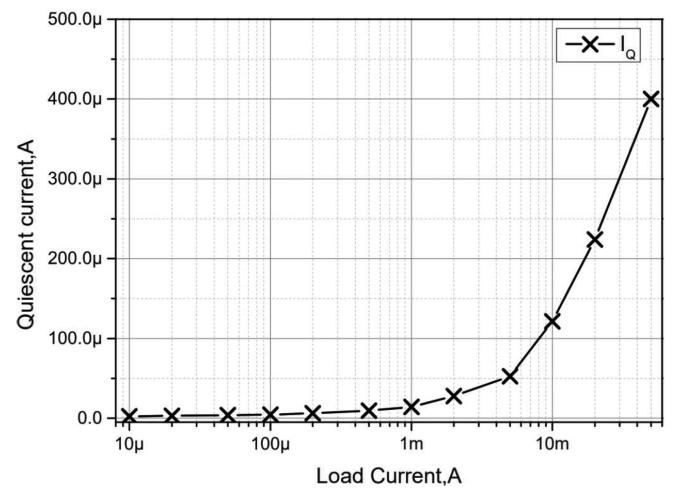


Fig. 16. Measured quiescent current versus load current.

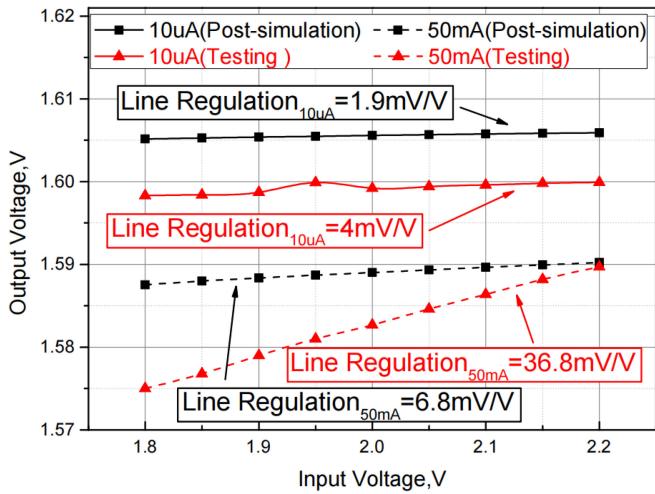


Fig. 17. Comparison of the line regulation postsimulation and testing results of the designed AB-LDO at  $10\ \mu\text{A}$  and  $50\ \text{mA}$ , respectively.

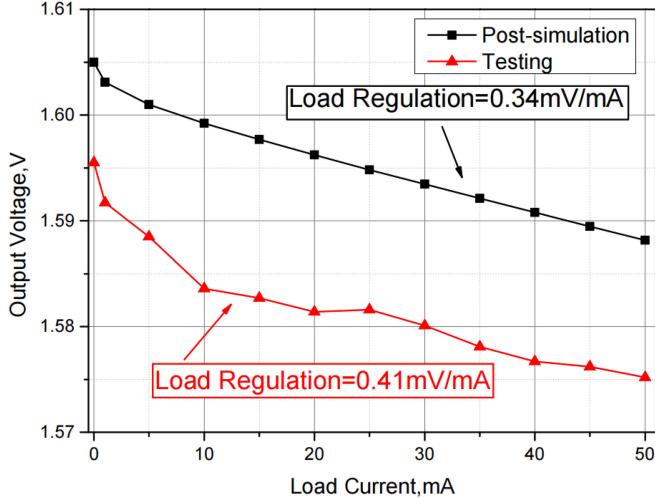


Fig. 18. Comparison of the load regulation postsimulation and testing results of the designed AB-LDO with the  $V_{\text{ref}}$  of  $1.6\ \text{V}$  at the load current varying from  $10\ \mu\text{A}$  to  $50\ \text{mA}$ .

regulation results of this LDO at the load current varying from  $10\ \mu\text{A}$  to  $50\ \text{mA}$  are displayed in Fig. 18, showing that the postsimulation and testing results of load regulation are  $0.34$  and  $0.41\ \text{mV}/\text{mA}$ . The power supply rejection (PSR) postsimulation and testing results of this designed AB-LDO from  $10\ \mu\text{A}$  to  $50\ \text{mA}$ , respectively, are shown in Fig. 19.

The transient response postsimulation of this design for a 10-ns step varying from  $10\ \mu\text{A}$  to  $50\ \text{mA}$  is given in  $I_o$  and  $V_o$  of Fig. 20 as well. The dc output variation is  $17\ \text{mV}$  and the undershoot is only  $30\ \text{mV}$ . The same 10 ns step current varying from  $10\ \mu\text{A}$  to  $50\ \text{mA}$  is set during the actual test as shown in Fig. 21 displaying that an undershoot of  $30.75\ \text{mV}$  and no overshoot is observed. Some spikes can be found in Fig. 21, which is caused by the  $LC$  series resonance due to the presence of parasitic inductance, conductance, and resistance in this design's actual measurement, especially the equivalent series inductance

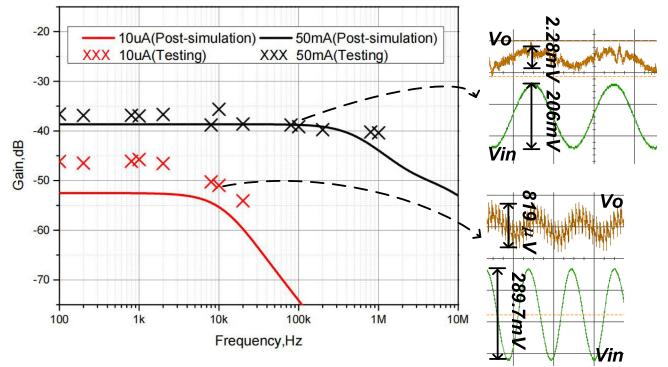


Fig. 19. Comparison of the PSR postsimulation and testing results of the designed AB-LDO from  $10\ \mu\text{A}$  to  $50\ \text{mA}$ , respectively.

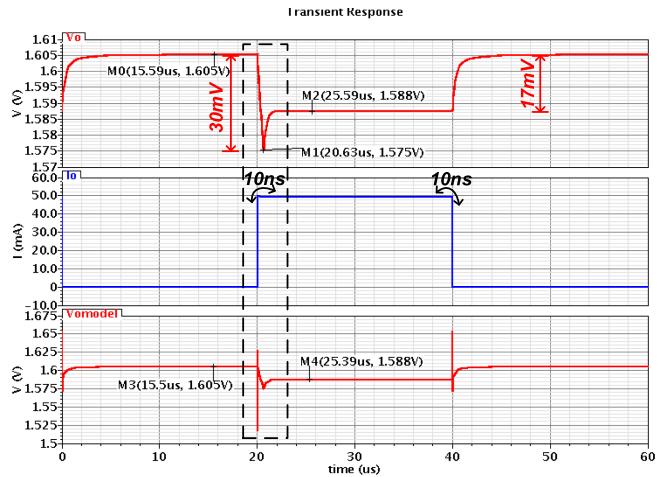


Fig. 20. Transient response postsimulation of the designed AB-LDO with  $V_{\text{in}}$  of  $1.8\ \text{V}$  for a 10-ns step varying from  $10\ \mu\text{A}$  to  $50\ \text{mA}$ .

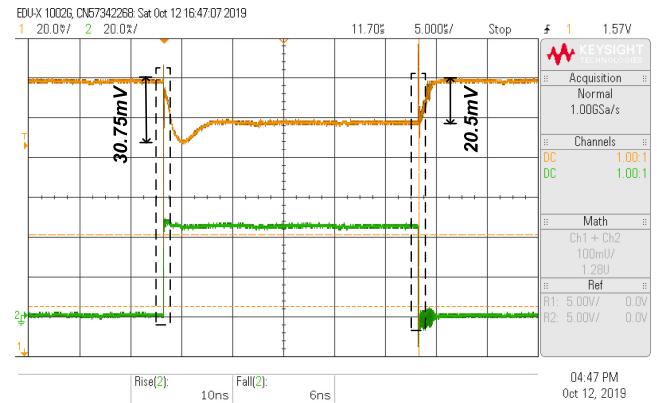


Fig. 21. Measured transient response of the designed AB-LDO with  $V_{\text{in}}$  of  $1.8\ \text{V}$  for a 10-ns step varying from  $10\ \mu\text{A}$  to  $50\ \text{mA}$ .

(ESL) of the output capacitance. The value of ESL is about  $1\text{--}3\ \text{nH}$ . After modeling an ESL of  $3\ \text{nH}$  in the postsimulation, the  $V_{o\text{model}}$  in Fig. 20 is obtained, which verifies that part of the reason for the spikes in the actual test is caused by ESL. In some specific applications, the inductance of various aspects needs to

TABLE I  
PERFORMANCE COMPARISON WITH PREVIOUS REPORTED LOW-DROPOUT REGULATOR

Parameter	This work	[20]	[21]	[22]	[16]	[12]
Year	2021	2021	2020	2018	2015	2010
Technology( $\mu\text{m}$ )	0.18	0.35	0.18	0.25	0.18	0.09
Chip Area( $\text{mm}^2$ )	0.0296	0.127	0.017	0.108	0.024	0.00274
Minimum $V_{in}$ (V)	1.8	2.7	1.4	1.5	1.2	1
Nominal $V_o$ (V)	1.6	2.5	1.2	1.0	1.0	0.9
Dropout Voltage(mV)	200	200	200	240	200	100
Quiescent Current $I_Q$ ( $\mu\text{A}$ )	2.5-400	124	13.5	1.24-100	135.1	9.3
Maximum Load Current(mA)	50	100	150	50	100	50
Current Efficiency(%)	99.2	99.88	99.9	99.9	99.86	99.9
Output Capacitance $C_o$ ( $\mu\text{F}$ )	1	4.7	4.7	1	1	1
ESR( $\Omega$ )	No	0.06	No	No	0.35	0.35
Load Regulation(mV/mA)	0.41	0.038	0.075	-	0.075	0.082
Line Regulation(mV/V)	4	1.667	7.785	-	22.7	14
Undershoot(mV)	30.75	11.2	20	85	25	6
Overshoot(mV)	0	8	17	32	0	8
FoM(ps)	20.3	287.7	52.2	20.9	168.9	52

be considered to avoid the influence of possible larger spikes. In both simulation and test results, no ringing occurs in the transient response, showing that the poles in the small-gain stages have no influence on the stability after using the multiple adaptive current feedbacks technique.

Table I gives the comparison of the performances with prior works. In contrast with [12] and [16], there is no need to use a resistor accurate to  $0.35\Omega$  in this design. In [22], despite a minimum quiescent current of only  $1.24\ \mu\text{A}$ , the overshoot/undershoot is still large. Compared with [20] and [21], although the maximum load current value in this design is not designed as high as these two papers, a smaller quiescent current consumption can be achieved due to the effect of the adaptive bias scheme. There is a figure of merit (FoM) from [4] [7] in the last row of the table, which means

$$\text{FoM} = \frac{C_o \cdot \Delta V_{o,pp} \cdot I_{Q,\min}}{\alpha \cdot \Delta I_{o,max}^2} \quad (14)$$

$\alpha$  is the ratio of the technology used in the present work to the minimum technology in all compared works.  $\Delta V_{o,pp}$  is the peak-to-peak voltage of the transient response, and the other symbols have the same meaning as usual. Under the precondition of using the multiple adaptive current feedbacks technique for small-gain stages to ensure the stability of LDO, this article realizes the minimum FoM value among all the works compared, which indicates that this AB-LDO design has a great response performance considering power consumption, output capacitance, technology, and other aspects.

## V. CONCLUSION

In this article, a multiple adaptive current feedbacks technique for small-gain stages in AB-LDO is adopted, which can improve the loop gain at high load and the loop bandwidth at low load of AB-LDO without the need for complicated frequency compensation to solve the stability problems caused by the internal poles from multiple small-gain stages. Additionally, for a circuit containing multiple loops, this article adopts a method of breaking at the common link for analysis, which can intuitively and simply obtain the frequency-response of the complete circuit. The postsimulation and testing results are presented, showing

that the designed AB-LDO performs well and conforms to simulation results. The AB-LDO with small-gain stages using multiple adaptive current feedbacks technique can provide an option for portable equipment due to its small area consumption and great transient response.

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