# Ultrahigh PSR Output-Capacitor-Free Adaptively Biased 2-Power-Transistor LDO With 200-mV Dropout

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***Abstract*—This letter presents an output-capacitor-free cascaded 2-power-transistor low-dropout (2-PT LDO) regulator with ultrahigh power supply rejection (PSR) and fast transient response for low-power biomedical system on chips. The proposed 2-PT LDO consists of two stages in series, and the total dropout voltage is 200 mV. In order to boost the total PSR in a wide frequency range, different PSR enhancement strategies are adopted in each stage and a reversed-phase supply-ripple-cancelation technique is provided by a proposed reference buffer to further improve the PSR performance. Furthermore, adaptive biasing with robust frequency compensation is utilized to maintain system stability with fast transient response. Designed and fabricated in a 0.18-$\mu$m CMOS process, the active area is only 0.0237 mm$^2$. With the input voltage of 1.1–1.2 V, the 2-PT LDO supplies 0.9–1 V with a total quiescent current of 24.2 $\mu$A at no-load current. Experimental results show that PSR is better than −95dB up to 100 kHz.**

***Index Terms*—2-power-transistor low dropout (2-PT LDO), adaptive biasing, reversed-phase power supply rejection (PSR) reference buffer (BUF), robust frequency compensation, ultrahigh PSR.**

## I. Introduction

In recent years, wearable and/or implantable biomedical electronics are becoming mainstream, making personal healthcare easy and convenient. To prolong the battery cycle time, low-power and high-efficiency system-on-chips (SoCs) are required by biomedical applications. A clean power supply is also instrumental in enhancing the signal-noise ratio (SNR) in reading vital signals. The analog biomedical frontend circuits have low-frequency signal bandwidth, such as electrode-based recording with a bandwidth of 250 Hz and neural activity recording with a bandwidth of up to 10 kHz [1]. The biomedical analog frontend circuits require clean power supplies in the sampling frequency up to 100 kHz.

Li-ion battery is widely used as the power source of a wearable biomedical device. The battery voltage is usually converted down by a switch-mode dc–dc converter, which supplies power to highly integrated SoCs with high power efficiency. The switching noise and voltage ripples generated by the switching converter may deteriorate the performance of noise-sensitive blocks. Low-dropout (LDO) regulators are widely used to provide clean voltage supplies with low ripple. With the advanced supply-ripple-cancelation techniques, LDOs may achieve high power-supply rejection (PSR) in a wide frequency range [2]–[10]. Note that low-power biomedical devices work in the sleep mode most of the time, and power consumption in the sleep mode is detrimental to the system power efficiency. Fast transient response is also needed to wake up the system in a short time. Adaptive biasing has been proven to achieve fast transient response without significant efficiency degradation under the sleep mode [8]. In multichannel bioelectronics, many LDOs are needed in a single SoC (eight LDOs in [1]), and external components such as output filtering capacitors should be eliminated to reduce the printed circuit board layout space. Hence, output-capacitor-free LDOs are preferred in wearable and implantable bio-SoCs.

The state-of-the-art one-power-transistor LDOs could achieve high PSR better than -50 dB in the range of 100 kHz by using the feedforward ripple cancelation (FFRC) technique in [2]–[4], as shown in Fig. 1(a). This technique relies on an ac current replica that uses a large on-chip RC-network. The feedforward ac current is injected into the gate [2] or the body [3] of the power transistor $M_P$, and it cancels the perturbation caused by the parasitics of $M_P$. This technique requires either a scaled ac current replica [2] or a drain-source impedance ratio sensor [3]. The ac current replica technique requires a high-precision power-hungry current amplifier to match the current generated by the PSR enhancer and the required compensated current [2]. Using a drain-source impedance ratio sensor is power efficient, but it requires a large chip area for a 20-pF gate-source decoupling capacitor and a large on-chip RC-network with a corner frequency of 6.5 kHz [3]. Instead of the one power transistor solution, a 2-power-transistor (2-PT) LDO with supply-ripple isolation (SRI) technique has been developed in [5]–[7], as shown in Fig. 1(b). This architecture consists of a nMOS power transistor and a pMOS power transistor. The nMOS power transistor is biased by a voltage reference generator (VRG) and a low-pass filter (LPF) powered up by a charge pump (QP) [6], or controlled by an auxiliary replica LDO with a first-order LPF [7]. The nMOS power transistor needs a step-up QP and sufficient dropout voltage for good SRI. This results in a large total dropout voltage, e.g., 600 mV in [6] and 400 mV in [7]. SRI technique also requires a large on-chip RC-network for low-pass supply-ripple filtering, e.g., 500-kΩ resistor and 15-pF capacitor in [6] and 50-kΩ resistor and 25-pF capacitor in [7].

This letter presents an ultrahigh-PSR output-capacitor-free LDO with a cascaded 2-PT topology and both power transistors are pMOS. The total dropout voltage is 200 mV. To boost the total PSR, the proposed LDO adopts different PSR enhancement strategies in each stage, and a novel reversed-phase PSR reference buffer (BUF) is designed for the first stage to enhance the PSR significantly in a wide frequency range. Thus, the proposed LDO achieves excellent tradeoffs among different design parameters.

## II. Implementation Of the Proposed 2-PT LDO

### A. Principle and Implementation

Fig. 1(c) and (d) presents the PSR sketch and schematic of the proposed ultrahigh PSR 2-PT LDO, respectively. To minimize the

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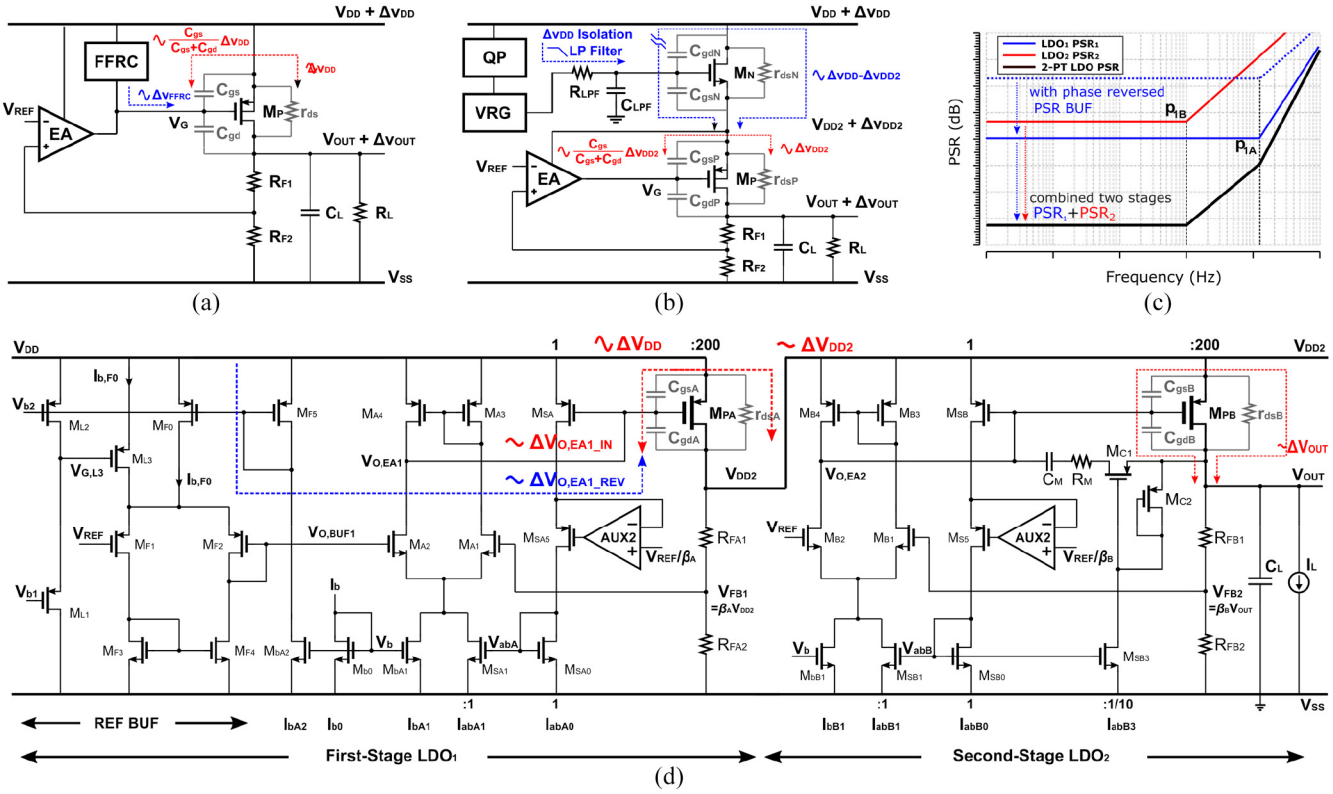


Fig. 1. (a) PSR enhanced with FFRC injected into the gate of $M_P$. (b) 2-PT SRI LDO with QP and VRG. (c) PSR sketch of the proposed 2-PT LDO. (d) Schematic of the proposed 2-PT LDO.

total dropout voltage, both power transistors $M_{PA}$ and $M_{PB}$ are realized by pMOS transistors each with a dropout voltage of 100 mV, and they work in the linear region at heavy load conditions. Since both power transistors are pMOS, QP and LPF are not needed in the first stage. The feedback voltages $V_{FB1}$ and $V_{FB2}$ are the scaled output voltages with feedback ratios $\beta_A$ and $\beta_B$, which are realized by resistor ladders ($R_{FA1}$, $R_{FA2}$, and $R_{FB1}$, $R_{FB2}$). Both stages utilize adaptive biasing to maintain a fast transient response with high power efficiency. The adaptive biasing currents are directly derived from power transistors using two current mirrors $M_{PA}/M_{SA}$ and $M_{PB}/M_{SB}$. The auxiliary amplifiers AUX1 and AUX2 are used for driving the source-drain voltages of $M_{SA}$ and $M_{SB}$ to be the same as the source-drain voltages of $M_{PA}$ and $M_{PB}$, respectively.

As shown in Fig. 1(c), the total PSR of the 2-PT LDO is the sum of $PSR_1$ (PSR of the first stage) and $PSR_2$(PSR of the second stage) in a log scale. Instead of simply cascading two stages, the proposed design employs different PSR enhancement strategies in each stage.

In the second stage, $PSR_2$ is achieved in the low-frequency range mainly thanks to the high dc gain, which also maintains high-precision output voltage control over a wide load current range. For a simplified analysis, dc-PSR ($PSR_{DC}$) is approximately equal to the inverse of the dc gain $1/A_{LDO2,DC}$, and the corner frequency is almost the same as the dominant pole $p_{1B}$. The stability of the second-stage $LDO_2$ is also essential as it has a large output capacitance. As a result, the dominant pole ($p_{1B}$) usually is relatively low and the PSR is enhanced in a narrow bandwidth. A pole-tracking compensation (PTC) network is used to provide sufficient phase margin (PM) and gain margin (GM) over the whole load current range. The PTC robust frequency compensation network is made up of $C_M$, $R_M$, and $M_{C1}$, which is adaptively biased by $I_{abB3}$ with $M_{SB0}$ : $M_{SB3}$ that equal to 10:1.

In the first stage, $PSR_1$ is boosted for wide bandwidth with a reversed-phase PSR reference BUF. It works by introducing a reversed-phase PSR path that counteracts the increase in the output voltage due to the in-phase PSR path [10]. Thus, PSR capability is greatly improved below the dominant pole ($p_{1A}$). As shown in Fig. 1(c), in order to provide a wide bandwidth PSR and keep the loop stable, the first-stage $LDO_1$ is designed with a relatively low dc gain and large $p_{1A}$. In addition, $LDO_1$ powers up the second-stage $LDO_2$ with a small equivalent load capacitance $C_{LA}$ (from $V_{DD2}$ to $V_{SS}$, $\sim$ 4 pF in this design), so the second pole $p_{2A}$ at the output node is far away from the dominant pole $p_{1A}$ at the gate of $M_{PA}$. Sufficient stability margins could be maintained over the whole load current range without compensation and still has a wide PSR bandwidth. Detailed stability condition analysis for the adaptively biased LDO could refer to [11].

### *B. Frequency Response and PSR Analysis*

The dc gain and dominant pole of both stages are listed as follows. For the first-stage $LDO_1$

$$A_{LDO1,DC} = \beta_A g_{m.,A1} g_{m,PA} R_{o,EA1} R_{o,A} K_A \tag{1}$$

$$K_A = \frac{1}{1 - \frac{g_{m,PA}}{2Bg_{m,A3}}} \tag{2}$$

$$p_{1A} \approx -\frac{1}{g_{m,PA} R_{o,A} R_{o,EA1} \left(K_A C_{o,EA1} - (K_A - 1) 2C_{gs,A3}\right)}. \tag{3}$$

For the second-stage $LDO_2$

$$A_{LDO2,DC} = \beta_B g_{m.,B1} g_{m,PB} R_{o,EA2} R_{o,B} K_B \tag{4}$$

$$K_B = \frac{1}{1 - \frac{g_{m,PB}}{2Bg_{m,B3}}} \tag{5}$$

$$p_{1B} \approx -\frac{1}{g_{m,PB} R_{o,B} R_{o,EA2} \left(C_M + K_B C_{o,EA2} - (K_B - 1) 2C_{gs,B3}\right)}. \tag{6}$$

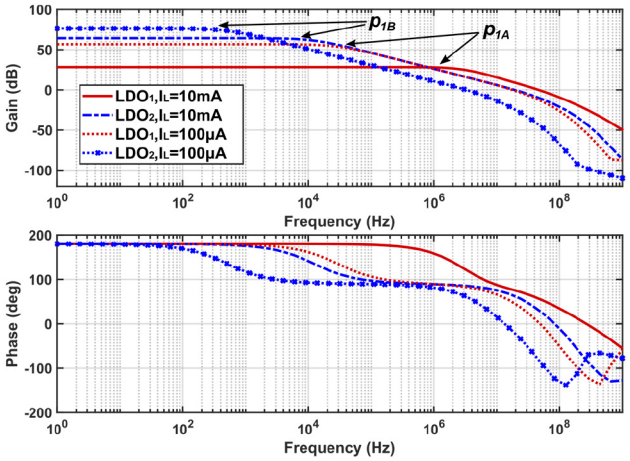


Fig. 2. Simulated frequency response of $LDO_1$ and $LDO_2$ under light load current $I_L = 100\mu A$ and heavy load current $I_L = 10$ mA.

In equations (2) and (5), $B$ is the size ratio of $M_{PA}$ : $M_{SA}$ ($M_{PB}$ : $M_{SB}$), which is set to 200:1 in this design. The adaptive current biasing to the error amplifier constitutes a common-gate feedback loop, and the gains of each stage are $K_A$ and $K_B$, respectively, which are around 10 dB. Fig. 2 shows the simulated frequency responses of both stages. $LDO_1$ has a wide 3-dB corner frequency and a relatively low dc gain, while $LDO_2$ has a large dc gain to generate an accurate output voltage. Moreover, simulations over all process and temperature corners and load current range are completed and the results show that the PMs are better than 42.2° and GMs are better than 14.2 dB for $LDO_1$, and PMs are better than 60.7° and GMs are better than 15.5 dB for $LDO_2$.

In the second stage, $PSR_2$ is mainly contributed by the gain of the loop, so the frequency response of $PSR_2$ can be estimated from $A_{LDO2,DC}$ and $P_{1B}$. In the first stage, the phase-reversed PSR BUF is proposed to enhance PSR with a low dc gain. Two paths are identified to analyze the PSR performance of $LDO_1$. The parasitics of $M_{PA}$ dominate in Path 1, which is from $V_{DD}$ through $EA_1$ and $M_{PA}$ to $V_{DD2}$. As $\Delta V_{DD}$ increases, the source-gate voltage of $M_{PA}$ increases, pumping more current to the output, and $\Delta V_{DD2}$ increases. The output ripples are in phase with the supply ripples. In Path 2, $\Delta V_{O,BUF1}$ decreases with the specially designed BUF ($g_{m,F7}/g_{m,F8} > 1$) when $\Delta V_{DD}$ increases. It drives the output of $\Delta V_{O,EA1}$ up, and $\Delta V_{DD2}$ decreases. The decrease in $\Delta V_{DD2}$ due to Path 2 will offset the increase in $\Delta V_{DD2}$ due to Path 1, and supply-ripple subtraction is achieved. The detailed PSR frequency analysis of the single-stage LDO with the phase-reversed PSR BUF is presented in [10]. For the interested frequency range, the PSR analysis can be simplified by giving their dc PSR and the location of the zeros. Therefore, the first-stage $PSR_1$ could be simplified as

$$\mathrm{PSR}_{1,DC} \approx \frac{K_A \cdot K_{psr}}{1 + A_{LDO1,DC}} \tag{7}$$

$$z_{psr1} \approx \frac{K_{psr} \cdot p_{1A} \cdot z_{\mathrm{BUF}}}{z_{\mathrm{BUF}} + (K_{psr} - 1)p_{1A}} \tag{8}$$

where

$$K_{\mathrm{psr}} = 1 - g_{m.,A1} g_{m,PA} R_{o,EA1} R_{o,A} g_{m,F6} \frac{\left(\frac{g_{m,F7}}{g_{m,F8}} - 1\right)}{2 g_{m,F1} g_{m,F3} r_{ds,F1}} \tag{9}$$

$$z_{\mathrm{BUF}} \approx -\frac{1}{2 C_{g,F3} r_{ds,F1}}. \tag{10}$$

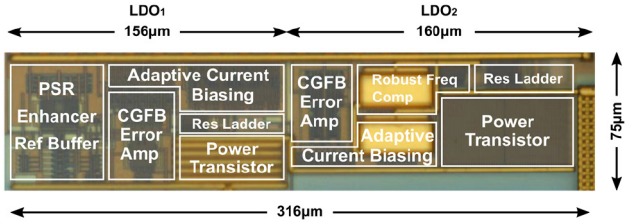


Fig. 3. Die photograph of the fabricated 2-PT LDO.

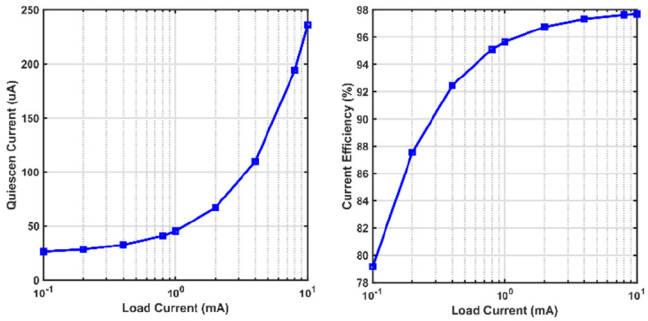


Fig. 4. Measured (a) quiescent current and (b) current efficiency versus $I_L$.

The second-stage $PSR_2$ could be simplified as

$$\mathrm{PSR}_{2,DC} \approx \frac{K_B}{1 + A_{\mathrm{LDO2,DC}}} \tag{11}$$

$$z_{psr2} \approx p_{1B}. \tag{12}$$

The total PSR analysis of the proposed 2-PT LDO is the sum $PSR_1$ and $PSR_2$. With an optimized designed BUF, $K_{psr}$ approaches to 0, and $PSR_1$ could be enhanced significantly below its 3-dB frequency range. It is expected that the first stage PSR corner frequency $z_{psr1}$ should cover the interested high-PSR frequency range, which is 100 kHz in this design. Thus, the proposed 2-PT LDO could achieve ultrahigh PSR for low-power biomedical electronics.

## III. Experimental Results

The proposed 2-PT LDO has been designed and fabricated in a 0.18-$\mu$m CMOS process with an active area of 0.0237 $mm^2$, as shown in Fig. 3. The design has an input voltage $V_{DD}$ range of 1.1–1.2 V, and the total dropout voltage $\Delta V$ is 200 mV. The quiescent current is 24.2 $\mu$A at no load current, where $LDO_1$ has 8.8 $\mu$A and $LDO_2$ has 15.4 $\mu$A. At full load current 10 mA, the total adaptively biased quiescent current is 243 $\mu$A (112 $\mu$A for $LDO_1$ and 131 $\mu$A for $LDO_2$), and the measured quiescent current and current efficiency under different load currents are shown in Fig. 4. An off-chip 100-pF load capacitor is included to emulate the capacitive loading.

Fig. 5 shows the transient response of the proposed 2-PT LDO under different supply voltages. With a load current step of 0–10 mA and edge time of 100 ns, the measured undershoot is below 282 mV, and the overshoot does not exceed 74 mV. Besides the adaptive current biasing technique, the dynamic biasing network, which could generate a charging/discharging current pulse to speed up the slew rate during transient response, can also be integrated into the proposed LDO in future work to further reduce the undershoot and overshoot. The dc load regulation is 0.69 mV/mA (including the on-chip routing and bonding resistance). Fig. 6 shows the measured PSR frequency response for three chips at 10-mA load current, 1.1 and 1.2-V supply voltages, and 200-mV dropout voltage. With the proposed reversed-phase PSR BUF, the total PSR is better than −95 dB up to 100 kHz

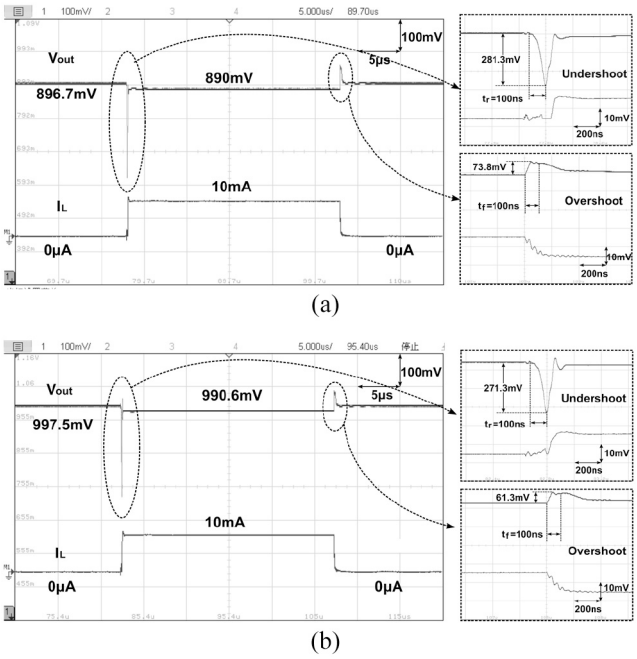


Fig. 5. Measured transient response with zoom-in undershoot and overshoot ripples, the rising and falling time is 100 ns: (a) $V_{DD} = 1.1$V, $V_{OUT} = 0.9$V, and $I_L = 0-10$ mA and (b) $V_{DD} = 1.2$V, $V_{OUT} = 1$ V, and $I_L = 0-10$ mA.

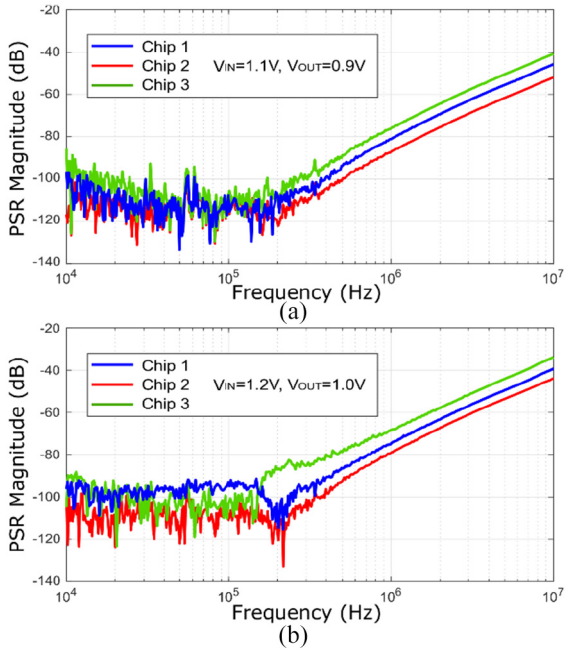


Fig. 6. PSR measurement results of the proposed 2-PT LDO with 200 mV dropout voltage. (a) $V_{IN} = 1.1$ V, $V_{OUT} = 0.9$ V. (b) $V_{IN} = 1.2$ V, $V_{OUT} = 1.0$ V.

for the worst case among the measured three chips, which covers the biosignal bandwidth. The summary of performance comparison with state-of-the-art LDOs is listed in Table I.

## IV. Conclusion

An ultrahigh PSR 2-PT LDO design with 200-mV total dropout voltage was proposed for low-supply voltage wearable bioelectronics. The PSR is better than −95 dB PSR up to 100 kHz, which covers the biosignal bandwidth. The proposed design achieved excellent tradeoffs among ultrahigh PSR, compact active area, fast transient response, and low-power consumption in the specified frequency range.

TABLE I
Performance Summary and Comparison for the Proposed LDO

| Parameter | This work | | [2] | [3] | [6] | [7] |
|---|---|---|---|---|---|---|
| Process [µm] | 0.18 | | 0.18 | 0.065 | 0.6 | 0.35 |
| Area [mm$^2$] | 0.0237 | | 0.14 | 0.087 | N/A | 0.055 |
| Type | PMOS+PMOS | | PMOS | PMOS | NMOS+ PMOS | NMOS+ PMOS |
| $V_{DD}$ [V] | 1.2 | 1.1 | 1.8 | 1.2 | 1.8 | 1.6 |
| $V_{OUT}$ [V] | 1 | 0.9 | 1.6 | 1 | 1.2 | 1.2 |
| Max. $I_L$ [mA] | 10 | | 50 | 25 | 5 | 12 |
| $C_L$ [pF] | 100 | | 100 | 240 | 10 | 100 |
| Load Reg. [mV/mA] | 0.67 | 0.69 | 0.14 | 0.06 | 10 | 0.68 |
| $I_q$ [µA] @no load | 24.2 | 24.1 | 55 | 8 | 70 † | 43.9 |
| $\Delta V_{OUT}$ [mV] / $T_{edge}$ [ns] | 271.3 / 100 | 281.3 / 100 | 75 / 100 | 225 / 100 | 710 / 10 | 105 / 500 |
| PSR [dB] @100kHz | < -95 # | < -105 # | -61 | -52 | -63 | -37 |
| $FOM_T$ * [ps] | 6.84 | 6.78 | 0.264 | 0.691 | 19.88 | 3.201 |

* $FOM_T = \frac{(C_L \times \Delta V_{OUT} \times I_q)}{(I_{MAX})^2}$
# Worst case among the measured three chips
† Exclude charge pump current consumption

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