An Adaptively Biased LDO Regulator with 11nA Quiescent Current and 50mA Available Load

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***Abstract*—This paper presents a low-dropout (LDO) regulator structure which sets its bias current adaptively based on its load current for energy efficiency. Over-current and short-circuit protection functions are implemented in the LDO with almost zero quiescent current addition. The proposed structure is inherent stable without output capacitance requirement. The proposed LDO was fabricated with a standard 0.18 µm technology with measured quiescent current consumption of 11nA under no-load condition and a maximum available load current of 50mA. The measured line and load regulations were 0.86mV/V and 0.2mV/mA, respectively.**

Keywords—LDO, Adaptive Biasing, Positive Feedback, Series-Series Feedback, Capacitor-less

I. INTRODUCTION

As a fundamental and essential building block, low-dropout (LDO) regulators in low power applications are designed to achieve low quiescent current (I_Q) and high load current (I_{LOAD}) deliverability [1]-[7]. However, a minimum quiescent current level is required in LDOs to balance the power consumption with loop stability, transient response, and safeguards like over-current and short-circuit protections [8]-[12]. Moreover, low power and miniature applications usually require a capacitor-less solution in LDOs designs [13].

This work presents a LDO structure which reduces quiescent current with an adaptive current biasing scheme. As shown in Fig. 1, unlike conventional structures with negative feedback loops, the presented LDO introduces a positive series-series feedback path to set the bias current proportional to the load current. By keeping the positive feedback ratio close to but less than one, the proposed structure achieves similar line/load regulations and transient response as conventional high open-loop-gain structures but consumes much less quiescent current. Moreover, owing to the positive feedback regulation scheme, the proposed structure is inherent stable without any requirement on the load capacitance.

II. PROPOSED LDO STRUCTURE

In a conventional LDO structure with an NMOS source follower output stage shown in Fig. 1(a), a negative feedback loop with high open loop gain is formed to regulate the output voltage (V_{OUT}) based on a reference voltage (V_{REF}). The output impedance of the LDO is lowered by the DC loop gain so a high load and line regulations are achieved. However, achieving a high open loop gain across a wide load current range with low quiescent current budget is difficult. The proposed LDO structure, as shown in Fig. 1(b), achieves a low biasing current without load capacitor requirement through a series-series feedback regulation. The equivalent loop transfer function is illustrated in Fig. 1(c) and the closed-loop output impedance R_{OUT0} can be calculated as

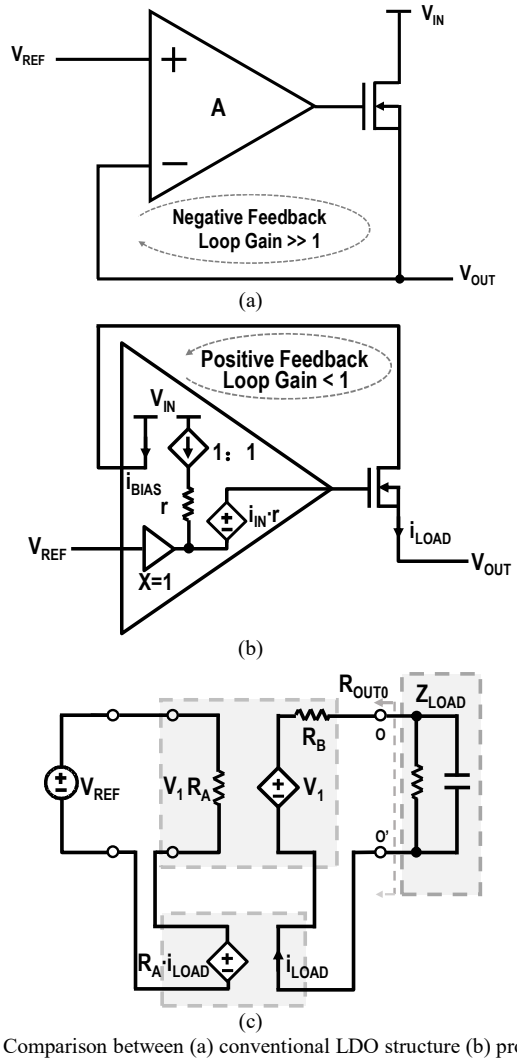

Fig. 1. Comparison between (a) conventional LDO structure (b) proposed LDO structure and (c) Equivalent series-series positive regulation loop.

$$R_{OUT0}=R_B - R_A \quad (1)$$

$$T_0= R_A/(R_B+Z_{LOAD}) \quad (2)$$

where T_0 is the loop gain, Z_{LOAD} is the impedance of the load. Since the DC feedback ratio is positive, the loop gain needs to be less than 1 for stability. The output impedance R_{OUT0} in (1) determines the line and load regulations of the proposed LDO. As expressed in (1), R_{OUT0} is equal to the impedance difference between R_B and R_A. Therefore, the voltage drop across R_B is regulated to the same voltage across R_A with a label of V_1 in Fig. 1(c). In this design, R_A and R_B are set equal for low output impedance, so the voltage drop across R_A is cancelled by V_1 and the output voltage remains almost constant as load current or supply voltage changes.

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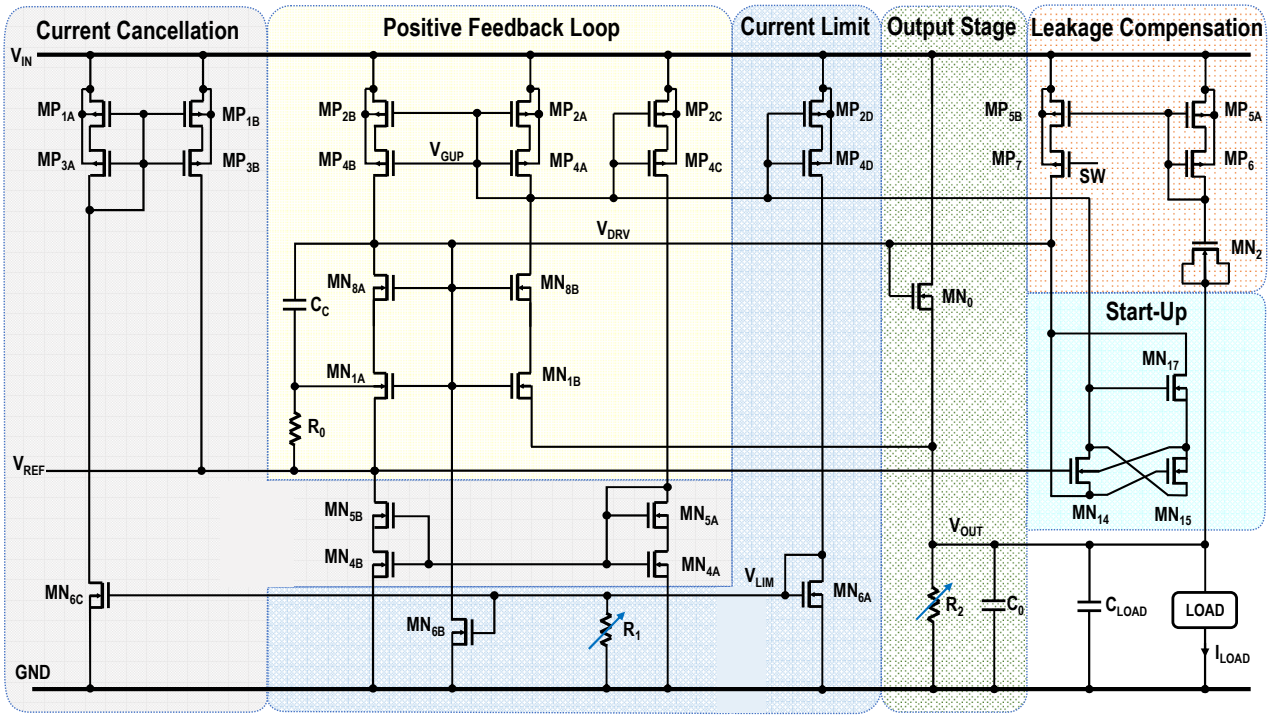


Fig. 2. Schematic of the proposed LDO regulator

Note that the load impedance (Z_{LOAD}) is always non-zero, so the feedback loop has a DC loop-gain in (2) less than one and is inherent stable without any frequency compensation capacitor needed. However, if a large load capacitor is used for output decoupling, the values of Z_{LOAD} and T_0 at high frequencies will approach 0 and 1, respectively. Regarding the mismatches in current mirrors and between R_A and R_B, the feedback ratio may exceed 1 and the loop could become instable at high frequencies. In this work, a high frequency pole is inserted to guarantee the loop gain to be less than one across the entire frequency band.

III. Transistor Level Implementation

The proposed LDO structure is implemented by the transistor level schematic shown in Fig. 2 which includes sub-functions of positive feedback regulation, current limit, input current cancellation, leakage compensation, start-up, and output source follower.

A. Regulation Loop

The output of the LDO is driven by a large NMOS follower (MN_0) stage. The gate voltage of MN_0 is under regulation by a series-series positive feedback loop formed of MP_{2A}, MP_{2B}, MN_{1A} and MN_{1B}, which corresponds to the loop illustration in Fig. 1(c). The voltage-control-voltage-source (VCVS) is realized by the diode-connected follower stage of MN_{1A} and MN_{1B}. The resistance of R_A and R_B corresponds to $1/GM_{MN1A}$ and $1/GM_{MN1B}$, respectively. As mentioned previously, R_{1A} and R_{1B} are chosen to be equal to achieve high line/load regulations. So, in this work, MN_{1A} and MN_{1B} are sized equal and the current mirror ratio between MP_{2A} and MP_{2B} is 1:1. With capacitive load, the total output impedance Z_{LOAD} decreases as frequency increases and the loop gain approaches one, which leads to a potential instability and oscillation problem. Therefore, in this design, C_C and R_0 are added to create a pole to limit the peak loop gain to be less than one under all conditions. Simulations with different load current and output load capacitors in Fig. 3(a) and Monte-Carlo results in Fig. 3(b) indicate a stable regulation across 0-50mA load current with 0-20µF load capacitor.

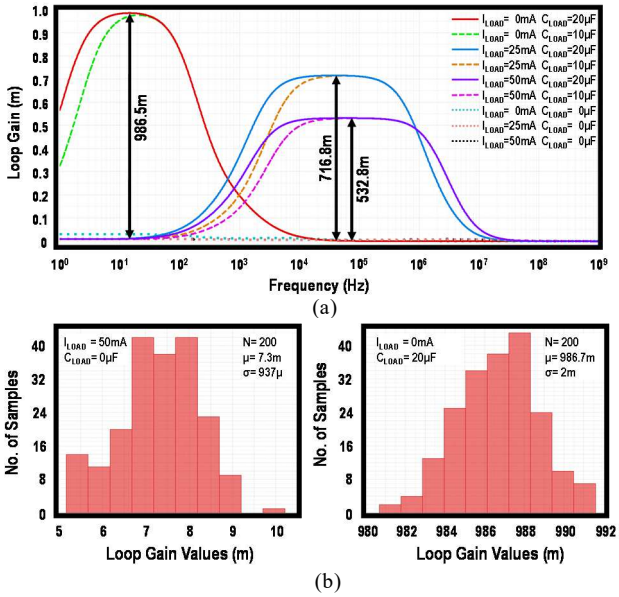


Fig. 3. Loop analysis with (a) different I_{LOAD}, C_{LOAD} and (b) Monte-Carlo mismatches.

B. Load Regulation

In the proposed design, high line and load regulations are achieved by setting MN_{1A} to be the same size as MN_{1B} as described in subsection III-A. In other words, the gate-to-source voltage drop of MN_{1B} due to the load current change is canceled by the inverse of the gate-to-source voltage change of MN_{1A}, so V_{OUT} remains almost the same across a wide load current range. With loop closed, the remaining dominant factor that affects load regulation is the output impedance of MN_{1B} and MP_{2B}, which causes the gate-to-source voltage of MN_{1B} to increase slightly as the load current increases. Therefore, cascode devices are utilized and the lengths of MP_{2A} and MP_{2B} are sized large to increase the output

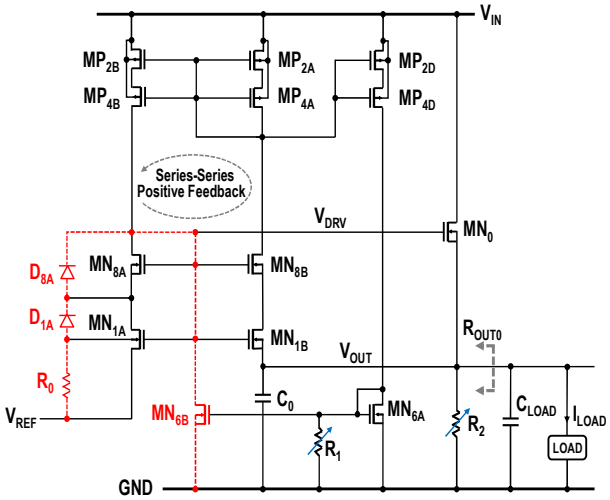


Fig. 4. Positive feedback loop and current limit function.

impedance of MN_{1B} and MP_{2B}. The closed-loop output impedance can therefore be approximated as

$$R_{OUT0}=\frac{1}{k}\cdot\frac{GDS_{MN1B}\cdot GDS_{MN8B}}{GM_{MP2A}\cdot GM_{MN1B}\cdot GM_{MN8B}} \quad (3)$$

where GDS_{MN1B} and GDS_{MN8B} refer to the inverse of output impedance of MN_{1B} and MN_{8B}, respectively, while GM_{MN1B}, GM_{MN8B} and GM_{MP2A} are the transconductance of MN_{1B}, MN_{8B} and MP_{2A}, respectively. The parameter k is the size ratio between MN_0 and MN_{1B} which is set to 1200 in this work for high output current deliverability. The ratios of (GDS_{MN1B}/GM_{MN1B}) and (GDS_{MN8B}/GM_{MN8B}) can therefore be interpreted as the gain of MN_{1B} stage and MN_{8B} stage, respectively. Both stages have a gain value from 5m to 250m across the full load and temperature range, which largely attenuate the output impedance of the LDO.

C. Current Limiting

Since the bias currents flowing in the proposed LDO are all proportional to the load current, the output current can increase to several amperes easily which will heat and damage the pass device MN_0. As a result, the output current limiting function is included in this design to pull the driving signal (V_{DRV}) low when the sensed output current exceeds the current limit set by R_1, which is trimmed in this design. The detailed over current protection circuit is shown in Fig. 4. The mirrored output current flowing in MN_{1B} generates a sensed voltage across the resistor R_1. If the sensed voltage exceeds the threshold of MN_{6A} and MN_{6B}, the driving signal V_{DRV} will be pulled low by MN_{6B}. Afterwards, the body diodes of MN_{1A} and MN_{8A} are turned on and the resistors R_0 limits the current in the V_{DRV} discharge path.

When the current limiting path is turning on, the addition of the limiting current from MN_{6A} and MN_{6B} will convert the phase of the main regulation loop by 180 degree. However, due to the large parasitic capacitance on the V_{DRV} net, the high frequency gain is attenuated, so both the main regulation loop and the current limiting loop are stable across a wide load capacitance range.

D. Input Current Cancellation

To achieve a high input impedance so that the LDO can be easily driven by a reference generator such as a bandgap, DAC or even a resistor divider, the current drawn from V_{REF} node should be minimized. As shown in Fig. 2, the current fed from

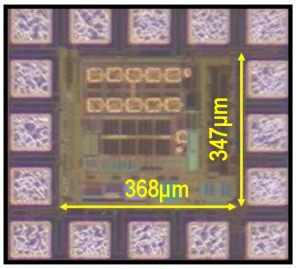
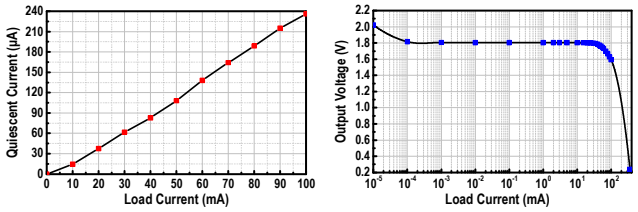


Fig. 5. Chip micrograph.



(a) (b)

Fig. 6. Measured (a) quiescent current and (b) output voltage as a function of the load current.

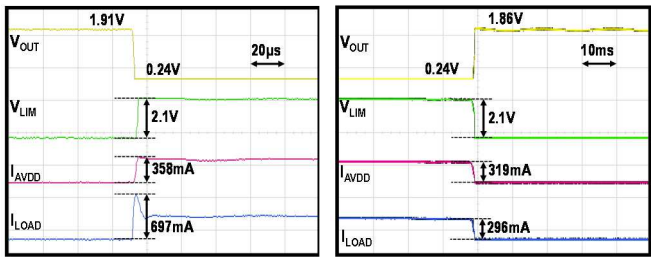
MN_{1A} into V_{REF} node is mirrored and canceled by the current sink in MN_{5B}. The current drawn by MN_{6A} during current limiting condition is also mirrored and canceled by the current sourced from MP_{3B}. If all current mirrors are matched perfectly, the 'net-current' drawn from V_{REF} should be zero and is independent of the load current. Monte-Carlo simulation shows a 3-sigma input leakage current of less than 1µA.

E. Start-Up and Leakage Compensation

There is a potential startup issue of the proposed structure if the initial bias currents in the mirrored feedback path is zero. In this condition, the LDO will stuck in the state and the V_{DRV} voltage stays low without current being mirrored from output. So, in this design, MN_{14} is added to catch this situation and feed current into the MP_{2B} and MP_{2A} current mirror when the V_{DRV} signal is initially low. To keep the body diode of MN_{14} off across a wide supply range, its body is adaptively connected to the lower side of its drain and source by MN_{15} and MN_{17}. After start-up, MN_{14} will remain off since its gate is connected to a potential much lower than its source voltage. Moreover, a current mirror of MP_{5A} and MP_{5B} are added to compensate the gate leakage current of MN_0 and help start up as well.

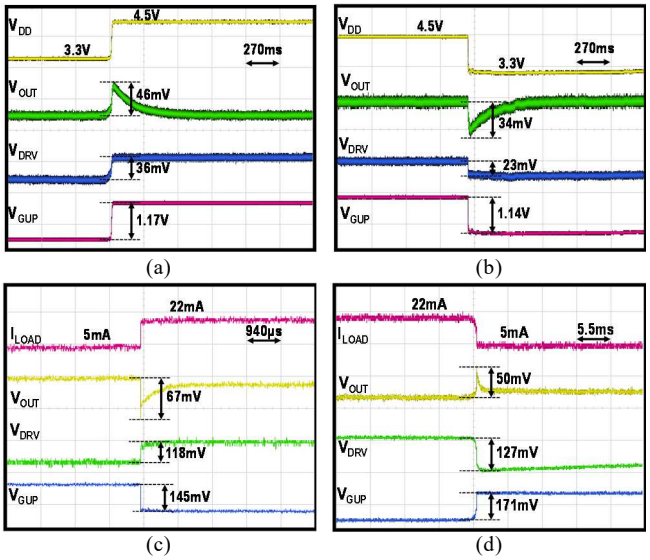
IV. Experimental Results

The proposed LDO was fabricated in a TSMC 0.18µm process with a chip area of $0.128mm^2$ as shown in Fig. 5. No off-chip capacitor is required for a stable operation in the proposed design. The measured quiescent current in Fig. 6(a) is proportional to the load current. The output voltage as a function of the load current exhibits a stable load regulation of 0.2mV/mA across a wide output range from 0.01mA to 10mA, and the output voltage shifts 50mV when the load current is 50mA. The measured line regulation is 0.86mV/V with 10mA load current. The maximum output current is limited to 700mA under output short condition shown in Fig. 7. The measured line and load step responses are shown in Fig. 8. The overshoot and undershoot voltages were 46mV and 34mV under 1.2V-step-up and 1.2V-step-down conditions, respectively. The measured output voltage varied within 70mV with a recovery time less than 2ms when the load current toggled between 5mA and 22mA.



(a) (b)

Fig. 7. Current limiting function under (a) output short to ground and (b) output released from short.



(a) (b) (c) (d)

Fig. 8. Measured waveforms of (a) input step-up, (b) input step-down, (c) load current step-up and (d) load current step-down.

Since the LDO's quiescent current is designed to be proportional to the load current, the proposed design reaches a low quiescent current without much compromising its maximum available output current. Fig. 9 shows the comparison between the state-of-the-art low power LDOs in terms of the minimum quiescent current and the maximum available load current. The detailed performance comparison is listed in Table I and a lowest quiescent of 11nA is achieved in this design owing to the current feedback architecture. As design predicted, the output impedance of the LDO is attenuated by the proposed feedback scheme so a decent line and load regulations were achieved. The primary limitation of the proposed structure lies in the dropout voltage of around 1.6 V which is required by the cascode current mirrors for self-biasing, so the proposed design may be confined to applications with sufficient headroom margin.

V. Conclusion

This paper presented a LDO structure which regulates its output voltage through a series-series positive feedback loop with 11nA quiescent current and a maximum available output current of around 50mA. Competitive line and load regulations are achieved by the proposed regulation scheme without load capacitor required for stability. Current limiting and input reference current cancellation functions are also included in the proposed LDO.

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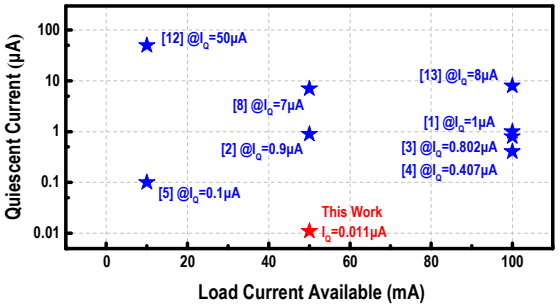

Fig. 9. Comparison of quiescent current and available current in LDOs.

TABLE I. Performance Comparision

Publication	[3] ICIEA	[5] TCAS-I	[6] ISCAS	[8] ISCAS	This work
Active Area (mm^2)	NA	0.0048	0.001473	NA	0.128
Technology (µm)	0.4	0.065	0.18	0.18	0.18
V_{IN} (V)	3.4-5.5	1	1.8	1.84-3.6	3.4-5.6
V_{OUT} (V)	3.3	0.8	1.044[a]	1.8	1.8[c]
I_{LOAD_MAX} (mA)	100	10	NA[b]	50	50
I_Q (µA)	0.802	0.1	0.00188	7	0.011
C_{LOAD} (nF)	NA	0.01	NA	0.1	0
Line Reg. (mV/V)	1.67	NA	1.7	0.159	0.86
Load Reg. (mV/mA)	0.045	1.58	40.2	0.017	0.2
Result Type	Simulated	Measured	Measured	Simulated	Measured

[a]. Average value [b]. Mentioned about milliampere [c]. Typical value and adjustable

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