

# Design of an Adaptively Biased Low-Dropout Regulator With a Current Reusing Current-Mode OTA Using an Intuitive Analysis Method

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**Abstract**—An adaptively biased low-dropout regulator (AB-LDO) with current mirror buffer has been proposed in previous literatures, which only solves a few of the specific problems of AB-LDO without additional synthetical analysis of the various performances. Based on the analysis, it is found that enhancing the current efficiency of operational transconductance amplifier (OTA) is a key factor to improve the performances of AB-LDO. A current reusing current-mode OTA (CRCM-OTA) with high current efficiency is proposed to apply to AB-LDO. Compared with the traditional AB-LDO, it can achieve an obvious improvement of AB-LDO performances including the current efficiency of AB-LDO, loop gain, and loop bandwidth without increasing the area and power consumption. This article also adopts an intuitive method different from the previous works to analyze the whole loop. The AB-LDO using an advanced CRCM-OTA was fabricated in SMIC 0.18  $\mu\text{m}$  CMOS process, which has a transient undershoot of 26.25 mV with an output capacitor of 1  $\mu\text{F}$  for a load step of 0–50 mA with edge time of 10 ns and realizes a performance figure of merit (FoM) value of 13.65 ps.

**Index Terms**—Adaptively biased, current efficiency, current reusing, current-mode operational transconductance amplifier (OTA), low-dropout regulator (LDO).

## NOMENCLATURE

AB-LDO	Adaptively biased low-dropout regulator.
ABL	Adaptive bias loop.
CM-OTA	Current-mode OTA.
CRCM-OTA	Current reusing current-mode OTA.
DM-OTA	Differential-mode OTA.
FoM	Figure of merit.
$G_{m,x}(g_{m,x})$	Effective transconductance of transistor x.
GBW	Gain-bandwidth of the corresponding OTA.
HM-OTA	Hybrid-mode OTA.

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$I_{ab}$	Adaptive current obtained from the adaptive bias scheme.
$I_f$	Fixed bias current.
$I_o$	Load current.
$I_{tot}$	Total current consumed by the corresponding OTA.
$I_t$	Tail current supplied to OTA composed of $I_f$ and $I_{ab}$ .
$K, A, M, N, \alpha, \beta, \gamma$	Size ratios between transistors marked in Fig. 4.
LDO	Low dropout regulator.
MFL	Main feedback loop.
OTA	Operational transconductance amplifier.
PSRR	Power supply rejection ratio.
$r_{o,x}$	Source-drain resistance of transistor x.
UGF	Loop gain-bandwidth of the corresponding AB-LDO.
$V_a$	Voltage at $V_a$ marked in Fig. 4.
$V_{thp}$	Threshold voltage of PMOS transistors.

## I. INTRODUCTION

WITH the increasing popularity of portable devices [1]–[4], low-dropout regulator (LDO) with high stability, fast dynamic response, and high efficiency has become a research hotspot [5]. In recent years, the adaptively biased LDO (AB-LDO) has attracted more and more attention due to its own distinctive advantages [6]. The general structure of a traditional AB-LDO with a current mirror buffer [7] is shown in Fig. 1 [8]. The merits of AB-LDO mainly include two aspects—first, the adaptive bias scheme provides a relatively large tail current for the operational transconductance amplifier (OTA) at high load condition [9], [10], which enhances the AB-LDO loop bandwidth and charging slew rate, leading to a diminution of overshoot; second, the presence of the current mirror buffer pushes the nondominant pole caused by the large parasitic capacitance at the gate of power transistor to high frequency, ensuring the AB-LDO stability at high load condition. However, there are still the following three major problems in the AB-LDO: 1) the loop bandwidth is limited and the discharging at the gate of power transistor is fairly slow due to the low current supplied to OTA at low load condition, which results in a large undershoot; 2) the loop gain at high load condition is limited by the ratio between power transistor and diode-connected

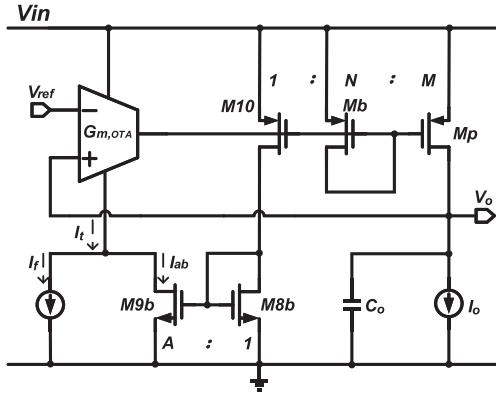


Fig. 1. Structure of AB-LDO with a current mirror buffer.

current mirror buffer and the reduction of power transistor's source-drain resistance, further affecting the load regulation and line regulation; and 3) the current efficiency of AB-LDO is severely degraded because the proportion of quiescent current consumption of OTA in total current consumption increases at low load condition. Obviously, implementing an OTA with improved transconductance is an effective means to solve the above-mentioned problems, especially under the premise of low current consumption and no excess area. This essentially requires a high current efficiency ( $G_{m,OTA}/I_{tot}$ ) OTA, which can increase AB-LDO current efficiency and loop bandwidth at low load condition and loop gain at high load condition to achieve the improvement of AB-LDO performances.

To solve the aforementioned issues, the following techniques are presented. Multiple small-gain stages are proposed in [11] and [12] to enhance the loop gain, which is realized at the cost of more power consumption and area. However, more poles are introduced into the circuit and the stability analysis gets more complicated. Besides, [8] advances a hybrid-mode OTA (HM-OTA) to reduce the undershoot of AB-LDO. It not only settles the matter of low gain and slow discharging slew rate of the conventional current-mode OTA (CM-OTA) [13], but also avoids the stability issue of the traditional differential-mode OTA (DM-OTA) [13] which combines the merits of CM-OTA and DM-OTA. However, with the enhanced loop gain and discharging slew rate, the stability issue of HM-OTA becomes more serious. So far, most of the previous literatures only address a few of specific issues of AB-LDO [14], which does not provide an analysis of the synthetical improvements directing at various performances, especially the analysis about the significance of the current efficiency of OTA to the AB-LDO performance. Moreover, the analysis of a dual-loop AB-LDO in prior works is deficient. In [9] and [15], main feedback loop (MFL) and adaptive bias loop (ABL) are analyzed separately, which is apparently incomplete. Hence, [6], [8], [16], and [17] consider the impacts between MFL and ABL by keeping one loop closed to seek the effect on the other. However, this method just focuses on the impacts between the amplitude-frequency responses of MFL and ABL which does not include an overall stability analysis of two loops working as an integrated scheme. Also, the calculation and analysis about this method are complex, especially for AB-LDO containing multiple loops.

Consequently, this article gives a sufficient analysis about the impact of the current efficiency of OTA on the performances of AB-LDO and proposes a current reusing current-mode OTA (CRCM-OTA) with high current efficiency for AB-LDO, achieving the improvement of AB-LDO performances without increasing more area and power consumption. In addition, for an AB-LDO containing dual loop, a compositive method for the analysis of circuit stability is also presented in this article, which can not only obtain the amplitude-frequency response as the previous works, but also further get the phase-frequency responses when two loops act simultaneously. Also, the influence of each loop on the overall circuit can be seen more intuitively from the amplitude-frequency response. Furthermore, it has potential advantages in the analysis of AB-LDO containing multiple loops.

The content of this article is arranged as follows. The analysis of the impact of OTAs' current efficiency on the performances of AB-LDO is shown in Section II and the proposed CRCM-OTA with high current efficiency for AB-LDO is discussed in Section III. In Section IV, the detailed analysis of complete AB-LDO using the CRCM-OTA is given and the corresponding test results are displayed in Section V. The conclusion is presented in Section VI.

## II. INFLUENCE OF OTAs' CURRENT EFFICIENCY ON THE AB-LDO

In fact, the current efficiency ( $G_{m,OTA}/I_{tot}$ ) of OTA has a direct impact on the tradeoff among the performances of AB-LDO, such as the current efficiency, loop bandwidth, and loop gain.

In AB-LDO, the current efficiency can be expressed as

$$I_{\text{eff}} = \frac{I_o}{I_o + I_{\text{tot}} + \frac{I_o}{M}} \quad (1)$$

where  $I_{\text{tot}}$  is determined by the fixed bias current  $I_f$  and the adaptive current  $I_{ab} = A \cdot I_o/M$  obtained from the adaptive bias scheme. It can be seen that the current efficiency of AB-LDO is mainly determined by  $I_f$  at low load condition and by the adaptive current  $I_{ab}$  at high load condition. Hence, in order to improve the current efficiency of AB-LDO, it is necessary to reduce the current consumed by the OTA itself, especially at low load condition. However, the reduction of OTA quiescent current affects its transconductance, further resulting in a decrease of loop gain under high load condition and a degradation of loop bandwidth under low load condition. The specific analysis is given as follows.

Under high load condition, the loop gain of AB-LDO is shown as [8]

$$A_{v,\text{loop}} = G_{m,OTA} \cdot g_{m,p} \cdot \left( r_{o,OTA} // \frac{1}{g_{m,b}} \right) \cdot r_o \approx \frac{G_{m,OTA} \cdot M \cdot r_o}{N} \quad (2)$$

where  $M/N$  is the ratio of  $g_{m,p}$  to  $g_{m,b}$ . As the load current increases, the reduction of power transistor's source-drain resistance and the restriction caused by the ratio  $M/N$  is evident which causes a lower loop gain of AB-LDO, affecting the load regulation and line regulation. The key to solving it is

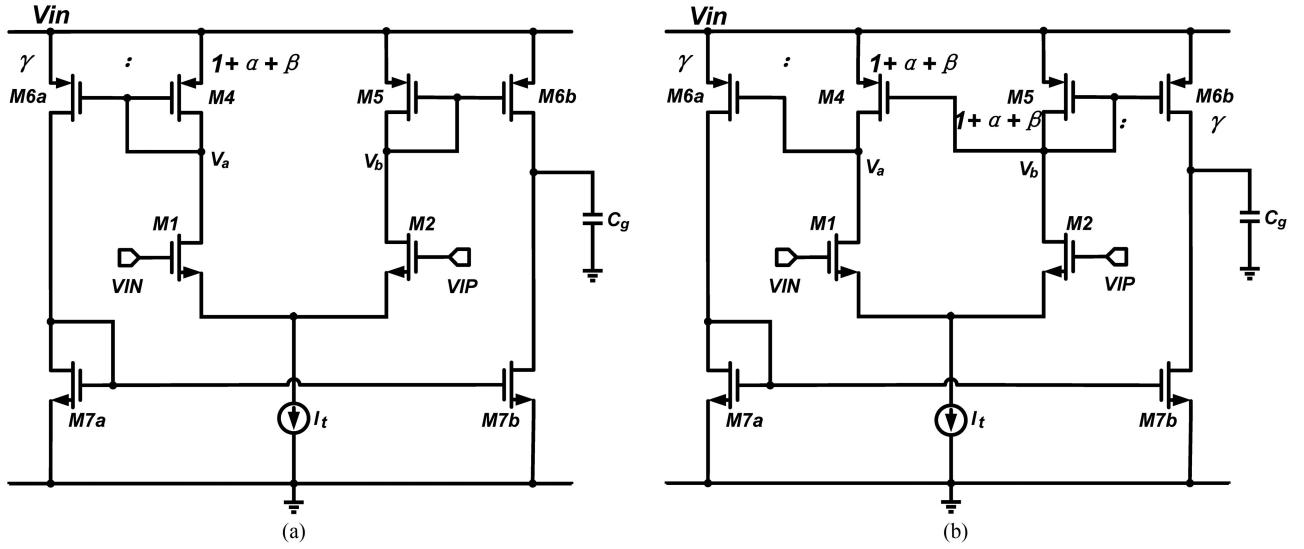


Fig. 2. Circuits of (a) CM-OTA and (b) DM-OTA.

to improve the transconductance of OTA. Combined with the above-mentioned analysis of the current efficiency of AB-LDO, it can be found that the OTA with higher current efficiency can enhance loop gain in the case of high load current and the current efficiency of AB-LDO simultaneously.

Under low load condition, the loop bandwidth of AB-LDO is given as [8]

$$\omega_{UGF,loop} = - \frac{G_{m,OTA} \cdot g_{m,p} \cdot \left( r_{o,OTA} // \frac{1}{g_{m,b}} \right)}{C_o}$$

$$\approx - \frac{G_{m,OTA} \cdot g_{m,p} \cdot r_{o,OTA}}{C_o}. \quad (3)$$

In the case of low load current, the decreased transconductance  $g_{m,p}$  of the power transistor further reduces the loop bandwidth, leading to a large undershoot. Therefore, improving the effective transconductance of OTA is feasible to deal with those issues. Similarly, considering the current efficiency of AB-LDO, only the OTA with higher current efficiency can improve the loop bandwidth and reduce the undershoot while increasing the current efficiency of AB-LDO. To sum up, increasing the current efficiency of OTA is a critical factor in improving the current efficiency of AB-LDO, loop gain, and loop bandwidth.

According to the analysis above, the most commonly used OTAs including the CM-OTA and the DM-OTA are displayed in Fig. 2. For fair comparison, all OTAs are set to have the same area and the same total current consumption  $I_{tot} = I_t \cdot (1 + K + \gamma)/(1 + K)$ .

The effective transconductances of CM-OTA and DM-OTA are  $G_{m,CM} = g_{m,1} \cdot \gamma/(1 + K)$  and  $G_{m,DM} = g_{m,1} \cdot (r_{o,1} // r_{o,4}) \cdot g_{m,6a}$ , respectively, where  $(r_{o,1} // r_{o,4}) \cdot g_{m,6a}$  is related to the process. The transconductance of DM-OTA is much higher than that of CM-OTA due to the contribution of the high impedance introduced by  $V_a$ , demonstrating that the DM-OTA has higher current efficiency. Nevertheless, compared with the CM-OTA, the pole  $\omega_p = -1/((r_{o,1} // r_{o,4}) \cdot C_{gs,6a})$  generated at  $V_a$  by the high impedance causes an adverse impact

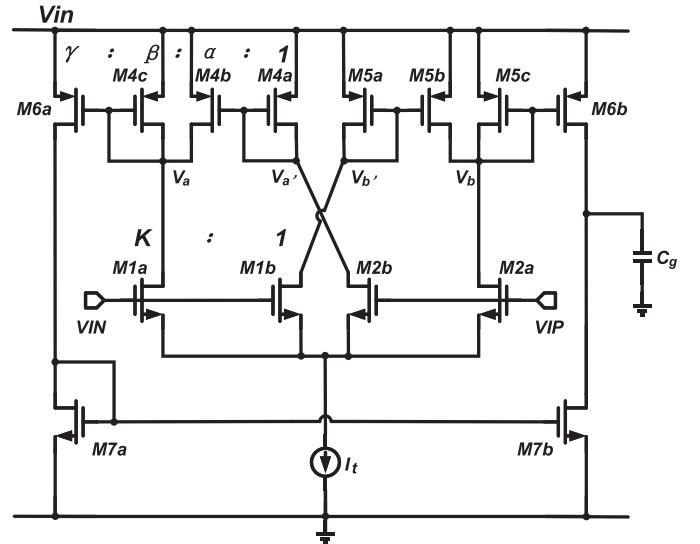


Fig. 3. Circuit of CRCM-OTA.

on the stability as the current efficiency of DM-OTA is improved. To get over this problem, this article proposes a CRCM-OTA for AB-LDO, which not only has high current efficiency but also does not have a stability problem on account of the absence of high impedance poles in all internal nodes. Section III gives the detailed analysis of the CRCM-OTA.

### III. PROPOSED CRCM-OTA ANALYSIS

This section proposes a CRCM-OTA for AB-LDO, which is modified by CM-OTA. The CRCM-OTA is presented in Fig. 3. The input transistors M1 and M2 are split into M1a - M1b and M2a - M2b with a ratio of K : 1, respectively, and have the crossover connections with current mirrors M4a - M4b and M5a - M5b to reuse the current flowing through M1b and M2b [18]. The ratio of current mirrors M4a - M4b and M5a - M5b is 1 :  $\alpha$ . M4b and M5b further amplify the current through M4a and M5a which meanwhile form the current shunt structures

TABLE I  
PERFORMANCE COMPARISON OF THREE OTAs

Performances	CM-OTA	DM-OTA	CRCM-OTA
$G_m$ (Effective transconductance)	$\frac{\gamma}{1+K} g_{m,1}$	$g_{m,6a} \cdot (r_{o,1}/r_{o,4}) \cdot g_{m,1}$	$\frac{\alpha+K}{1+K} \frac{\gamma}{\beta} g_{m,1}$
$SR+$ (Charging slew rate)	$\frac{\gamma}{1+K} \frac{I_t}{C_g}$	$\frac{\gamma}{1+K} \frac{I_t}{C_g}$	$\frac{K}{\beta} \frac{\gamma}{1+K} \frac{I_t}{C_g}$
$SR-$ (Discharging slew rate)	$\frac{\gamma}{1+K} \frac{I_t}{C_g}$	$\frac{g_{m,6a} \cdot (V_{in} - V_a -  V_{thp} )}{2 \cdot C_g}$	$\frac{K}{\beta} \frac{\gamma}{1+K} \frac{I_t}{C_g}$
$\eta$ (Current efficiency)	$\frac{\gamma}{1+K+\gamma} \frac{g_{m,1}}{I_t}$	$\frac{g_{m,6a} \cdot (r_{o,1}/r_{o,4}) \cdot (1+K)}{1+K+\gamma} \frac{g_{m,1}}{I_t}$	$\frac{\gamma \cdot (\alpha+K)}{\beta \cdot (1+K+\gamma)} \frac{g_{m,1}}{I_t}$
$\omega_{p2}$ (The non-dominant pole)	$-\frac{1+K}{1+K+\gamma} \frac{g_i}{C_i}$	$-\frac{1}{(r_{o,1}/r_{o,4}) \cdot \gamma \cdot C_i}$	$-\frac{\beta}{\beta+\gamma} \frac{g_i}{C_i}$
$FOM_{CE-STB}$ (Figure of merit)	$\frac{\gamma \cdot (1+K)}{(1+K+\gamma)^2} \frac{g_{m,1} \cdot g_i}{C_i \cdot I_t}$	$\frac{1+K}{1+K+\gamma} \frac{g_{m,1} \cdot g_i}{C_i \cdot I_t}$	$\frac{\gamma \cdot (\alpha+K)}{(1+K+\gamma) \cdot (\beta+\gamma)} \frac{g_{m,1} \cdot g_i}{C_i \cdot I_t}$
	$= \frac{40}{169} \frac{g_{m,1} \cdot g_i}{C_i \cdot I_t}$	$= \frac{65}{169} \frac{g_{m,1} \cdot g_i}{C_i \cdot I_t}$	$\approx \frac{81}{169} \frac{g_{m,1} \cdot g_i}{C_i \cdot I_t}$

with  $M4c$  and  $M5c$ , respectively [19], where the ratio of  $M4b$  -  $M4c$  and  $M5b$  -  $M5c$  is  $\alpha : \beta$ . According to the current relation, it is obvious that  $\alpha + \beta = K$ . After the current shunt is composed, the current mirrors  $M4c$  -  $M6a$  and  $M5c$  -  $M6b$  are constituted again with a ratio of  $\beta : \gamma$  separately.  $\alpha$ ,  $\beta$ ,  $\gamma$ , and  $K \geq 1$  and the relation and range of their values are given in the following analysis.

As mentioned above, CRCM-OTA is set to have the same area and tail current as the previous two OTAs; hence, it does not consume extra area and power. Its effective transconductance is calculated as

$$G_{m,CRCM} = \frac{\alpha + K}{1 + K} \frac{\gamma}{\beta} g_{m,1} \quad (4)$$

where  $g_{m,1}$  is the total effective transconductance of input transistors. The quiescent current consumed by the three OTAs is the same as  $I_{tot} = I_t \cdot (1 + K + \gamma)/(1 + K)$ . Therefore, the current efficiency  $\eta$  of CRCM-OTA is given by

$$\eta_{CRCM} = \frac{G_m}{I_{tot}} = \frac{\gamma(\alpha + K)}{\beta(1 + K + \gamma)} \frac{g_{m,1}}{I_t}. \quad (5)$$

In consideration of stability, the nondominant pole  $\omega_{p2}$  needs to meet the requirement of more than twice the GBW, which should be as large as possible. In CRCM-OTA, there are poles introduced at both the nodes of  $V_a$  and  $V_{a'}$ . For the target of a higher transconductance, the ratio of  $\gamma : \beta$  is larger in general, resulting in a high capacitance and a high impedance at  $V_a$ , causing the associated pole to become  $\omega_{p2}$ . Assume that  $C_i$  is the unit capacitance and  $g_i$  is the unit transconductance of all PMOS. In consequence, when  $K^2 < 4\gamma$  is satisfied, which is concluded from the relationship between the poles at  $V_a$  and  $V_{a'}$ , it can be confirmed that  $\omega_{p2}$  expressed as

$$\omega_{p2} = -\frac{1}{\frac{1}{g_{m,4c}}(\beta + \gamma)C_i} = -\frac{\beta g_i}{(\beta + \gamma)C_i} \quad (6)$$

is introduced at  $V_a$ .

For the slewing operation, assuming a large positive step signal is applied to the left port,  $M1a$  and  $M1b$  are turned ON while  $M2a$  and  $M2b$  are turned OFF. Then, the voltages at  $V_{a'}$

and  $V_b$  increase, causing  $M4a$ ,  $M4b$ ,  $M5c$ , and  $M6b$  to also turn OFF and  $M5b$  to go into the deep triode region. Hence, even though  $M1b$  is turned ON, the current flowing through it cannot ultimately reach the output. Finally, the current  $K \cdot I_t/(1 + K)$  is through  $M1a$  -  $M4c$  -  $M6a$  -  $M7a$  -  $M7b$  to drive the capacitor  $C_g$ .  $SR-$  can be expressed as

$$SR- = \frac{\gamma}{\beta} \frac{K}{1 + K} \frac{I_t}{C_g}. \quad (7)$$

Since CRCM-OTA is symmetrical,  $SR+$  can realize the same as  $SR-$ .

The performances of the three OTAs are compared and listed in Table I. A figure of merit  $FoM_{CE-STB} = \eta \cdot \omega_{p2}$  is adopted to characterize the combination of the current efficiency and stability of OTA for intuitive comparison. The higher the  $FoM_{CE-STB}$  value, the higher the current efficiency of the OTA while maintaining the same stability, which also indicates that the OTA obtains a better value in the tradeoff among transconductance, current consumption, and stability. On the basis of fully considering the tradeoff of the ratio  $\gamma : \beta$  between  $\omega_{p2}$  and  $SR+/-$ , as well as the restrictive relationship between  $\gamma$  and  $K$ , the relationship of  $\alpha$ ,  $\beta$ ,  $\gamma$ , and  $K$  can be chosen to be 3:1:8:4 according to the foregoing analysis. Table I illustrates that when the foregoing relationship of  $\alpha$ ,  $\beta$ ,  $\gamma$ , and  $K$  is appropriate, the CRCM-OTA with high current efficiency is better than that of the other two under the same area and power consumption.

#### IV. COMPLETE AB-LDO WITH CRCM-OTA ANALYSIS

The complete schematic of AB-LDO with CRCM-OTA is shown as Fig. 4. The schematic mainly includes two loops—the main feedback loop (MFL) and the adaptive bias loop (ABL). The MFL with negative feedback consists of CRCM-OTA -  $Mb$  -  $Mp$ . The ABL containing positive feedback has CRCM-OTA -  $M9b$  -  $M8b$  -  $M10$ . This analysis part proposes a comprehensive method different from previous works, which can not only analyze the two separate loops and the complete circuit intuitively in terms of amplitude-frequency response, but also acquire the corresponding phase-frequency response.

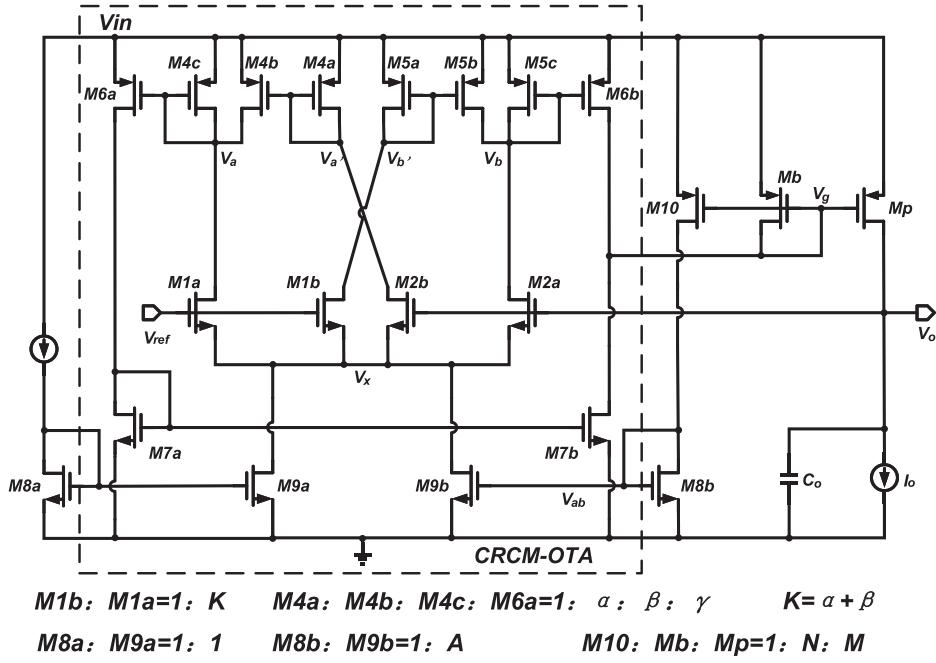


Fig. 4. Complete AB-LDO with the proposed CRCM-OTA.

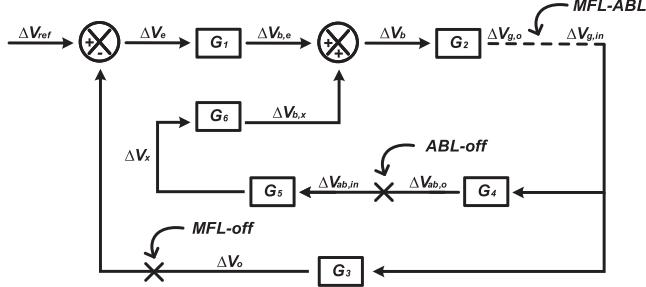


Fig. 5. Subsignal structure diagram containing MFL and ABL.

The signal structure diagram of the overall circuit is adopted in Fig. 5. In order to study the complete circuit under the combined action of MFL and ABL, when both loops are closed, stability (stb) analysis is carried out at the common node (MFL-ABL) of the two loops and the impedance at this node should be placed at  $\Delta V_{g,o}$  as the load. When each loop is broken at MFL-OFF and ABL-OFF, respectively, the other loop can also be analyzed separately at the MFL-ABL node without considering the disconnected loop. In this method, there is no need to calculate the case of one open loop and the other closed loop as in [6], [8], [16], and [17]; thus, it is convenient to comprehensively consider

$$A_{vMFL}(s) = -\frac{[(K + \alpha)g_{m,1b}g_i + K(1 + \alpha)g_{m,1b}C_i s]\gamma g_i(r_{o,6b}/r_{o,7b}/g_{m,b})r_o g_{m,p}(1 + m)}{2[g_i + (1 + \alpha)C_i s][\beta g_i + (\beta + \gamma)C_i s][1 + C_g s(r_{o,6b}/r_{o,7b}/g_{m,b})](1 + C_o r_o s)} \quad (8)$$

$$A_{vABL}(s) = \frac{[(K - \alpha)g_{m,1b}g_i + K(1 + \alpha)g_{m,1b}C_i s]\gamma g_i g_{m,9b}g_{m,10}(r_{o,6b}/r_{o,7b}/g_{m,b})(1 - m)}{[2(1 + K)g_{m,1b} + C_x s][g_i + (1 + \alpha)C_i s][(\alpha + \beta)g_i + (\beta + \gamma)C_i s][1 + C_g s(r_{o,6b}/r_{o,7b}/g_{m,b})](g_{m,8b} + C_{ab}s)} \quad (9)$$

two loops to obtain the complete stability analysis. The specific analysis is as follows.

#### A. Analysis of Complete Circuit Consisting of Two Loops

In Fig. 5, each broken node is annotated in the diagram. In the differential mode for the analysis of MFL, the open-loop transfer function of MFL is expressed as (8). On the contrary, in the common mode of the ABL analysis, its open-loop transfer function is presented as (9). The transfer functions (8) and (9), shown at the bottom of this page, for two separate loops can also be expressed as

$$A_{vMFL}(s) = G_1 G_2 G_3 \quad (10)$$

$$A_{vABL}(s) = G_2 G_4 G_5 G_6. \quad (11)$$

In (8) and (9), a mismatch factor  $m = g_{m,6a} \cdot g_{m,7b} / (g_{m,6b} \cdot g_{m,7a})$  is introduced in the calculation for analyzing MFL and ABL [8]. For the whole circuit, the transfer functions is represented as

$$\begin{aligned} A_{vMFL-ABL}(s) &= G_2(G_1 G_3 + G_4 G_5 G_6) \\ &= G_1 G_2 G_3 + G_2 G_4 G_5 G_6 \\ &= A_{vMFL}(s) + A_{vABL}(s). \end{aligned} \quad (12)$$

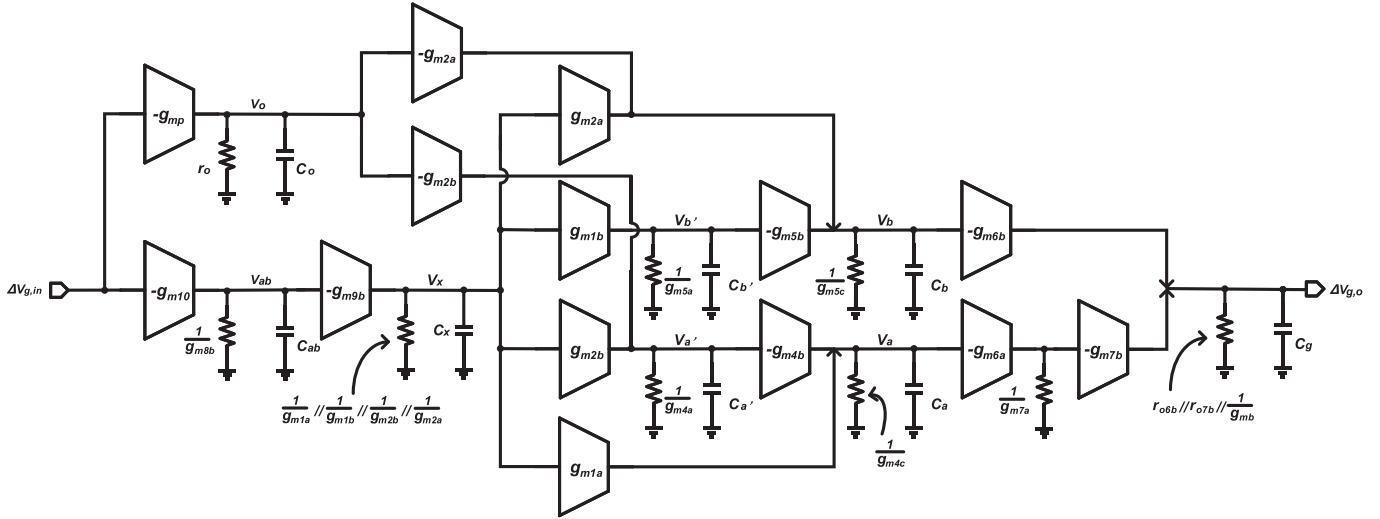


Fig. 6. Block diagram of the small signal of MFL-ABL.

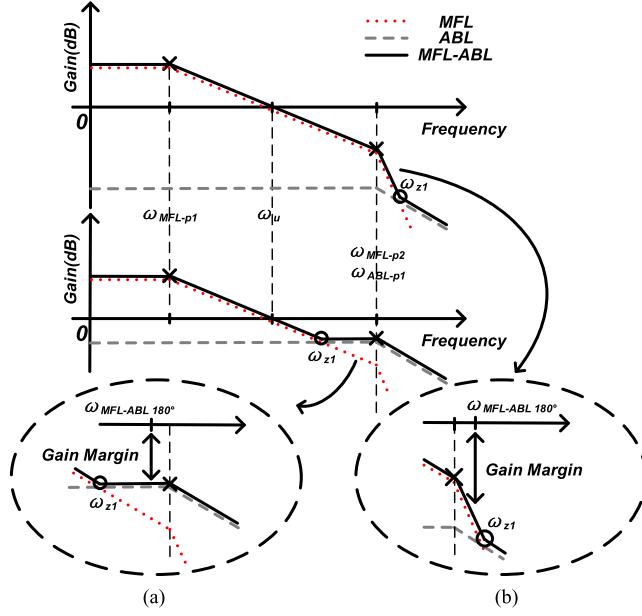


Fig. 7. Amplitude-frequency response under different ABL gain.

The detailed block diagram of the small signal of the whole circuit is presented in Fig. 6. The open-loop transfer function of the whole circuit is expressed as (13), shown at the bottom of this page, which satisfies  $A_{vMFL}(s) + A_{vABL}(s)$  approximately.

In Fig. 7, the relationship between the two separate loops and the whole loop is intuitively shown in a Bode diagram from

which can be seen that the gain of ABL has a great influence on the stability of the whole circuit. From the transfer functions in (8) and (9) of the two loops,  $\omega_{p2} = -1/[(r_{o,6b}/r_{o,7b})/\frac{1}{g_{m,b}}] \cdot C_g$  of MFL is the same as  $\omega_{p1}$  of ABL. When MFL and ABL are added in parallel, the zeros are generated, the position of which is determined by the dc gain and left-half-plane zeros of two loops,  $\omega_{p1} = -1/(r_o \cdot C_o)$  only existing in MFL, and  $\omega_p = -g_{m,8b}/C_{ab}$  and  $\omega_p = -2(1+K)g_{m,1b}/C_x$  only existing in ABL. When the ABL gain is relatively small, a zero is generated after  $\omega_{MFL-p2}$  as shown in Fig. 7(b). After calculation, it is found that the zero is on the left-half-plane and does not have a baneful influence on the phase due to its position at a relatively high frequency. As the gain of ABL increases, the zero gradually moves to a lower frequency. In Fig. 7(a), the zero locates before  $\omega_{MFL-p2}$  which is a right-half-plane zero by calculation and it affects both gain margin and phase margin.

On the basis of the above analysis,  $A_{vABL}$  is expected to be as low as possible. According to the dc gain of ABL

$$A_{vABL}(0) = \frac{A\beta\gamma(r_{o,6b}/r_{o,7b})/\frac{1}{g_{m,b}}g_{m,9}(1-m)}{2(1+K)(\alpha+\beta)} \quad (14)$$

the value of  $m$  is 1 and the loop gain of ABL is 0 in the ideal situation. However, it is just an ideal situation. To make the ABL gain lower, first, the mismatch factor  $m = g_{m,6a} \cdot g_{m,7b}/(g_{m,6b} \cdot g_{m,7a})$  is supposed to be closer to 1. In fact, besides the inevitable reasons for the mismatch in actual processing and production, the impact of current mirror buffer in the circuit should be considered.  $M7b$  and  $M7a$  directly constitute the current mirror

$$A_{vMFL-ABL}(s) = \frac{\gamma g_{m,1b} g_i (r_{o,6b}/r_{o,7b})/\frac{1}{g_{m,b}} [(K-\alpha)g_i + K(1+\alpha)C_i s] g_{m,9b} g_{m,10} (1+C_o r_o s) (1-m)}{(g_{m,8b} + C_{ab}s)[2(1+K)g_{m,1b} + C_x s][g_i + (1+\alpha)C_i s][\beta g_i + (\beta+\gamma)C_i s]} \\ - \frac{[(K+\alpha m)g_i + K(1+\alpha)C_i s] r_o g_{m,p} (g_{m,8b} + C_{ab}s)[2(1+K)g_{m,1b} + C_x s]}{[1+C_g s(r_{o,6b}/r_{o,7b})/\frac{1}{g_{m,b}}](1+C_o r_o s)} \quad (13)$$

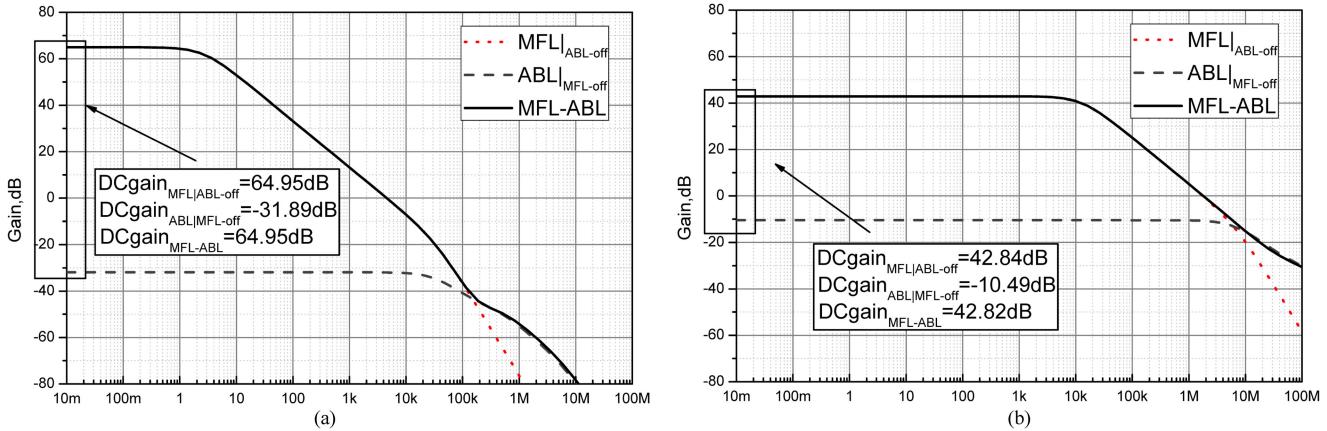


Fig. 8. Gain of MFL-ABL under (a)  $10 \mu\text{A}$  and (b)  $50 \text{ mA}$  load current conditions, respectively.

with the ratio of 1:1 so the value of  $g_{m,7b}/g_{m,7a}$  is generally approximately equal to 1. On the contrary,  $M6a$  and  $M6b$  do not form the current mirror structure. The difference between  $g_{m,6a}$  and  $g_{m,6b}$  is related to the current flowing through  $Mb$  and the difference is especially large when the load current is high, leading to the value of  $N$  not being chosen to be large. Besides, this also helps reduce quiescent current consumption. However, a low  $g_{m,b}$  will influence the stability of AB-LDO. Second, the value of  $A$  also cannot be excessively large for a low ABL gain, which is also conducive to the reduction of quiescent current consumption. Likewise, an extremely low  $A$  affects the loop bandwidth and slewing operation. The above-mentioned analysis of the value of  $N$  and  $A$  represents the tradeoff among the loop gain, stability, loop bandwidth, and quiescent current consumption.

The amplitude-frequency of the two individual loops and the whole loop at MFL-ABL are displayed in Fig. 8. It is obvious that the gain at MFL-ABL is dominated by MFL in the low frequencies. There is a zero at the frequency where MFL and ABL gains are equal and at frequencies higher than the zero, the gain starts to be controlled by ABL. Owing to that  $A_{vABL}$  is much lower at low load current, there is usually no case as shown in Fig. 7(b). Fig. 9 displays the simulated frequency response of AB-LDO with CRCM-OTA at low and high load condition respectively, proving the correct analysis of the variation of loop gain, loop bandwidth, and phase response at low and high load current.

In [8], the consideration of aiming at a single MFL or ABL is apparently improper. When two loops surround each other, the analysis about stability needs to pay attention to the zero caused by parallel connection which has an impact on the gain and phase, especially the phase. While in [6], [8], [16], and [17], the influence of one loop on the other one is studied by closing the loop, which focuses more on gain and lacks the consideration of phase. Moreover, this method is used to study the complete circuit stability by analyzing the influence between two loops. Once the ABL gain is not low enough, the analysis of MFL is different from that of the entire loop, even though ABL is closed. In this article, the method of comprehensively considering the

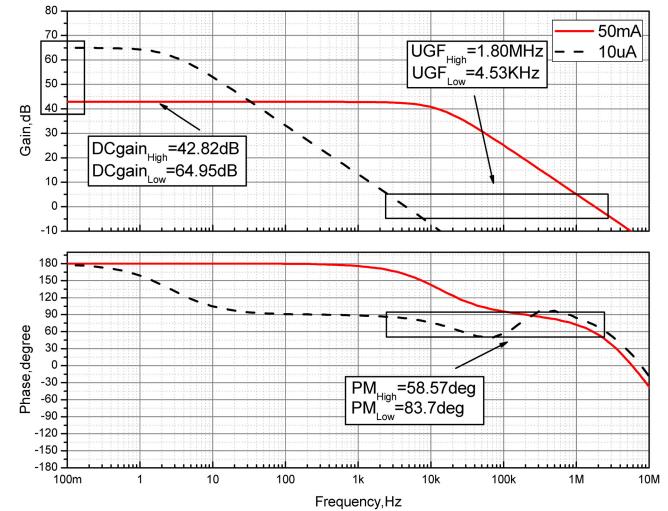


Fig. 9. Simulated frequency response of AB-LDO with CRCM-OTA at the load current of  $10 \mu\text{A}$  and  $50 \text{ mA}$ , respectively.

two loops from the common link of the two loops is adopted, which can not only obtain the respective gain and phase of the two separate loops but also intuitively understand the influence of the two loops on the overall loop in the amplitude-frequency and phase-frequency analysis. Compared with [6], [8], [16], and [17], this article provides a more convenient and simple method in both analysis and calculation.

### B. Stability Analysis

Based on the analysis of the overall loop, ABL gain is assumed to be as low as possible in Fig. 7(a). According to the transfer function, the poles  $\omega_p$  and the loop bandwidth  $\omega_u$  of LDO are given as

$$\omega_{p1} = -\frac{1}{r_o C_o} \quad (15)$$

$$\omega_{p2} = -\frac{1}{(r_{o,6b} // r_{o,7b} // \frac{1}{g_{m,b}}) C_g} \quad (16)$$

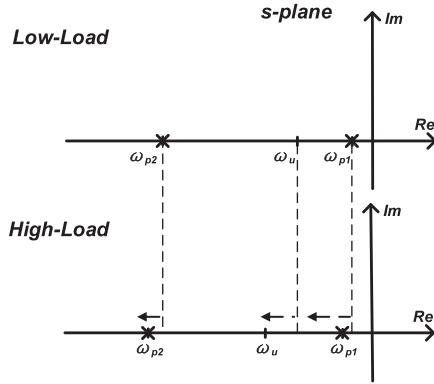


Fig. 10. Locations of poles and loop bandwidth of AB-LDO in s-domain.

$$\omega_{p3} = -\frac{1}{\frac{1}{g_{m,5b}}(\beta + \gamma)C_i} = -\frac{\beta g_i}{(\beta + \gamma)C_i} \quad (17)$$

$$\begin{aligned} \omega_u &= -\frac{G_{m,\text{CRCM}}g_{m,p}(r_{o,6b}/\parallel r_{o,7b}/\parallel \frac{1}{g_{m,b}})}{C_o} \\ &= -\frac{(K + \alpha)\gamma g_{m,1b}g_{m,p}(r_{o,6b}/\parallel r_{o,7b}/\parallel \frac{1}{g_{m,b}})(1 + m)}{2\beta C_o}. \end{aligned} \quad (18)$$

For  $\omega_{p2}$ , the pole is generally introduced by the node  $V_g$ , which can be expressed as  $-g_{m,b}/C_g$  in high-load-current condition and  $-1/(r_{o,6b}/\parallel r_{o,7b}) \cdot C_g$  in low-load-current condition separately.

In Fig. 10,  $\omega_u$ ,  $\omega_{p1}$ , and  $\omega_{p2}$  are displayed simultaneously in the s-domain. In high-load-current condition, with the load current  $I_o$  increasing,  $\omega_u$  and  $\omega_{p2}$  move on Im-axis in the same way and the relative distance between them is almost fixed, resulting in an approximately constant PM.  $-\omega_{p1}$  is also increased due to  $r_o$  decreasing with increasing  $I_o$ . However, in low-load-current condition,  $\omega_{p2}$  is stationary by the limitation of the fixed bias current. And  $-\omega_u$  decreases as  $I_o$  decreases, which makes the distance between  $\omega_u$  and  $\omega_{p2}$  increase gradually. This also leads to an increase in PM. The direction of movement of the poles and  $\omega_u$  with increasing  $I_o$  is also indicated by dotted arrows in Fig. 10. From the above, in order to ensure the stability of the circuit, PM in the case of high load current is more worthy of attention.

Therefore, PM in the case of high load current is discussed in detail. To ensure stability,  $\omega_{p2}$  is supposed to be at least greater than twice the value of  $\omega_u$ .  $M < g_{m,b} \cdot C_o \cdot N / (2 \cdot G_{m,\text{CRCM}} \cdot C_g)$  is obtained after calculation. This equation provides an upper limit for  $M$  value selection. At the same time, it also proves the practical meaning of the tradeoff again in the circuit because the selection of  $M$  value needs to be considered by combining the loop gain and stability.

### C. Analysis of the Impact of the Current Efficiency of CRCM-OTA on AB-LDO Performances

As mentioned ahead, for the current efficiency of CRCM-OTA, its improvement has a positive effect on the various

performances of the AB-LDO, which can make the tradeoff among the performances get an optimal value.

Under low load condition, the expression of current efficiency of CRCM-OTA is

$$\eta_{\text{Low}} = \frac{(1 + K)G_{m,\text{CRCM}}}{(1 + K + \gamma)I_f}. \quad (19)$$

The improvement of this value can not only increase the current efficiency of the AB-LDO on the premise of consuming a low-fixed-bias current  $I_f$  but also get a promotion of loop gain and loop bandwidth by improved transconductance of CRCM-OTA.

While under high load condition, the current efficiency of CRCM-OTA is expressed as

$$\eta_{\text{High}} = \frac{(1 + K)MG_{m,\text{CRCM}}}{(1 + K + \gamma)AI_o} \quad (20)$$

where the enhanced transconductance and the appropriate selection of  $M$  can effectively improve the loop gain and loop bandwidth of the AB-LDO while ensuring stability. Also, in the ABL loop gain impact analysis, it can be concluded that the appropriate value of  $A$  can be used to improve the loop bandwidth, slewing operation, and the current efficiency of AB-LDO at a lower power consumption of CRCM-OTA.

## V. SIMULATION AND EXPERIMENTAL RESULTS

Fig. 11 shows the simulated frequency response of the proposed AB-LDO with CRCM-OTA and traditional AB-LDOs with CM-OTA and DM-OTA under the same area and power consumption at different load currents, demonstrating that the loop gain of the AB-LDO with CRCM-OTA is relatively high on the premise of ensuring stability. It can also be seen that the phase-frequency response of AB-LDO with CM-OTA is greatly affected by the presence of the zero before  $\omega_{p2}$ , which is because its ABL gain is not low enough, further confirming the necessity of ABL gain being as low as possible.

In Fig. 12, the simulated line regulations of three AB-LDOs under different load current conditions demonstrate that AB-LDOs with CRCM-OTA and DM-OTA have better line regulations than the other one, where the best line regulations of the three AB-LDOs are 5, 2.5, and 27.5 mV/V corresponding to the AB-LDO with CRCM-OTA, DM-OTA, and CM-OTA at 10  $\mu A$  load current, respectively.

The simulated load regulations of different AB-LDOs with three OTAs are displayed in Fig. 13, representing that AB-LDOs with CRCM-OTA and DM-OTA are better than the other one in load regulation as well. The load regulation are 0.2, 0.02, and 0.86 mV/mA corresponding to the AB-LDO with CRCM-OTA, DM-OTA, and CM-OTA, respectively.

In Fig. 14, the simulated transient response of different AB-LDOs with three OTAs are compared for a load varying from 0 to 50 mA with an edge time of 10 ns. Although the AB-LDO with DM-OTA has the smallest dc output variation and undershoot, and the best line regulation and load regulation in Figs. 12 and 13 by reason of its high loop gain, there are plenty of ringings because of its poor stability.

The AB-LDO with CRCM-OTA was fabricated in SMIC 0.18  $\mu m$  CMOS process and the die photo is displayed in Fig. 15.

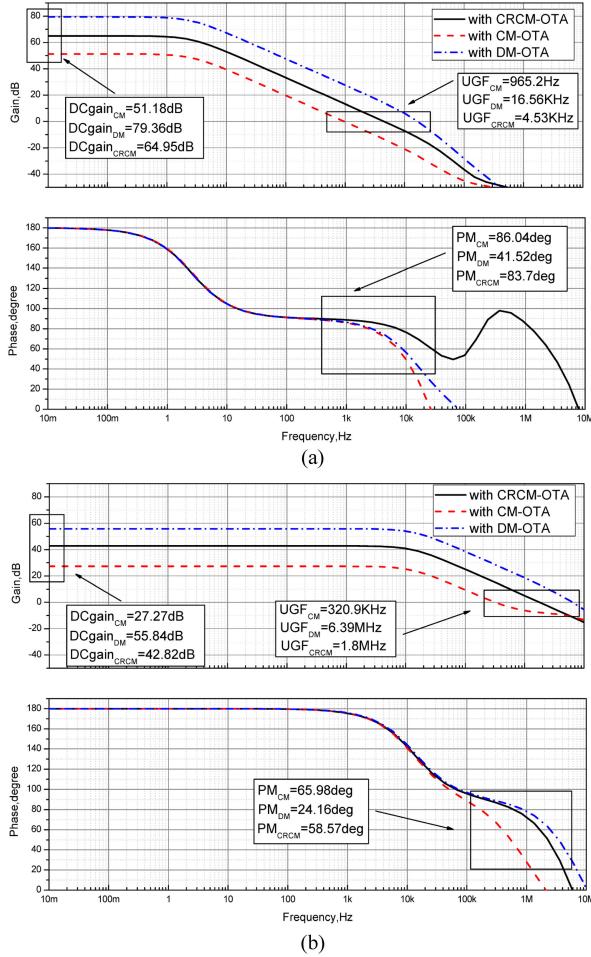


Fig. 11. Simulated frequency response of different AB-LDO with three OTAs at (a) 10  $\mu$ A and (b) 50 mA load, respectively.

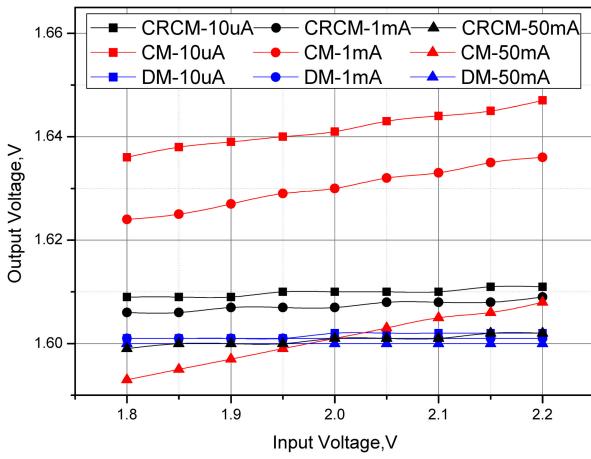


Fig. 12. Comparison of the simulated line regulation of different AB-LDOs with three OTAs at 10  $\mu$ A, 1 mA, and 50 mA, respectively.

The implemented AB-LDO achieves an output voltage of 1.6 V with an input voltage  $V_{in}$  of 1.8 V and can reach a maximum output current of 50 mA. Besides, a capacitor of 1  $\mu$ F is added at output  $V_o$  during the experiment.

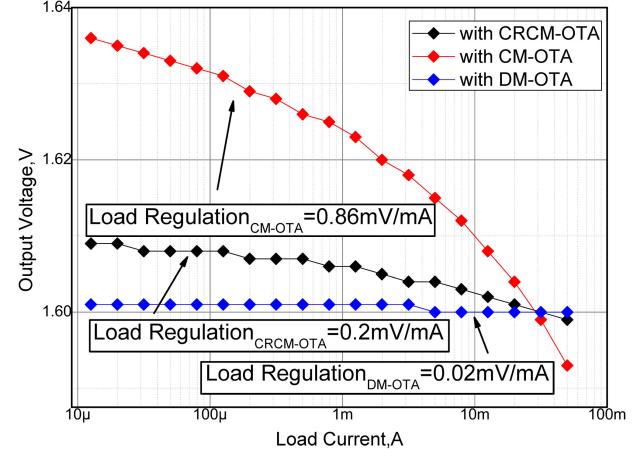


Fig. 13. Comparison of the simulated load regulation of different AB-LDOs with three OTAs at the load current varying from 10  $\mu$ A to 50 mA.

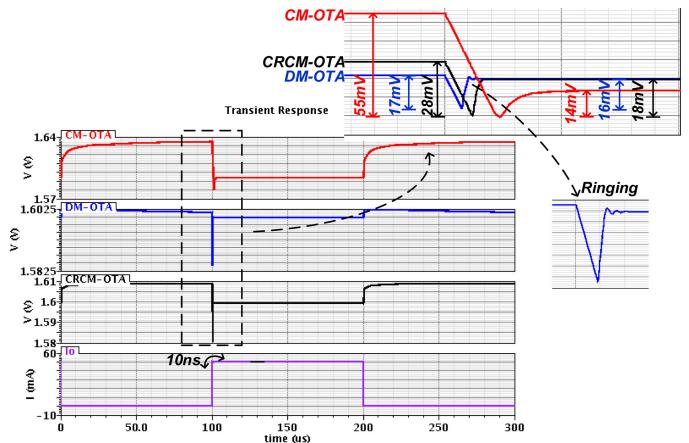


Fig. 14. Comparison of the simulated transient response of different AB-LDOs with three OTAs for a 10-ns step varying from 0 to 50 mA.

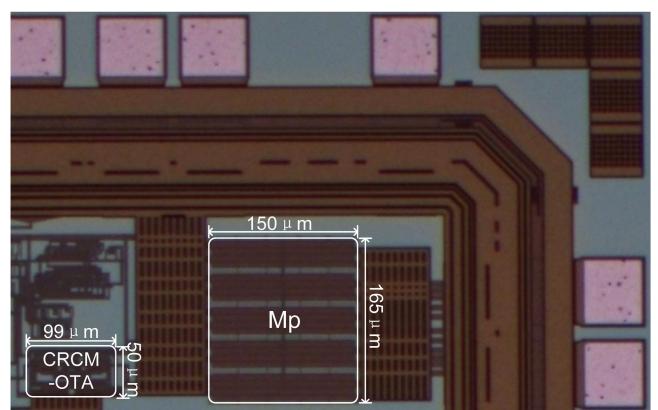


Fig. 15. Microphotograph of the proposed AB-LDO.

Fig. 16 displays the testing setups for line and load regulations, transient response, and PSRR measurements. Fig. 17 shows that the output voltage varies in a range of 0.43, 0.93, and 2.88 mV with input voltage changing from 1.8 to 2.2 V at 10  $\mu$ A, 1 mA, and 50 mA load current, respectively, demonstrating that the

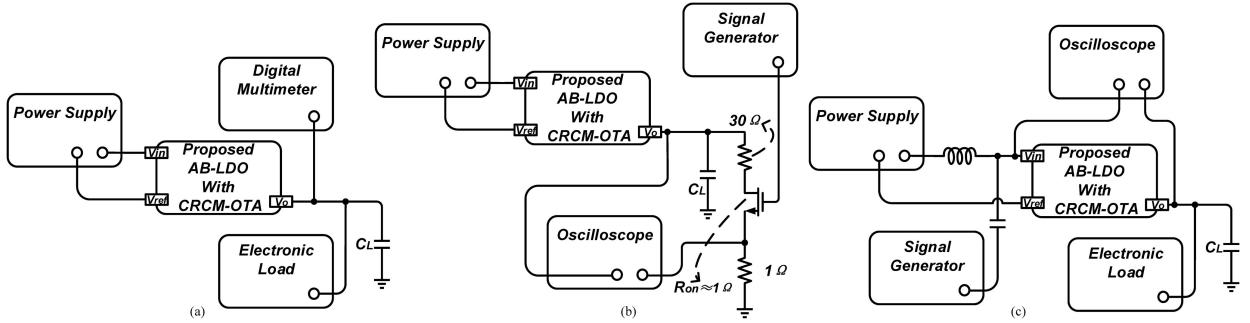


Fig. 16. Testing setups for (a) line and load regulations and (b) transient response, and (c) PSRR of proposed AB-LDO.

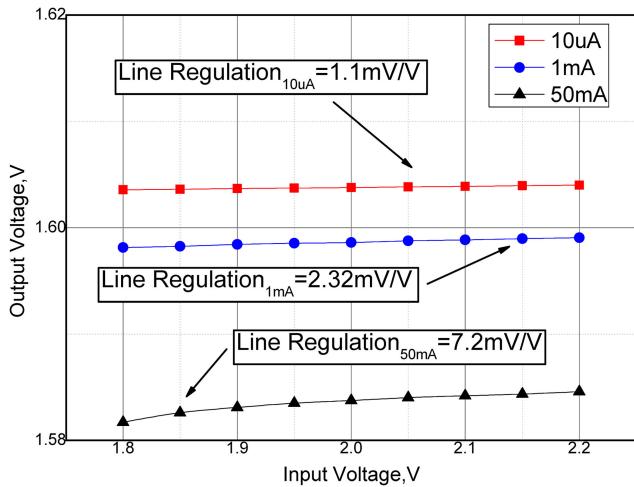


Fig. 17. Measured line regulation of the proposed AB-LDO.

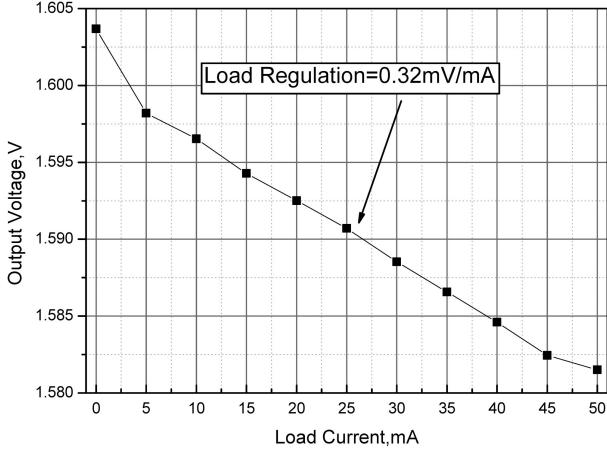


Fig. 18. Measured load regulation of the proposed AB-LDO.

measured line regulation of the proposed AB-LDO is 1.1, 2.32, and 7.2 mV/V corresponding to the 10- $\mu$ A, 1-mA, and 50-mA load conditions. This result confirms that with the increase of load current, the loop gain is seriously reduced, which affects the line regulation. Fig. 18 shows that the output voltage changes 21 mV in the observed range of load current from 10  $\mu$ A to 50 mA, demonstrating that the measured load regulation is 0.32 mV/mA.

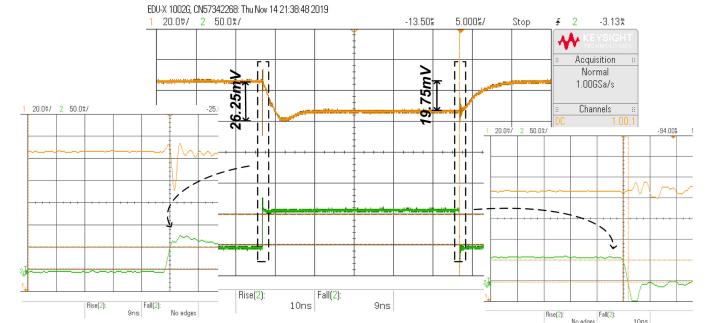


Fig. 19. Measured transient response of the proposed AB-LDO for a 10-ns step varying from 10  $\mu$ A to 50 mA.

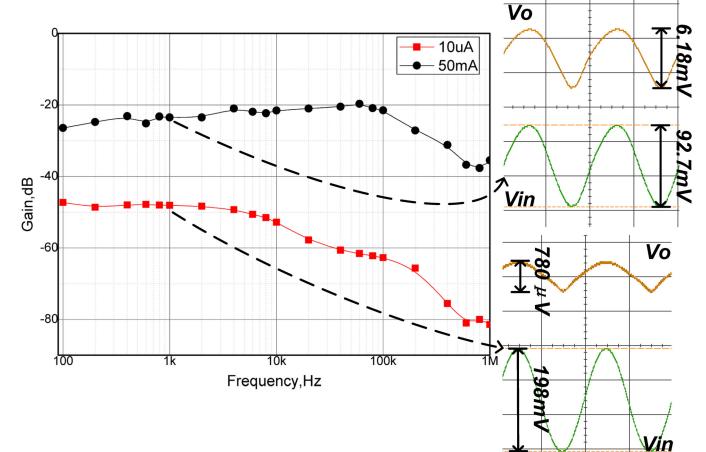


Fig. 20. Measured PSRR of the proposed AB-LDO.

In Fig. 19, the measured transient response of the proposed AB-LDO for a load varying from 10  $\mu$ A to 50 mA with edge time of 10 ns is displayed, which shows that the undershoot and dc output variation are 26.25 and 19.75 mV, respectively. Furthermore, the zoom-in figures of both step change conditions are in the same diagram, where there are some small fluctuations that may be caused by the inductance from bond wires and jumper wires [11].

As shown in Fig. 20, the performance PSRR at 10  $\mu$ A and 50 mA loads are measured using a sinusoidal signal superimposing onto  $V_{in}$  at the frequencies ranging from 100 Hz to 400 KHz. The  $V_{in}$  and  $V_o$  signals corresponding to PSRR measured at

**TABLE II**  
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED LDOs

Parameter	This work	[8]	[16]	[11]	[20]	[21]	[22]
Year	2019	2015	2015	2015	2010	2010	2007
Technology( $\mu\text{m}$ )	0.18	0.18	0.18	0.18	0.35	0.35	0.35
Chip Area( $\text{mm}^2$ )	0.0297	0.0285	0.03	0.024	0.2254	0.146	0.12
Minimum $V_{in}$ (V)	1.8	1.4	1.5	1.2	2	2	3
Nominal $V_o$ (V)	1.6	1.2	1.2	1.0	1.8	1.8	2.8
Dropout Voltage(mV)	200	200	300	200	200	200	200
Quiescent Current $I_Q$ ( $\mu\text{A}$ )	1.3-270	1.6-200	2.4-242	135.1	4	30-75	65
Maximum Load Current(mA)	50	50	100	100	100	200	50
Current Efficiency(%)	99.46	99.6	99.75	99.86	99.9	99.9	99.87
Output Capacitance $C_o$ ( $\mu\text{F}$ )	1	1	1	1	1	1	0.1
Load Regulation(mV/mA)	0.32	0.1	0.14	0.075	0.1	0.09	0.56
Line Regulation(mV/V)	1.1	5.5	12.3	22.7	17	6	23
PSRR(dB)	-35.5	<-30	<-38	<-25	<-32	-	-57
@(Hz)	@1M	@10M	@1M	@1M	@1M	-	@1K
Undershoot(mV)	26.25	29	62	25	55	45	90
Overshoot(mV)	0	0	0	0	0	50	90
Edge Time(ns)	10	10	10	10	50	100	1000
$K_1$	1	1	1	1	5	10	100
$K_2$	1	1	1	1	1.9	1.9	1.9
FoM(ps)	13.65	18.56	15	422.2	57.9	375	24631.6

1 KHz are given in Fig. 20, indicating that PSRR is  $-48.09$  dB under  $10 \mu\text{A}$  load condition and  $-23.52$  dB under  $50 \text{ mA}$  load condition.

Table II gives a performance comparison with previous works. A figure of merit

$$\text{FoM} = \frac{K_1 \cdot C_o \cdot \Delta V_{o,pp} \cdot I_{Q,\min}}{K_2 \cdot \Delta I_{o,max}^2} \quad (21)$$

is given in the last row of the table, where  $K_1$  is the ratio of the edge time in the measurement to the minimum edge time in all the measurements compared,  $K_2$  is the ratio of the technology used in the present work to the minimum technology in all the works, and the other symbols have the usual meanings [8], [16]. A smaller value of FoM that takes into account the performances of the technology, transient, and static current consumption means that the corresponding AB-LDO achieves a better tradeoff among these performances. Table II notes that this work has the smallest value of FoM, proving that the implemented AB-LDO with CRCM-OTA is excellent under the full consideration of various performances.

## VI. CONCLUSION

In this article, it is concluded that increasing the current efficiency of OTA is a critical factor in the improvement of the various performances of AB-LDO based on the analysis of the impact of the current efficiency of OTA on the performances of AB-LDO. Hence, the CRCM-OTA with high current efficiency is adopted and enables the proposed AB-LDO to improve loop gain, loop bandwidth, and other performances while maintaining stability in the case of small current consumption. In addition, this article adopts an advantageous method to analyze the complete circuit containing dual loop, which gives full consideration to amplitude-frequency and phase-frequency responses. The superiority of the proposed AB-LDO is reflected in the small undershoot, line regulation, and load regulation, which can be indicated by the minimum FoM value in the measurement

comparison as well, certifying that the tradeoff among the performances of AB-LDO gets an optimal value.

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