An Integrated Low Drop Out Regulator with Independent Self Biasing Start Up Circuit

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***Abstract*—The start-up behaviour of LDOs is critical for many ICs to function. Especially in multi supply voltage ICs, many constraints have to be fulfilled. So, additional circuitry is necessary for a reliable start-up. This paper proposes an LDO with additional circuitry which ensures a safe start-up without the need for other external voltages or signals. The proposed LDO allows the IC to rely on a stable supply voltage which can be used to control and coordinate the start-up of all other on chip circuitry.**

I. Introduction

Low drop out regulators (LDO) are a key element in today's integrated circuits (IC) [1][2][3]. They are widely used to provide different supply and auxiliary voltages with a wide range of various demands. Due to their low output ripple at constant loads, they are often used in radio frequency (RF) applications to decouple the analog RF circuits from other loads [1][2]. Moreover, they are used to generate auxiliary voltages with low output currents in HV CMOS circuits, due to their low effort to implement. Another advantage is the low demand of external components since they can operate properly with a single external capacitance which is not even necessary in some applications. Due to these features, LDOs are commonly used, although their efficiency suffers from high voltage conversion ratios [2].

While LDOs are widely discussed in various publications, the LDO start-up is rarely addressed. Especially, if the main supply voltage ($HVDD$) is high enough to cause damage to the connected circuitry, the start-up behaviour has to be carefully considered. The limiting constraint at start-up is that the only voltage available is $HVDD$ which is not even necessarily at a distinct stable level but rising from $0\,\mathrm{V}$ to the specified supply voltage with a possibly significant slope. As a result, no reliable voltages are available for the supply of other circuitry. Therefore, it is desirable to use an LDO which reliably starts operation without any input but the main supply voltage.

This paper proposes an integrated LDO which becomes active right after the main supply voltage is provided to the IC. The LDO generates a lower supply voltage $AVDD$ out of $HVDD$ without the need for any other supply voltage or start signal. It provides a reliable start-up for a rise time of the main supply voltage up to $70\,\mathrm{ms}$. The start-up circuitry is completely switched off after start-up and does not require quiescent current during regular operation of the LDO. The functionality of the proposed circuit is verified for temperatures between $-40\,^{\circ}\mathrm{C}$ and $140\,^{\circ}\mathrm{C}$ in corner simulations.

II. System Concept

The proposed LDO was integrated in an IGBT gate driver IC, whose power generation concepts is shown in fig. 1.The system has three supply voltages, $HVDD$, $AVDD$ and $DVDD$ which are all buffered by external capacitances. $HVDD$ is the main supply voltage at around $15\,\mathrm{V}$ and externally provided to the IC. $AVDD$ provides $5\,\mathrm{V}$ to the bandgap reference, which is directly connected and, thus, is already active during the start-up. Moreover, $AVDD$ supplies the second LDO and power switches on the IC. $DVDD$ supplies the digital part as well as various analog circuitry on the IC with $1.8\,\mathrm{V}$. The supply voltages are generated by the proposed start-up (SU) LDO which generates $AVDD$ and another LDO which, in combination with a DCDC converter, provides $DVDD$ to the IC. An LDO has been chosen to generate $AVDD$, because this supply is only responsible for a small amount of the used power and, therefore, additionally external components should be prevented. The second LDO is only active during start-up and generates the initial level of $DVDD$. Since a significant amount of current is drained from $DVDD$, an additional DCDC converter is implemented to efficiently convert $HVDD$ to $DVDD$ during normal operation of the IC. The reference voltage V_{ref} is generated out of $AVDD$ by the bandgap reference when the voltage rises and provides a reference of $1.19\,\mathrm{V}$. Simultaneously to V_{ref}, the bandgap provides a reference current to analog circuitry of the IC.

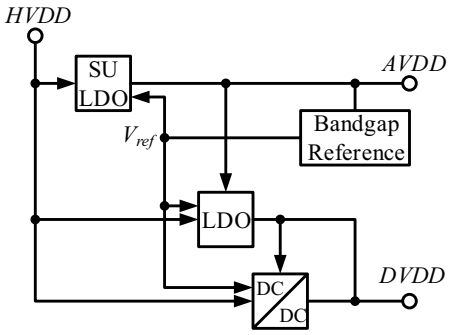

Fig. 1. Power management concept of the IC.

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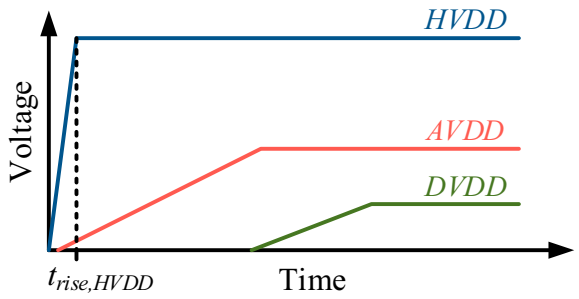


Fig. 2. Supply start-up sequence.

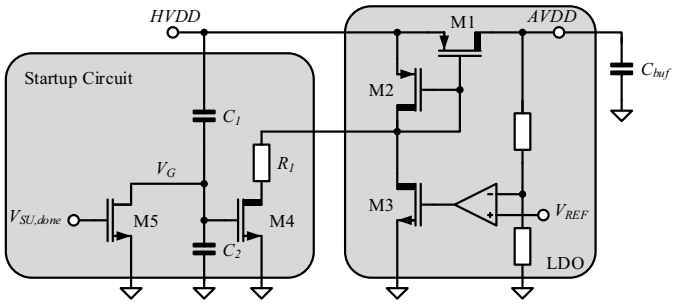


Fig. 3. Schematic of the start-up LDO.

Fig. 2 shows the sequence of the supply voltages during start-up of the IC. The start-up is initialized by externally providing $HVDD$ to the IC. Since the input capacitance has to be charged, $HVDD$ is not available instantaneously but shows a rise time of $t_{rise,HVDD}$. Depending on the voltage source and the input capacitance, the time $t_{rise,HVDD}$ can vary from a few µs up to tens of ms. At this point, no other external voltages or signals are available at the IC and the start-up LDO generates $AVDD$ out of $HVDD$. The circuit detects a sufficiently stable level of $AVDD$ and activates the second LDO which regulates $DVDD$. The DCDC converter is enabled after $DVDD$ reached its targeted voltage level.

Before $HVDD$ is applied to the IC, all nodes are considered to be discharged. At a specific, but unknown to the IC, time, $HVDD$ is provided to the IC. Since no other voltages are available, the start-up LDO has to start operation right after $HVDD$ is provided independently from $AVDD$. Additionally, it has to show a high robustness against the slope of $HVDD$. During its generation, $AVDD$ will ramp up to a defined level at which the bandgap reference as well as the control loop of the LDO will be functional. Consequently, the start-up circuitry is no longer necessary and is switched off to avoid quiescent current.

III. Implementation

Fig. 3 shows the implementation of the proposed start-up LDO. The highlighted part on the right of the schematic is a common implementation of an LDO [1]. The output voltage $AVDD$ is buffered by the external capacitance C_{buf}. M1 is the pass transistor of the LDO and interconnected as a current mirror to the minimal sized M2 with a width ratio of $1:20$ which is a trade-off between current efficiency and area on the IC. The current through M2 is controlled by M3 and the operational amplifier (OP) which compares a fraction of $AVDD$ to the bandgap voltage. The bandgap reference circuit itself is implemented in a common topology as in [4] and autonomously starts when $AVDD$ rises to a specific level without the need for a start-up signal.

On the left side, the additional circuitry for the start-up is shown. The general idea is, to introduce a current into M2 which is mirrored to M1 and charges C_{buf}. The current is controlled by the resistance R_1 and can be switched off after start-up. Therefore, the transistor M4 is capacitively switched on by C_1 and C_2 when $HVDD$ rises. Via $V_{SU,done}$ M5 can be activated so M4 is switched off when the LDO gets to regular operation.

A. Self Starting LDO

When $HVDD$ rises, the capacitive voltage divider of C_1 and C_2 determines the gate source voltage of M4. Therefore, C_1 and C_2 have to be designed to reliably switch on M4 in all working conditions. For a high robustness against different $t_{rise,HVDD}$, it is important that the maximum gate source voltage of M4 is not exceeded even if $HVDD$ is provided quasi instantaneously. Thus, C_1 and C_2 are dimensioned in a way to set M4 to its maximum gate source voltage when $HVDD$ reaches its target voltage. For high values of $t_{rise,HVDD}$ the limiting factor is the leakage current of M5, which discharges the gate source node of M4. Therefore, M5 has to be designed for low leakage.

When the gate source voltage of M4 reaches the threshold voltage, M4 starts to conduct. M4 is designed to work as a switch so the current through M2 and M4 is limited by R_1. Thus, M1 conducts a scaled current into the buffering capacitance and $AVDD$ starts to rise. The slope of $AVDD$ is determined by the size of R_1, C_{buf} and the supply voltage $HVDD$.

The voltage at R_1 equals $HVDD - V_{GS,M2} - V_{DS,M4} \approx HVDD$. For really short $t_{rise,HVDD}$, $AVDD$ rises at a nearly constant rate. The maximum start current is determined by the mirroring ratio of M1 to M2 and the maximum start current through M2 which is $\frac{V_{HVDD,target}}{R_1}$. For large $t_{rise,HVDD}$, $AVDD$ starts to rise, long before $HVDD$ has reached its target voltage. Thus, $AVDD$ is limited by the momentary voltage of $HVDD$.

Due to process variations, the voltage of $AVDD$ at which the bandgap provides the reference current and voltage cannot be specified exactly. However, simulations show that the interaction of the bandgap reference and the LDO works properly. At a voltage between 1.1 V and 1.6 V a reference current from the bandgap is provided to the OP of the LDO. This activates the control loop and $AVDD$ is actively controlled with respect to V_{ref}, which itself is currently generated and not yet at its final voltage.

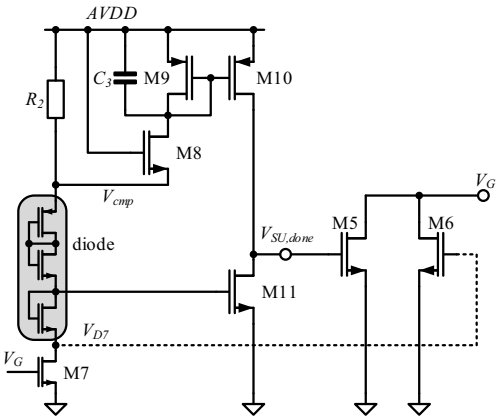


Fig. 4. Schematic of the start-up done circuit.

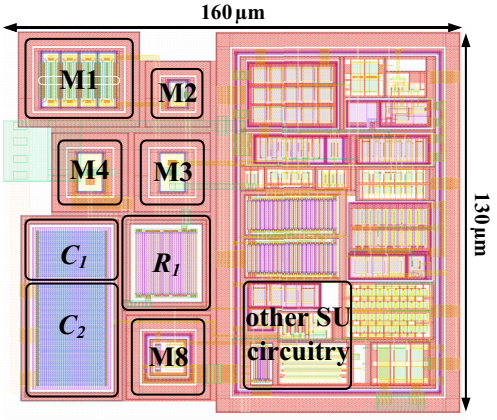


Fig. 5. Layout of the LDO.

B. Start-up Done Detection

To determine when the LDO's control loop is active and the start-up circuit can be switched off some constraints have to be taken into account. The most important issue is that the start-up circuit cannot be switched on again after it is switched off once since it is based on a capacitive power up. Another consideration is that the start-up circuit is allowed to be active in parallel to the feedback loop as long as $AVDD$ is lower than the targeted voltage. So the range for switching off the start-up circuit is between 2.2 V and the target voltage of 5 V.

A first idea is to detect, if the feedback loop of the LDO is active. This can easily be done by checking if the gate of M3 is driven by the OP which is the case when some reference current is available and V_{ref} is above the feedback voltage of the OP. The drawback of this solution is that it is not reliable since the positive feedback from V_{ref} to $AVDD$ is not always given when the feedback loop is first activated. Thereby, the start-up might be stopped prematurely causing failure to the complete IC. Therefore, the start-up done detection has to operate independently from the rest of the circuit.

Fig. 4 shows the proposed circuit for the start-up done detection. At start-up conditions, $AVDD$ is at 0 V and V_G is capacitively activated by the rising $HVDD$ as indicated in fig. 3. M5 and M6 are switched off, M7 conducts and M8-10 do not conduct, where C_3 ensures this for M9 and M10. The proposed circuit works on the principle that M8 only starts to conduct if the voltage drop over R_2, V_{R2}, is high enough. At this point, C_3 is discharged and a current flows through M9. This current is mirrored to M10 until it gets higher than the current through M11 so $V_{SU,done}$ rises. Since M11 is designed to conduct only a very small current, this is roughly the case when $V_{R2} = AVDD - V_{cmp} > V_{th,M8}$ holds. M7 conducts during the complete start-up, so V_{cmp} is determined by the diode and $V_{cmp} \approx AVDD$ holds. To reduce the substrate effect, a combination of NMOS and PMOS diodes is used. At the time, the diode saturates, V_{cmp} stops to further increase and V_{R2} increases. At $AVDD \approx V_{diode} + V_{th,M8}$, V_{R2} exceeds $V_{th,M8}$ so M8 starts to conduct current. This activates M5 and, thus, discharges V_G.

To switch off the start-up circuit when the start-up is done, a cross coupling from V_G to the diode current path is implemented via M6 and M7. M7 is switched off together with V_G. This causes V_{D7} to increase, activating M6 and further discharging V_G. Thus, in normal operation of the LDO, neither the start-up circuit nor the start-up done detection draws any quiescent current and V_G is clamped to ground by M6.

C. Layout

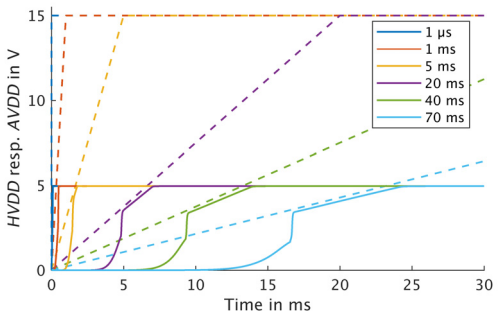
Fig. 5 shows the layout of the IC in a 0.18 µm triple well process. Due to technology constraints, the transistors M1-4 as well as R_1, C_1 and C_2 require an own well. To reduce the substrate effect of M8, which otherwise would strongly lower the transconductance of the transistor resulting in poor performance of the start-up detection circuit, it is layouted in its own well too. The rest of the start-up circuitry which are the diode and M5-M11 are layouted at the bottom left of the $AVDD$ well. The layout of the LDO requires a total size of 160 µm × 130 µm which is 20 800 µm^2, whereof about 7700 µm^2 are additional area for the start-up circuit.

IV. Simulation Results

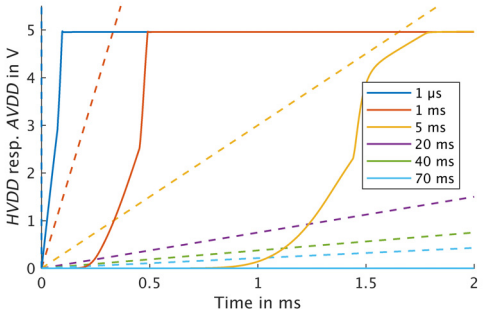
Fig. 6 shows simulation results of the start-up behaviour of the LDO, simulated in interaction with the bandgap reference, for different values of $t_{rise,HVDD}$. $HVDD$ (dashed trace) and $AVDD$ (solid trace) are depicted, whereby the graphs which are related to one $t_{rise,HVDD}$ are shown in the same colour.

The graph of $t_{rise,HVDD} = 70$ ms in fig. 6a illustrates how the start-up circuit starts at $HVDD = 2.8$ V. This is the voltage at which V_G exceeds V_{th} of M4 so the current flow through R_1, M2 and M1 starts. At $AVDD = 1.7$ V the slope rapidly increases due to the now activated control loop until a drop-out voltage $HVDD - AVDD \approx 210$ mV remains. Fig. 6b shows the correct functioning of the LDO for short $t_{rise,HVDD}$. Even for $t_{rise,HVDD} = 1$ µs which for the circuit is quasi instantaneous, the start-up reliably works and $AVDD$ is available after approximately 100 µs.

To verify the circuit, corner simulations of the extracted view of the layout were done for a temperature range from −40 °C to 140 °C. The circuit showed proper operation for



(a) Overview



(b) Zoomed

Fig. 6. $HVDD$ and $AVDD$ start-up for different $t_{rise,HVDD}$.

all corners up to $t_{rise,HVDD} = 70\,\text{ms}$. For higher rise times of $HVDD$, single failures at $140\,°\text{C}$ could be observed. At $70\,°\text{C}$, the circuit correctly operates up to $t_{rise,HVDD} = 200\,\text{ms}$. These failures can be ascribed to the leakage current through M5 and M6 which then too strongly discharges C_1 and C_2. Nevertheless, $70\,\text{ms}$ are sufficient for most applications of LDOs.

In addition to the start-up time, robustness against different buffering capacitors C_{buf} at $AVDD$ was tested. For capacitances of C_{buf} between $1\,\text{nF}$ and $1\,\mu\text{F}$, the LDO successfully starts for $t_{rise,HVDD} \leq 70\,\text{ms}$ at all corners. This wide range of $t_{rise,HVDD}$ must be supported, because it highly depends on the performance of the external voltage source for $HVDD$ and its connection to the chip. For $C_{buf} > 1\,\mu\text{F}$ failures at high $t_{rise,HVDD}$ and high temperatures at some corners occur. This can be handled by smaller $t_{rise,HVDD}$. E.g. for $t_{rise,HVDD} \leq 60\,\text{ms}$, the circuit functions up to $C_{buf} = 10\,\mu\text{F}$. For $C_{buf} < 1\,\text{nF}$, the control loop of the LDO becomes unstable which, if required, could be countered by a better compensation of the control loop.

Fig. 7 shows the voltages and currents of the start-up detection circuit for $t_{rise,HVDD} = 5\,\text{ms}$. Mind the different time scale of the lowest graph. The previously described sequence of voltages and currents can be observed. V_G rises, scaled to $HVDD$ by the capacitive voltage divider and at a certain point enables M4 so that current runs through R_1 and $AVDD$ starts to rise. At $1.5\,\text{ms}$, when $AVDD = 2.2\,\text{V}$, $V_{OP,out}$ gets to a significant level which indicates that the control loop gets active. From this time on, the slope of

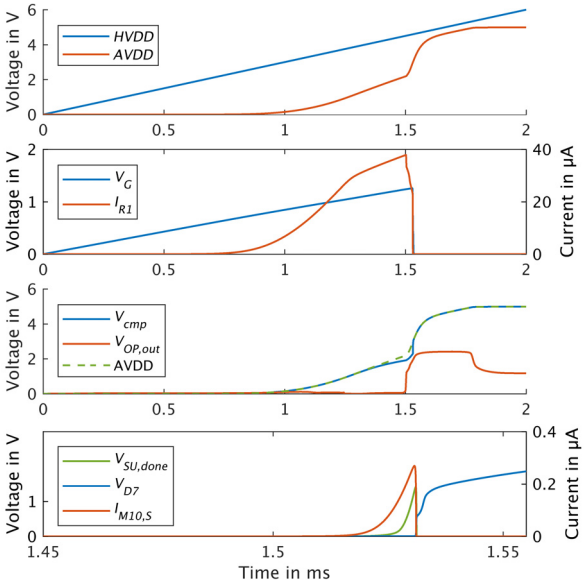


Fig. 7. Simulation results of start-up done detection.

$AVDD$ steepens due to the additional current through M2, drained to M3 and the start-up circuit is no longer necessary.

At $AVDD \approx 3\,\text{V}$ the start-up circuit is disabled. The voltage over the diode V_{cmp} saturates, so the voltage at R_2 rises, which enables M4 resulting in a current $I_{M10,S}$. $V_{SU,done}$ rises above $1.4\,\text{V}$ which discharges V_G and thus, disables the start-up circuit. Thereby, V_{D7} activates M6 which clamps V_G to ground.

V. Conclusion

A start-up circuit for an integrated LDO which independently becomes active when the supply voltage $HVDD$ is provided to the IC was proposed. It does not need any additional external components and switches itself off after the start-up is done, so it drains no quiescent current during the normal operation of the LDO. The functionality was verified for a temperature range between $-40\,°\text{C}$ to $140\,°\text{C}$ where it successfully starts the LDO at rise times of the supply voltage from $0\,\text{V}$ to $15\,\text{V}$ of $70\,\text{ms}$.

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