An ULP and Very Efficient Adaptively Biased LDO Regulator for Harvesting Application

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***Abstract*—This paper presents an ultra-low power (ULP), low quiescent current, low-dropout regulator with a class-AB and an adaptively biased error amplifier (EA). The high slew rate (SR) and the closed loop bandwidth improve the regulator transient response. Adapting the quiescent current regarding the transient response permits a high current efficiency at steady state. The stability is ensured for the entire output current range (1 µA – 3 mA) and for a maximum output capacitor of 100 pF by the current buffer compensation technique and the standard Miller capacitor compensation. The output voltage is set to 0.8 V with a minimum supply voltage of 0.92 V and a maximum quiescent current of 3.2 µA.**

Keywords—ULP, Adaptively Bias, Buffer Current Compensation, FVF Cells, SR Enhance, LDO, Voltage Regulator

I. INTRODUCTION

Low dropout regulator (LDO) is a crucial block in modern portable system-on-chip (SoC) design. Compared to switching regulators, LDO regulators provide a faster transient response, a stable supply voltage with a nearly-zero noise at the output which is well suited for mixed analog/RF circuits. Today one of the most critical issues in SoC design is the power consumption. This is a more prominent aspect in harvesting system where the power available is in the order of tens of µW. Lowering the supply voltage and decreasing the quiescent current leads the design toward low-power consumption. Nevertheless several challenges are imposed for LDO regulator, in terms of large and small signal behaviors.

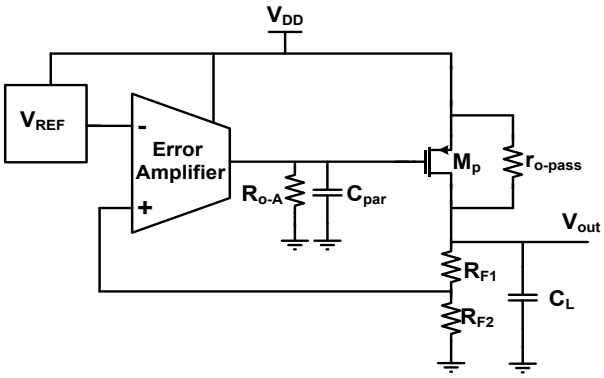

Fig.1 Circuit diagram of a classical LDO

A PMOS pass transistor, a resistor feedback circuit, an error amplifier and a voltage reference form a classical LDO regulator presented in fig. 1 [1], [2]. The fast transient response is due to the simplicity of the regulator. When a current load pulse occurs, the time needed to recover the proper output voltage is:

$$\Delta t_{tr} \approx \frac{1}{BW_{cl}} + t_{SR} \qquad (1)$$

where BW_{cl} is the closed loop bandwidth and t_{SR} the slew rate time. However, especially when a small on-chip capacitor is imposed at the regulator output, a decrease in Δt_{tr} is mandatory to limit the output voltage spikes $\Delta V_{out} = (\Delta I_{load} \cdot \Delta t_{tr})/C_L$. Several techniques have been introduced to improve the transient response in capacitor-less regulators. In [3] and [4] a push-pull error amplifier is proposed to enhance the SR. In [5] and [6] a spike voltage detector is inserted to instantaneously increase or decrease the gate voltage of pass transistor; while in [7] and [8] an adaptive bias circuit is used to increase the bandwidth of the regulator.

In this paper both SR enhancement and adaptive bias current methodologies are adopted to overcome the previously design challenges. These techniques permit to use a very low quiescent current ensuring a high current efficiency for the entire output current range. In addition, a minimum phase margin for the closed loop stability is achieved with a current buffer compensation technique.

II. PROPOSED LDO REGULATOR

The detailed schematic of the LDO is shown in fig. 2, where M_p is the PMOS pass transistor, transistors M_{AB1}-M_{AB4} implement the adaptively circuit, and capacitors C_M and C_{MB} with transistors M_{C1}-M_{C2} create the compensation circuit. The transistors M_{A1}-M_{A4} and M_1-M_8 implement respectively the flipped voltage follower (FVF) cells and the current mirror OTA [9]. Together the two blocks form the class AB error amplifier [10]. The output capacitor C_L, in the range of 2-100 pF, represents the parasitic capacitance associated to the interconnections. The class AB amplifier overcomes the limit of the fixed bias current I_B in a classical class A amplifier. Normally an important bias current is required to enhance the SR of the amplifier:

$$SR = \frac{I_B}{C_{par}} \qquad (2)$$

where C_{par} is the amplifier output capacitor. The two FVF cells replace the constant-current source permitting to separate this relation, with a remarkable advantage in terms of speed and power consumption.

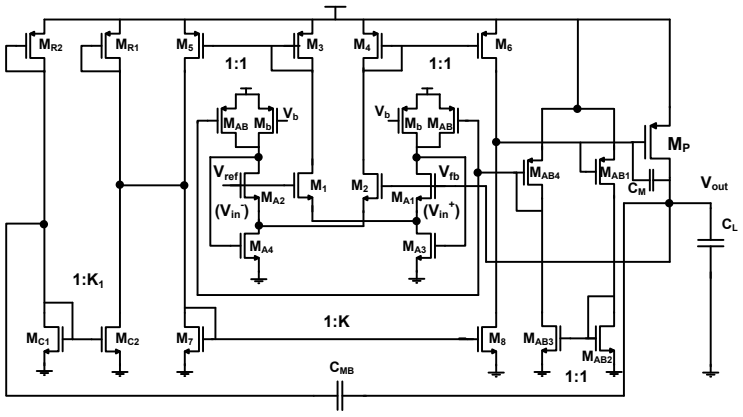

Fig.2 Transistor level schematic of LDO

All transistors of the amplifier operate in the subthreshold region, so the drain currents I_{D1} and I_{D2} of the differential input pair can be expressed as:

$$I_{D1} = I_{D0}\left(\frac{W}{L}\right)_{M1} \exp\left[\log\left(\frac{I_{DA1}}{I_{D0}\left(\frac{W}{L}\right)_{MA1}}\right) - V_{diff}\frac{k}{\eta V_T}\right] \quad (3)$$

$$I_{D2} = I_{D0}\left(\frac{W}{L}\right)_{M2} \exp\left[\log\left(\frac{I_{DA2}}{I_{D0}\left(\frac{W}{L}\right)_{MA2}}\right) + V_{diff}\frac{k}{\eta V_T}\right] \quad (4)$$

where I_{DO} is the saturation current, k the Boltzmann's constant, V_T the thermal voltage, η the slope factor and V_{diff} the input differential voltage. In steady state, $V_{diff} = 0$, the amplifier can be biased with very low quiescent current, setting the aspect ratio of transistors M_1/M_{1A}, M_2/M_{2A} and the bias current of M_b into FVF cells. When a positive or negative voltage overshoot occurs at the output of the LDO, the drain currents increase or decrease accordingly; thus the current delivered at the output of the amplifier is no longer limited by the constant current I_B as in classical amplifier. A higher slew rate in both positive and negative side is achieved, as the gate capacitance is charged or discharged despite of the low bias current used.

A good design approach for a LDO regulator suggests having a fast transient response, seeking to conserve an acceptable value of current efficiency for the entire range of load current:

$$\eta_c = \frac{I_{LOAD}}{I_{LOAD} + I_q} \quad (5)$$

where I_{LOAD} is the output current of the regulator and Iq the quiescent current. A higher value of the gain-bandwidth product GBW permits to improve the speed of the closed loop response, but at cost of a high transcondutance g_{M1} ($\omega_{GBW} = g_{M1}/C_L$). As a consequence, if the bias current of the amplifier is constant at the highest value for the entire load current range, the current efficiency will be degraded at light load.

Adapting the bias current of the amplifier to the regulator output current variations, it is possible to circumnavigate this limitation [7]. The transistors $M_{AB1} - M_{AB4}$ sense the voltage variations at the output of the amplifier. Sizing the transistor M_{AB1} m-times smaller than M_P, a scaled value of load current is mirrored to the second bias transistor M_{AB} through the transistors M_{AB2}-M_{AB4} (6).

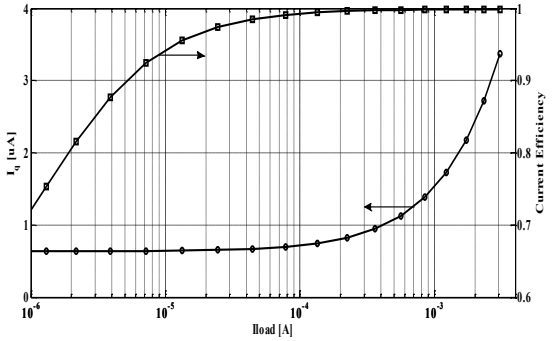

Fig. 3 LDO quiescent current and current efficiency versus load current

Figure 3 demonstrates the increase of the quiescent current of the error amplifier when the output current varies from 1μA to 3mA:

$$I_{AB} = \frac{I_{LOAD}}{m \times n} \quad (6)$$

where m is the scaled factor of transistor M_{AB1} respect to the pass transistor and n is the aspect ratio between M_{AB4} and M_{AB}.

As shown in fig. 4 at light load, the GBW is low, 118 kHz, due to the quiescent current in the range of few tens of nano-ampere; at heavy load the GBW extends to 1 MHz and the transient response of the regulator is improved. Taking into the account that the maximum output current determined by our application is 3 mA and in order to maintain the current efficiency > 99%, the maximum quiescent current of the LDO regulator must be less than 15 μA, which limits the SR enhancement and the GBW extension.

The closed loop of the LDO has to be stabilized to ensure the proper operation. The methodology used in this work to accomplish the goal is the same reported in [11], [12], where a standard Miller capacitor compensation is used to split the two main poles and a current buffer is inserted to break the forward path created by the capacitor. The effect of the current buffer is to mitigate the degradation of the phase margin caused by the right half-plane zero (RHPZ) generated through the forward path.

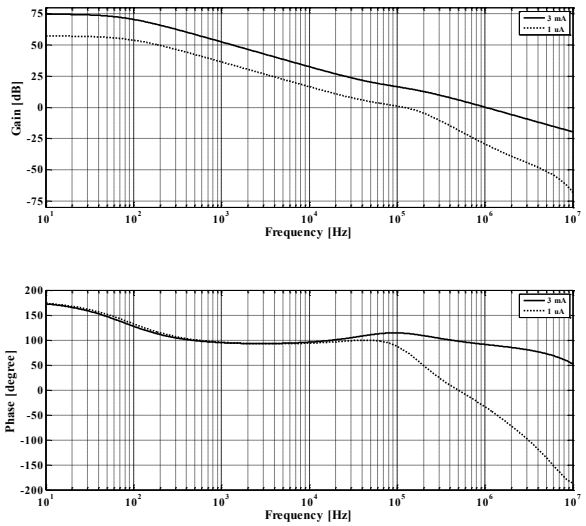

Fig.4 Open loop gain and phase for I_{Load} = 1µA (dashed line) and for I_{Load} = 3mA (solid line)

The compensation in the adaptively biased LDO involves an attentive study of the movement of the poles, due the significant span of the I_{Load}. Not only g_{mp} and R_{out} change with the value of the load current, but also the input transcondutance g_{m1} and the output resistance $R_{o\text{-}A}$ of the error amplifier. Using the current buffer, the LDO has a no quasi oscillating response with a damping factor about 1, when both the internal and the external loop have a phase margin greater than 60°. Generally a two poles system presents this response when the ratio between the second pole and GBW is greater than 1.5. This condition must be assured in both loops. From [11] the two ratios are:

$$K_I = \frac{|p_{2I}|}{GBW_I} = \frac{\left[C_L(C_{fb}+C_{o1})R_{o-A} + \frac{C_{MB}}{G_{CB}}\left(C_{fb}g_{mp}R_{o-A}+C_L\right)\right]^2}{\left[g_{mp}R_{o-A}(C_{CB}+C_{fb})+C_L\right]C_LC_{MB}(C_{fb}+C_{o1})\frac{R_{o-A}}{G_{CB}}} \quad (7a)$$

$$K_E = \frac{GBW_I}{GBW} = \frac{\left[g_{mp}(C_{fb}+C_{CA})R_{o-A}+C_L\right]^2}{\left[C_L(C_{fb}+C_{o1})R_{o1}+\frac{C_{CA}}{G_{CA}}\left(C_{fb}g_{mp}R_{o-A}+C_L\right)\right]g_{m1}R_{o-A}g_{mp}} \quad (7b)$$

Where K_I and K_E are internal and external stability parameters, C_{fb} is the sum of C_M and $C_{gd\text{-}p}$, C_{o1} mainly the gate capacitance of the pass transistor, G_{CB} the input transcondutance of current buffer. (7a) and (7b) show that R_{out} does not affect the stability, and g_{m1} appears only into external loop equation. So the study of K_I and K_E relates to g_{mp} and $R_{o\text{-}A}$. Figure 5 shows the trend of stability parameters when g_{mp} and $R_{o\text{-}A}$ change with the I_{Load}. Limiting the adaptively bias current of EA, its output resistance does not change substantially (a factor 6). Therefore the variations of K_E and K_I depending on $R_{o\text{-}A}$ are largely less important when compared to the variations depending on g_{mp}.

Thus, only the behavior of K_E and K_I with g_{mp} has to be observed. In figure 6 the phase margin is depicted depending on the output current. A minimum phase margin of 70° is achieved in the operating range, assuring a stable regulation

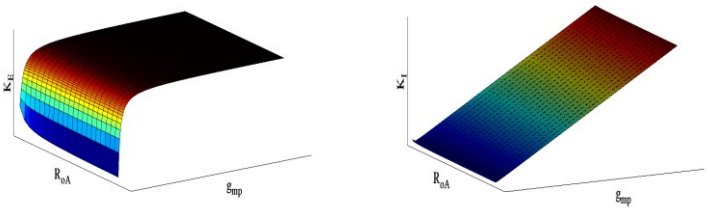

Fig.5 Parameters K_E and K_I versus g_{mp} and $R_{o\text{-}A}$

also at light load. It is also worth noting that the LDO can present a very low stand-by current (~100nA) since the PM is well above the critical value.

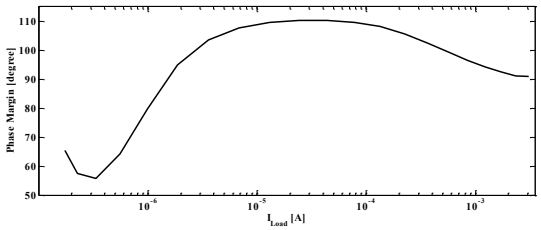

Fig.6 Phase margin versus output current

III. SIMULATION RESULTS

The circuit was simulated in a standard 130 nm CMOS technology. The output voltage is 0.8 V with a minimum supply of 0.92 V. The maximum output current is 3mA. To reduce the global quiescent current, the aspect ratio of current mirrors which goes into the error amplifier and the buffer, is chosen equal to 1. As a consequence the current gain of the current buffer is unitary $G = K \bullet K_1 = 1$. The trade-off accepted in this case is a larger occupied area due to a higher value of the required compensation capacitor; thus $C_M = 3$ pF and $C_{MB} = 7$ pF have been chosen. The output current scaled factor is 7500 and the bias current of transistor M_{AB} is 400 nA at high load.

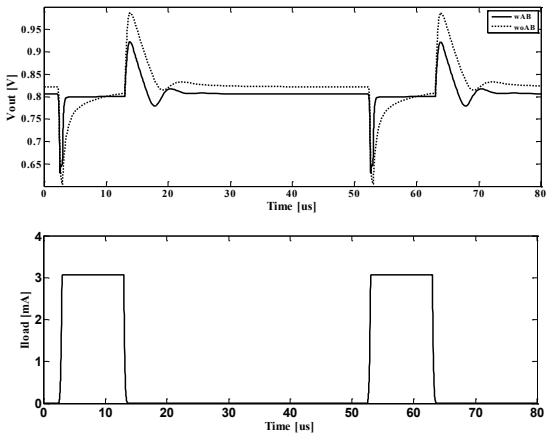

Fig. 7 Transient response

The transient response was simulated with an output capacitor of 20 pF and an output current step from 1 µA to 3 mA. The transient response is shown in figure 7 with and without the adaptively bias circuit. The voltage spike is about 150 mV with a recovering time about 1 µs.

The line regulation in fig. 8 was simulated with an output current of 3 mA with a variation of the voltage supply between 1 and 1.2V.

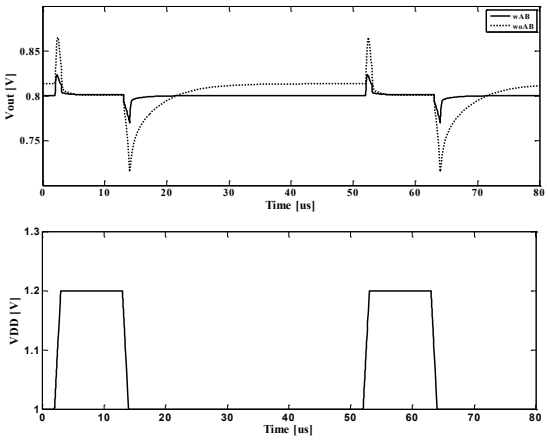

Fig. 8 Line transient when I_{Load} = 3mA

The LDO regulator with the adaptively bias circuit exhibits -53 dB of power supply ripple rejection PSRR as shown in figure 9.

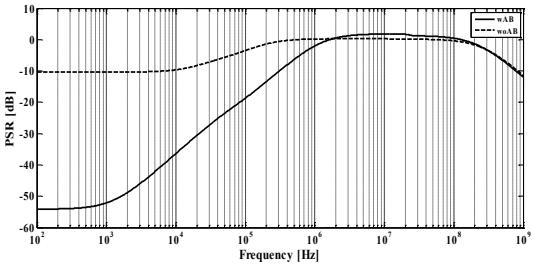

Fig. 9 Simulated PSRR at V_{DD} = 1V, V_{out} = 0.8V, I_{LOAD} = 3mA and C_L = 20pF

The table I shows performances comparison between this work and others published works for LDO regulator in harvesting applications. In order to evaluate the impact of the quiescent current on the regulator performance, the figure of merit used in [13] is introduced: $FOM = C_L \cdot \Delta V_{out} \cdot \frac{I_q}{I_{Load,max}^2}$

A lower FOM implies better performances.

IV. CONCLUSION

This paper presents a ULP LDO regulator for harvesting application. With the aim of reducing the quiescent current at the steady state assuring a good output voltage regulation for transient response, an adaptively bias and a class AB error amplifier were used. This permits to extend the closed loop bandwidth of the regulator and to increase the SR at the gate of the pass transistor. Even though the FOM reported in table I is slightly higher than that [13], the high current efficiency for all output current range, the improvement of the transient response and line transient confirm that this LDO is suitable for Harvesting applications.

TABLE I
PERFORMANCES SUMMARY

PARAMETER	[13]	[14]	This work
Tech [µm]	0.13 CMOS	0.25 BICMOS	0.13 CMOS
V_{in} [V]	3.4	1.2 - 2.75	0.92 – 1.4
V_{DO} [V]	0.109	0.2	0.12
$I_{Load,max}$ [mA]	5	1	3
I_q [µA]	12	7.6	0.58 - 3.2
Efficiency [%]	99	> 99	> 99
t_R [µs]	0.9	> 0.7	1.15
PSSR [dB]	-62	-	-53
FOM [ps]	0.34 @ C_L = 2 pF	437 @ C_L = 250 pF	1 @ C_L = 20 pF

REFERENCES

[1] G. A. Rincon-Mora e P. E. Allen, «A low-voltage, low quiescent current, low drop-out regulator», *IEEE J. Solid-State Circuits*, vol. 33, n. 1, pagg. 36–44, gen. 1998.

[2] M. Day, «Understanding Low Drop Out (LDO) Regulators». Analog Applications Journal, Texas Instruments, 1999.

[3] T. Y. Man, P. K. T. Mok, e M. Chan, «A High Slew-Rate Push-Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators With Transient-Response Improvement», *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 54, n. 9, pagg. 755–759, set. 2007.

[4] X. Ming, Q. Li, Z. k Zhou, e B. Zhang, «An Ultrafast Adaptively Biased Capacitorless LDO With Dynamic Charging Control», *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 59, n. 1, pagg. 40–44, gen. 2012.

[5] H. Wang e M. Sun, «A dynamic-biased dual-loop-feedback CMOS LDO regulator with fast transient response», apr-2014.

[6] P. Y. Or e K. N. Leung, «An Output-Capacitorless Low-Dropout Regulator With Direct Voltage-Spike Detection», *IEEE J. Solid-State Circuits*, vol. 45, n. 2, pagg. 458–466, feb. 2010.

[7] C. Zhan e W. H. Ki, «A high-precision low-voltage low dropout regulator for SoC with adaptive biasing», in *2009 IEEE International Symposium on Circuits and Systems*, 2009, pagg. 2521–2524.

[8] Y.-H. Lam, W.-H. Ki, e C.-Y. Tsui, «Adaptively-biased capacitor-less CMOS low dropout regulator with direct current feedback», in *Asia and South Pacific Conference on Design Automation, 2006.*, 2006, pag. 2 pp.-pp.

[9] R. G. Carvajal, J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, J. A. G. Galan, A. Carlosena, e F. M. Chavero, «The flipped voltage follower: a useful cell for low-voltage low-power circuit design», *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 52, n. 7, pagg. 1276–1291, lug. 2005.

[10] A. J. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, e R. G. Carvajal, «Low-Voltage Super class AB CMOS OTA cells with very high slew rate and power efficiency», *IEEE J. Solid-State Circuits*, vol. 40, n. 5, pagg. 1068–1077, mag. 2005.

[11] G. Giustolisi, G. Palumbo, e E. Spitale, «Robust Miller Compensation With Current Amplifiers Applied to LDO Voltage Regulators», *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 59, n. 9, pagg. 1880–1893, set. 2012.

[12] G. Palmisano e G. Palumbo, «A compensation strategy for two-stage CMOS opamps based on current buffer», *IEEE Trans. Circuits Syst. Fundam. Theory Appl.*, vol. 44, n. 3, pagg. 257–262, mar. 1997.

[13] M. Zargham e P. G. Gulak, «Fully-integrated, power-efficient regulator and bandgap circuits for wireless-powered biomedical applications», in *2012 IEEE International Symposium on Circuits and Systems*, 2012, pagg. 2873–2876.

[14] M. Paavola, M. Kamarainen, M. Saukoski, e K. Halonen, «A micropower low-dropout regulator with a programmable on-chip load capacitor for a low-power capacitive sensor interface», in *15th IEEE International Conference on Electronics, Circuits and Systems, 2008. ICECS 2008*, 2008, pagg. 450–453.