Adaptively Biased Output Cap-Less NMOS LDO With 19 ns Settling Time

Debashis Mandal, Chirag Desai, Bertan Bakkaloglu, *Fellow, IEEE*, and Sayfe Kiaei, *Fellow, IEEE*

***Abstract*—This paper presents an output external capacitor-less, fully integrated, fast settling NMOS low-dropout (LDO) regulator with adaptively biased error amplifier (EA) for system-on-chip core applications. The adaptive biasing technique increases both loop bandwidth and slew-rate of the LDO by 100% at full load condition without changing no-load quiescent current. Direct feedback to gate-to-source voltage of the NMOS regulation FET provides fast load transient response. The proposed LDO employs a cross-coupled common-gate input based EA, with transconductance boosting, achieving twice unity-gain bandwidth in comparison to a typical folded-cascode common-source input stage. Low output impedance of NMOS regulation stage and low input impedance of the EA reduce load dependent stability issue. The proposed regulator is designed and fabricated in a 0.18-μm CMOS technology with die-area of 0.21 mm^2. The LDO generates a regulated output voltage of 1.4–1.6 V from an input voltage of 1.6–1.8 V, consumes 133 μA quiescent current, and supports 0 pF to 50 pF load capacitance. Measured results show 166 mV undershoot with 19 ns settling time for a load step from 9 mA to 40 mA in 350 ps edge-time for zero-load capacitance. After using adaptive biasing, the settling time is reduced by 37% and 36% for 0 pF and 50 pF load, respectively.**

***Index Terms*—Adaptively biased error amplifier, NMOS low-dropout (LDO) regulator, cross-coupled common-gate input stage, fast load transient response, fast slew-rate.**

I. Introduction

DUE TO low output noise and fast load transient response, high performance linear low-dropout (LDO) regulators are indispensable for system-on-chip (SoC) dynamic voltage and frequency scaling (DVFS) core applications. Usually a large off-chip load capacitor (C_L) in micro-Farad range is used at LDO output (V_{OUT}) to get small output undershoot/overshoot and fast output voltage settling during load transients. The large C_L also improves LDO power supply rejection (PSR). However, due to a large area requirement, C_L in micro-Farad range is not integrated in SoC. This results in a significant degradation of both PSR and load transient response (undershoot/overshoot and settling time) for the fully-integrated output external capacitor-less (OECL)-LDOs.

The output C_L, and the gate capacitor (C_G) of regulation FET are two largest capacitors for an LDO. Hence, there are at least two low frequency poles: one located at the LDO output (ω_{POUT}), and other at the gate of regulation FET (ω_{PG}), where ω_{POUT} is load current (I_L) dependent. For a large off-chip C_L, LDOs are designed to be ω_{POUT} dominant, and a large quiescent current (I_Q) is burned to move ω_{PG} to high frequency. However, OECL-LDOs are designed to be ω_{PG} dominant, and such LDOs with limited on-chip C_L up to a few hundred pico-Farad are reported in [1]–[8]. In [9], to support a wide range of C_L at LDO output, an error amplifier (EA) based on current operational amplifier with input common-gate (CG) transistors is used.

To achieve a fast load transient response with a small or no on-chip load capacitor C_L, OECL-LDOs are required to be designed with a wide loop unity-gain bandwidth (UGB), and a faster slewing during load transient. The OECL-LDOs in [1]–[6] are designed with PMOS regulation FET. The smaller C_G of an NMOS regulation FET, compared to a PMOS FET, provides relatively high frequency ω_{PG}, hence a wider loop UGB, and a faster slew-rate (SR) during load transient. Moreover, the source follower configuration of the NMOS regulation FET provides an inherent low output impedance, which reduces load dependent stability issues. Due to a direct feedback to gate-to-source voltage of the regulation FET, NMOS regulation FET LDO (NMOS LDO) gives a faster load transient response than the PMOS regulation FET LDO (PMOS LDO). Also, the NMOS LDO inherently provides better PSR.

To enhance the SR, an EA with input cross-coupled CG transistors and output current summing stage is implemented in PMOS LDO [3]. However, the load transient settling time of V_{OUT} is about 4 μs, which is a quite large for DVFS applications. In [10], a linear voltage regulator based on cascode NMOS regulation FET is designed for minimum 1.67 V dropout voltage (V_{DROP}) between input voltage (V_{IN}) and V_{OUT}, hence it is not suitable for low dropout applications. A switched-capacitor step-down DC-DC converter with series NMOS LDO is presented in [7], where the input voltage of the converter is directly used as the supply voltage for the EA of LDO. For the NMOS LDO in [8], the maximum I_L is 1 mA. However, the V_{OUT} settling time during load transient is more than 300 ns in [7], and 10.4 μs in [8], which are quite large for DVFS SoC applications. An OECL analog-assisted digital LDO (AA-DLDO) using output PMOS regulation switches is presented in [11], however its load transient V_{OUT} settling time is more than 3 μs.

In this paper, a wide bandwidth OECL-NMOS LDO with adaptively biased EA is proposed that achieves 166 mV undershoot and 19 ns settling time for 4.5X load step in 350 ps edge-time for zero C_L. A wide bandwidth EA with

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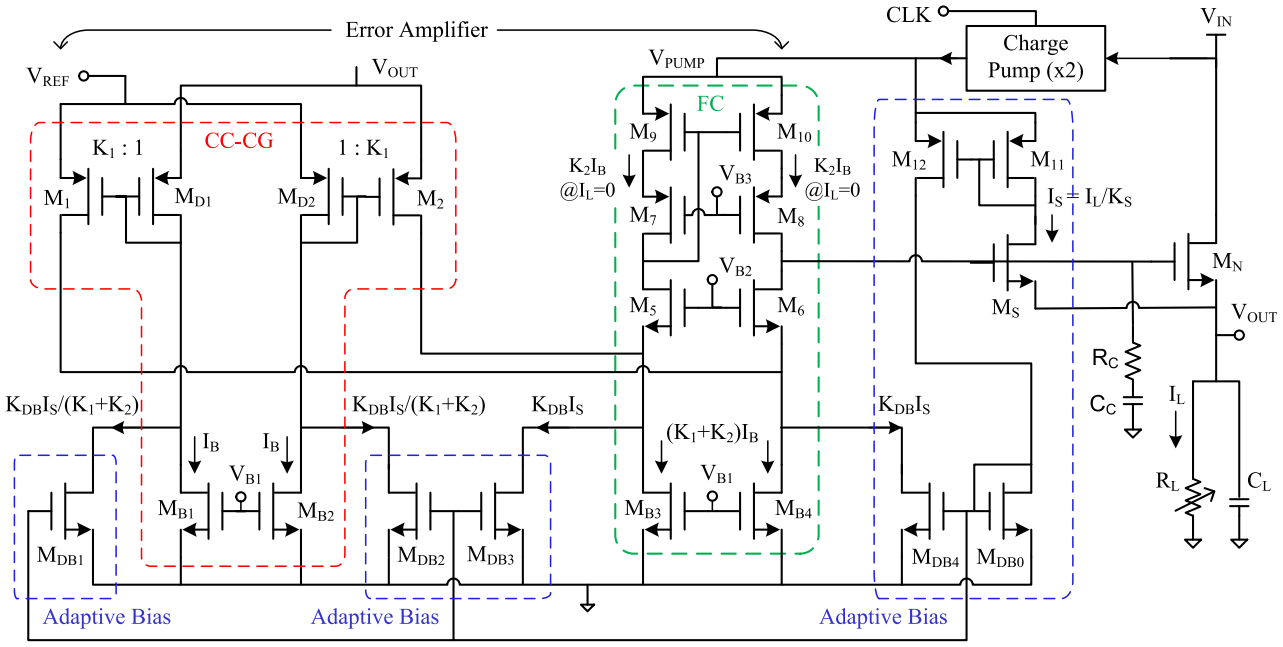

Fig. 1. Proposed NMOS regulation FET LDO with adaptive biasing.

a low input impedance and a high DC gain is designed using a cross-coupled (CC) CG input differential pair and a folded cascode (FC) output stage. The low input impedance of the EA further reduces LDO output impedance at no-load condition hence reduces the effect of output load variation on the LDO loop stability. The CC-CG input differential pair provides twice transconductance compared to a conventional CG stage with negligible increment of input bias current. Moreover, an adaptive-biasing circuit is designed to sense the regulation FET current, which enhances loop UGB and boosts the SR, hence, further improving the load transient response. A charge-pump voltage doubler (CPVD) in [12] is used to generate the supply voltage for the EA output stage to raise the gate voltage of NMOS regulation FET, ensuring the V_{DROP} of 200 mV across the regulation FET. The rest of this paper is organized as follows. The proposed LDO is discussed in Section II. Section III presents the loop stability analysis. Section IV summarizes the measurement results and Section V concludes this paper.

II. Proposed LDO Architecture

The schematic of the proposed NMOS LDO is shown in Fig. 1. It consists of an NMOS regulation FET (M_N) at output, an error amplifier (EA), an adaptive biasing circuit (ABC), and a CPVD. The EA compares V_{OUT} with a reference voltage (V_{REF}), generates the required gate drive voltage for M_N, and regulates V_{OUT} to V_{REF}. The EA is a FC-CG amplifier. The CG input stage provides a low input resistance of the EA. Thus, the direct feedback of V_{OUT} to the EA input maintains the low output resistance at quiescent mode of operation, hence stabilizing the regulation loop across a wide load range. High output resistance of the FC output stage sets the pole ω_{PG} as the dominant pole of the system, and also provides high DC loop gain. The ABC improves V_{OUT} regulation during load transient and also improves loop UGB. Using clock (CLK) frequency of 20 MHz, two flying capacitors of 5 pF each, and an output capacitor of 30 pF, the CPVD generates $2V_{IN}$ nominal supply voltage (V_{PUMP}) of 3.4 V for the EA output stage from the V_{IN} of 1.8 V, to raise the gate voltage of the NMOS regulation FET above V_{IN}. By using a switching frequency of 20 MHz, the output ripple of CPVD is negligible, hence the output of the LDO is immune to the switching noise coupling through the EA and the C_{GS} of the NMOS regulation FET.

A. Error Amplifier (EA)

Error amplifier is a folded cascode common-gate amplifier. Transistor pairs M_{D1}-M_1 and M_{D2}-M_2 are two transconductance (g_m) stages at the input of EA. The source of M_1 (M_2) and source of diode-connected transistor M_{D1} (M_{D2}) are the two inputs, and the drain of M_1 (M_2) is the output of the g_m-stage. The bias current of M_1 (M_2) is set K_1 times of that of M_{D1} (M_{D2}). Two such g_m-stages are cross-coupled to form differential input stage for the EA with a low input impedance. Due to the CC structure, twice input differential swing gets amplified, which provides twice the overall transconductance for the EA, enabling twice UGB with respect to a conventional FC-CS amplifier, and consequently twice the speed. Equivalent transconductance (G_{mEA}) and single-ended input resistance (R_{IEA}) of the EA are written as (ignoring transistor's output resistance),

$$G_{mEA} = 2g_{mI}, R_{IEA} \approx \frac{K_1}{(K_1+1)(g_{mI}+g_{mbI})} \quad (1)$$

where, g_{mI}, g_{mbI} are transconductance, body-effect transconductance of transistor M_1 or M_2, and g_{mI}/K_1, g_{mbI}/K_1 are transconductance, body-effect transconductance of M_{D1} or M_{D2}, respectively. The source terminals of transistors M_2 and M_{D1} are directly connected to the output of the LDO.

The FC output stage, formed by transistors M_{B3}, M_{B4}, M_5-M_{10}, provides a high output resistance at EA output, and high open loop DC gain. The output resistance (R_{OEA}) of the EA is written as (ignoring transistor's body effect),

$$R_{OEA} = \frac{1}{\frac{1}{g_{mM8}r_{oM8}r_{oM10}} + \frac{(r_{oM1}+r_{oMB4})}{g_{mM6}r_{oM1}r_{oMB4}r_{oM6}}} \quad (2)$$

where, g_{mM6}, g_{mM8}, are transconductance of M_6, M_8; and r_{oM1}, r_{oMB4}, r_{oM6}, r_{oM8}, r_{oM10} are output resistance of M_1, M_{B4}, M_6, M_8, M_{10}, respectively. The bias current

of current source transistors M_{B3} and M_{B4} is $(K_1 + K_2)I_B$. In quiescent mode of operation (i.e., $I_L = 0$), output current of adaptive bias circuit is negligible (i.e., $I_{MDB1} = I_{MDB2} = I_{MDB3} = I_{MDB4} = 0$), hence current through M_1 or M_2 is $K_1 I_B$ and current through each output branch is $K_2 I_B$. The SR at the gate of regulation FET (SR_G) is expressed as,

$$SR_G = \frac{(K_1 + K_2)I_B}{C_G} \tag{3}$$

Therefore, to support load current change in a very short time (a few hundred pico-second), SR_G is required to be large. This can be achieved by increasing the bias current $(K_1 + K_2)\ I_B$, which increases LDO quiescent current I_Q.

B. NMOS Regulation FET

The smaller C_G of NMOS regulation FET, compared to the PMOS FET, moves the dominant pole ω_{PG} to higher frequency, hence a wider loop UGB and a fast SR are achieved, improving the load transient response (undershoot/ overshoot and settling time) as well as the PSR. The low output resistance due to the source follower configuration of NMOS regulation stage maintains a good loop stability over a wide I_L range. The equivalent output resistance of the LDO is expressed as,

$$R_{OUT} = \frac{1}{[(g_{mMN} + g_{mbMN} + \frac{1}{r_{oMN}}) + \frac{1}{R_{IEA}}] + \frac{1}{R_L}} \tag{4}$$

where, g_{mMN}, g_{mbMN}, r_{oMN} are transconductance, body-effect transconductance and output resistance of M_N. DC voltage gain of the output regulation stage is $g_{mMN}.R_{OUT}$, with a maximum value of unity. At light-load this gain is less than unity, and it reaches close to unity at full-load condition.

C. Adaptive Biasing

A typical digital current load in a DVFS system includes thousands of gates turning on in a very short time (in order of few hundred pico-seconds). Consequently, there is a significant undershoot at V_{OUT}. The LDO needs to react, and settle the V_{OUT} to its steady state value, quickly. Employing adaptive biasing technique, as the load changes EA bias current increases, which improves SR_G, hence the LDO load transient response.

In Fig. 1, the transistor M_S is placed in parallel with the output regulation FET M_N, which senses a fraction $(1/K_S)$ of I_L flowing through M_N. This sensed current (I_S) is mirrored by a transistor pair M_{11}-M_{12} and fed to the EA through transistors M_{DB0}, M_{DB1}, M_{DB2}, M_{DB3}, M_{DB4}. Assuming the current through M_{DB3} (M_{DB4}) is $K_{DB}.I_S$, and the current through M_{DB1} (M_{DB2}) is $K_{DB}.I_S/(K_1+K_2)$, the SR_G is expressed as,

$$SR_G = \frac{(K_1 + K_2)I_B + \frac{K_{DB}}{K_S} I_L}{C_G} \tag{5}$$

In quiescent mode, I_S is negligible. It increases when load current increases. At full-load condition if the bias current of the EA is increased by a factor of K_m, the dominant pole ω_{PG} and the loop UGB are moved to higher frequencies by K_m and $\sqrt{K_m}$ times, respectively; the SR_G is increased by K_m times; and the EA DC gain is reduced by $\sqrt{K_m}$ times. However, the reduction of the EA DC gain is compensated to a certain extend by the increased gain of the NMOS regulation FET.

During load transients when output sees undershoot (ΔV_{OUT}), the transistor M_S detects the variation at V_{OUT} and generates a load dependent transient current $g_{mS}.\Delta V_{OUT}$, where g_{mS} is load dependent transconductance of M_S. Through the current mirrors, the ABC enables the tail transistors M_{DB1}-M_{DB4} to effectively increase the transient bias current of the EA. Hence, the SR_G is represented as,

$$SR_G = \frac{(K_1 + K_2)I_B + \frac{K_{DB}}{K_S} I_L + K_{DB}\ g_{mS}\Delta V_{OUT}}{C_G} \tag{6}$$

Therefore, with the adaptive biasing circuit the SR_G becomes a function of I_L and transient V_{OUT} change. As the integrated CPVD supplies the EA output stage bias current change, the K_m is kept 2 in the design.

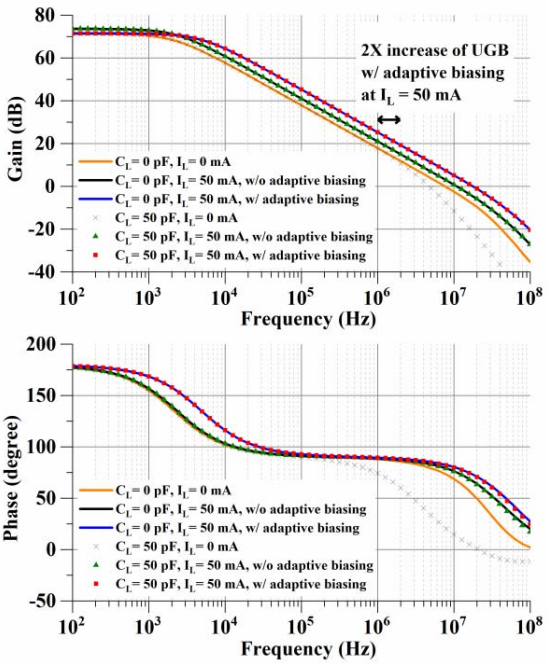

Fig. 2. LDO open-loop gain and phase plots.

III. Small Signal AC Analysis

Small signal AC model of the LDO is approximated by two low frequency poles: ω_{PG} at the gate of M_N and ω_{POUT} at the V_{OUT}. The open loop transfer function of the LDO is written as,

$$H_{LDO}(s) = \frac{G_{mEA}R_{OEA}\ g_{mMN}R_{OUT}\left(1 + \frac{s}{\omega_{ZC}}\right)}{\left(1 + \frac{s}{\omega_{PG}}\right)\left(1 + \frac{s}{\omega_{POUT}}\right)} \tag{7}$$

where, $\omega_{PG} = 1/R_{OEA}(C_G+C_C)$, $\omega_{POUT} = 1/R_{OUT}(C_L+C_P)$, $\omega_{ZC} = 1/R_C C_C$, and C_P is a parasitic capacitance at V_{OUT} that is limited to a few pico-Farad. For OECL-LDOs, ω_{PG} is the dominant low frequency pole. The pole ω_{POUT} is a function of I_L (i.e., $1/R_L$) as shown in (4), and is moved to high frequency when I_L increases. At no-load or light-load condition, low R_{IEA} pushes ω_{POUT} to high frequency and improves loop phase margin (PM) for zero C_L. To improve the loop PM at no-load and light-load for 50 pF C_L, a small series R-C compensation network (R_C of 5 kΩ and C_C of 2 pF) is added at EA output. The other design parameters are: $I_B = 2.3$ μA, $K_1 = 10$, $K_2 = 4$, $K_m = 2$.

Fig. 2 shows the small-signal AC response of the LDO open-loop at no-load and full-load ($I_L = 50$ mA), with and without using adaptive biasing along with 0 pF and 50 pF C_L.

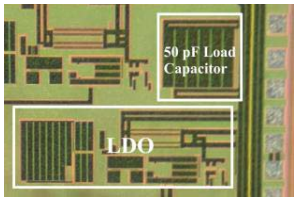

Fig. 3. Die micrograph.

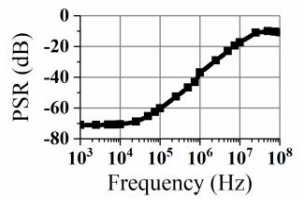

Fig. 4. PSR at $I_L = 50$ mA.

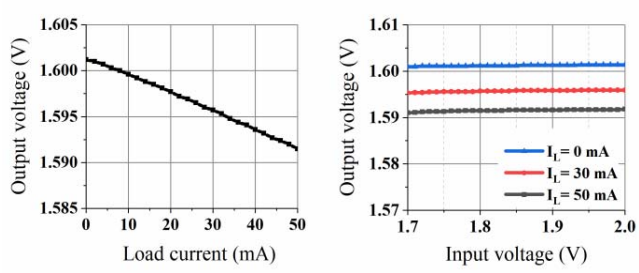

Fig. 5. Measured DC load and line regulations.

High open-loop DC-gain of 71.5 dB and UGB of 18 MHz at full-load condition are achieved. For a 2X increase of bias current (as $K_m = 2$) in the EA (due to adaptive biasing) at full-load condition, LDO UGB is increased by 2X instead of $\sqrt{2}$X, and DC loop gain remains constant instead of decreasing by $\sqrt{2}$X. This is due to about $\sqrt{2}$X increase of gain at the LDO output regulation stage.

As ω_{PG} is the dominant pole in the design, a trade-off exists between the achievable UGB and the I_L requirement, where the I_L requirement decides the size of the NMOS regulation FET. Hence, the EA has been designed with required output impedance to achieve the maximum loop UGB ensuring sufficient loop gain to provide a good steady-state regulation.

IV. Measurement Results

The proposed LDO regulator is designed and fabricated in a 0.18 µm CMOS technology and occupies 0.21 mm^2 die area. The die micrograph is shown in Fig. 3. A C_L of 50 pF capacitor is also integrated on-chip. The implemented LDO provides a regulated V_{OUT} of 1.4 -1.6 V from a V_{IN} range of 1.6 -1.8 V with V_{DROP} of 200 mV across the regulation FET. The measured I_Q including the CPVD is 133 µA. The DC load and line regulations are measured less than 194 µV/mA at $V_{IN} = 1.8$ V, and 2.67 mV/V at $I_L = 50$ mA as shown in Fig. 5, respectively. The obtained PSR is 71 dB @ 1 kHz as shown in Fig. 4.

Fig. 6 shows the line transient response for 200 mV step in 10 ns edge-time at $V_{IN} = 1.8$ V. The maximum ΔV_{OUT} observed is 36 mV for $C_L = 0$ pF, and 34 mV for $C_L = 50$ pF, respectively. The load transient response is measured at $V_{IN} = 1.8$ V, $V_{OUT} = 1.6$ V, and edge-time of 350 ps

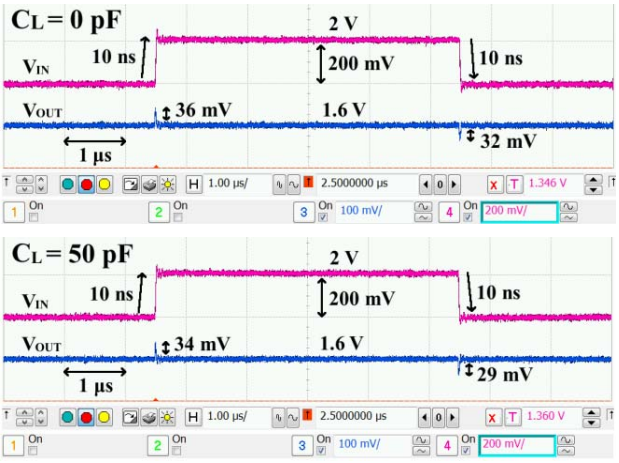

Fig. 6. Measured line transient response at $I_L = 40$ mA.

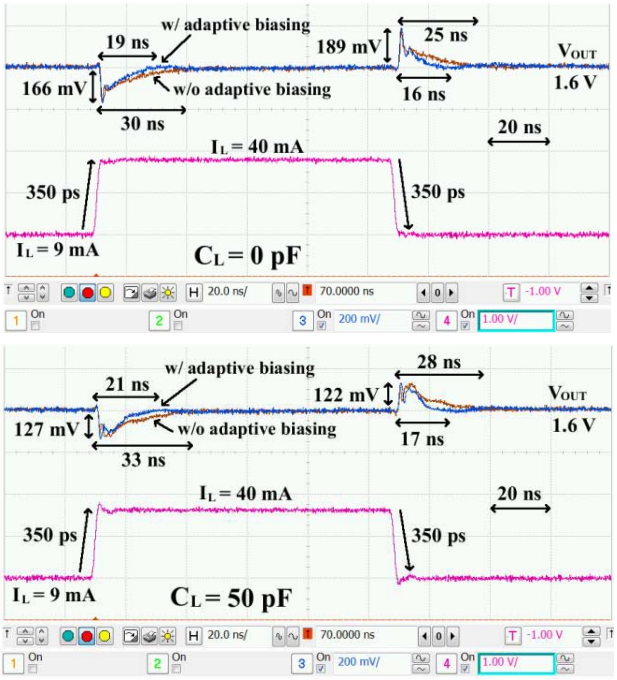

Fig. 7. Measured load transient response w/ and w/o adaptive biasing.

for the load step. Fig. 7 shows the load transient response for 4.5X I_L step between 9 mA and 40 mA. The undershoot voltages (ΔV_{OUT}) are 166 mV and 127 mV for 0 pF and 50 pF C_L respectively, and overshoot voltages are 189 mV and 122 mV for 0 pF and 50 pF C_L, respectively. The observed settling times (T_{SETTLE}) from undershoot are less than 19 ns and 21 ns for 0 pF and 50 pF C_L, respectively. The settling times from overshoot are less than 16 ns and 17 ns for 0 pF and 50 pF C_L, respectively. The figure also shows the load transient response for the same set-up when the adaptive biasing is disabled. After using the adaptive biasing, for low-to-high I_L step, the T_{SETTLE} is reduced by 37% and 36% for 0 pF and 50 pF C_L, respectively. The settling time reduction is 36% and 39%, respectively, for high-to-low I_L step. Fig. 8 also shows load transient response for I_L step from no-load condition.

Different performance parameters of the proposed LDO are summarized and compared with state-of-the-art OECL-LDOs designed with different specifications using different technologies in Table I. The edge-time of output load step is one of the

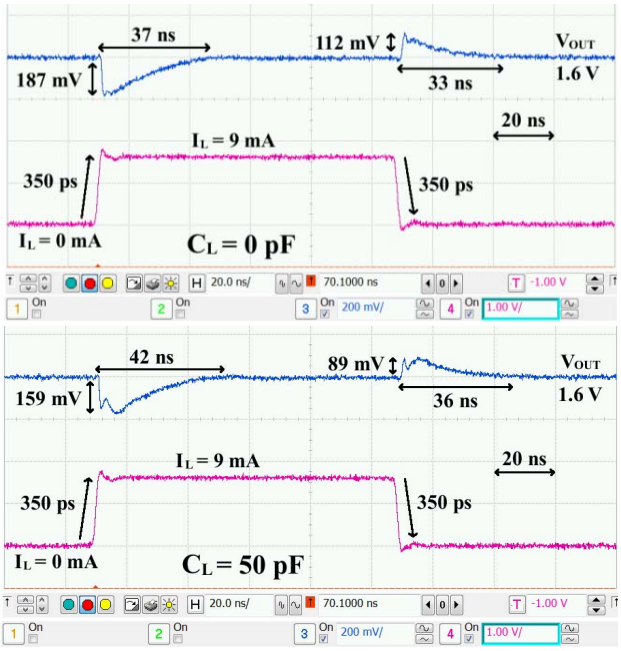

Fig. 8. Measured load transient response for load step from no-load condition.

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART OECL-LDOS

Parameters	This work	TCAS-I 2017 [8]	TPE 2016 [7]	TCAS-II 2013 [1]	ESSCC 2012 [10]	TCAS-II 2010 [6]
Technology (µm)	**0.18**	0.35	0.065	0.11	0.065	0.35
Regulation FET	**NMOS**	NMOS	NMOS	PMOS	NMOS	PMOS
V_{IN} (V)	**1.6-1.8**	1.4-2.7	2.4-2.6	1.8-3.8	2.07-5.5	1.8-4.5
V_{OUT} (V)	**1.4-1.6**	1.2-2.5	1	1.6-3.6	1.3	1.6
Max I_L (mA)	**50**	1	30	200	200	100
I_Q (µA)	**133**	1	161	41.5	176	20
C_L (pF)	**0-50**	0-1000	30	40	4400	0-100
ΔV_{OUT} (mV)	**166**	128	195	385	104	97
ΔI_L (mA)	**31**	0.8	30	199.5	149	100
T_{SETTLE} (ns)	**19**	~ 10400	~ 500	650	~ 60	< 9000
PSR (dB) @ Hz	**71 @1k**	~ 47 @10k	~ 40 @ 10 k	NA	50 @1k	40 @10k
Edge time (ns)	**0.35**	76	0.2	500	16	100
K ratio*	**1.75**	380	1	2.5k	80	500
FOM (mV) [4] **	**1.25**	60.80	1.05	200.22	9.83	9.70
FOM_N (mV/µm²)***	**38.47**	496.33	247.69	16547.05	2326.07	79.18

$$^{**}FOM = K\left(\frac{\Delta V_{OUT} I_Q}{\Delta I_L}\right);\ ^{***}FOM_N = K\left(\frac{\Delta V_{OUT} I_Q}{\Delta I_L}\right)\frac{1}{L^2};$$

$$^{*}K = \frac{\text{Δt used in the measurement}}{\text{the smallest Δt among designs for comparison}}$$

key parameters to determine the load-transient response of the OECL-LDO. Hence, the figure-of-merit (FOM) defined in [4] is used here for the comparison, and the smaller FOM indicates the better performance. If a technology offering a smaller minimum transistor length (L) is used, the FOM could be better due to the lower parasitic capacitance of the transistor [5]. Therefore, for fair comparison the FOM should include the parasitic capacitance, which is proportional to transistor area, hence, the square of transistor length (L) assuming an identical aspect ratio of the transistor. Therefore, a new FOM (FOM_N) is introduced by including L^2 in the denominator of FOM in [4]. The LDO performance is also compared based on FOM_N as shown in Table I. The FOM of the proposed LDO is smaller than other LDOs excluding FOM in [7], which has used 65 nm technology. However, the smallest FOM_N of 38.47 mV/µm² is achieved for the proposed LDO.

V. CONCLUSION

A fully-integrated output load capacitor-less NMOS LDO using adaptive biasing designed with cross-coupled common-gate input stage error amplifier is presented. The low output impedance of the NMOS regulation stage and low input impedance of the error amplifier reduces no-load stability issue, and provides a wide LDO bandwidth hence fast load transient response. The direct gate-to-source feedback in NMOS regulation FET and the adaptive biasing further improve load transient response without consuming extra quiescent current. A prototype is designed and fabricated in 0.18 µm CMOS technology for zero-to-50 pF load capacitance. High open-loop DC gain provides accurate load regulation of 194 µV/mA and line regulation of 2.67 mV/V. The proposed LDO achieves 166 mV undershoot and 19 ns settling time with zero load capacitance for 9 to 40 mA load step in 350 ps edge-time. It consumes 133 µA quiescent current, and achieves the smallest FOM_N of 38.47 mV/µm².

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