Low Quiescent Current, Capacitor-Less LDO with Adaptively Biased Power Transistors and Load Aware Feedback Resistance

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***Abstract*—This brief presents a novel low-power and area-efficient LDO that satisfies all primary requirements of power mapping for a Power Management IC (PMIC). The design introduces a dynamically biased feedback resistor which responds instantly to the output voltage variations, thereby achieving better load transient behavior. Besides, the employed adaptive-biasing technique contributes in architectural transformation to attain stability over a wider range of load currents (0-100mA). It provides a regulated voltage of 1.87V from a supply ranging from 1.92V to 3.6V with a reported load and line regulation of 0.00136mV/mA and 0.078mV/V respectively. Moreover, the circuit potentially supports the load transients either from 0A to 100mA or 100mA to 0A with a rise and fall times of 10μs. The achieved overshoot and undershoot values are 160mV and 154mV respectively. Hence, it demonstrates a substantial steady-state and transient performance with low-power thus making it suitable for battery-operated portable devices.**

***Index Terms*—Capacitor-Less Low Dropout (CL-LDO), Quiescent current (I_Q), Error Amplifier (EA), PMIC, Baseband (BB)**

I. Introduction

The growing demand for battery-operated portable devices (like cellular phones and cameras) throws a greater challenge in designing sophisticated PMICs [1]. In PMIC of cellular phone, distinct LDOs are employed to power up a variety of blocks (Baseband (BB), RF and audio sections) to meet the requirements in terms of voltage and current levels. The BB chipset of cellular phones requires a highly accurate voltage (1.8 V) with a decaying battery (Li+ battery). Therefore, the LDOs designed for this purpose should have a better load regulation, line regulation and ripple rejection (to reject battery ripples) at low frequencies (217 Hz for GSM phones) with limited I_Q ($\leq 1\mu$A) [2].

Several techniques [3]–[7] have been proposed in the literature to ameliorate different performance parameters of the LDO. However, the I_Q requirement of these circuits make them unfavorable for the applications discussed earlier. Few other LDO architectures proposed in [8]–[13] have demonstrated a good power efficiency. In [9], the use of a digital error amplifier (EA) has greatly minimized the I_Q at an expense of settling time (during load transients) and drop-out voltage. The design proposed in [10] used a feed-forward compensation technique with a flipped voltage follower as a power stage. It achieved good performance in terms of I_Q and settling time but the load current (I_{load}) is limited to 10mA. [8], [11] obtained better performance during load transients but with $I_Q \geq 7\ \mu$A. Also, [12] and [13] exhibits a good transient behaviour but the I_{load} of [12] is limited up to 50mA and [13] requires an output capacitance of 10pF.

By virtue of this background, there is a requirement of the design that delivers a wider load current (0-100mA) with better transient behavior, load and line regulation at low I_Q. The paper is organized as follows; Section II explains the architectural details of the proposed design. Section III shows the design verification and Section IV concludes the brief.

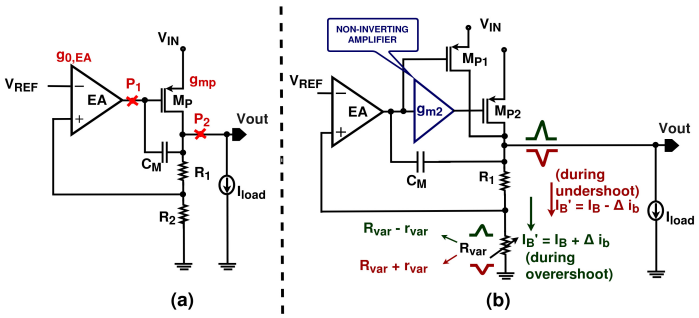

Fig. 1. (a) 2-stage CL-LDO (b) Proposed architecture

II. Proposed Architecture

The conventional (gate capacitance dominant) 2-stage CL-LDO is shown in Fig. 1(a). It contains a dominant pole ($P_1 \propto g_{o,EA} \propto \sqrt{I_L}$) at the output of EA and a non-dominant pole ($P_2 \propto g_{out} \propto I_L$) at the output of LDO [14]. During the smaller I_{load}, these two poles tend to come closer causing the problem of instability. Besides, the EA driving the power transistor (M_P) should have a higher slew rate to support load transients (0-100mA-0) but this results in the increased power consumption.

The proposed design with dynamically biased feedback resistor (R_{var}) enhances the slew rate during transients, load-based architectural transformation provides stability over the entire range of load currents (0-100mA). The conceptual schematic of the suggested architecture is shown in Fig. 1(b). It contains a high gain EA implemented by using a folded-cascode op-amp (M_1-M_{14} as shown in Fig. 2), power transistors M_{P1}, M_{P2} and a non-inverting amplifier (NIA). When the I_{load} to be delivered is less than a threshold value (I_{switch}), M_{P1} alone is responsible for providing the required

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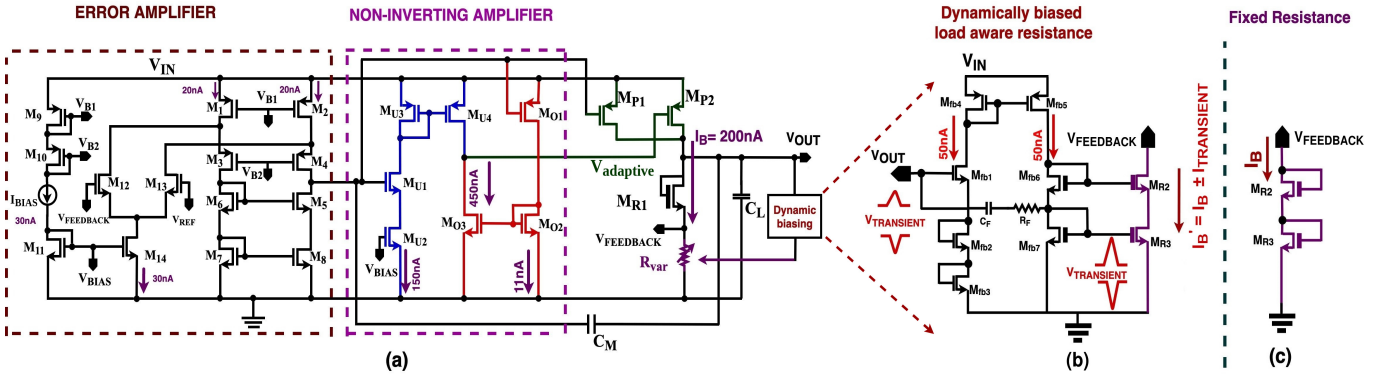

Fig. 2.(a) Circuit diagram (b) Dynamically Biased Load Aware Feedback Resistor (R_{var}) (c) Fixed resistor

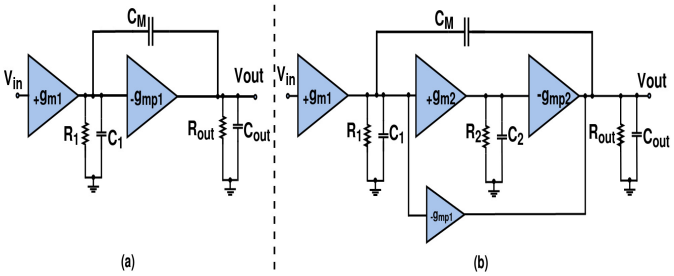

Fig. 3. Small signal model of (a) 2-stage LDO (b) 3-stage LDO

amount of current. But during higher load currents ($I_{load} \geq I_{switch}$), M_{P2} is also turned on through an adaptive-biasing provided by NIA. Hence, the architecture transforms automatically from 2-stage LDO (EA-M_{P1}) to 3-stage LDO (EA-NIA-M_{P2}) when I_{load} exceeds I_{switch}. Furthermore, the instant variation in ac resistance of the R_{var} highly improves the transient behavior.

A. Stability analysis

1) Case I: When $I_{load} \leq I_{switch}$, the non inverting amplifier (2^{nd} gain stage formed by transistors M_{U1}-M_{U4} and M_{O1}-M_{O3} as shown in Fig. 2) operates in triode region thereby driving M_{P2} (W/L=14000/1) into cut off region. Therefore, the I_{load} is supplied by M_{P1} (W/L=150/1) alone making M_{P2} insignificant as shown in Fig. 4. The resulting architecture act as a 2-stage LDO whose small-signal model is shown in Fig. 3(a) where C_M is the compensation capacitance.

The transfer function of EA (with single dominant pole at its output) and power transistor are modeled as [14]:

$$A_{EA}(S) = \frac{A_{0,EA}}{(1+\frac{S}{P_1})} : A_P(S) = \frac{A_P}{(1+\frac{S}{P_2})} \quad (1)$$

where, $A_{0,EA}$ is the DC gain of EA and A_P is the power transistor gain. Therefore from Fig. 3(a), it is evident that it contains two significant poles P_1 and P_2 at the output of EA and LDO respectively.

$$P_1 = \frac{-1}{R_1(C_1+(1+g_{mp1}R_{out})C_M)} \; ; \; P_2 = \frac{-g_{out}}{C_{out}} \quad (2)$$

where R_1 and C_1 are equivalent resistance and capacitance at the output of EA, C_{out} and g_{out} are the output equivalent capacitance and conductance respectively. From (2), it is clear that P_1 is the dominant pole closer to origin and P_2 is the non-dominant pole which is located far away from P_1. To ensure stability, the pole P_2 is further shifted to a frequency greater than UGF ($\cong \frac{\beta \cdot g_{m1}}{C_M}$) with sufficient phase margin (PM). This

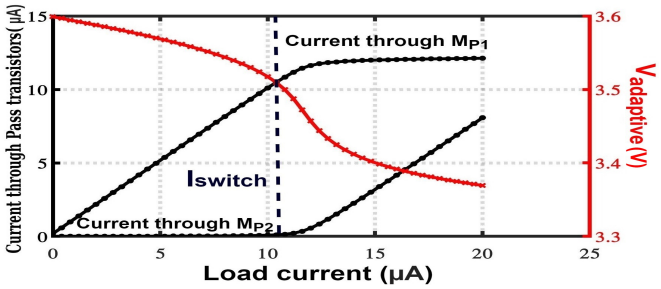

Fig. 4. Variation of current through M_{P1}, M_{P2} and $V_{adaptive}$ with I_{load}

is done by biasing R_{var} with minimum current I_B (Fig. 2), which resulted in a PM of 38^o at no load condition.

2) Case II: When $I_{load} > I_{switch}$, the output voltage of EA drives NIA into a saturation region (acts as an amplifier). Consequently, M_{P1} which is capable of supplying I_{load} up to I_{switch} (whose presence becomes insignificant) is now accompanied by the NIA which provides adaptive-biasing voltage ($V_{adaptive}$) to turn on M_{P2} (Fig. 4). Hence, the architecture is transformed into 3-stage LDO, whose small-signal model is shown in Fig. 3(b). The approximated open-loop transfer function is given by:

$$A_{openloop}(S) = \frac{-\beta g_{m1}g_{m2}g_{mp2}R_1R_2R_{out}}{(1+\frac{s}{P_1})(1+\frac{s}{\omega_o Q}+\frac{s^2}{\omega_o^2 Q})} \quad (3)$$

where $P_1 \approx \frac{-1}{R_1(C_1+(1+g_{m2}g_{mp2}R_2R_{out})C_M)}$ located at the output of EA act as a dominant pole. The pole at the output of LDO along with another pole at the gate of M_{P2} generates a biquad. The quality factor and natural frequency of the biquad are represented by Q($\propto \frac{1}{\sqrt{g_{mp2}}}$) and ω_o respectively. To ensure stability, g_{mp2} is chosen in such a way that these two poles were placed at a frequency greater than UGF which in turn avoids peaking in open-loop response (by realizing Q$\leq$0.707) [14]. When a conventional 3-stage LDO is subjected to light loads, these two non-dominant poles forming biquad become

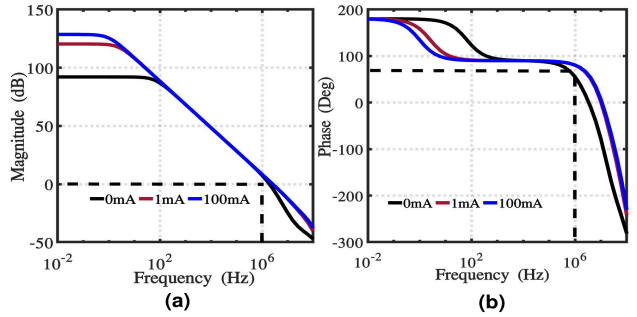

Fig. 5. (a) Gain vs Freq. @ I_{load}. (b) Phase vs Freq. @ I_{load}.

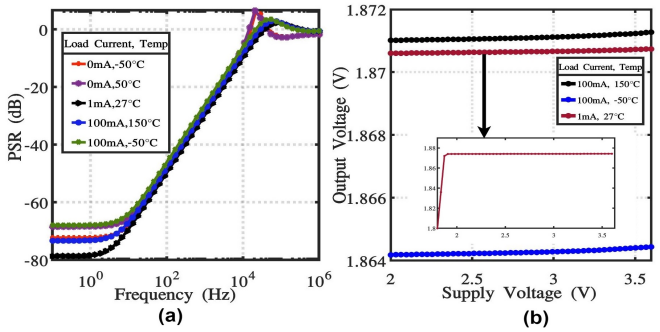

Fig. 6. (a) PSR at different temp. and I_{load}. (b) Variation of V_{out} with supply at different temp. and I_{load}

complex and result in peaking due to high Q [5], [15], [14]. In contrast, the proposed architecture dynamically transforms into 2-stage LDO during light load condition thereby assuring stability.

B. Dynamically Biased Feedback Resistor (R_{var})

The proposed architecture of R_{var} is as shown in Fig. 2(b). The sudden variations in the output voltage during load transients are sensed by R_F and C_F through which these variations are applied at the gate of M_{R3}. Therefore, the ac resistance of R_{var} increases (at undershoot) and decreases (at overshoot) instantly during the load transients.

$$I_B{}' \cong \frac{V_{FEEDBACK}}{R_{var} \pm r_{var}} \tag{4}$$

From (4), it is noticeable that the current ($I_B{}'$) flowing through the feedback resistance is increased ($\because R_{var}{}' = R_{var}\text{-}r_{var}$) or decreased ($\because R_{var}{}' = R_{var}\text{+}r_{var}$), hence resulting in respective discharging or charging of the output node. Subsequently, the designed R_{var} improves transient response.

C. Architectural performances

1) PSR and Line regulation: PSR of an LDO mainly relies on the loop gain and bandwidth. From (3), it is evident that the proposed CL-LDO provides high loop gain with limited bandwidth (as I_Q is limited) thereby resulting in high PSR at low frequencies ($\leq$ 1KHz) as shown in Fig. 6(a). The line regulation can be related to the PSR at low frequencies (DC). Hence, exceptional performance in line regulation is observed as shown in Fig. 6(b).

2) Load regulation and Load transient: A steady-state variation of output voltage with the load current is specified as load regulation (LR) of an LDO.

$$LR = \frac{\Delta V_{out}}{\Delta I_{out}} = R_{out,cl} \cong \frac{1}{\beta g_{m1} R_1 g_{m2} R_2 g_{mp} R_{out}} \tag{5}$$

From (5) it is apparent that, the proposed LDO achieves smaller $R_{out,cl}$ due to its high loop gain (Fig. 5 and Eq. (3)) resulting in a good load regulation (Fig. 9).

The load transient behavior of CL-LDO is highly dependent on the slew rate of the block that drives the gate of the power transistor. In the proposed CL-LDO, the NIA driving M_{P2} provides the required slew rate during load transients. Accordingly, the gate capacitance of M_{P2} is charged through the feedback path containing M_{U1}-M_{U4} and discharged through the feedback path containing M_{O1}-M_{O3} during the occurrence of undershoot and overshoot respectively. Besides, the introduced architecture of R_{var} (as explained earlier) further enhanced the transient response which is evident from Fig. 7(a) and 7(b).

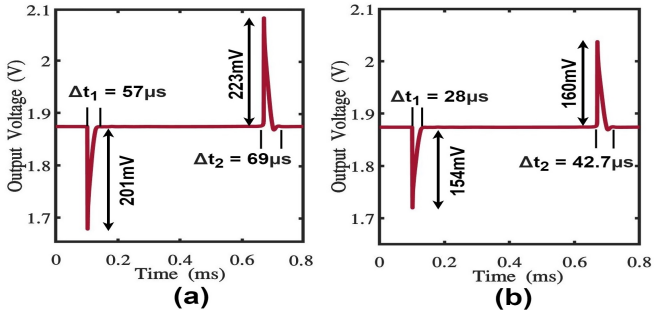

Fig. 7. Full load (0-100mA-0) transient response: (a) Fixed Resistor (b) R_{var}

III. Results and Discussion

The proposed architecture has been implemented in TSMC 0.18μm CMOS technology. The circuit uses an output capacitance (C_{out}) of 4pF, compensation capacitance (C_M) of 2pF, feedback capacitance (C_F) of 1pF and resistance (R_F) of 1KΩ. The frequency response of the circuit is analyzed at different load currents (0A, 1mA, 100mA) as shown in Fig.5. A phase margin in the range of 38^o to 81^o is observed (Fig. 5(b)) thereby ensuring stability across the load currents from 0A to 100mA. PSR at different load currents and temperatures is plotted as shown in Fig. 6(a). The overall variation of PSR at 100Hz is noted to be in the range of -55dB to -48dB. The line regulation at different load currents and temperatures is monitored as shown in Fig. 6(b). The line regulation of 0.095mV/V, 0.078mV/V and 0.082mV/V is observed at 100mA@150^oC, 1mA@27^oC and 100mA@-50^oC respectively.

The full load transient response (0-100mA-0 with rise and fall times of 10μs) of the proposed LDO employing fixed-resistor and R_{var} is shown in Fig. 7(a) and 7(b) respectively. The proposed LDO with R_{var} exhibits a better transient behavior with an overshoot of 160mV at 42.7μs settling time and an undershoot of 154mV at 28μs settling time. Monte-Carlo simulations (with process variations and mismatches) on undershoot and overshoot are performed for 1000 samples as

shown in Fig. 8(a) and 8(b) respectively. A mean of 168.2mV, 156.8mV and a standard deviation of 35.1mV, 42.5mV are noted for undershoot, overshoot respectively. Moreover, the

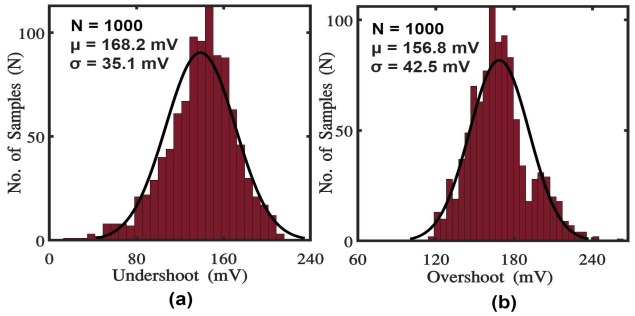

Fig. 8. Monte-Carlo simulation for 1000 Samples on: (a) Undershoot (b) Overshoot

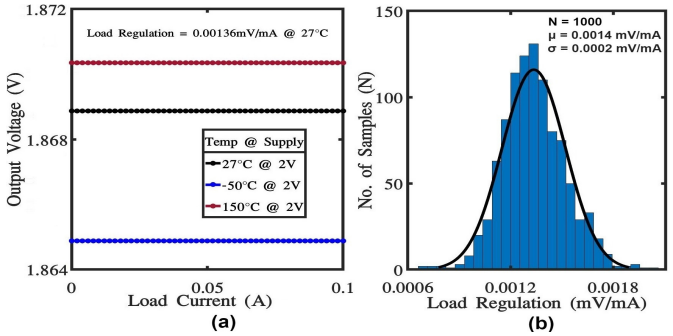

Fig. 9. (a) I_{load} vs V_{out}@27^{o}C, -50^{o}C and 150^{o}C (b) Monte-Carlo simulation for 1000 Samples on load regulation

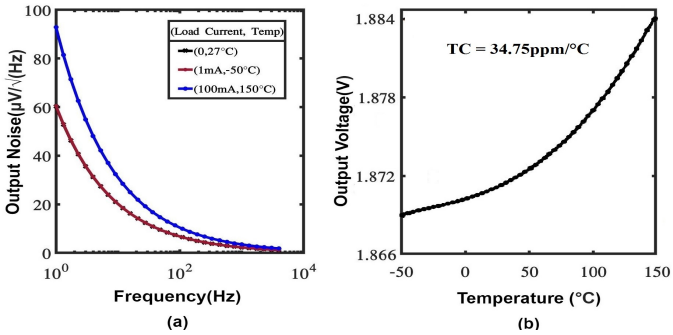

Fig. 10. (a) Output Noise (b) Temperature vs V_{out} @ no load

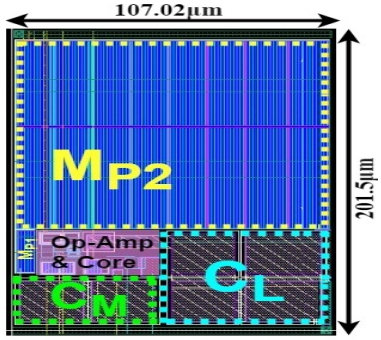

Fig. 11. Layout

TABLE 1: PERFORMANCE COMPARISION

Parameters	[11]	[8]	[10]	[9]	[13]	THIS WORK
CMOS Technology	350nm	180nm	65nm	350nm	180nm	180nm
Vin (V)	2.65 - 4	1.84 - 3.6	1.2	0.9 - 2	1.2 - 2.5	1.92 - 3.6
Vout (V)	2.5	1.8	0.9 - 1.1	0.5	1	1.87
I_{load}(mA)	0.05 - 100	0 - 50	0 - 10	0 - 50	±100	0 - 100
I_q(μA)	8	7	3	0.103	3.14	1
PSR (dB)	NA	-53@1kHz	-70@100Hz	NA	-50@100Hz	-53@100Hz
C_{out}	0 - 100pF	0 - 100pF	1 - 100pF	NA	10pF - NA	4 - 100pF
T_{settle}(μs)	0.2	<5	<1	400	3.6	42.7
Overshoot (mV) Undershoot (mV)	236 251	560 390	250 40	~320	150 220	160 154
Dropout (mV)	150	59	~100	400	200	50
FOM(ns)	0.016	0.7	0.3	0.824	0.11	0.428
Area(mm^2)	0.057	NA	NA	0.096	0.022	0.0215
Noise(μV/√Hz)	NA	NA	NA	NA	NA	58@1Hz 8@100Hz
Line regulation (mV/V)	1.156	0.00647	NA	21.76	0.69	0.078
Load regulation (mV/mA)	0.017	0.0024	NA	0.324	0.023	0.00136
Result Type	Measured	Simulated	Simulated	Measured	Simulated	Simulated

load regulation for the input of 2V is analyzed at different temperatures as shown in Fig. 9(a) which achieves a very less value of 0.00136mV/mA@27^oC. Besides, a Monte-Carlo simulation (with process variations and mismatches) on load regulation is performed for 1000 samples as shown in Fig 9(b). A mean of 0.0014mV/mA and a standard deviation of 0.0002mV/mA is achieved.

Likewise, the output noise of the proposed LDO is also examined at different load currents and temperatures as shown in Fig. 10(a). An output noise of 58μV/$\sqrt{Hz}$ at 1Hz with no load at room temperature is noted. Variation of output voltage with temperature at no load current with 2V supply is shown in Fig. 10(b). The worst-case temperature coefficient is found to be 34.75 ppm/^{o}C. The layout of the circuit is shown in Fig. 11, occupies an active area of 0.0215mm^2.

The performance comparison with the recently reported works is put forward in Table I. Comparatively, it achieved a good load regulation with less quiescent current. The figure of merit (FOM=$\frac{T_{settle} \cdot I_Q}{I_{out,max}}$) [16] is used here to compare the efficiency with prior architectures. It achieved reasonably less FOM of 0.428ns thus indicating a better transient behavior.

IV. Conclusion

An output CL-LDO with adaptively biased power transistors and dynamically biased load aware feedback resistance is designed. Its performance metrics are analyzed in all possible cases. From the results, it is evident that the proposed design achieved better performance parameters with very less quiescent current. Thus, the design is highly suitable for battery-operated portable devices particularly for the Baseband chipset of cellular phones.

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