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Verilog module instantiations

- Port connections by ordered list.

```
module mydesign (input x, y, z,
                 output o);
// x, y, z and o are at 1, 2, 3 and 4 position.
endmodule.

module tb_top;
    wire [1:0] a;
    wire       b, c;
mydesign d0 (a[0], b, a[1], c);
  // a[0] at 1 so connected with x
  // b[0] "  2  "          y
  // a[1] "  3  "          z
  // c    "  4  "          o
endmodule.
```

- Port connection by name.

```
module design_top;
    wire [1:0] a;
    wire       b, c;
mydesign d0 (.x(a[0]),
             .y(b),
             .z(a[1]),
             .o(c));
// x connected to a[0] . . .
   y      "      (b)  . . .
endmodule.
```

Teacher's Signature:.....

- Multiple module instance port connections are not allowed.

unconnected / floating ports.

- Ports that are not connected to any wire in the instantiating module will have a value of high-impedance.

module design_top

mydesign d0 (

.y(a[1]),

.0 (0));

endmodule.

// x, not connected and 0 not connected to c will be z.

- Such unconnected ports will be declared as high impedance (1'bz) typically in the waveforms.

→ It is perfectly legal to connect two ports with varying vector sizes, but the one with lower vector size will prevail and the remaining bits of the other port with a higher width will be ignored.