

Verilog Ports

- · Set of vignals that acr as imputes and ourputs
  to a paricular module and are primary ways
  of communicating with it.
- · It madure yarmicated as chip placed on pcp.

  · Poets are like pins and one used by the design to send and treceive signals from the outside would.

Let a letter gering the many of I get an absence

and the land to the land of th

(input) any receive values (autput) only send values (inout) simer send or receive

· Pours are by departs considered as nots of type wine.

book and and produced when show shows some shows some states

Syntac on some more than some one

input [net-type] [range] vistag-names;

inout [net-type] [namge] list of-names;

omput [net-type] [range] list-oy-names;

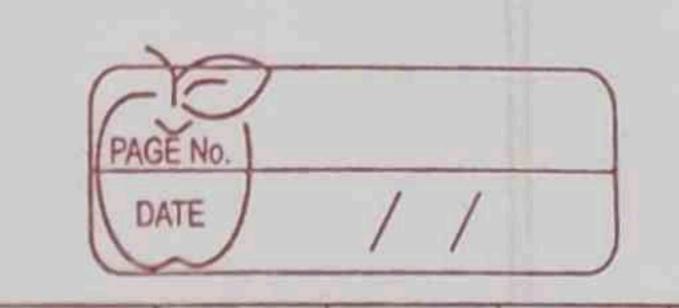
"output pour driven by a wire.

output [van\_type] [range] list\_og\_names;

Moutput pour driven by variable.

- It is illegar to use the same name you multiple pours.

Signed pours
and the administration of the same alarge to the
mædule Cinpur a,
The second secon
amput c);
1 parts a, b and c one by dejanur unsigned
endmædule.
mædule Cinput signed a, b,
aurpur c).
wire a, b.
reg signed c;
as bone siand co
bigned your rea
and madule,
this 1-c shipe pour namina mains
2001 and allowed my
specified inside the pour wish
mædule test (inpur [7:0], 9;
The state of the s
Ompu (7:0] c);
endmædule
endmæderle a 8-bit inpur



· It is illegal to redectare me same point in a not on variable type dectaration.
module tost (hput [7:0] a, output reg [7:0] e);  // a,e are implicitly doctored of typo wino
uire signed [7:0] a; // illegal uire [7:0]e; declaration already endmadule completed.
e de declaration door not include a not on variable type declaration again.
mædure tæst (input [7:0] a,  output [7:0] e);  reg[7:0] e;  // okay - typer was nær declared)
endura dula.