Verilag always black

Always block is one of the procedural blocks in varilag. Statements inside always block are accounted sequentially.

Syntax:

always @ Carent

[statement]

always @ (avent) begin [mulliple gratements]

end.

· Events are defined by sensitivity list.

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Sonsitivity list:

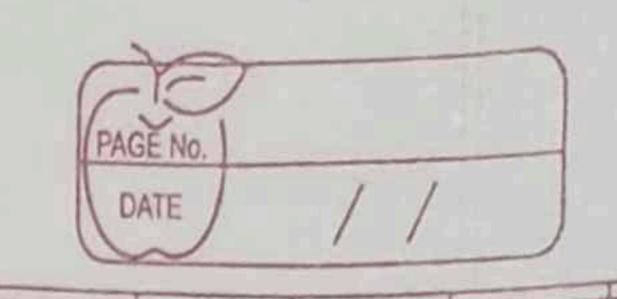
Is the expression that defines when the always block should be executed and is executed and is executed agree the Q operator within parantheses ().

of signals whose value changes will execute the always block.

Ex- always stock gets executed unementer the value of signals a on b change.

always @ (a conb) begin (8tatoments)

end



If there is no sensitivity list, the always block repeats continuously throughout the duration of a simulation.

Ex- always de = ~ cle;

· Even if there is no sonsitivity list,

there should be some type of delay

Simulation time is advanced by a delay

statement within the always.

Ex- always #10 clk = ~ clk;

Note-Explicit delays one not synthesizable into lagic gates.

Mence, real revilag design code always require a sensitivity list.

Example of simple combinational logic

(dorign. SV)

module combo (input a,b,c,d,e

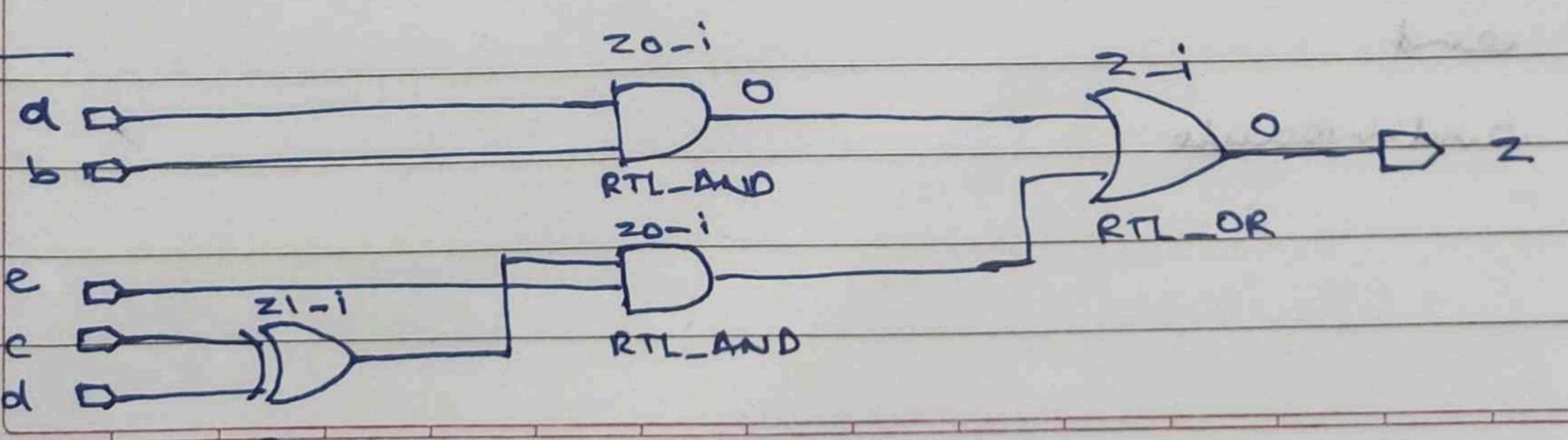
output reg z);

amays @ (a on b on c ondone) begin

z = ((a&b)1(c^d)&~e);

end

andmodule



(testbench)

madule Ho

rega, b, c, d, e;

mire 2,

integeni;

comba u0 (.a(a), .b(b), c.(c), .d(d), .e(e), .z(z));

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initial begins and of the

a & = 0;

b L= Osjana son son sentob distant - store

c <= 0;

d <=0; selection political hour assiste

e (=0; -table principle man a somment

\$ monitor ("a=1.0b b=1.0b c=1.0b d=1.0b e=1.0b z=1.0b", a,b,c,d,e,z);

tretted areas selected to the content of the selected

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// As there one Sinputs more con be 32 digerent input combinations.

Jan (i=0; i < 32; i=i+1) begin
{a,b,c,d,e}=i;

#10;

and

end

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