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Verilog Ports

- Set of signals that act as inputs and outputs to a particular module and are primary way of communicating with it.
- If module fabricated as chip placed on PCB
- Ports are like pins and are used by the design to send and receive signals from the outside world.

Types:

(input) only receive values
(output) only send values
(inout) either send or receive

- Ports are by default considered as nets of type wire.

Syntax

```
input [net_type] [range] list_of_names;
    // input port
inout [net_type] [range] list_of_names;
    // input and output port
output [net_type] [range] list_of_names;
    // output port driven by a wire.
output [var_type] [range] list_of_names;
    // output port driven by variable
```

- It is illegal to use the same name for multiple ports.

Teacher's Signature:.....

Signed ports

```
module (input  a,
               b,
       output c);
// ports a,b and c are by default unsigned
endmodule.

module (input signed a,b,
        output c);
  wire a, b;
  reg signed c;
 // a,b are signed from port
 // c is signed from reg
endmodule.
```

→ ANSI-C style port naming was introduced in 2001 and allowed the type to be specified inside the port list.

```
module test (input [7:0] a;
                         b,
             output [7:0] c);
      :
      :        // "b is considered
endmodule          a 8-bit input
```

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- It is illegal to redeclare the same port in a net or variable type declaration.

```
module test (input [7:0] a,
             output reg [7:0] e);
// a, e are implicitly declared of type wire.

wire signed [7:0] a;   // illegal
wire        [7:0] e;   declaration already
:                      completed.
endmodule
```

- If the port declaration does not include a net or variable type, then the port can be declared in a net or variable type declaration again.

```
module test (input  [7:0] a,
             output [7:0] e);
  reg [7:0] e;
  // okay - type was not declared)
  :
endmodule.
```

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