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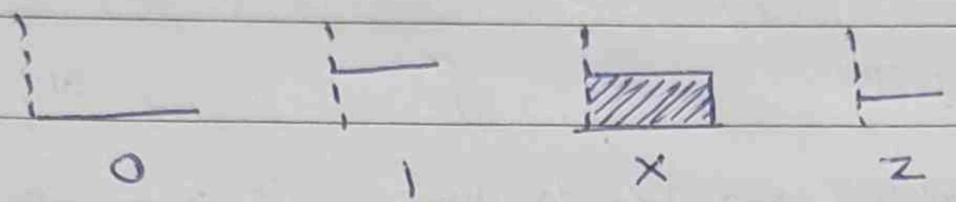
Data types

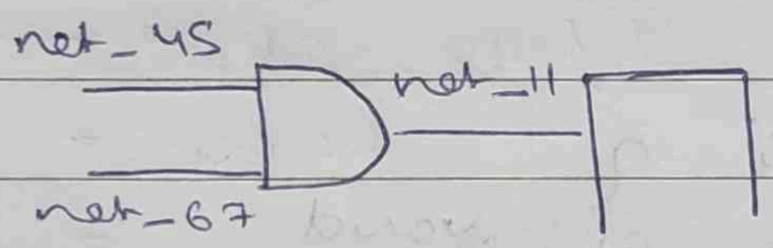
All data types can have 4 diff values except your **real** and **event** data types.

0 - logic zero, false condition
1 - logic one, true condition
x - unknown logic value
z - high-impedance state



Nets

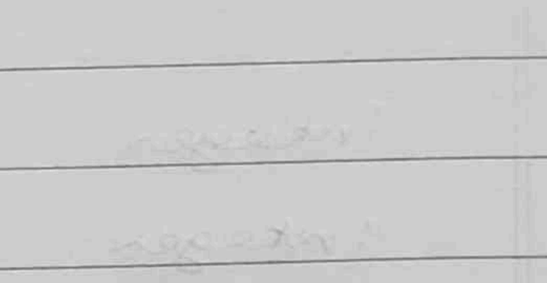
Used to connect between hardware entities like logic gates and hence do not store any value on its own.



- most popular and widely used net is wire.
  - wire is a Verilog data-type used to connect elements

- when requirement of multiple nets is required, they can be bunched into a single wire.

wire [3:0] n0;



4-bit wire that can send 4 seperate values on each one of the wires

- Such entities with more than one are called vectors.

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- Illegal to redeclare a name already declared by a net, parameter or variable

Variables

as an abstraction of a data storage element and can hold values. ex - flip-flop

verilog data type reg : can be used to model hardware registers since it can hold values between assignments.

- reg need not always represent flip-flop because it can also be used to represent combinational logic.

Other data - types

- integer : general purpose - variable of 32 bits wide that can be used for other purposes while modelling hardware and store integer values.

```
integer count;
```

- time : variable is unsigned, 64-bits wide and can be used to store simulation time quantities for debugging purposes.
- real time variable simply stores time as a floating point quantity.

```
time end_time;
realtime rtime;
```

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vreal

can store floating point values and can be assigned the same way as integer and reg

verilog strings through an example

reg [8*11:1] str = "Hello world"
// store 11 bytes.
reg [8*5:1] str = "Hello world"
// store 5 bytes, leftmost bits of string get truncates.
reg [8*20:1] str = "Hello world"
// store 20 bytes, leftmost extra bits padded with zeros.

∴ - Hello world
- world
- hello world