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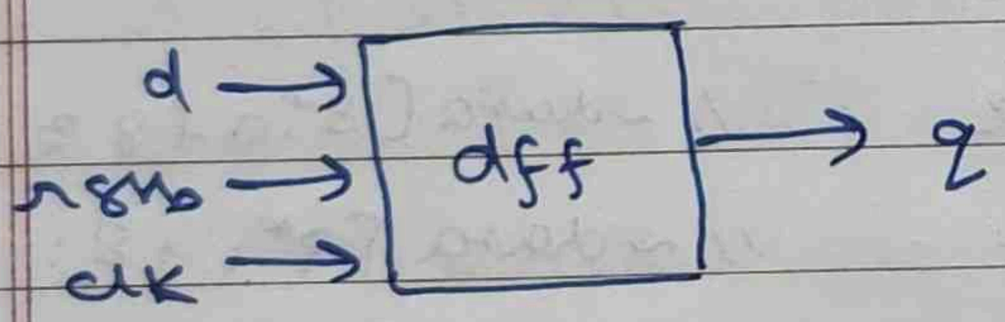
Verilog Module

- Should be enclosed within module and endmodule
- Name of module should be given right after the module keyword and an optional list of ports may be declared as well.
- Ports declared in the list of port declarations cannot be redeclared within the body of the module.

```
module <name> ([port-list]);
    // contents
endmodule
```

- You cannot have any code written outside a module.

Ex - D-flip flop.




```
module dff ( input d,
             input clk,
             input rstn,
             output reg q, );
always @ (posedge clk) begin
    if (!rstn)
        q <= 0;
    else
        q <= d;
end
endmodule
```

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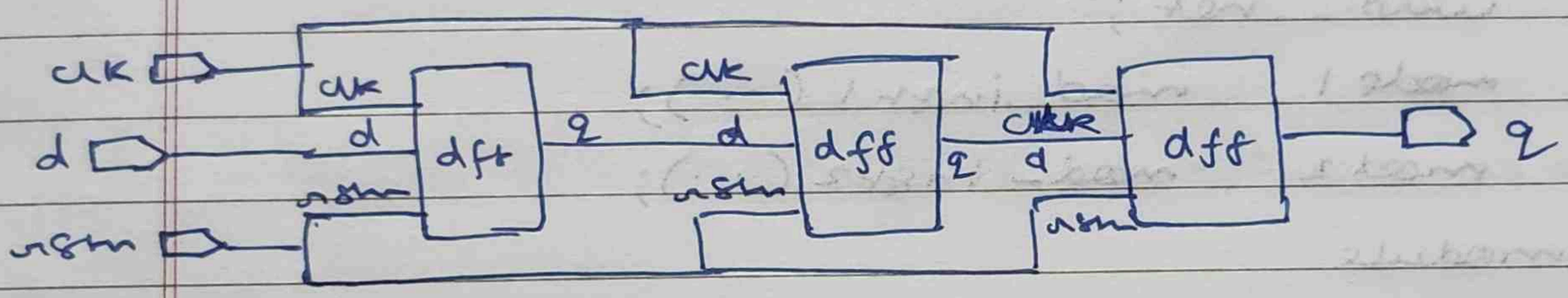
Purpose:

- Module represents a design unit that implements certain behaviour characteristics and will get converted into a digital circuit during synthesis.
- Any combination of inputs can be given to the module and it will provide a corresponding output.
- Allows the same module to be reused to form bigger modules that implement more complex hardware.

ex- can be chained to form a shift register.



Top-level module

for example, Sub modules like mod3 inside mod1 and mod4 inside mod2 Anyhow all these are included in the top level module when mod1 and mod2 are instantiated. in module design.

```
module mod3 ([port_list]);
    reg c;
endmodule.
module mod4 ([port_list]);
    wire a;
endmodule.
```

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```
module mod1 ([port_list]);
    wire y;
    mod 3    mod_inst1 (..);
    mod 3    mod_inst2 (..);
endmodule.

module mod2([port_list]);
    mod 4    mod_inst1 (...);
    mod 4    mod_inst2 (..);
endmodule

// Top level module
    module design ([port_list]);
        wire _net;
        mode 1    mod_inst1 (..);
        mod 2     mod_inst2 (...);
endmodule
```

test bench top level

The design is instantiated and called DO inside the testbench module.

```
module testbench;
    design d0([port_list_connections]);
endmodule.
```

Hierarchial names

design.mod_inst1 // access module instance mod_inst1

design.mod_inst1.y // access signal "y" inside mod_inst1

design.mod_inst2.mod_inst2.a // access signal "a" within mod4 module

testbench.d0._net;

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