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Verilog operators

- **Arithmetic**

a + b	plus
a - b	minus
a * b	multiplied
a / b	divided
a % b	modulo
a ** b	power of b

- **Relational**

a < b	less than
a > b	greater than
a <= b	less than equals to
a >= b	more than equals to

- **Equity**

a === b	a equal to b, including x and z
a !== b	a not equal to b, including x and z
a == b	a equal to b, result unknown
a != b	a not equal to b, result unknown

- **Shift**

  - Logical shift : << and >>
  - Arithmetic shift : <<< and >>>

Teacher's Signature:

- Logical

a && b (evaluates to true if a and b are true)

a || b (evaluates to true if a or b are true)

!a (converts non-zero to zero, and vice versa)

→ x will remain x

- Bitwise

This operator will combine a bit in one operand with its corresponding bit in the other operand to calculate a single bit result.

&	0	1	x	z
0	0	0	0	0
1	0	1	x	x
x	0	x	x	x
z	0	x	x	x

|	1	0	x	z
1	1	1	1	1
0	1	0	x	x
x	1	x	x	x
z	1	x	x	x