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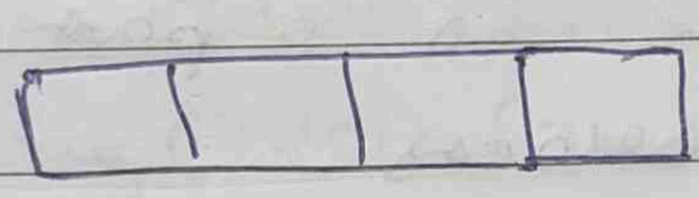
Scalars and Vectors

net or reg declarations without a range specification is considered 1-bit wide and is a scalar. If a range is specified, then the net or reg becomes a multibit entity known as a vector.

vector	scalar
wire [3:0] no	wire n1
reg[3:0] do	reg d1



[range gives ability to address individual bits in a vector.

```
wire [msb:lsb] name;
integer my_msb;

wire [15:0] priority
wire [my_msb:2] prior; // illegal.
```

- lsb value can be greater than, equal to or less than msb value.

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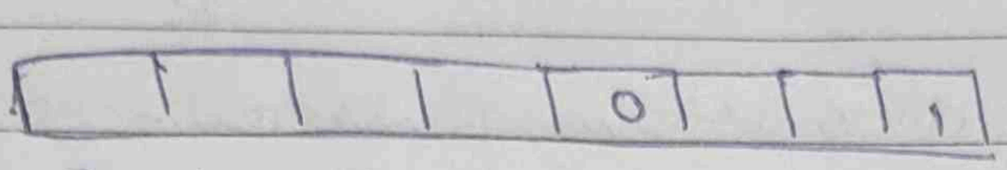
Bit selects

addr 


```
reg [7:0]   addr ;
addr [0] = 1;
addr [3] = 0;
addr [8] = 1;
```

Part select

A range of contigous bits can be selected and is known as a part-select.
Two part selects.

- constant
- indexed.

```
reg [31:0]   ddrr;
addr [23:16] = 8'h23;
// bits 23 to 16 will be replaced by
the new value 1h23 → constant
    part-select.
```

[<start-bit> + : <width>]

// increments from start-bit

[<start-bit> - : <width>]

// decrements from start-bit

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Ex-

```
module des;
    reg [31:0] data;
    int i;

initial begin
    data = 32'hFACE_CAFE;
for (i=0; i<4; i++) begin
  $ display ("data[8*%.0d+:8] = 0x%.0h",
                data[8*i+:8]);

end
  $ display ("data[7:0] = 0x%.0h", data[7:0]);
  $ display ("data[15:8] = 0x%.0h", data[15:8]);
  $ display ("data[23:16] = 0x%.0h", data[23:16]);
  $ display ("data[31:24] = 0x%.0h", data[31:24]);
```

Simulation log

```
ncsim> run
data[8*0+:8] = 0xfe      // ~data[8*0+8:8*0]
data[8*1+:8] = 0xca      // ~data[8*1+8:8*1]
data[8*2+:8] = 0xce      // ~data[8*2+8:8*2]
data[8*3+:8] = 0xfa      // ~data[8*3+8:8*3]

data[7:0] = 0xfe
data[15:8] = 0xca
data[23:16] = 0xce
data[31:24] = 0xfa
ncsim: *W, RNQUIE: Simulation is complete.
```

Teacher's Signature:.....