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Verilog

Syntax

- Case sensitive so var a and var A are diff
- Comments (// or /* */)

Number format

[size]'[base_format][number]

size - written only in decimal to specify number of bits in the number.

base_format - can either be decimal ('d or 'D) hexadecimal ('h or 'H) and octal ('o or 'O)

number - specified as consecutive digits from 0,1,2 .. 9 for decimal base format and 0,1,2..A.. F for hexadecimal

Ex 3rd

- Uppercase letters are legal for number specifications when base format is hex

Ex - 3'b010; // binary

8'h70; // hex

16'h cafe; and 16'h CAFE; (valid)

unsized

- Numbers without base_format specifications are by default decimal
- Numbers without size have a default number of bits depending on type of simulator

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Negative

- Negative numbers specified by placing - sign before the size of a number. Illegal to have - sign between base - format and number.

Strings

Sequence of characters enclosed in double quote " "

Identifiers

names of variables so that they can be referred later on.

made of alphanumeric characters (A-Z) (a-z) (0-9), underscores _ or dollar sign $ and are case sensitive.

- cannot start with digit or dollar sign.

integer vara_a ;
integer v$ar_a ;
integer var23_g ;
} valid

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