

Varilag assign statement

The assign statement uners any unine or other similar unine like data-types can be driven continuously uim a value.

total the same below to the property of the same Below the

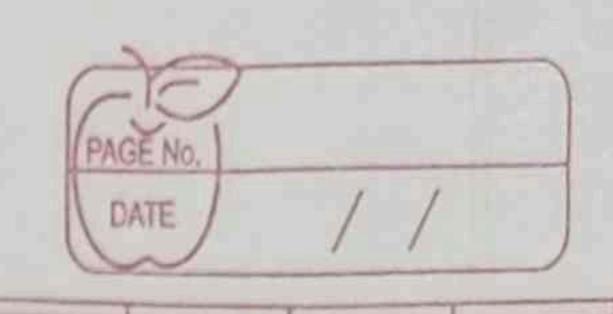
Assign syntax:

[assign < not_corpression?]
= [drive = 8+rength] [delay]
< corpression of different signals on constant
value >.]

- Etarts with key word assign
- · signal name union can be simen a single signal on a concatenation of different signals
- · drive strongth and delay are optional and one mostly used you dataflow modeling than synthesizing into real flow.
- expression on signal an the right hand side of expression of reks on the left hand side

LAND MARKE MALLEN SENDS - MARKEN

Delay values are held you specifying delays you gotes and one used to medal to be a gotes and one used to medal the min of the conditions are near that dicatars when and second to be assigned with the enducted one.



Rulas

- · LMS should always be scalar or rector not an a concatanation of uscalar as ugeton nets and vouser a scalar as voctor regisser.
- · RHS can consain scalon on voctor registers and Junction cours.
- · whenever any operand on me kns changes in value, en min be updated min me new value
 - assign statements are also called assignments and are always continuous active

lagic gates. Example - vsed seen windering (Md file me bot dunger) 2/5/10

Contract Of the moderate and the

It is illegal to drive or assign reg type variables with an assign statement. This is because a reg variable is capable of storing data and does not require to be driven continuously, reg signals can only be driven in procedural blacker like initial ed = 1.69. and almays.

Implicit cominace assignment.

mire [1:0] carine : so : mile accident assign a = x By; // explicit. mine [1:0] a = oc & y; // Implicit