Introduction to FPGA

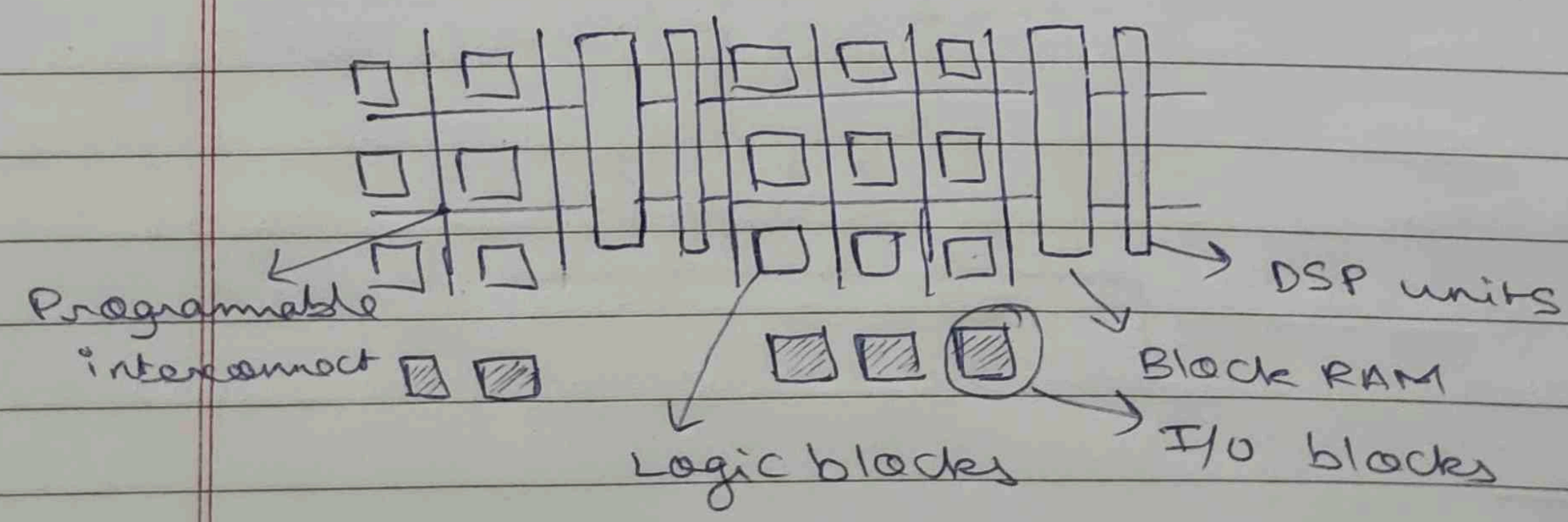
(e-yantra session)

PLD (Programmable Logic Device (PLD):

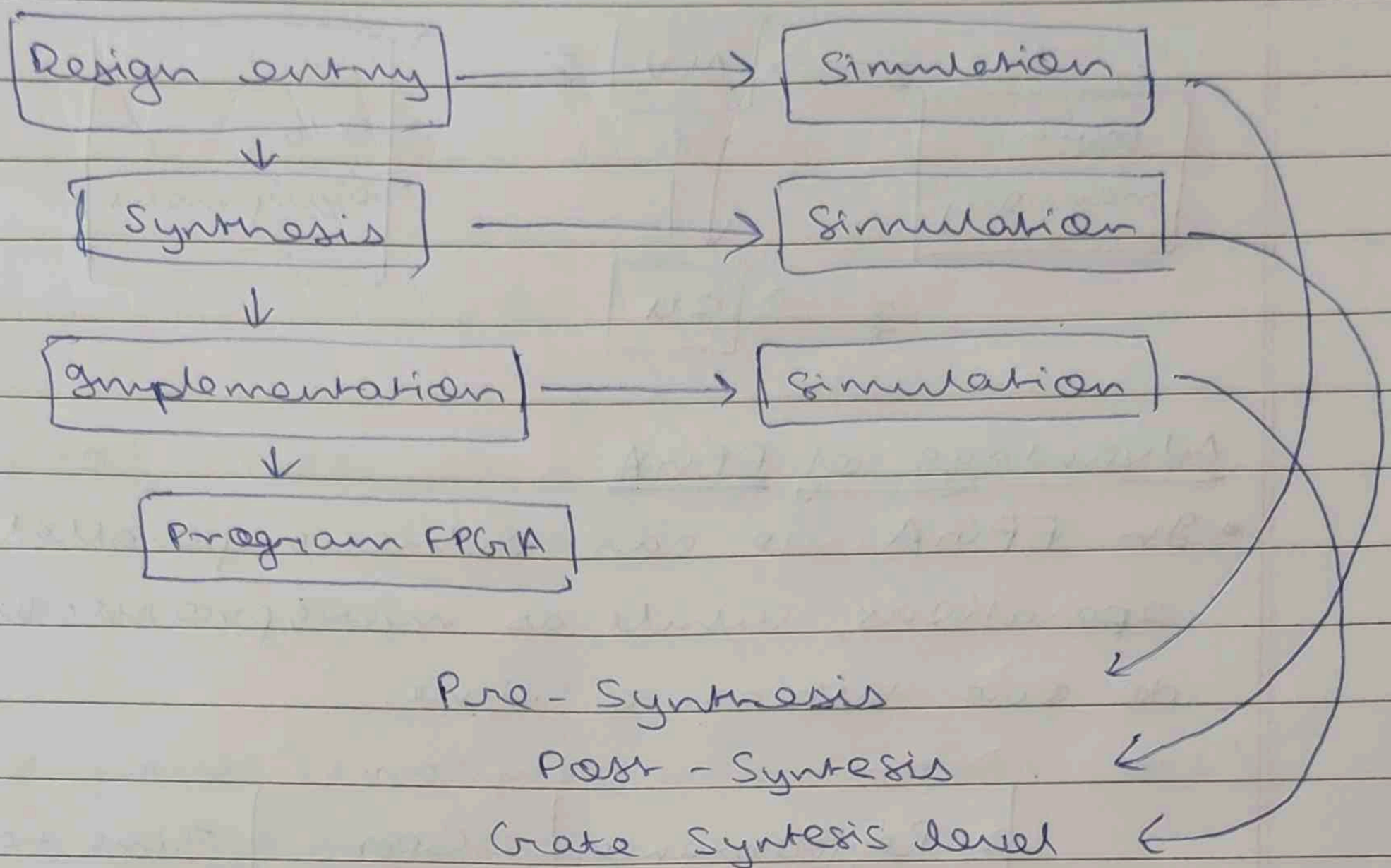
- used to build reconfigurable digital circuits
- has an undefined function at the time of manufacture.
- configuring a PLD changes the connections made between the logical elements in the device.
- PLDs : PAL
  PLA
  CPLDS
  FPGAs

Field-Programmable Gate Arrays (FPGAS)

- Array of logic elements (LEs) or logic blocks (LBs) or configurable logic blocks (CLBs)
- Configured in the field
- Logic blocks, I/O blocks.
  Block RAM , DSP units.



FPGA design flow:



FPGA Simulation flow:

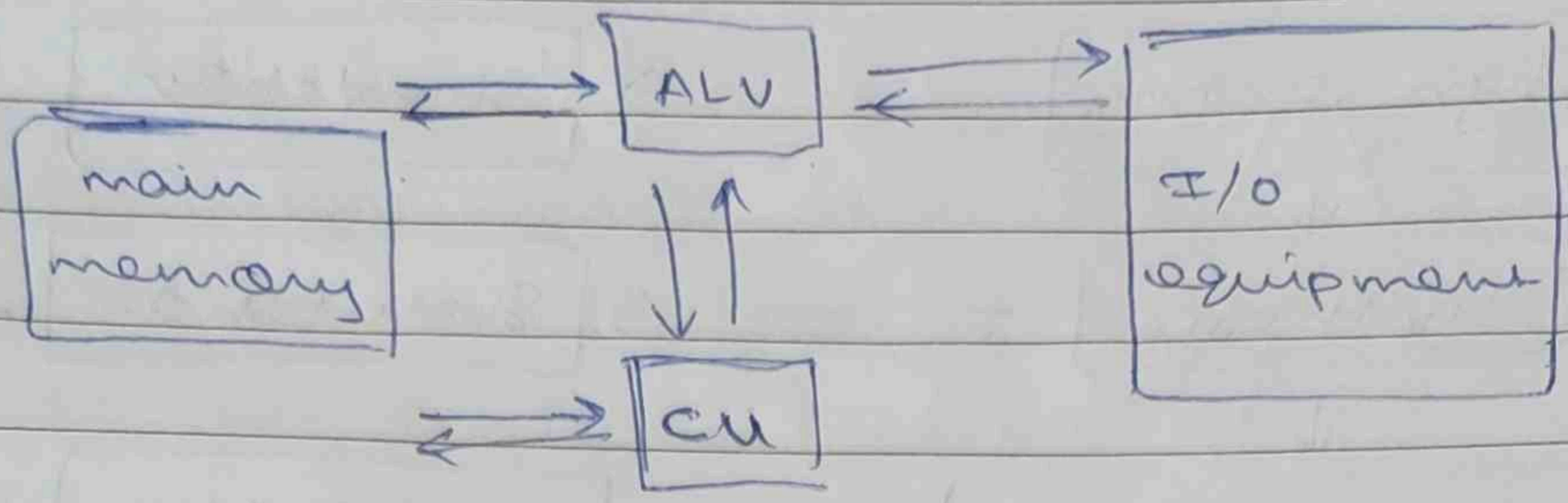
Full - custom and semi - custom design

1) Full.
   - Transistor - level customization
   - Granular control over performance
   - Costly
   - Time to market is high
   - Ex - ASICs (Application specific ICs)

2) Semi
   - Use of standard library components
   - Using half Adder to create full adder
   - Cheaper in comparision
   - Time to market is less
   - FPGA application

μP

Simplified architecture of microprocessor.



Advantage of FPGA

- In FPGA we can achieve parallel operations, while as microprocessor can do one task at a time.

	Performance	Cost	Time to market
μP/μC	Low	Low	low
FPGA	Moderate	Moderate	low
ASIC	high	high	high

→ Because the high-end and low-end processors in comparision to FPGA matter in better or lower performance.

Verilog HDL Basics

HDL (Hardware description language)

- VHDL - Very high speed IC hardware description language
- Verilog - verification and logic.

Verilog code structure

- Starts with module and ends with endmodule.

```
module module_name (port_list);
  port_declarations
  data_type_declarations
  functionality
endmodule
```

// Modelling styles.

1. Behavioral modelling
   - only functionality is defined, no structure
   - Synthesized circuit cannot be guessed

2. Structural modelling
   - Functionality defined, Synthesized circuit guessed easily

3. Dataflow modelling
   - Hardware is described in terms of the flow of data from input to output
   - Synthesized circuit cannot be guessed

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Data types

1. Net data type:
   Represents physical interconnect between components.

2. variable data type:
   Represents element to store data temporarily.

net → wire — Represents a node
net → tri — Represents a tri-state node
net → supply0 — Logic 0
net → supply1 — Logic 1

variable → reg — unsigned variables
variable → integer — signed 32-bit number
variable → real, time, realtime — Not synthesizable

Bus declarations

```
wire [7:0] out;
reg [15:0] q;
```

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// Continuous assignment Statements -

- Model the behavior of combinational logic by using expressions and operators.
- LHS must be a net data type
- Always active.

// Procedural assignment state -

1) initial block - executed only once
2) always block - executed sequentially

- Each always and initial block represents a separate process.
- Processes run in parallel
- Statements inside process blocks execute seperately.