Verilog initial block

Verilog statements are usually executed in a simulation sequentially.
Statements are placed inside procedural blocks - initial and always.

Syntax

```
initial
    [single statement]

initial begin
    [multiple statements]
end
```

Use: initial block is not synthesizable and hence cannot be converted into a hardware schematic with digital elements. Hence initial blocks do not serve much purpose than to be used in simulations.
These blocks are primarily used to initialize variables and drive design ports with specific values.

- Execution of an initial block finishes once all the statements within the block are executed.

```
module behave
  reg [1:0]  a, b;

  initial begin
      a = 2'b10;      // a will get value 2'b10 at 0ns
    #10 b = 2'b00;    // b will be assigned 2'b00
                      at 10ns
  end
endmodule
```

→ Delay of 10ns

— There are no limits to the number of initial blocks that can be defined inside a module.

$finish is a Verilog system task that tells the simulator to terminate the current situation.

```
initial begin
  ~~#$finish~~
  #30 $finish
end
```