

Building the project:

· idy py build # command you building the code

Flashing the code command:

idj. py - P PORT [- b BAUD] ylash

(PORT ? Stands for the Serial Part Number

@ ESP-32)

(BAUD & Atonds you the Bound Rate Criate of

information transfer to the ESP-32)

Example pours -

for Linux: /der/ tty USBO

for Macos: Iden/ cu. usbserial - 0001

for windows: / Con1#/2/3/...

checking posts:

for linux: donesq 1 grep try

for Macos! (der/w. *

for windows: (from Device manager)

Monitoring the output yronn ESP-32

use can achieve this by going into the project

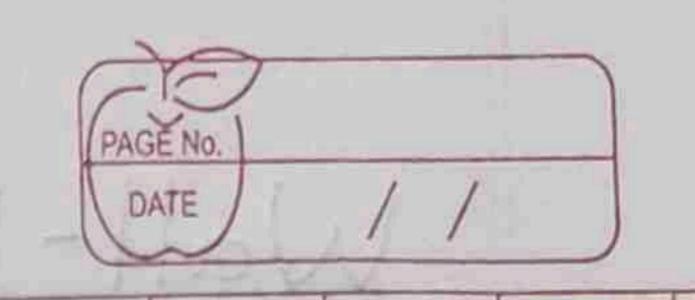
directory via the terminal and giving the

command:

1 3 17

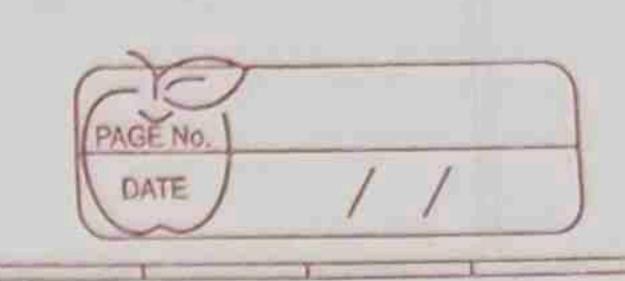
idf. py moniton

Teacher's Signature:....



LED (Light emitting diade) is a semiconductor device that amits dight when an electric current is passed through it.

Decimal	nex		
Larry Charles		44.45.070	
2	2	Convert	760 inte hor.
3 7	A 12 2 2 2 2 2		60
4-920	Secretary of the second	60/16 -> 3	
5	S	3/16 -> 0	
6	6		
7	30.930	·. (960), =	(300).
8 000			20 0000
9		Hex	
10		0	Binary
11	2	2	0000
12	C	3	0010
13		4	0011
14		S	0100
1 (6	010
			0110
	5 92 3 - Annie 10 - 2		0111
12227 12 1 2 2 2 1 1 1		8	1000
		9	1001
		A	1010
		B	1011
		C	1100
		D ,	1101
		E	1110
		F	1111
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SRA-der-Board includes:

- · Microcontroller (ESP32)
- · Mater drivers (TB6612FNG)
- a Push buttons
- " MPV and LSA
- anboard power management · OLED and serva marans
 - The first that the second of t

Micracontroller: Single Fritegrated circuit (IC) that is sypically used for a specific application and designed to Implement certain stasks. The state of the s

IDF -> IDF stands you 10T development framework.

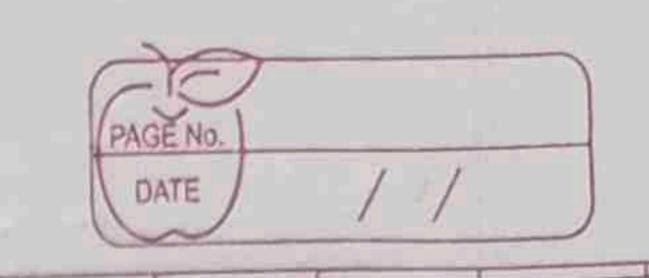
IDF is ESP'S i.e Espressif's our authoritically created official toolchain to work on and program build compile code on ESP based microcont voller

Buck conventor: - 9t is a voltage regulation, nointains a constant voltage avan mough the input voltage changes. S Converts input vallage to 5V.

AMSIII7: Coonverts input vallage to 3.3V

Motor Driver: [TB6612FNG]

IC used as a motor controlling device (as in adjustes the voltage applied to the motors).



ADC (Analog to digital convertours)

Vsed to convert an analog vigral to

digital form so that it can be read and

procassed by a microconstraller.

Analog signals

Continuous signals

Represented by sine Represented by square

warres.

Tuman voice, analog Compitars, optical drives

electronic devices

Continuous values Discontinuous values

Records sound wares Converse into a binary

as they are

worreform.

tree requires TOI LOUIST STREET STEET

Arocs Johnson a sequence when converting analog signals to digital they first sample the signal, then quantify it to determine the resolution of the signal and finally yet binary values and send it to the system to read the digital signal that aspects of AOC are its sampling nate and resolution.

ADC -> gnoundes 2 processes.

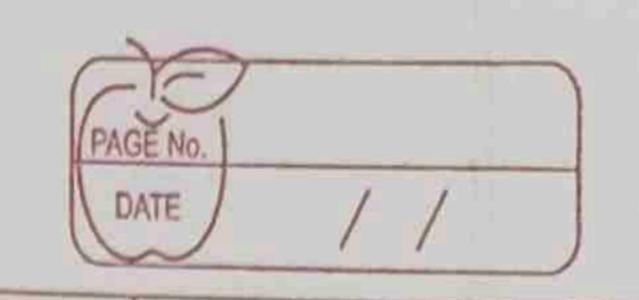
- · Sampling
- · Quantization.

Johns of continuous - sine signal in discrete

Johns. Sample is a piece of data taken

A STATE OF THE REAL PROPERTY.

Just the Delivery Land Control As I have



from the unale data which is cominnous in the time domain.

This discretization of analog signal is cauded sampling.

Quantization:

Rounding of the values which are approximately equal to the analog values. The method of sampling character a few points on the analog signal and then these points are joined to round of the value to near stabilized value.

the second with the second with the second second to the second s

The quantizing of an andag signal is done by

discretizing the signal with a number of

quantization levels duentization is representing

the sampled values of the amplitude by a

finite set of levels, which means converting a

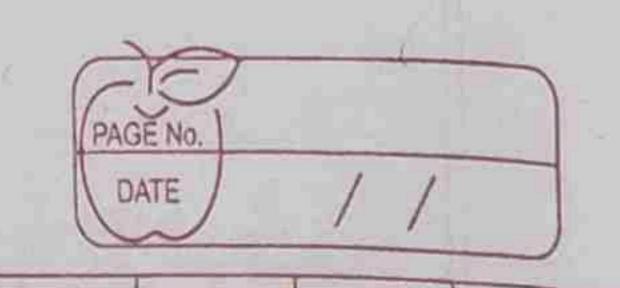
continuous amplitude sample into a discrete

time signal.

- No of quarrization levels = 2°

Orientizing a sequence of numbers produces a sequence of quantization occurs which is sometimes most modeled as an additive random signal could quantization raise because of its stochastic behaviour.

is its quantization voice pourer



LSA [Line senson among] AZI

LSA has set of LEO'S which and light and after reflection the light is absorbed by photo diado. Nom trere is a carch, tre reflection part, that is the reglection percentage are not same your subsite and black surgaces and then this becomes differentiating Jacton LEVI DE L'ARTER BOUNT PARTIE DE CONTRA LA CONT

The state of the second state of the second state of the second s

· Light from LED after reflecting from surjece yours on the reverse biased phorodiode · Should be kept close to the ground " photo diodo should be surrounded by a shield to minimize effect of ambient dight

Flores 128 State 100 State

1C LM 324 14 pin 10 consisting of your operational Amplifiers (op-Amps) in a single package · OP-Amps is a vign gain ampligier. Used to amplify ament with congrant vallage we need to increase the significance of very snow an photo diade. 4 Amplified outputs are RAW LSA SENSOR values from about 400 (BLACK) to 2000 (WHITE) -mapped from O(BLACK) to 1000 (WHITE) your convinience.

Défining constraints. CONSTRAINT LSA - LOW - 0 CONSTRAINT - LSA - HIGH - 1000

~	Communication protocols
	Communication
	Paraulel Serial
	8-bits are transferred. • word of 8-bits in
	in corresponding 8 channels, length is sent sequentially
	every chand transmits and is received alter all
	a bit and a byte of data 8-bits are sent and
	is recieved simultaneously but a sine , the bits are
	then assembled back
	inte one byte union
	is initial comme
	~ 810mm
	More connections, Ferrer connections
	theresone distanted cleans in
	Loss suitable since. More suitable
	signals
	a UH'Li-a.
	date
	devicer
	Start and show bit.
	caps one also used
	Eg-VART

Synchranaus

· clock vine is present

Eg - SPI, 120

UART (Universal Asynchronous receiver transmission).

Steps to follow:

- · Stant (Data line goes low you come bit
- · Dara (send dara bits)
- · Parity (send parity bit for error chocking)
- " Stap (send snoop is)

Erran detecting codes
Additional data added to a given digital mag

to help us detect if an erran accumed

during transmission of the message

Simple ex - parity check.

Parity - it contains enon number of 1 bits
on odd number of 1 bits

10011010 > Even 1's > Parity: 1

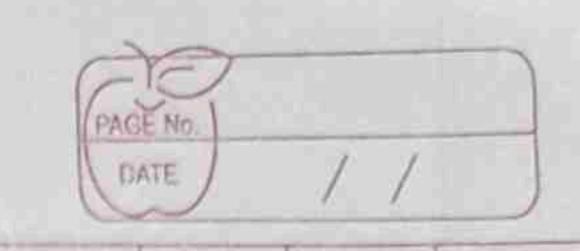
10111010 > odd 1's > Parity: 0

And the second of the second o

wanking -

- · Sender will calculate parity
- "Transmitter will transmit data
- * Receiver will receive
- · Receiver will check parity
- of garing marches & process dara

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Band note: note at which information is

transferred in communication channel

commonly used in serial communication

By serial port context, "9600 band" means that

part is capable of transferring a maximum

of 9600 bits per second.

trade and the first trade of the state of th

Required countigs you UART:

- · Regulatory bits (start and stop bits)
- · Band vate
- · Parity bit

Advantages

- · Consigurable spead
- " No need of dock wine
- · Parity bit ensures basic error checking

Disadvantages

- · Size of data frame is limited
- " Less speed of data transmission
- « No conjunction about successful recieving of data from reciever to transmitter.

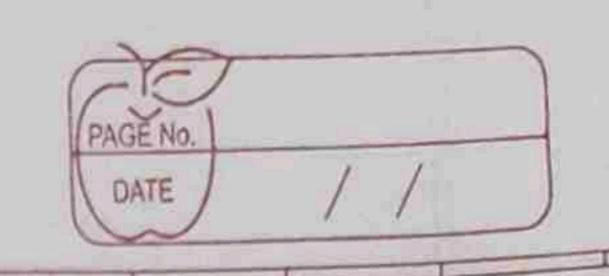
Steps Jon UART communication

Transmitting VART receives data græn the data bus in parallel.

William the committee of the state of the st

Transmitting UART adds the start, paning and stoop bit to the date packet.

) The ontire packet is sent from the thoughing



UART to receiving UART serially. Using the configured band nate the nocciving UART samples the dara packed.

UART converts the dara back to its configural form and then transfers it to the dara bus where it can be used or visualized.

I2C (Inter-integrated circuit)

- · Each bit of data is sent through a digital
- o therefore 8 pins one required you 8 bits of
- can't connect more devices.

-> Lines/pins involved in I2C comminication

SDA (Serial Data) - line you mastrer and stares

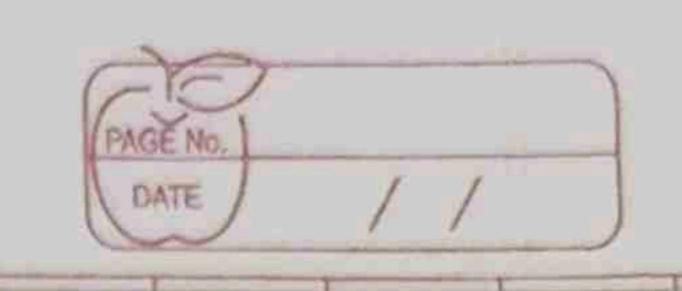
The Later Andrews of the American State of the American State of the American State of the State

SCL (Sevial clock) - Line that carries the clock

· Izc is serial communication, data is transferred bit by bit along single wire · Clock signal is always controlled by the maxin.

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Teacher's Signature:....



Working—

T2C master sends out one grow bit

T2C master calls out to a specific T2C stand

Using a 7-bit address

Slave corresponds

Master sends specific command to slave

Slave answer's master's request.

Master acknowledges the 18t bit of data

before slave continues delivering info

Slave now sends the next byte of data

After receiving data master ands the commiscation

Address frame - A 7 or 10 bit sequence unique

to each slave than identifies the slave when

Read/write Bit! - A single bit specifying whoten the marker is sending data to the Mare (John voltage) on requising data from it (high worldge)

the master wants to talk to it.

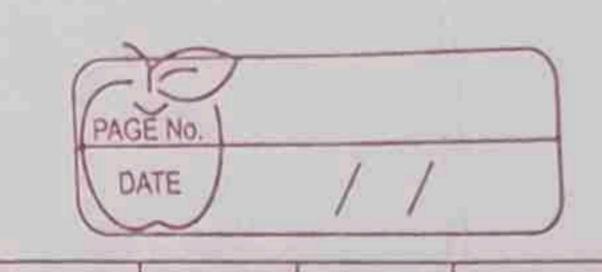
ACK/NACK Bit: Fach frame in a mostage is

Johanned by an acknowledge (no - acknowledge bit.

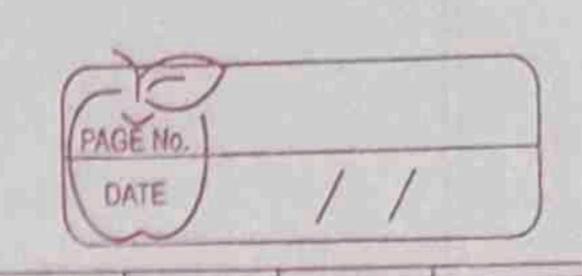
8) an address frame on data frame was

successfully received, on ACK bit is returned
to the sender from the receiving data

Stort condition & SDA sine smitches from a high voltage level to a low voltage level before the SCL sine smitches from high to low.



Stap coondition! SOA line suitches from a low vollage level to a night workings level agree the SCE dine Duritches from dow to high STEPS OF IZC tnansmission: Master Bends start condition every connected Slave. by suitching SDA line Master sends For 10 bit Address of stance to grant commication, Each slave companes address, if address match sand back ACK bit by pulling SDA line down for one bis. If address don't match Dave dances SDA line high 4) Magter sends on receives dara 5) After each dara frame has been transperred the recairing device returns another ACK bit to the sender to acknowledge successful receipt of the frame. Stop - matter sends a strop condition to the stone by suritaring SCL high begare suitaing SDA high. Mumple nasters min numple slaves. line is down, wis means that another naster has commed of the bus, and the master Should wait to send the message. If me SDA vine is high men its vage to Inansmit the nessage



THE RESERVE OF THE PARTY OF THE

SPI (Serial peripheral interface)

PIN interjace:

				SCK >	Serial dock
S	CKI	>	SCIS	MOSIA	master out
M	051		NOS1		Stare in
~	1180		MISO	M150 >	master in
	cs	>	CS		Dans our
Mas	ren		Slave	e SS)cs ->	Stane select/
					Chip select.

It is serial and synchronous interface

How SPI works

The clock: commication always initiated by matter, bus master commods the clock, using a frequency supported by the stone device.

One bit of data is transferred in each

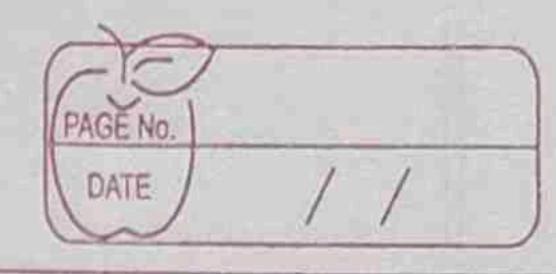
clock cycle, so speed is determined by threamency of dock cycle.

and the about the same of the same of the same

MOSI and MISO

Master sends dara smough MOSI in most significant bit Slave sends back to master through MISO in least significant bit

Starre select: " Master can chaose which slave it wants by serving the slave's CS/SS line to low vallage. · en idle dine is kept at high vollage IZC doesn't have slave select lines like SPI voo it makes comminication by oddressing. - Steps og data tnansmission The state of the s master outputs the clock signal 2) master suntenes me SS/CS pin to Tow voltage Magher sends dans one bit at a time mængh mosi dina chaquer ends bebeen ai senegaer fl enie 021th approve A TRANSPORT OF THE STATE OF THE Muniple slaves: · Single masten - single slave single masten - multiple sauce >> 2 ways Independent o master win multiple SS pins Slave compig so saves connected in parallel master with one SS pin despendent SO Mones commer daisy-chained going sons



	Advantages
	. NO Start and Stop bits, so dara can be
	streamed continuously without interruption
	· Not complicated slave addressing
	· fast data thansjer
	· Separate MOSI and MISO lines no dara can
	be sent and received at same time.
	Dis advantages
	· vees four unives
	· Now acknowledgement that data has been
	successfully received (12c has this)
	· No yann og enar cheeking
	· ony allows single master
	VART SPI IZC
رعمنده	UART SP1 IZC word 2
	used 2
	used 2 4 2 ed upto 115200 band upto 10Mbps upto 5Mbps usnally 9600 band
	used 2 4 2 ed upto 115200 band upto 10Mbps upto 5Mbps usually 9600 band
Masc	ed upro 115200 band upto 10Mbps upto 5Mbps usually 9600 band Asynchronous Synchronous Synchronous Seial Serial untimited
Masc	used 2 4 2 ed upto 115200 band upto 10Mbps upto 5Mbps usually 9600 band Asynchronous Synchronous Synchronous Serial Serial Serial
Masc	ed upro 115200 band upto 10Mbps upto 5Mbps usually 9600 band Asynchronous Synchronous Synchronous Seial Serial untimited
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