Verilag initial black Verilog statements are usually executed in a simulation segnemially. Statements one placed inside procedural blacks - initial and always. Land and the second services Sympac initial [single shatement] initial begin [muriple statements] and only organizate and with the organization margarden et diese Use: initial block is not synthesizable and hence cannot be converted into a hardware schematic with digital elements. Hence initial blacks do not seme much purpose than to be used in simulations. These blacks are primarily used to initialize variables and drive design parts with specific values. · Execution of an initial black ginishes once au me gratements within me block are exe cuted

madule behave rag[1:0] a, b; 11 a mill get value 2' bio at ons initial begins a = 21610; 11 buin be assignmed 21 b00 #10 b= 21 b 00; at 10 ms > Delay of 10 ms end madule There are no dimins to the number of initial blackes that can be defined inside a module. A DINE A DINE \$ yinish is a verilag system task that talk the simulator to terminate the current situation. Let be be a second and the second of the sec initial begin a true + & dimension location which stream and a #30 \$ ginish bone mencestale de la comina de maior de sustant abstractive that he said a made and are been as a lost said and the material mesons replaced straint business and and and