Wilkinson power divider

EERF – 6396

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1. Introduction

Objectives:

a. Design, simulate and build 3 dB Wilkinson power divider with f_o = 2.5 GHz
b. Compare the design against physical results and Axiem simulation

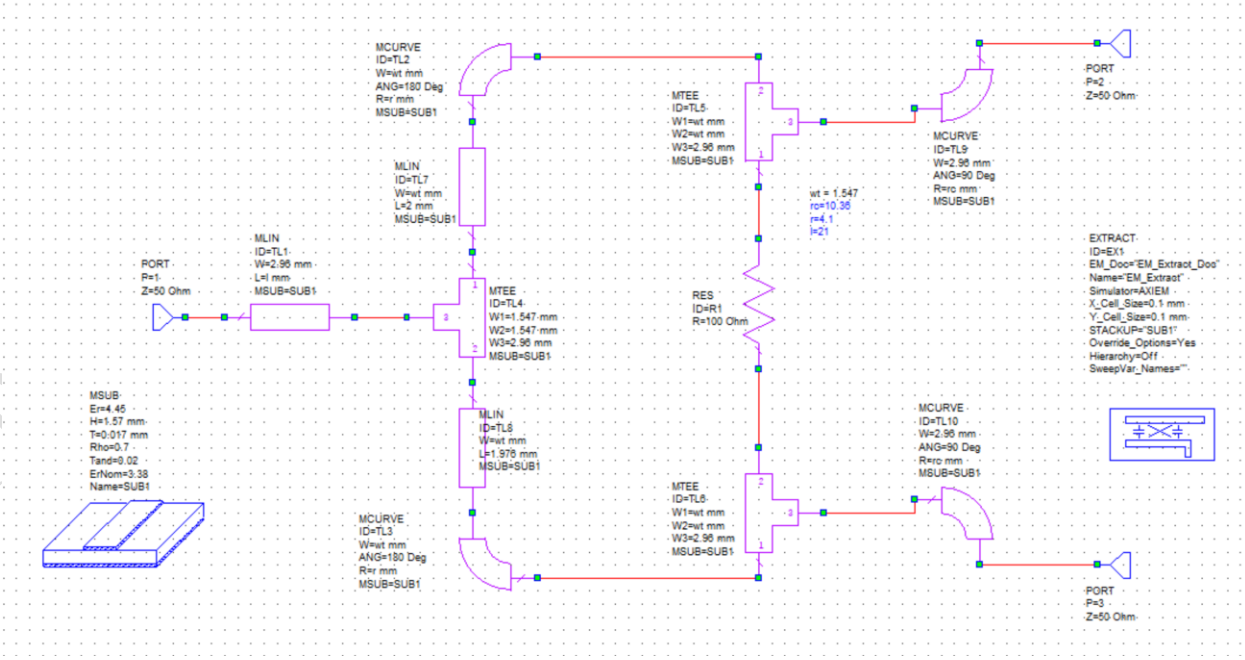
2. Significance

The Wilkinson power divider is an important microwave circuit. It can achieve isolation between the output ports while maintaining matched conditions at all ports. It is a reciprocal device and made up of only passive elements hence it can also be used as a power combiner.

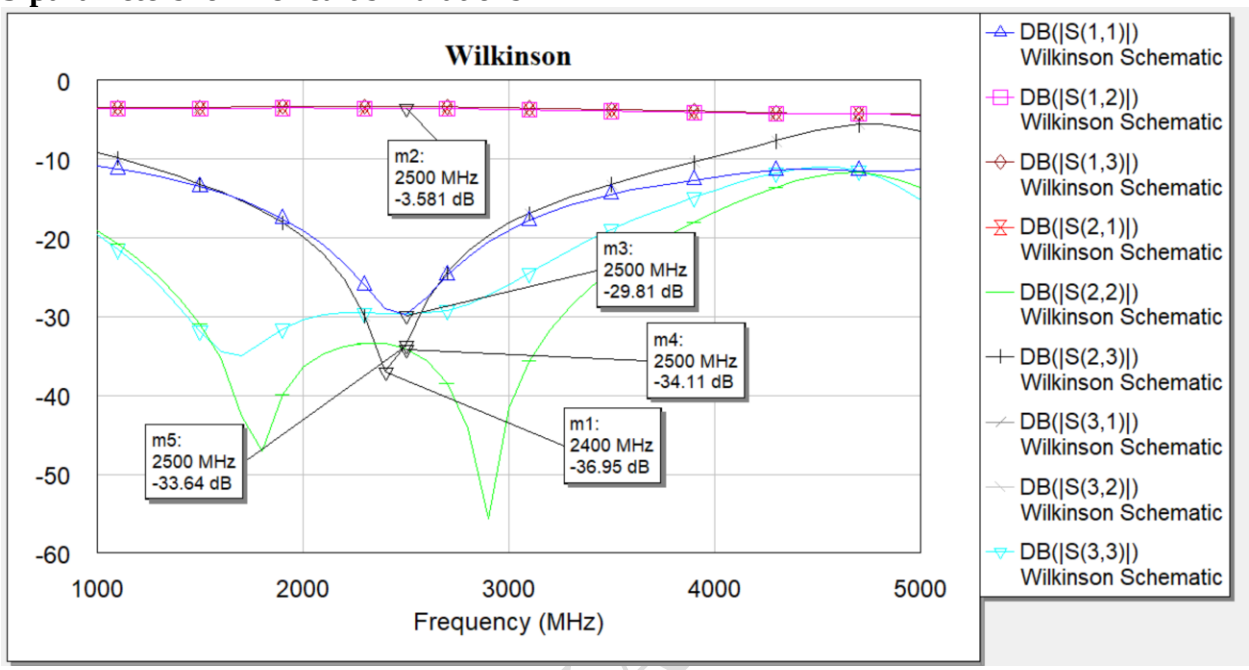
3. Design -Omkar Kulkarni

1. The design goal is to build a Wilkinson power divider with center frequency of 2.5 GHz.
2. Accordingly, the values of width, λ_{eff} and length were calculated from Tx line tool in AWR MWO
3. The Wilkinson power divider analysis is accomplished with even odd mode analysis
4. The resultant $Z_0\sqrt{2}$ line width are obtained from Tx line tool
5. Layout of the circuit is of utmost importance in the case of Wilkinson power divider to avoid coupling between the output lines and avoid phase changes in the output. The output lines should quickly diverge from the $2Z_0$ resistor for this.
6. The circuit was built in MWO and tuned for the required results
7. The design goals were met at the resonant frequency
8. Axiem mesh was built and the performance was noted
9. The circuit was built, and the S-parameters were measured in the lab

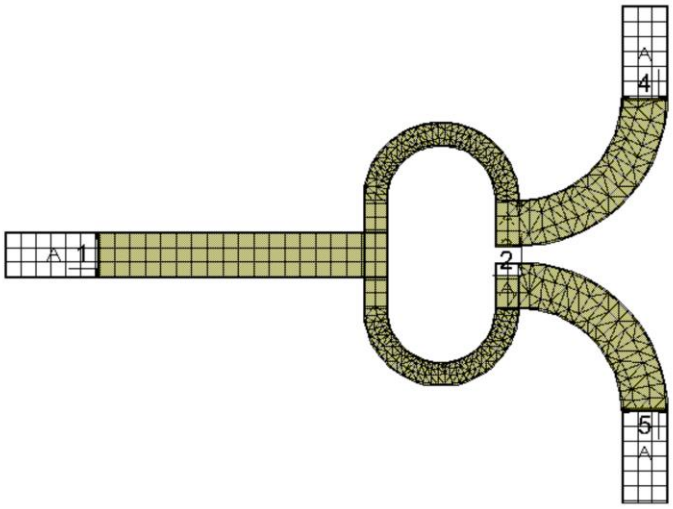
- **Schematic**



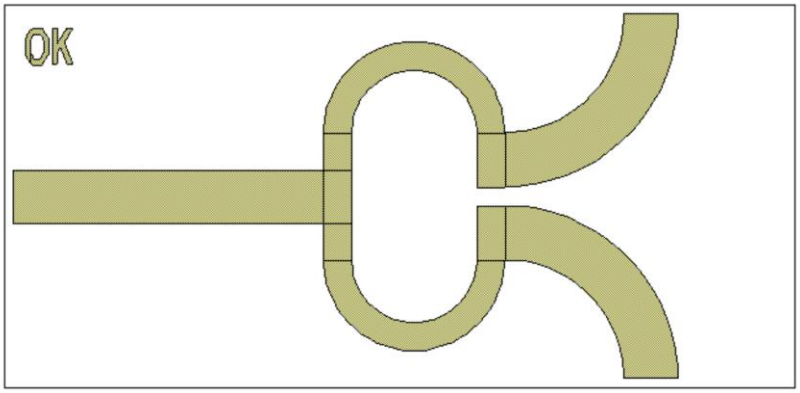
- **S-parameters form circuit simulations**



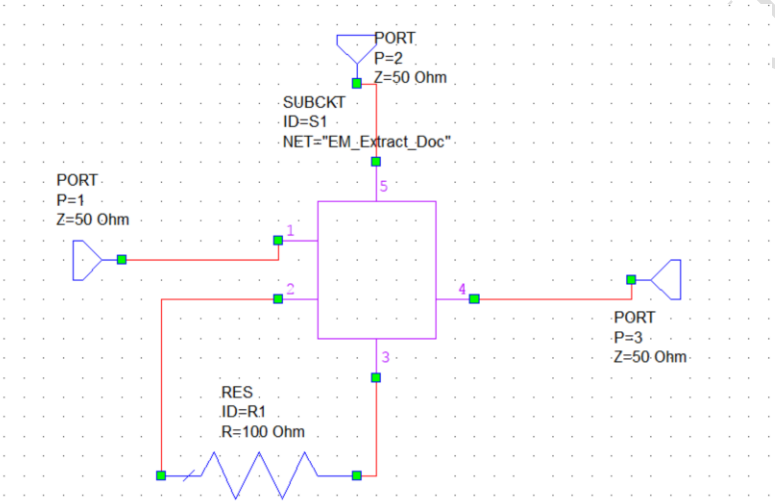
- **Axiem Mesh**



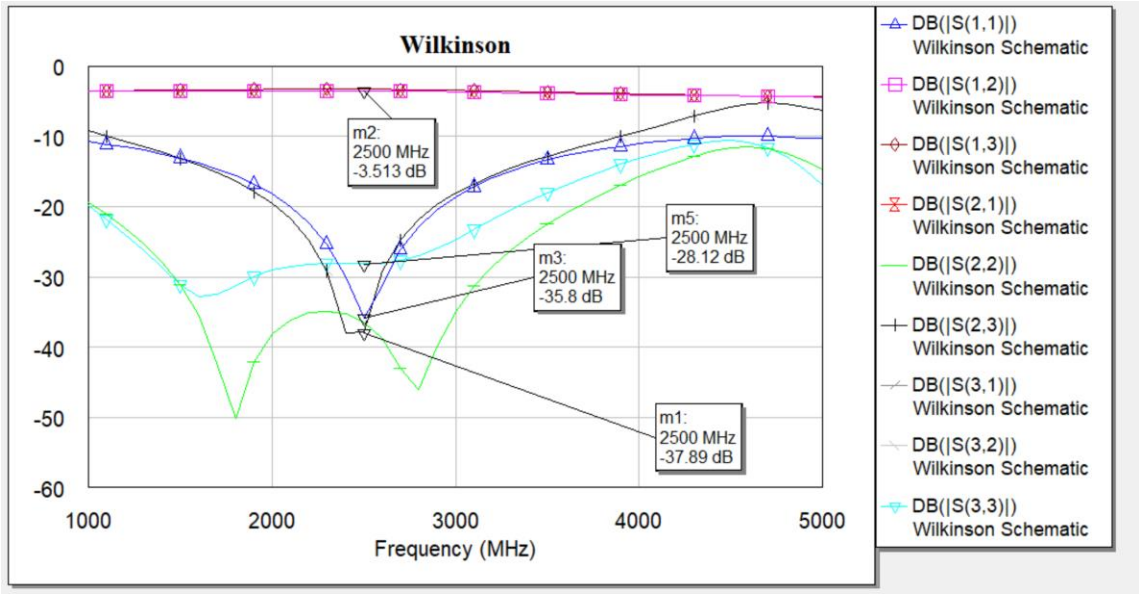
- **Board layout**



- **Sub circuit simulation for testing the effect of 100Ω resistor**



- **Axiem mesh simulation results**

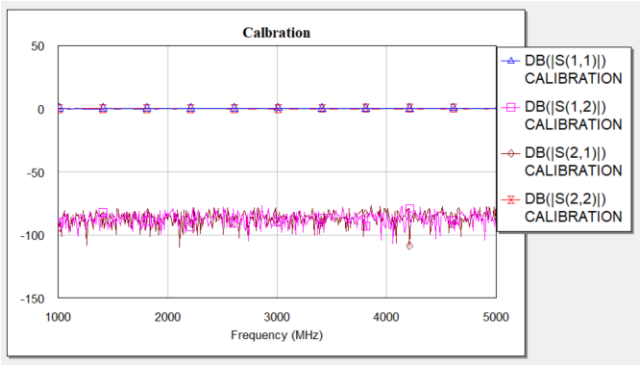


- **Summary:**
  The results obtained from the circuit simulation and Axiem simulation are close to each other. Initially the design values didn't lie near the objectives. After tuning the design goals were achieved

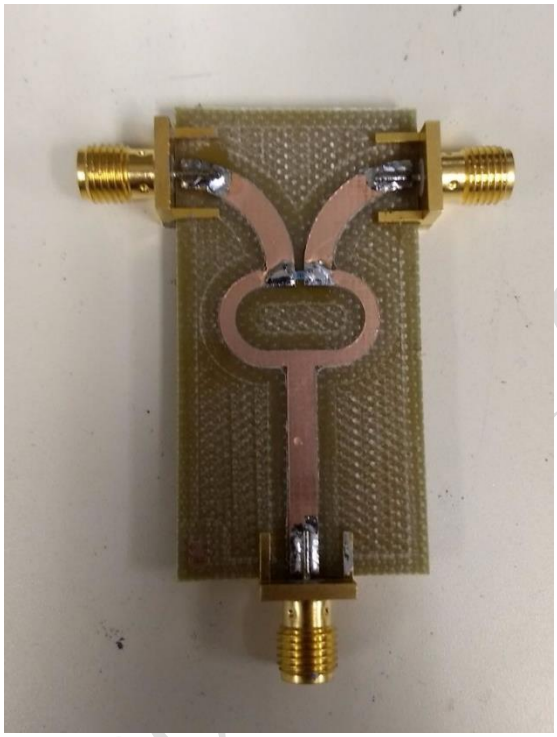
4. Lab Measurements

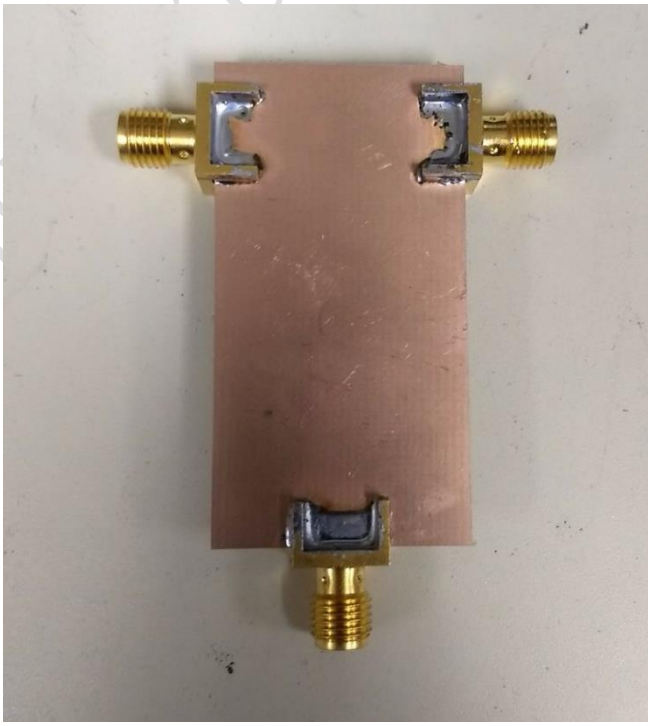
Thickness	14 mm
Length	48.9 mm
Breadth	26.1 mm
50Ω line width	2.97 mm
70.7Ω line width	1.71 mm

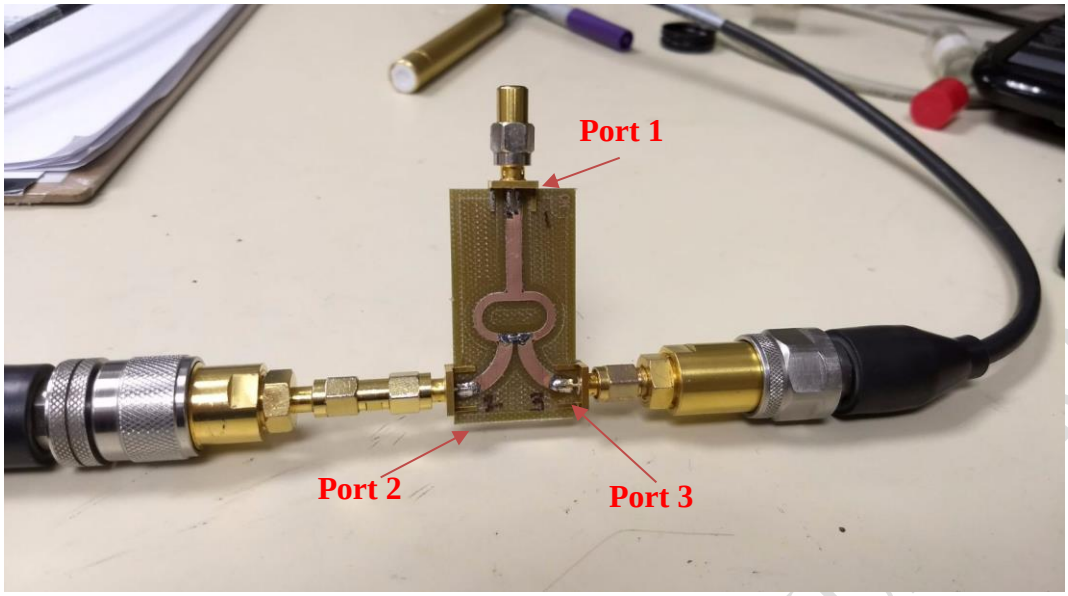
- **VNA Calibration**



- **Lab setup photographs**

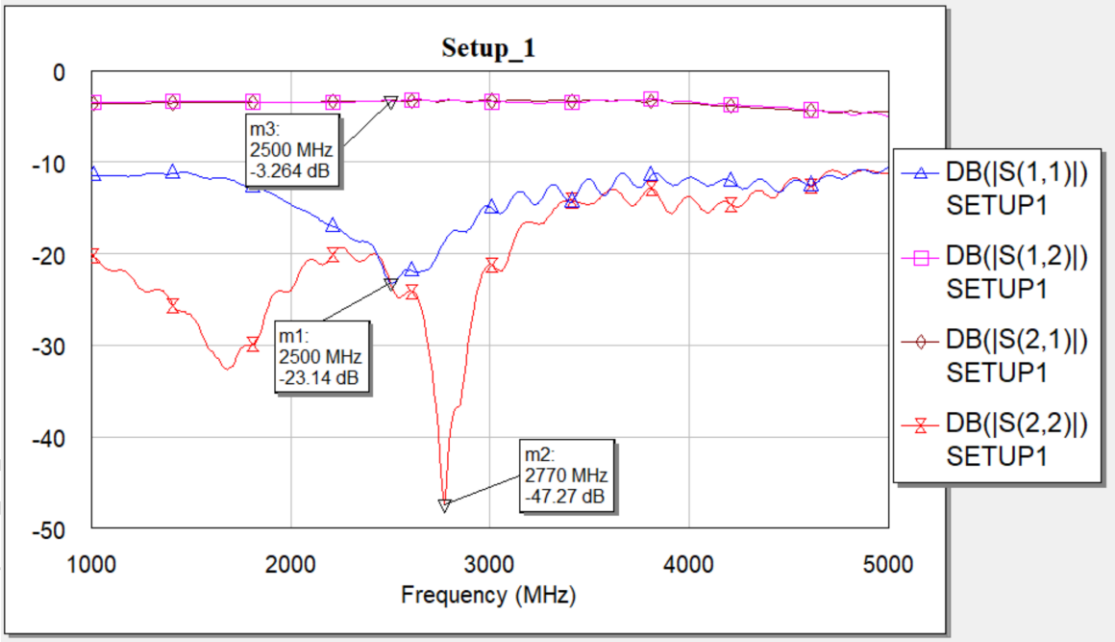






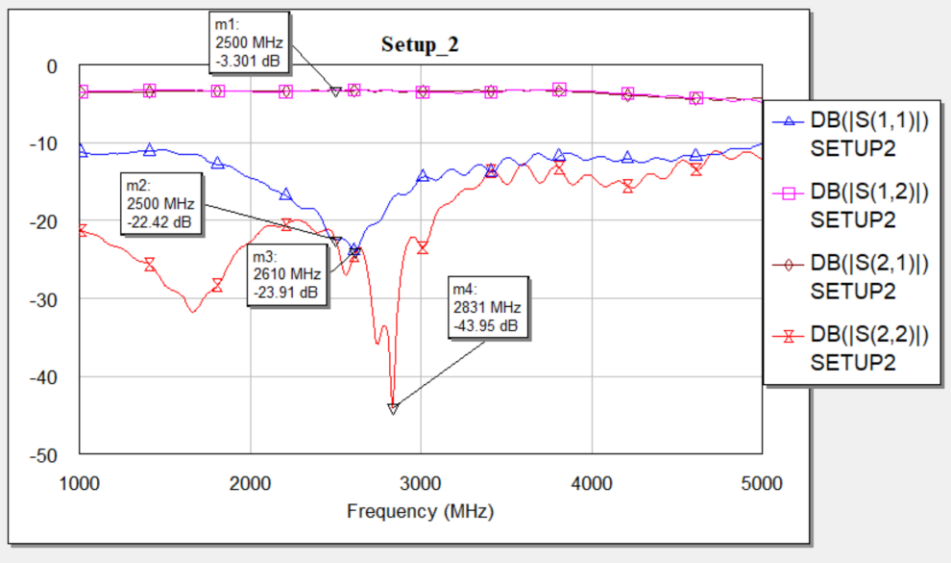
- **Setup 1:**

Port 1 of VNA connected to port 1 of board (ref pic) and port 2 of VNA connected to port 2 of board. Port 3 of board terminated in $Z_0 = 50\Omega$



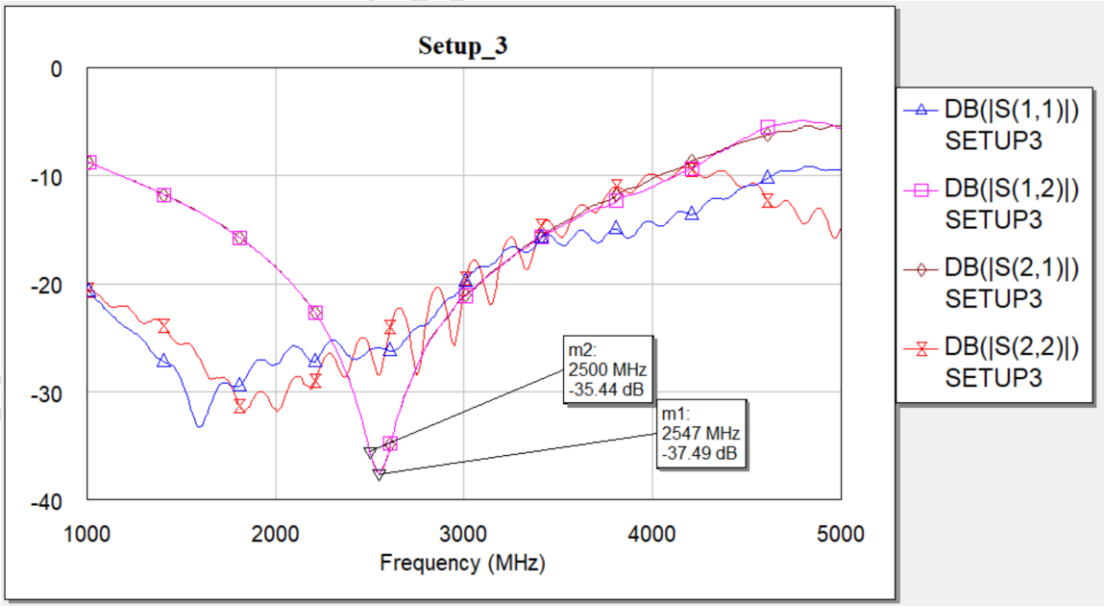
- **Setup 2:**

Port 1 of VNA connected to port 1 of board (ref pic) and port 2 of VNA connected to port 3 of board. Port 2 of board terminated in $Z_0 = 50\Omega$

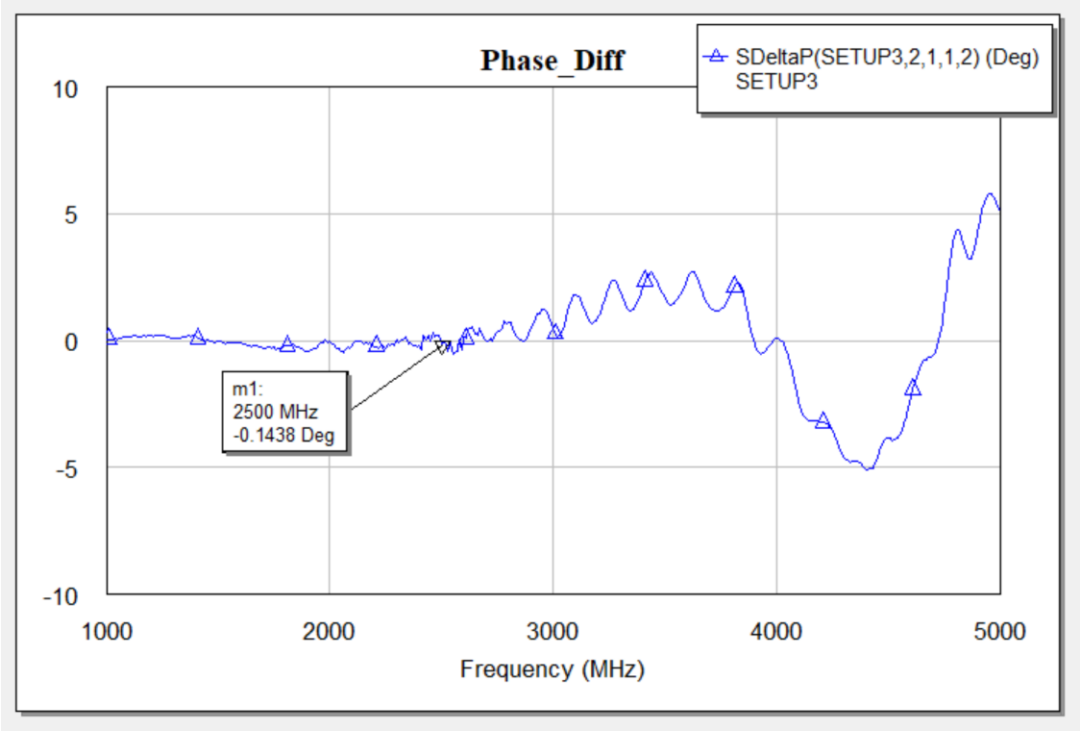


- **Setup 3:**

Port 1 of VNA connected to port 2 of board (ref pic) and port 2 of VNA connected to port 3 of board. Port 1 of board terminated in $Z_0 = 50\Omega$



- **Phase difference between output ports**



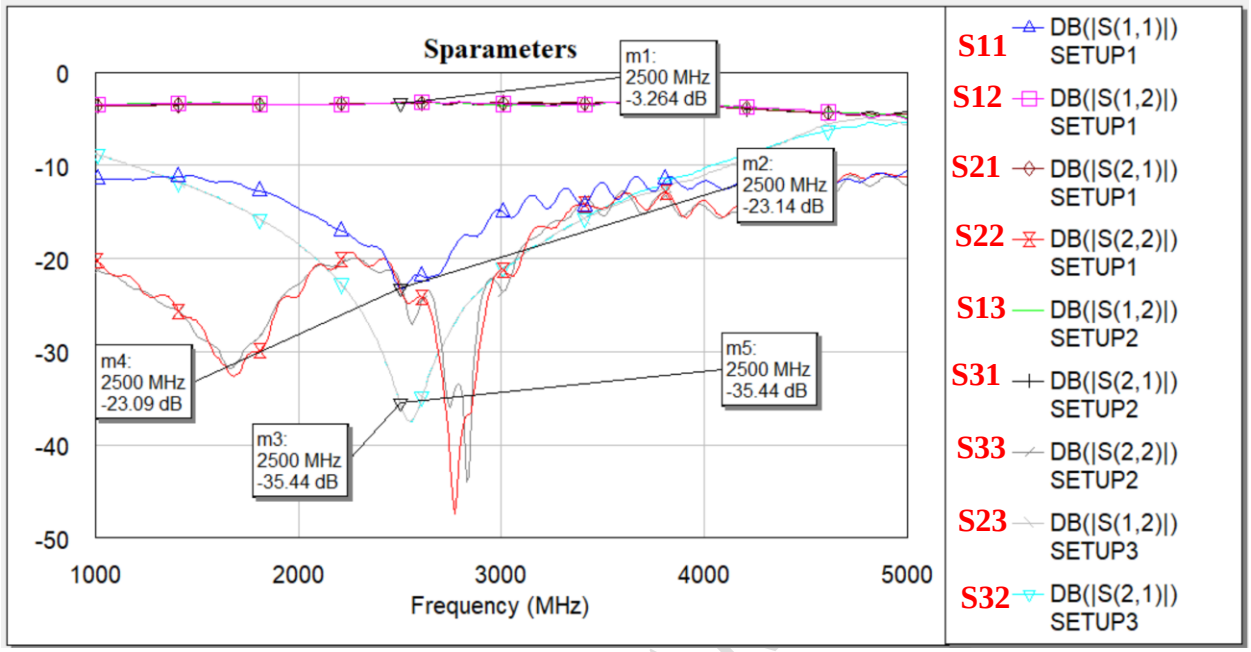
Summary:

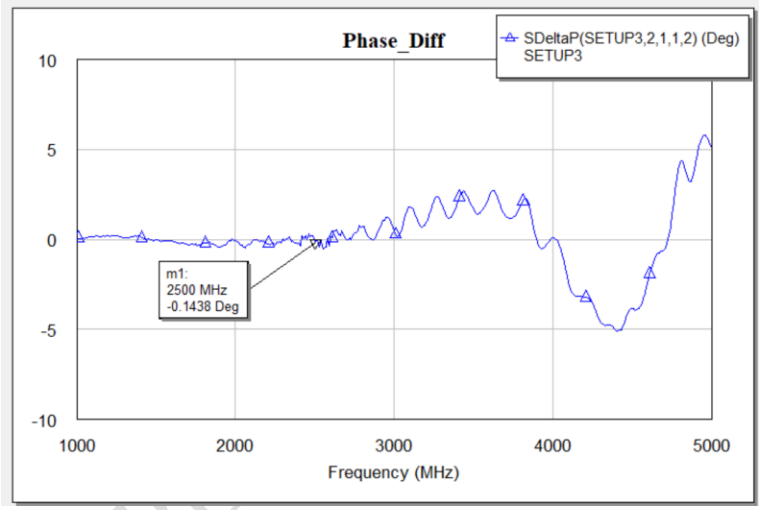
The board gave a slight non- symmetric response. From the setup 1 graphs it can be observed that the resonant frequency form S_{11} is 2.5 GHz and 2.77 GHz from S_{22}. All the other design specs have been met. 3 dB split was achieved over the required frequency range. The insertion loss between port 1 and 3 is 0.301 dB and between port 1 and 2 is 0.264 dB. Isolation between the output ports is 35.44 dB. The phase difference between the output ports is 0.1438^{o}.

Analysis:

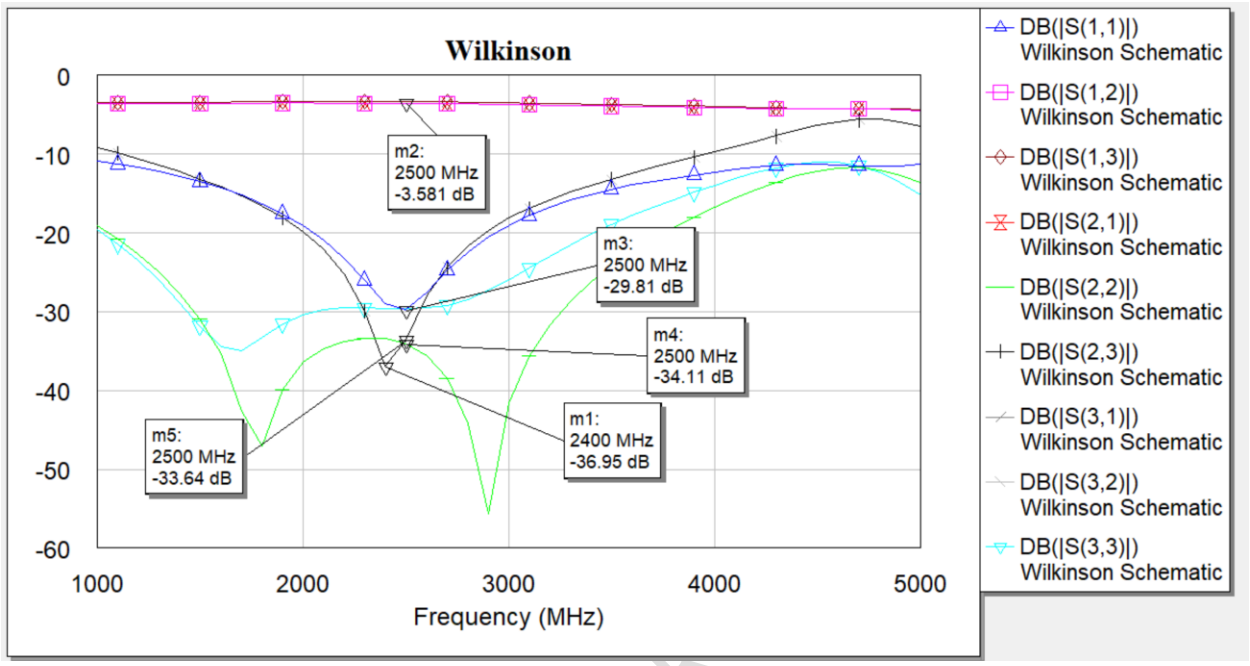
I. Comparison of measured and predicted data:

- **Measured Data**

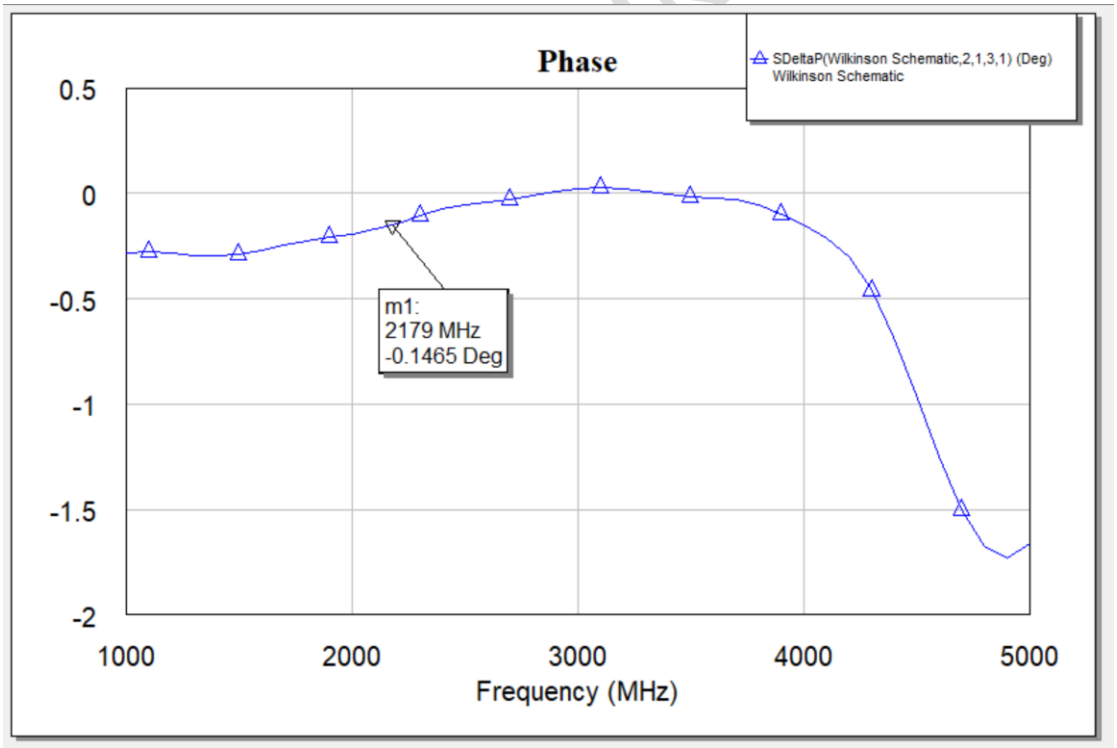




- **Simulated performance**



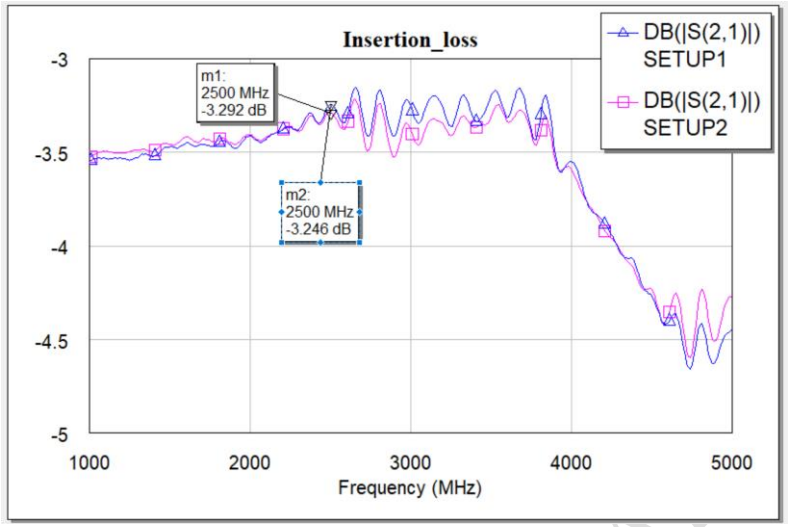
- **Phase difference between output ports**



Questions

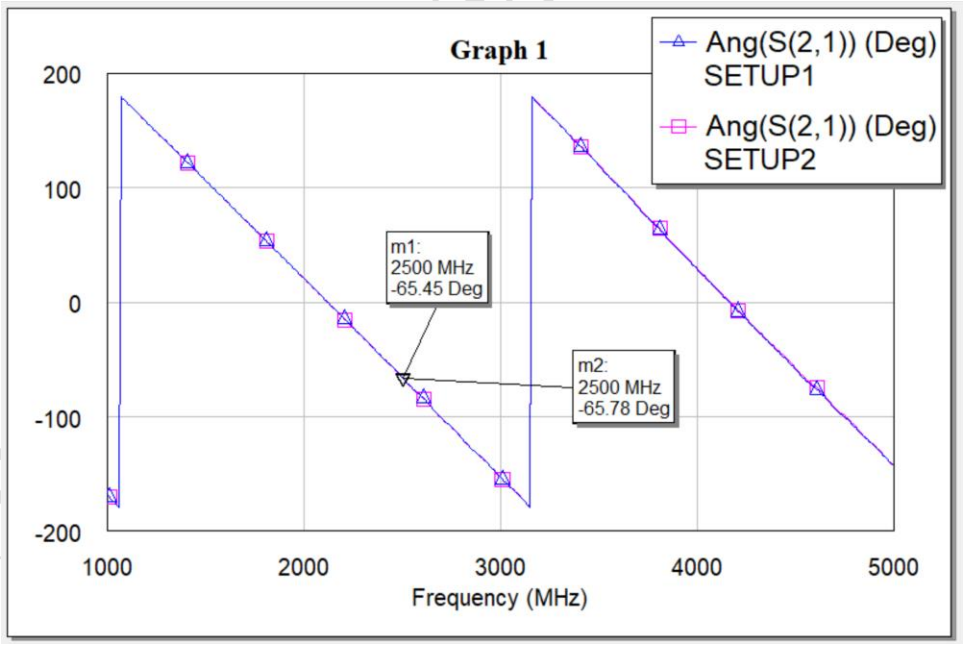
1. Knowing that you designed your divider to have an intentional 3-dB split, what is the actual insertion loss in <u>each</u> arm of your divider (over and above your 3-dB split)?

- Insertion loss for arm 1 = 0.246 dB
- Insertion loss for arm 2 = 0.292 dB



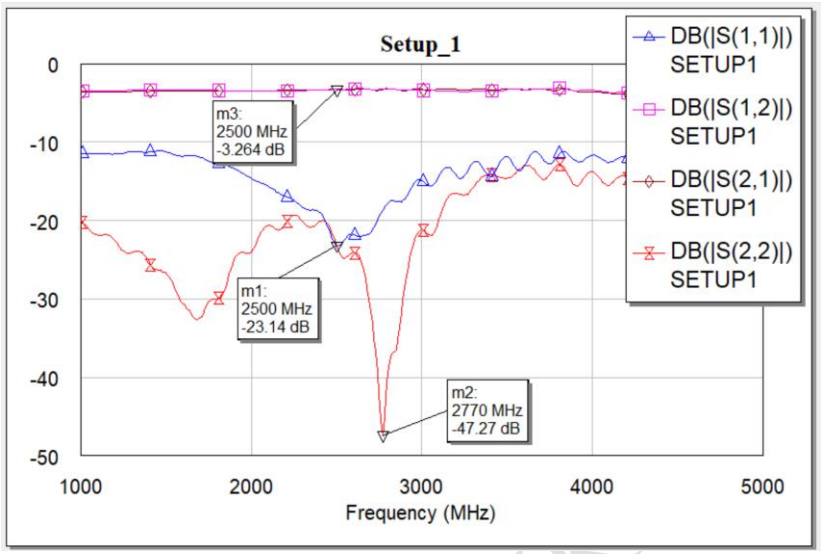
2. Similar question regarding phase: we know this should be an equal-phase power divider. What is the delta phase between S21 phase and S31 phase?

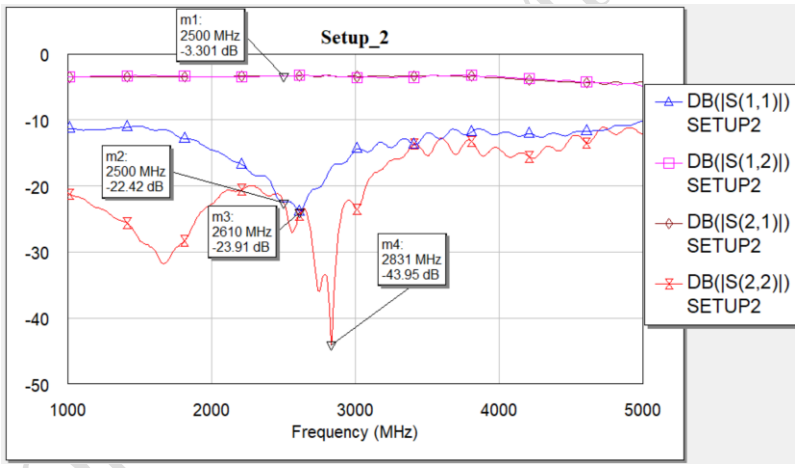
- The Phase difference between S_{21} and S_{31} is 0.33°



3. At what frequency did you measure the greatest return loss (in dB)? If it is not at the design frequency, f_o, what is the most likely cause of the shift?

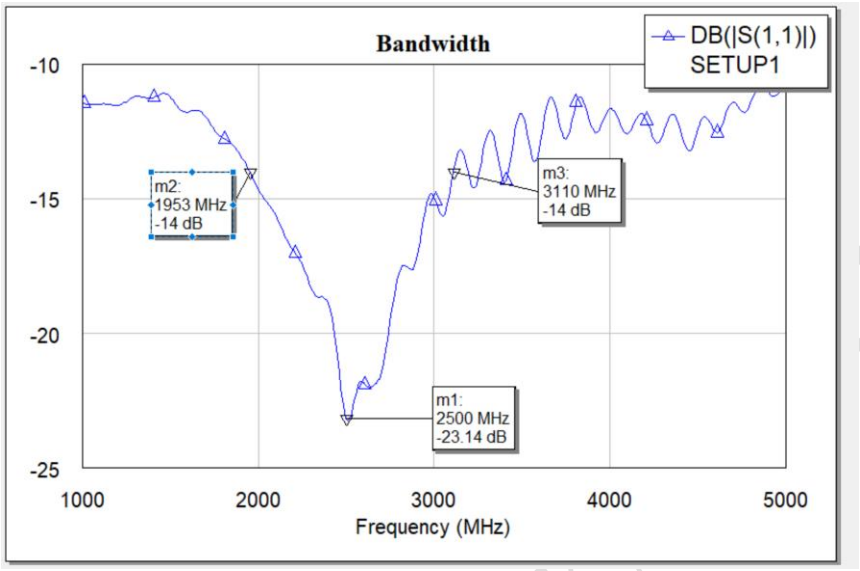
- Return Loss
  Port 1 = 23.14 dB at 2.5 GHz
  Port 2 = 47.27 dB at 2.77 GHz
  Port 3 = 43.95 at 2.831 GHz





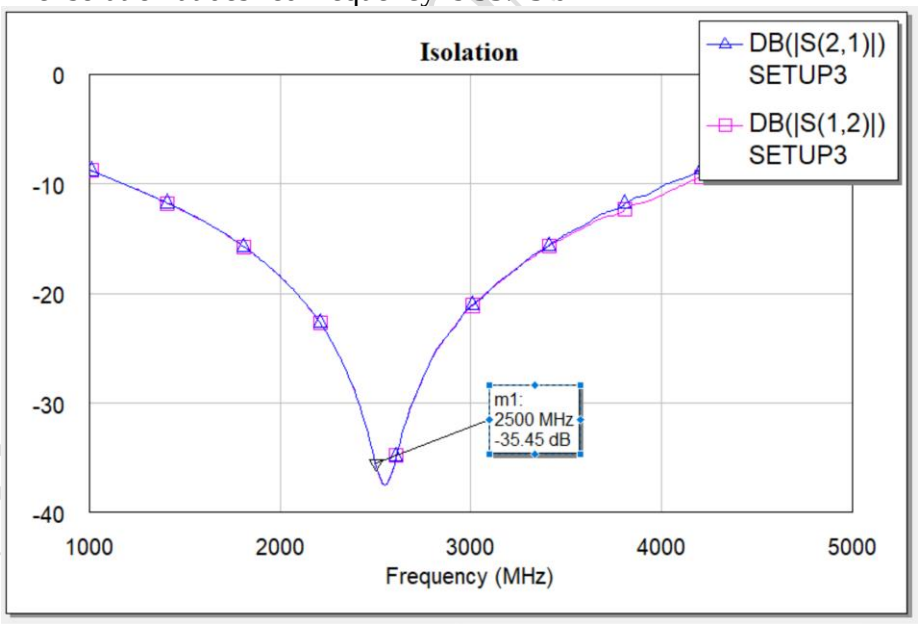
4. Using 14dB as the allowable worst-case measured return loss, what is the useable bandwidth for this power divider in absolute frequency (GHz) and percentage bandwidth (%)?

- From the graph: f_{low} = 1.953 GHz and f_{high} = 3.11 GHz
  ∴ BW = 1.157 GHz
  Fractional BW = 1.157/2.5 = 46.28%



5. What is the isolation between the output ports (in dB) at the design frequency, f_o?

- The isolation at desired frequency is 35.45 dB

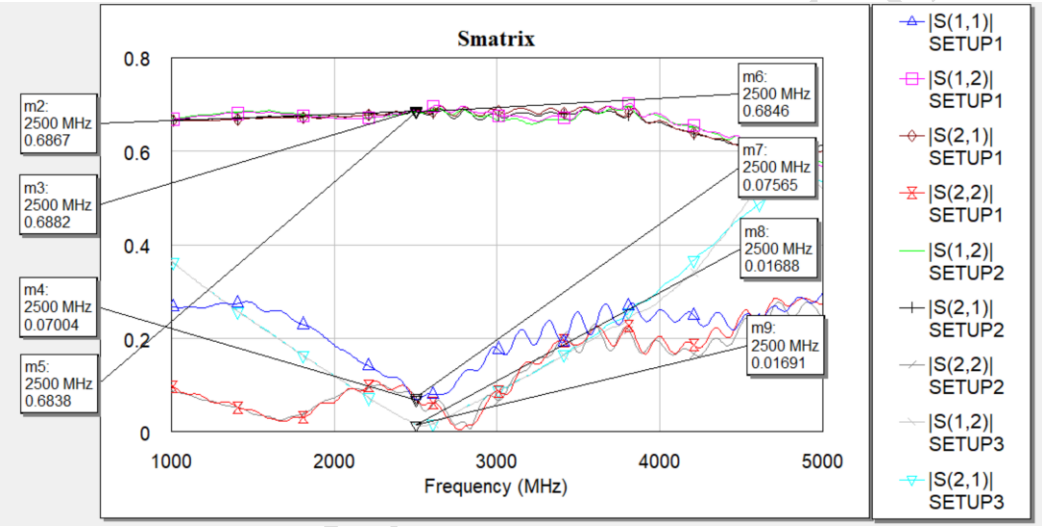


6. Construct a 3-port S-parameter matrix for your power divider

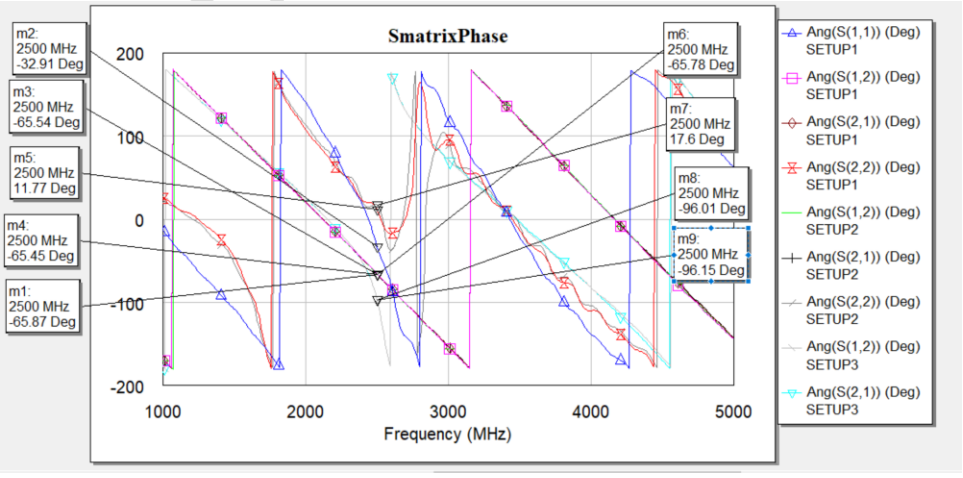
- **S Parameter matrix:**

S	**1**	**2**	**3**
1	0.06967∠ -32.91	0.6867∠ -65.54	0.6838∠-65.87
2	0.6882∠-65.45	0.07004∠11.77	0.01691∠-96.01
3	0.6846∠-65.78	0.01688∠-96.15	0.07565∠17.6

- **Magnitude of S parameter**



- **Angles of S-Parameters**



II. Compliance Matrix:

Parameter	Design Goal	Simulated Performance	Measured Performance **Built**	Compliant (Yes/No)
Center Frequency (GHz)	2.5	2.5	S_{11} = 2.5 S_{22} = 2.7	Yes No
Insertion Loss at output ports (dB)	< 1	S_{21} = 0.581 S_{31} = 0.436	S_{21} = 0.26 S_{31} = 0.25	Yes
Relative Phase Difference (degrees)	0	0.1465	0.1438	Yes
Input Return Loss (dB)	>20	S_{11} = 29.81	S_{11} = 23.44	Yes
Output Return Loss (dB)	>20	S_{22} = 34.11 S_{33} = 35.47	S_{22} = 23.09 S_{33} = 22.42	Yes
Isolation at f_0 (dB)	>20	S_{23} = 34 S_{32} = 34.1	S_{23} = 35.44 S_{32} = 35.45	Yes

Summary:

All the design goals were within accepted variance as reflected from the compliance matrices.

The practical performance was not the same as the simulated one due to the complexities involved in practical implementation like junction capacitances, non-ideal bends and fringing effects. Non-homogenous nature of FR 4 material.

Conclusion:

I. Was your design successful? Why or why not?

All of the design goals were met except for the center frequency.

The effect of these stray capacitances and undesirable fringing effects cause the practical results to be deviated from the ideal value.

II. What lessons did you learn from the lab?

The lossy nature of FR4, the inhomogeneities in the material, the oxide film on the copper, inherent inaccuracies in the milling process all cause deviation in the practical performance. Having knowledge of effective dielectric constant will be helpful to attain desired results.