MMIC Chip Design

EERF – 6396

Prof. Dr. Randall E. Lehmann
Dept. of Electrical Engineering
The University of Texas at Dallas

Submitted by: Omkar Kulkarni

11/20/2017

1. Introduction

Objectives: Design two Butterworth High Pass Filters:

a. Ideal (lumped element) HPF
b. MMIC HPF of GaAs

2. Design

a. **PART – 1: Ideal (lumped element) HPF**

Parameter	Design Goal
f_C (GHz)	10.0
Rejection at 5GHz (dB)	≥30
No. of elements (N, odd)	Minimum
Pi topology	
Z_G and Z_L = 50Ω	

1. From the attenuation behavior chart the number of elements chosen to achieve the desired attenuation is 7.
2. Coefficients for N = 7 Butterworth are:

7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2470	0.4450	1.0000

3. Calculating the Values:

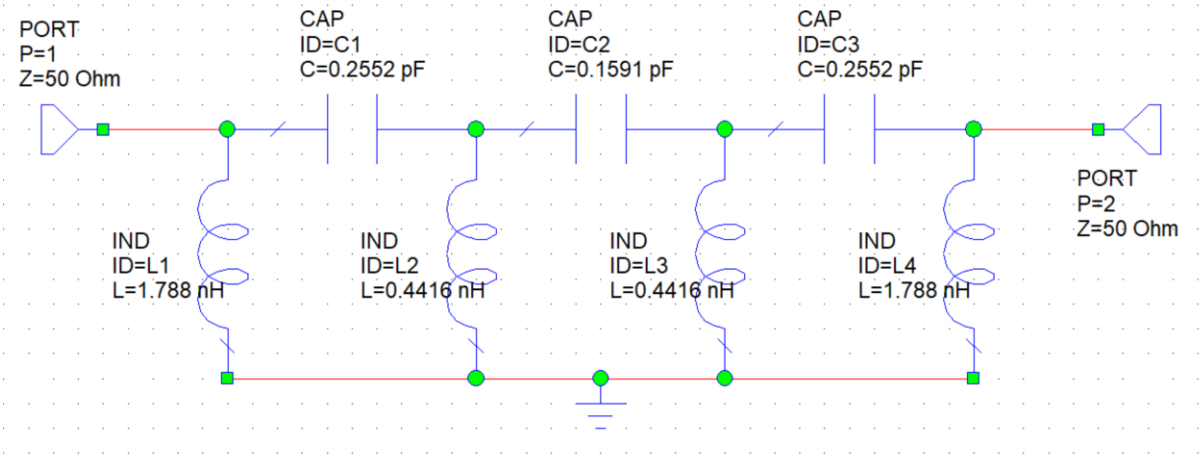
$L_1 = L_7 = \frac{R}{2\pi \times fc \times gn} = \frac{50}{2\pi \times 10G \times 0.445} = 1.788$ nH

$C_2 = C_6 = \frac{1}{2\pi \times R \times fc \times gn} = \frac{1}{2\pi \times 10G \times 50 \times 1.247} = 0.2552$ pF

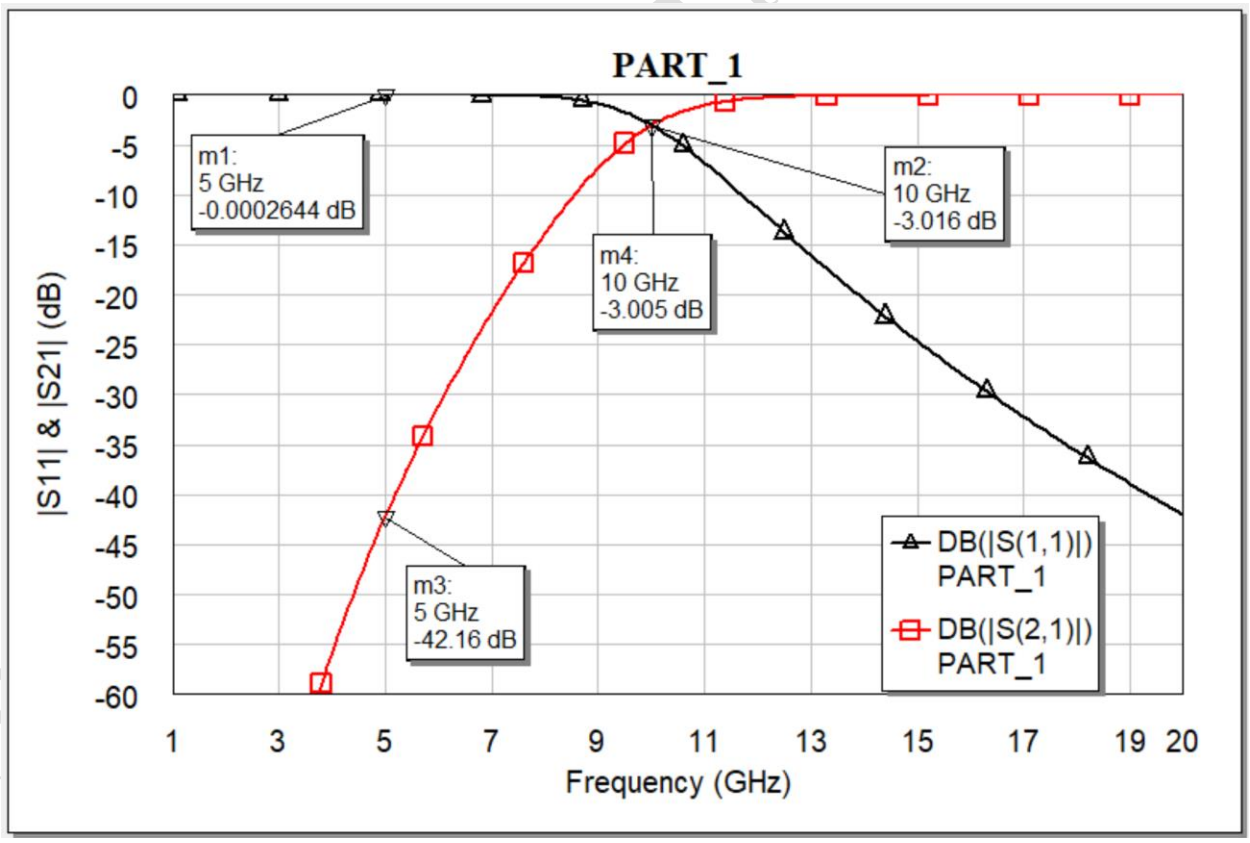
$L_3 = L_5 = \frac{R}{2\pi \times fc \times gn} = \frac{50}{2\pi \times 10G \times 1.8019} = 0.4416$ nH

$C_4 = \frac{1}{2\pi \times R \times fc \times gn} = \frac{1}{2\pi \times 10G \times 50 \times 2} = 0.1591$ pF

- **Schematic**



- **S-parameters form circuit simulations**



- **Compliance Matrix:**

Parameter	Design Goal	Simulated Performance	Compliant (Yes/No)
f_c (GHz)	10	10	Yes
Rejection at 5GHz (dB)	> 30	42.16	Yes

Summary: The results exceed the required specifications with N = 7. We will design the next part with N = 5.

b. **PART – II: MMIC HPF on GaAs**

Parameter	Design Goal
f_C (GHz)	10.0
Rejection at 5GHz (dB) (actual |S21|)	≥25
No. of elements (N, odd)	Minimum
Tee topology	
Z_G and Z_L = 50Ω	
MMIC Chip Size (sq. mm)	Minimum

1. Butterworth coefficients for N = 5:

5	0.6180	1.6180	2.0000	1.6180	0.6180	1.0000

2. Calculating the values:
   T topology is chosen to minimize the number of inductors which would save chip area.

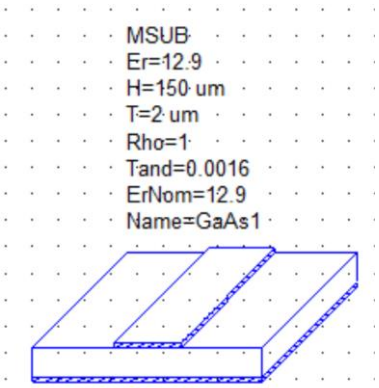
$C_1 = C_5 = \frac{1}{2\pi \times R \times fc \times gn} = \frac{1}{2\pi \times 10G \times 50 \times 0.6180}$ = 0.515 pF

$C_3 = \frac{1}{2\pi \times R \times fc \times gn} = \frac{1}{2\pi \times 10G \times 50 \times 2}$ = 0.5 pF

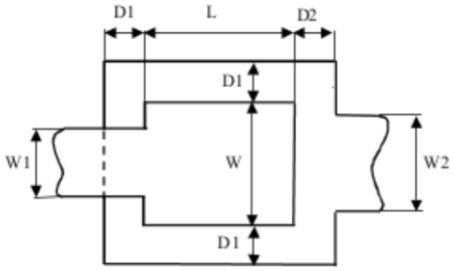
$L_2 = L4 = \frac{R}{2\pi \times fc \times gn} = \frac{50}{2\pi \times 10G \times 1.618}$ = 0.4918 nH

3. Realizing the L and C on GaAs substrate:

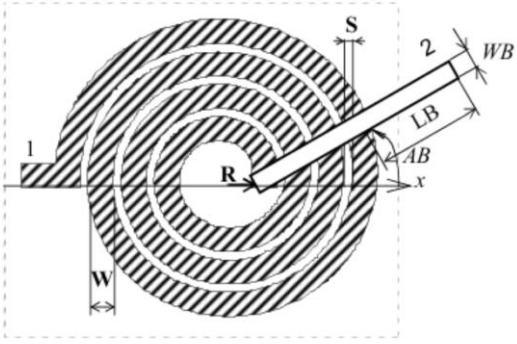
   i. AWR MESFET library is used to streamline the MMIC design process
   ii. MSUB is defined as follows:



   iii. TFCM element is used for capacitors: TFCM shows the calculated capacitance in green for the set parameters. Adjusting the values of width, length the required C values are achieved. The length of all capacitors is kept constant and the width is tuned which further helped in reducing the x dimension.

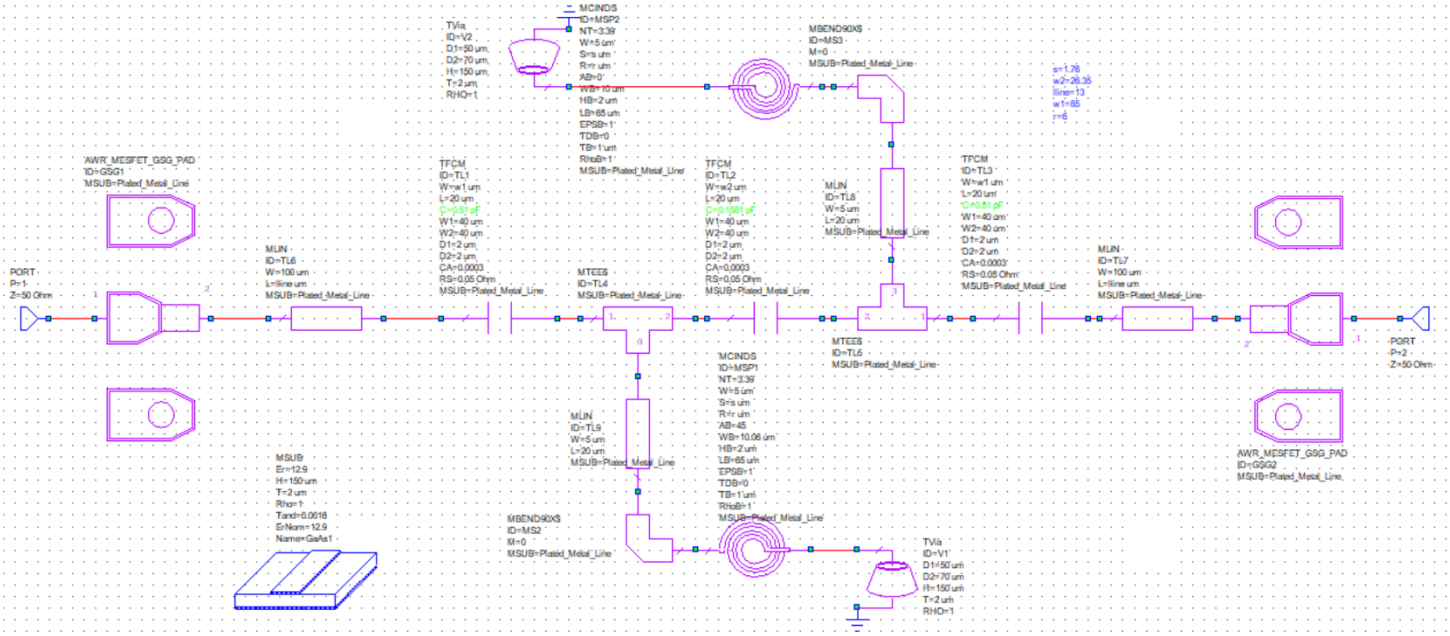


   iv. MCINDS element is used for inductors: Z_{IN} was plotted on smith chart to achieve the required X_L at 10 GHz by tuning radius, width, number of turns, length of the bridge and spacing.

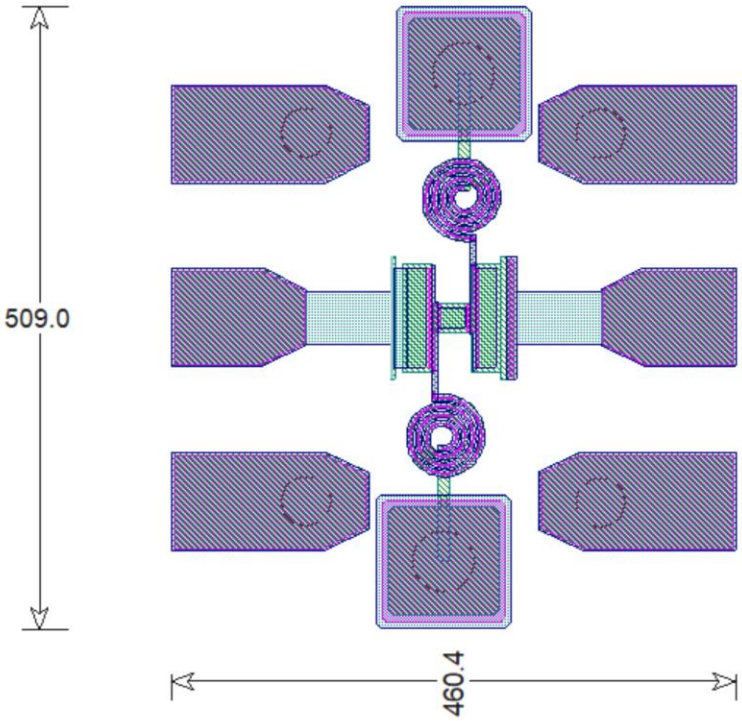


v. Appropriate connecting elements are added to make a practically realizable layout.
vi. TVIA are used to connect the inductors to the ground plane and GSG pads are added for auto-probing capability on both sides.
vii. Tuning was done as necessary to compensate for the connecting elements.

- **Schematic:**

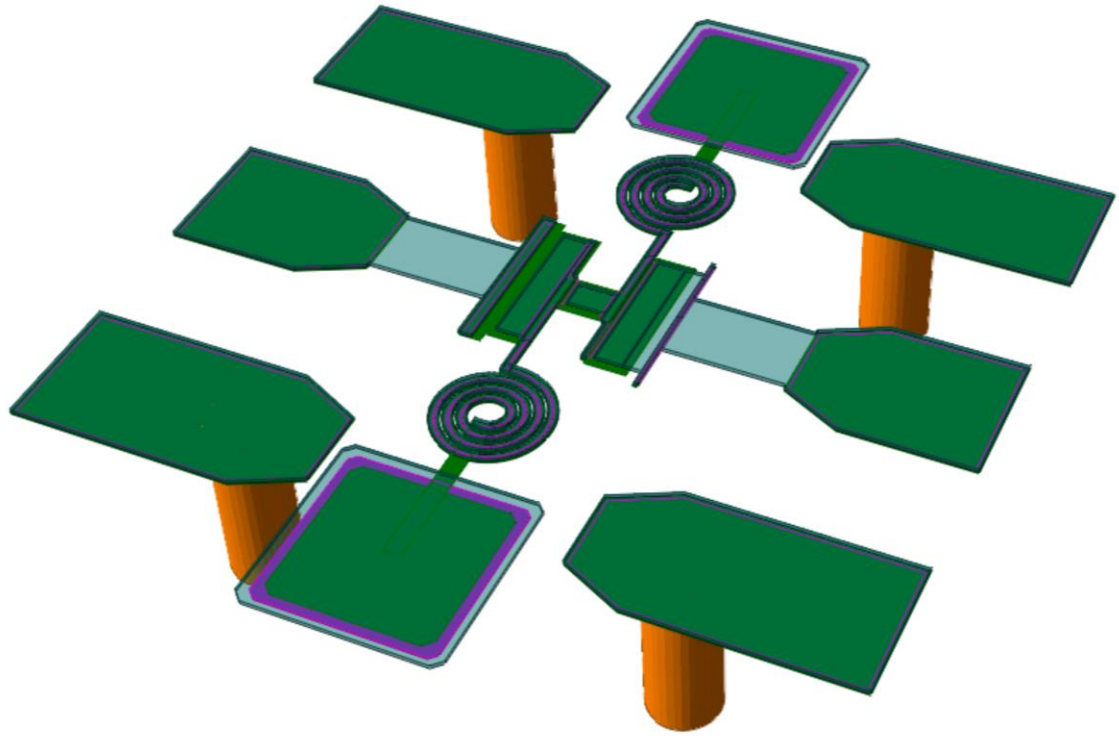


- **Layout:**

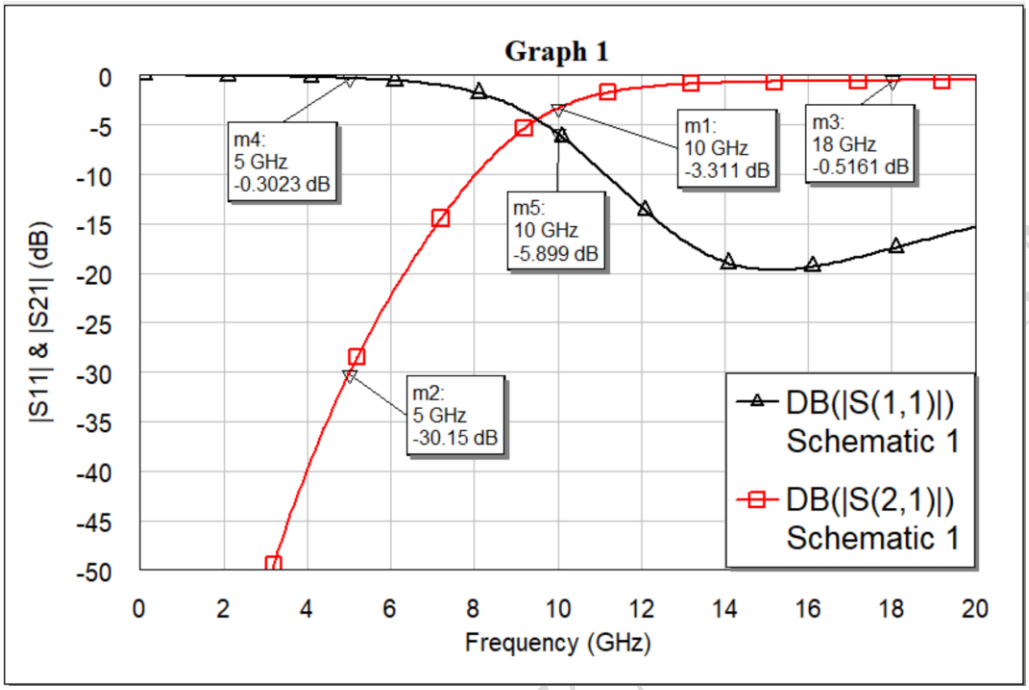


All dimensions in micrometer

- **3-D Layout:**



- **Measurements:**

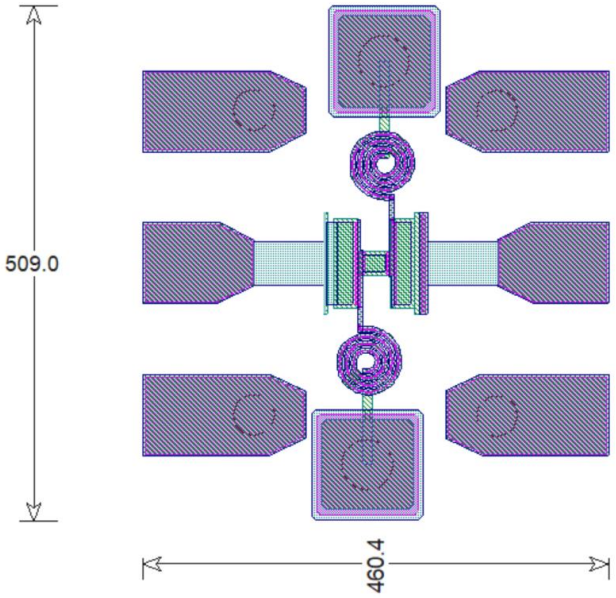


- **Compliance Matrix:**

Parameter	Design Goal	Simulated Performance	Compliant (Yes/No)
f_c (GHz)	10	10	Yes
Rejection at 5GHz (dB)	>25	30.15	Yes

- **MMIC yield**

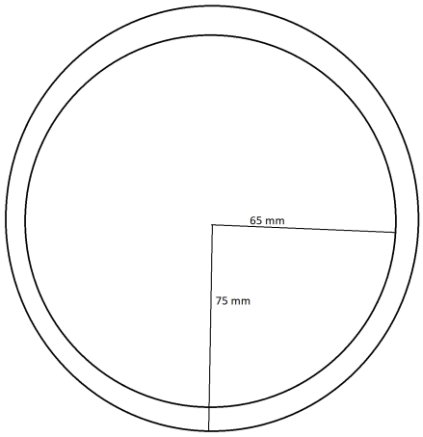
  - Area of 1 chip:



Leaving a margin of 25 μm from all 4 sides:
Length = 460 + 25 + 25 = 510 μm
Width = 509 + 25 + 25 = 559 μm
Total area of unit chip = Length × Width = 0.510 mm × 0.559 mm = **0.285 mm^2**

  - Calculating the available wafer area:

Wafer diameter = 150 mm; wafer radius = 75 mm
Discounting the outer 10 mm:



Remaining area = $\pi r^2 = \pi \times 65^2 = 13273$ mm^2
Discounting 5% area for PCM chips = 13273 × 0.95 = 12609.56 mm^2
Considering the total process and RF yield of 90% = 12609.56 × 0.90 = **11348.6 mm^2**

- Expected yield = $\frac{Available\ wafer\ area}{Unit\ chip\ area} = \frac{11348.6}{0.285} =$ **39816**

Summary: The MMIC HPF has a cutoff frequency of around 10 GHz with rejection of 30.15 dB at 5 GHz. Around 39800 chips can be expected from a 150 mm diameter GaAs wafer.