Lab9 Microwave Amplifier

EERF – 6396
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1. Introduction

Objectives:

Design a microwave amplifier using pHEMT for the given design specs

2. Significance

An amplifier is an electronic device that increases the amplitude of the signal by using electric power. At microwave frequencies the design of matching circuit and stability factors are of critical importance for attaining desired performance and avoiding oscillations. Microwave amplifiers have wide spread uses in modern communications systems at both, transmitter and receiver points.

3. Design

The subject pHEMT is not unconditionally stable for the frequency range, so stability is induced by resistive feedback.

The design is for maximum gain.

$G_T = G_i \, G_{FET} \, G_o$.

Where, G_i = Gain of input matching

G_{FET} = Gain of FET

G_o = Gain of output matching

Now the input and output impedance of the pHEMT is determined from the S2P file provided by the manufacturer at the center frequency of 938 MHz. This is to be matched to 50Ω input and output lines. The matching networks should pull the Z_{in} and Z_{out} points to the center of the Smith Chart. As the length of the 50Ω lines was getting larger, higher impedance lines were used to reduce the lengths of the series lines which have an inductive response. The final values of the lengths and widths are obtained by optimization.

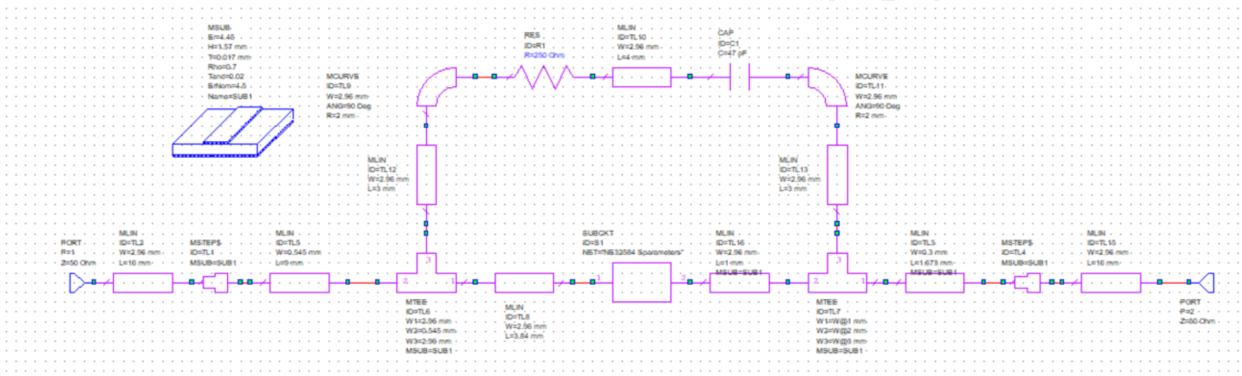
Design Considerations:

- Substrate = FR-4; ε_r = 4.45
- FR-4 substrate thickness = 1.57 mm
- Conductor = Copper
- Conductor thickness = 17 µm
- Dielectric loss tangent = 0.02
- Assume Zo = 50 Ω system
- Minimum line widths and spacing = 254 µm

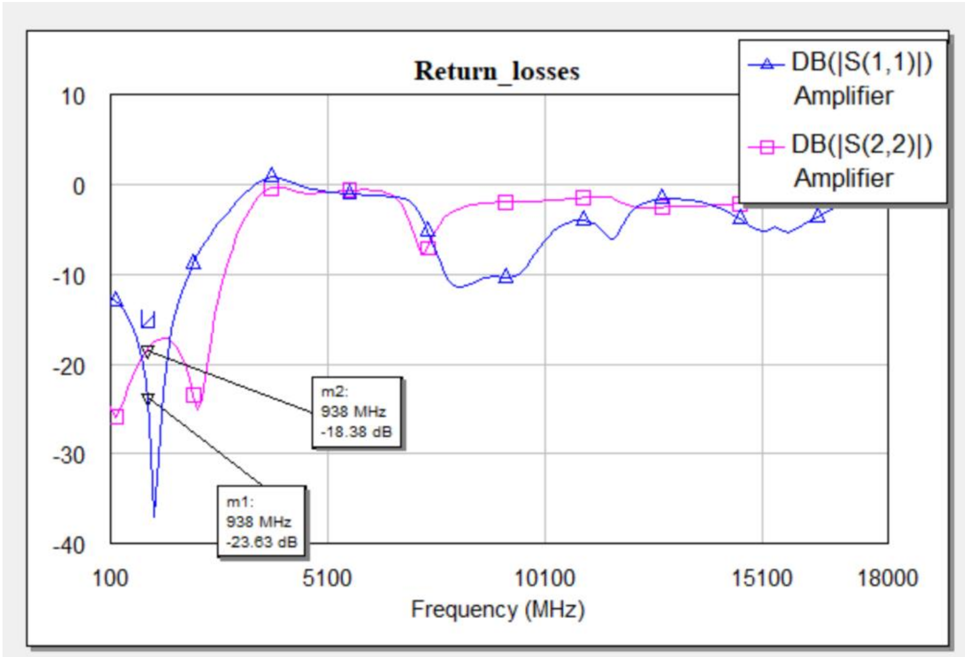
Design Goals:

Parameter	Design Goal
Frequency Range (GHz)	0.8 – 1.1
Linear Gain (dB)	>8
Gain Flatness across band (dB)	<1.0
Input Return Loss (dB)	>15
Output Return Loss (dB)	>15
V_D (volts)	2
I_{DS} (mA)	10
k-Factor (predicted stability over 0.1-18GHz)	>1

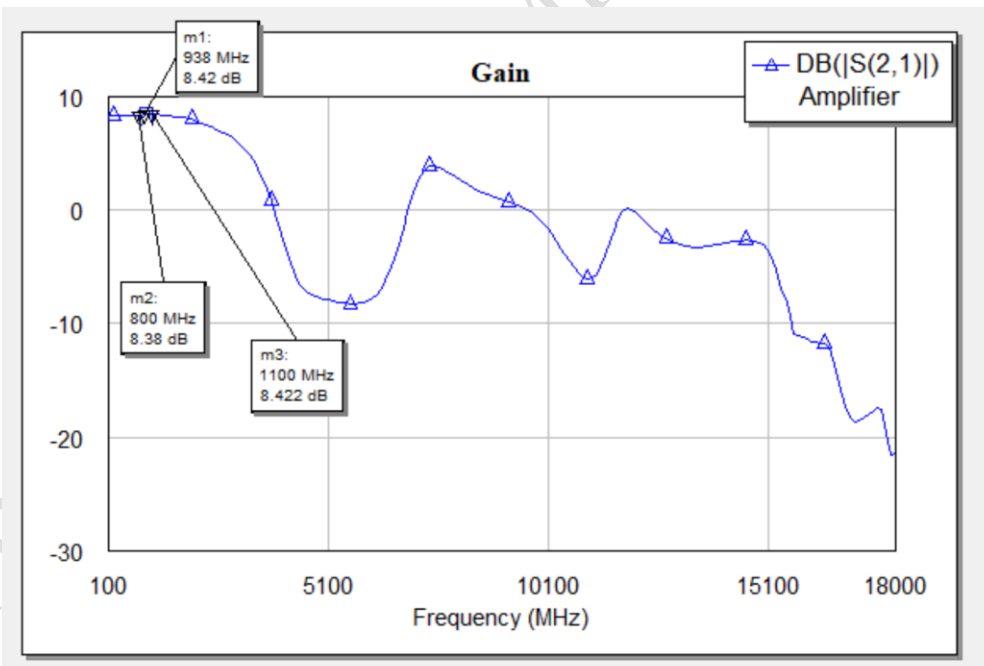
- **AWR MWO Schematic**



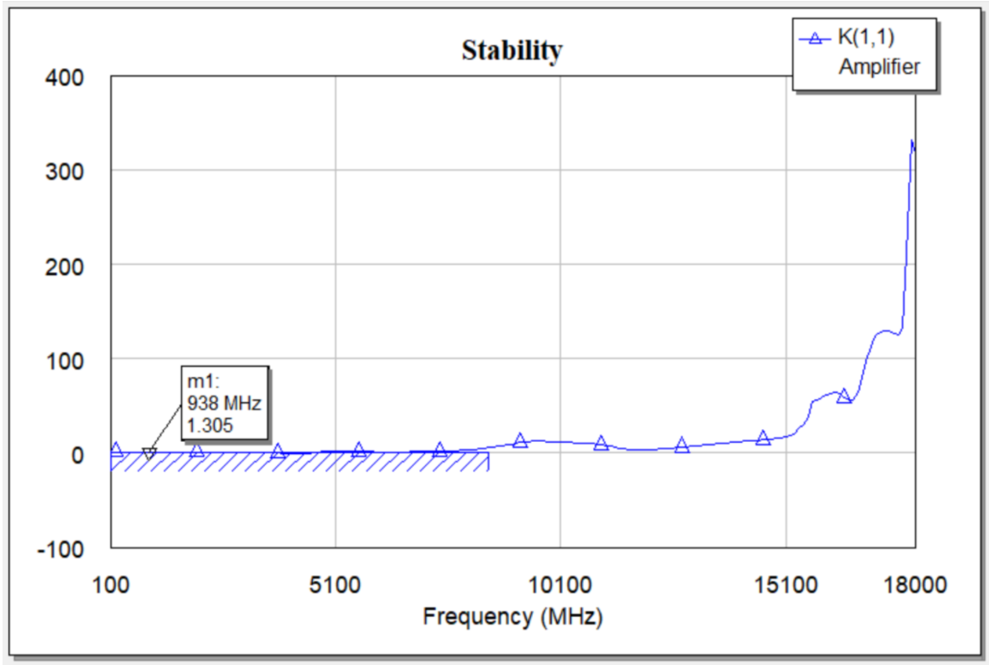
- **Return Losses from circuit simulations**



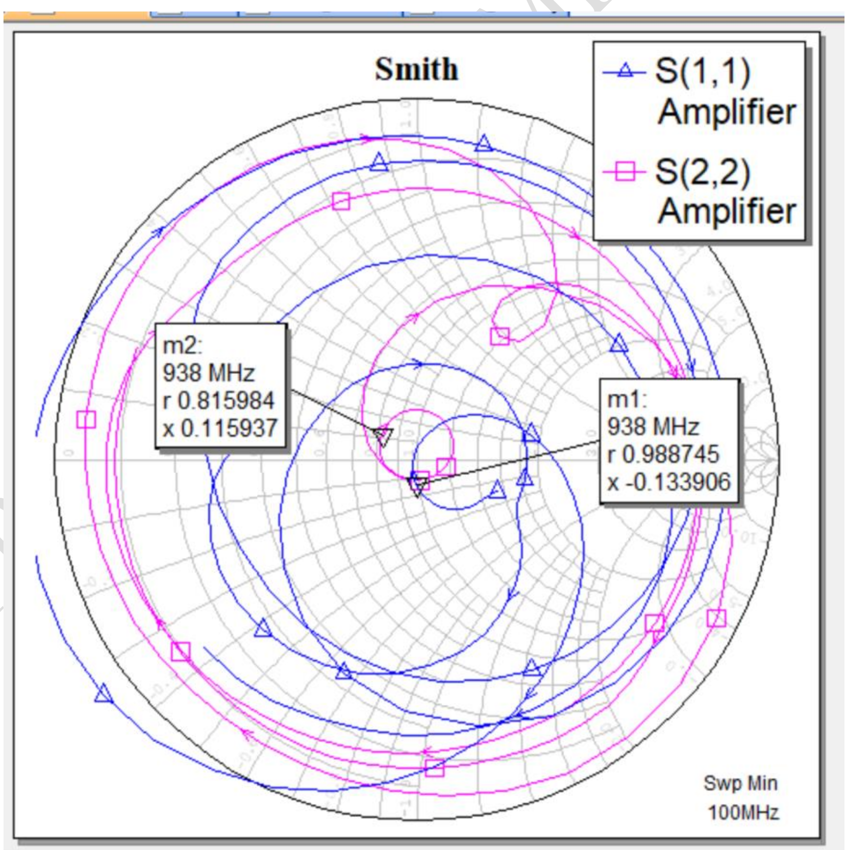
- **Gain from circuit schematic**



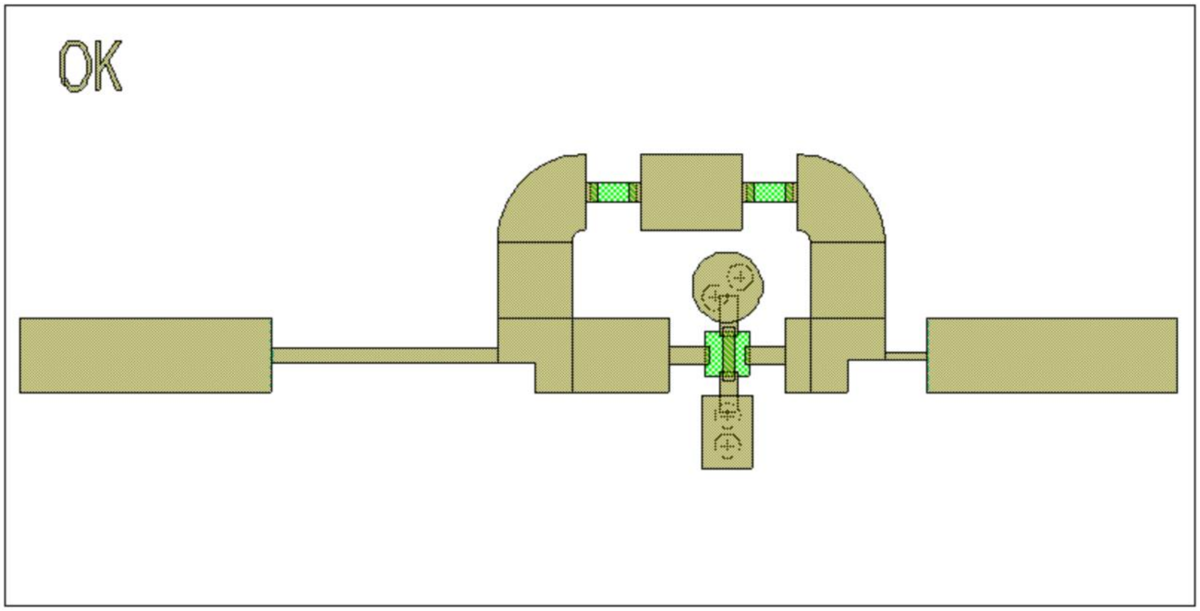
- **Stability:**



- **Smith Chart**



- **Board layout**

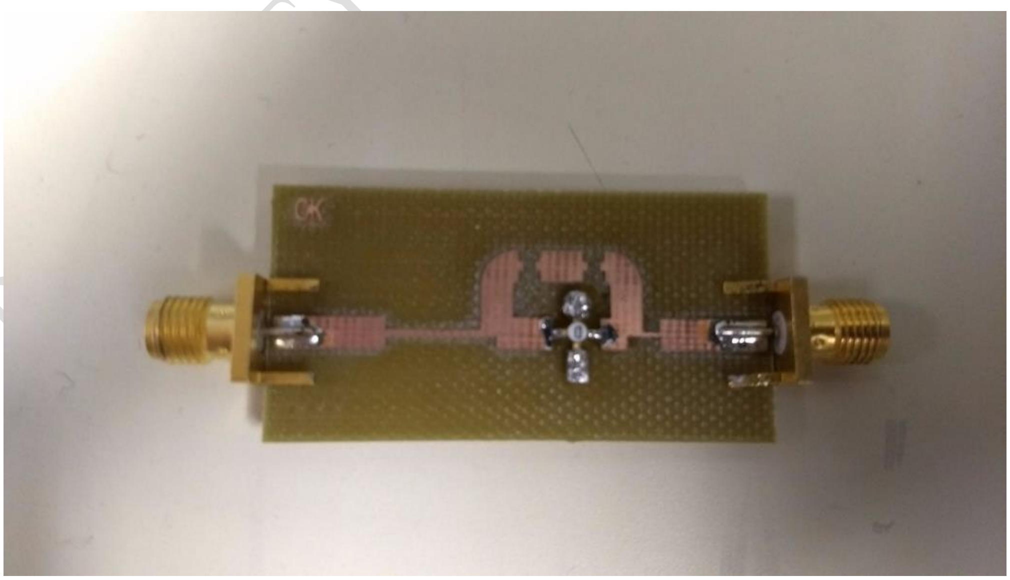


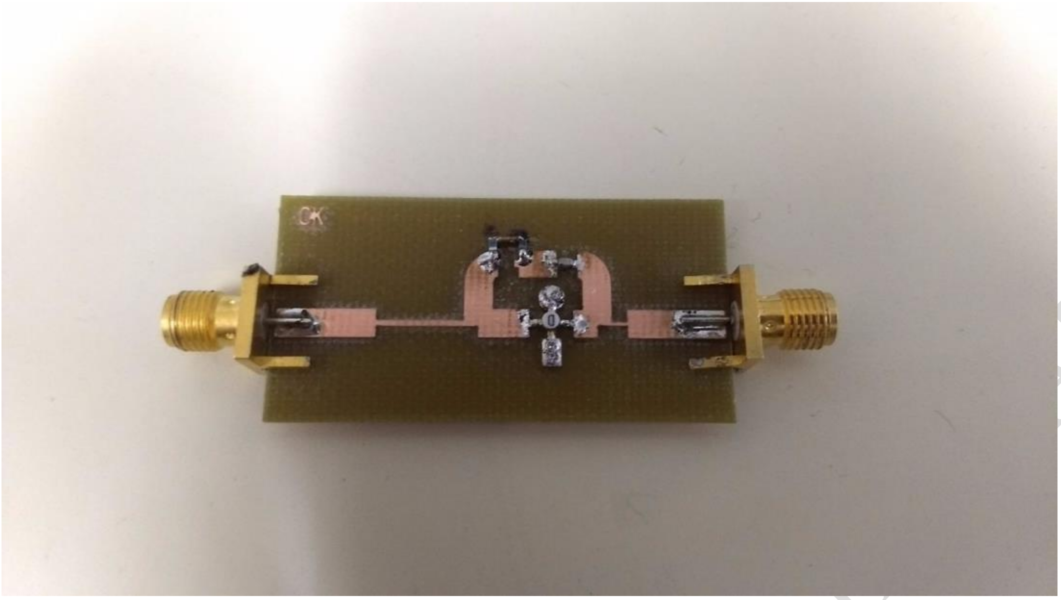
- **Summary:**

The Return losses, gain are in the acceptable range. It is observed that amplifier is unconditionally stable till 4600 MHz and again from 5800 MHz.

4. Lab Measurements

- **Lab setup photographs**

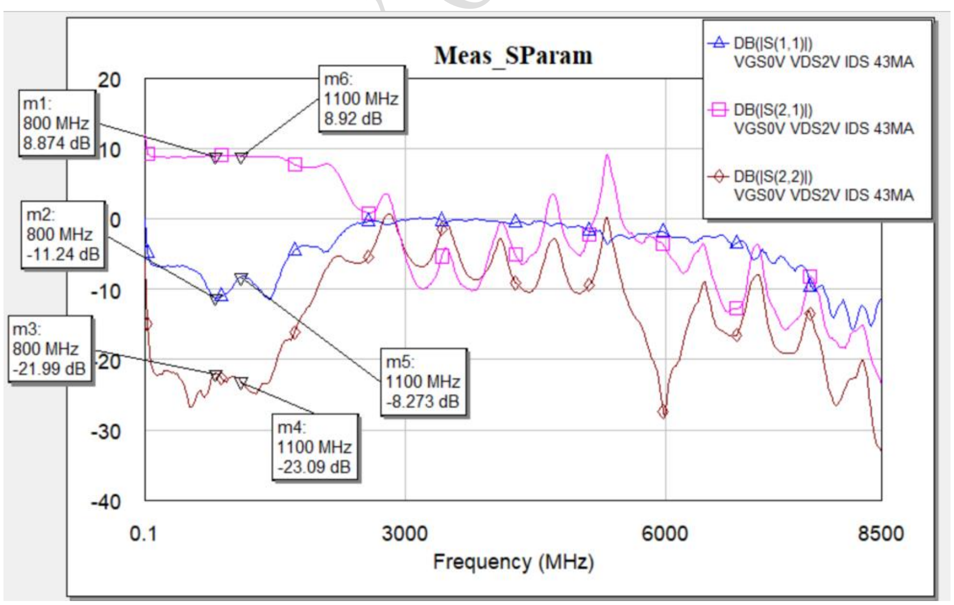


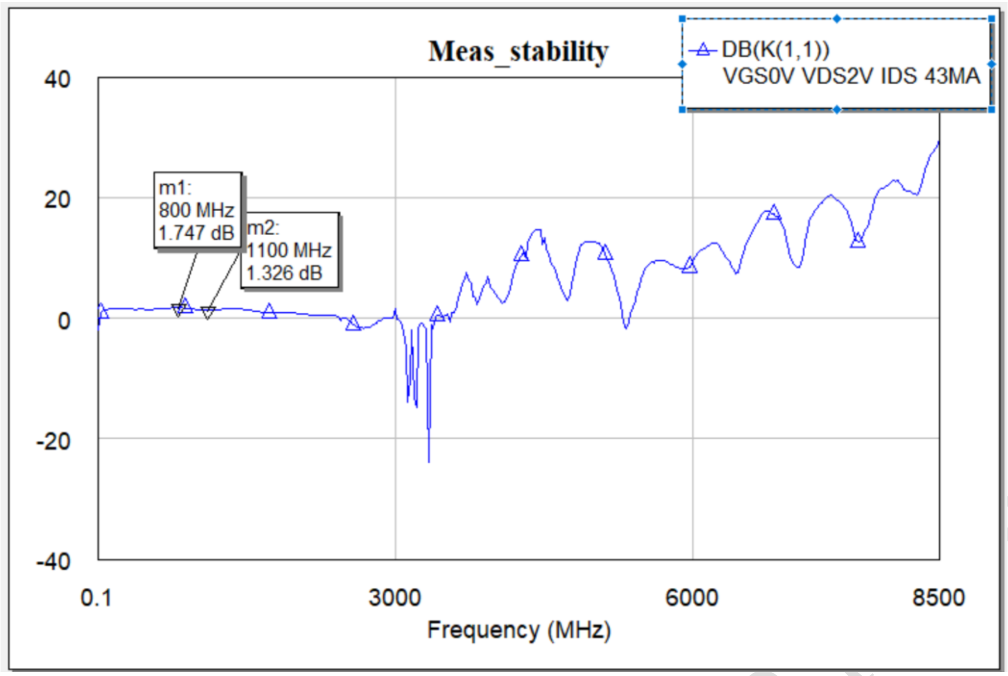


DC Measurements

1. **Idss** [**Vds** = 2V and **Vgs** = 0V] → 43 mA
2. **Vpo** = -0.71 V
3. **Gm = (ΔIds)/ (ΔVgs)** = (0.01)/ (0.24) = 41.6 mS

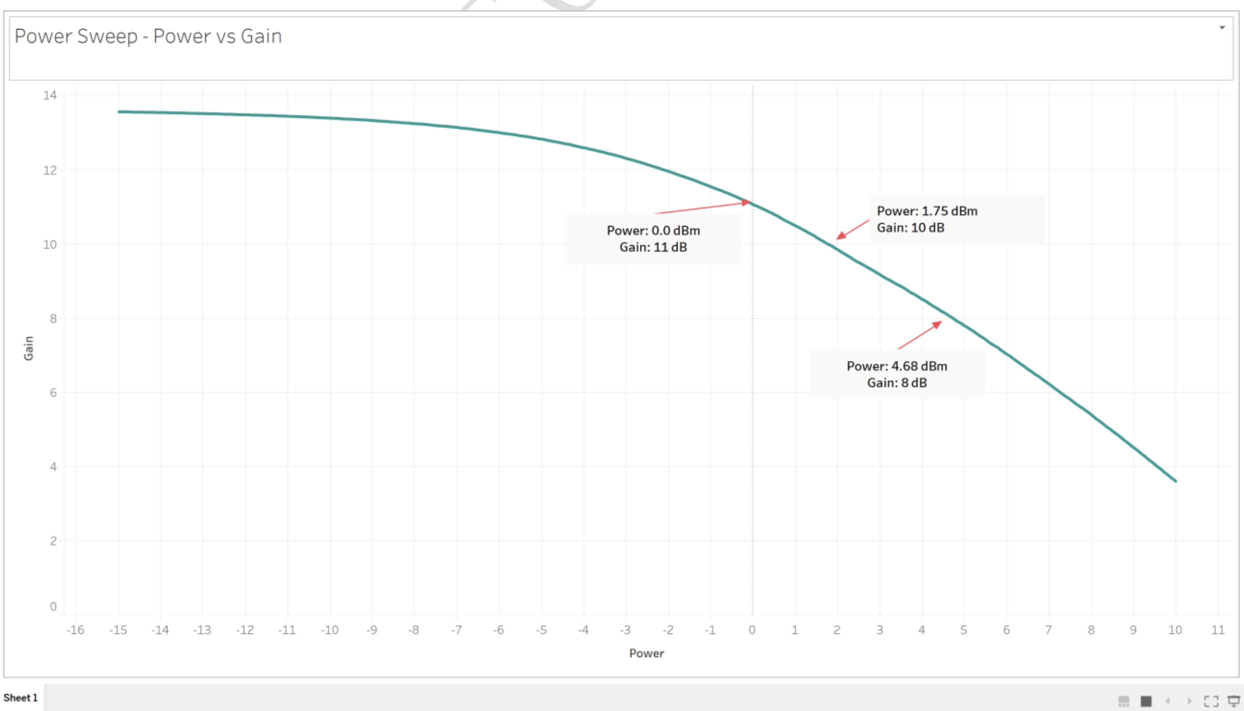
- **Lab Measurements**





5.Analysis:

For the second day in the lab another 200Ω resistor was added in the feedback network (As seen in the photograph) to see the effect of changing resistance in the feedback path. The power sweep is performed on this modified circuit.



Plotted on Tableau

	Power (dBm)	Gain (dB)
	0.0	11
1 dB Point	1.75	10
3 dB Point	4.68	8

Pout = Pin + Gain

P1 dB compression point = 11.75 dBm

P3 dB compression point = 12.68 dBm

- **Compliance Matrix**

Parameter	Design Goal	AWR Simulation	Measured	Compliance
Frequency Range (GHz)	0.8 – 1.1			
Linear Gain (dB)	>8	8.42	8.8	YES
Gain Flatness across band (dB)	<1.0	0.042	0.048	YES
Input Return Loss (dB)	>15	23.63	11.24	NO
Output Return Loss (dB)	>15	18.38	22	YES
k-Factor (800 – 1100 MHz)	>1	1.305	1.5365	YES

Summary: All dimensions of compliance are within acceptable variance.

- **Questions**
  - What is the RF output power at the 1dB gain compression point (P_{1dB}) at 1GHz?
    → 11.75 dBm
  - What is the RF output power at the 3dB gain compression point (P_{3dB}) at 1GHz?
    → 12.68 dBm
  - What could you do to increase overall performance (gain, I/O return loss, BW, etc.) of your amplifier?
    → Using simultaneous conjugate matching for designing the matching networks would reduce the return losses and would also increase the gain. Determining the optimum bias point for the specifications would help as well. Use of CPW is known to increase the bandwidth.

Summary:

Some of the design goals were within accepted variance as reflected from the compliance matrices. The practical performance was not the same as the simulated one due to the complexities involved in practical implementation.