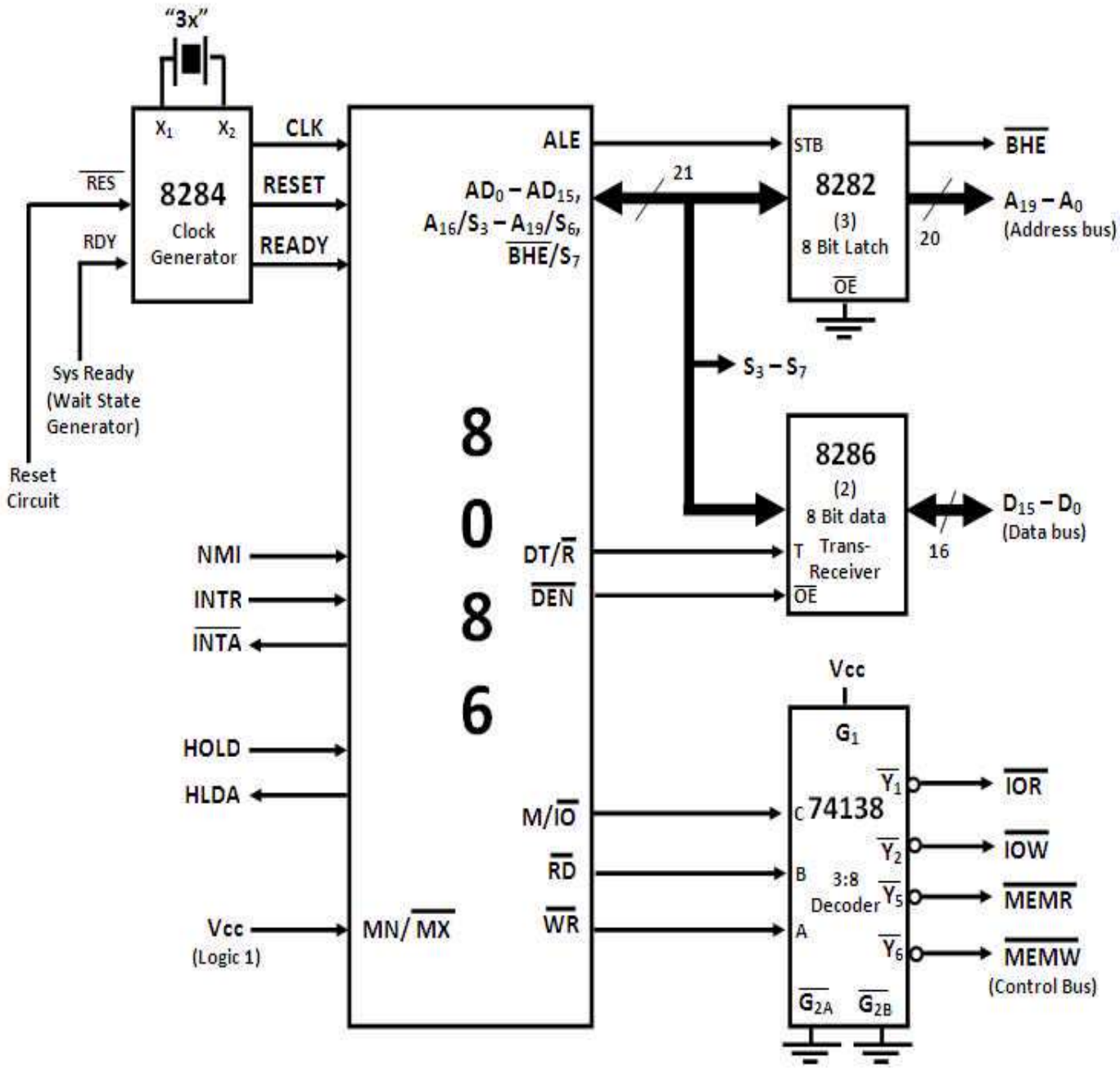
8086 MINIMUM MODE CONFIGURATION



1) **8086 works in Minimum Mode, when MN/ $\overline{MX}$ = 1.**

2) **In Minimum Mode, 8086 is the ONLY processor in the system.**
The Minimum Mode circuit of 8086 is as shown above.

3) Clock is provided by the 8284 Clock Generator.

4) Address from the address bus is latched into 8282 8-bit latch.
Three such latches are needed, as address bus is 20-bit.
The ALE of 8086 is connected to STB of the latch.
The ALE for this latch is given by 8086 itself. #Please refer Bharat Sir's Lecture Notes for this ...

5) The data bus is driven through 8286 8-bit transreceiver.
Two such transreceivers are needed, as the data bus is 16-bit.
The transreceivers are enabled through the **$\overline{DEN}$** signal, while the direction of data is controlled by the **DT/ $\overline{R}$** signal. **$\overline{DEN}$** is connected to **$\overline{OE}$** and **DT/ $\overline{R}$** is connected to T. **Both $\overline{DEN}$ and DT/ $\overline{R}$ are given by 8086 itself.**

$\overline{DEN}$	DT/ $\overline{R}$	Action
1	X	Transreceiver is disabled
0	0	Receive data
0	1	Transmit data

6) **Control signals for all operations are generated by decoding M/ $\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ signals.**

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M/ $\overline{IO}$	$\overline{RD}$	$\overline{WR}$	Action
1	0	1	Memory Read
1	1	0	Memory Write
0	0	1	I/O Read
0	1	0	I/O Write

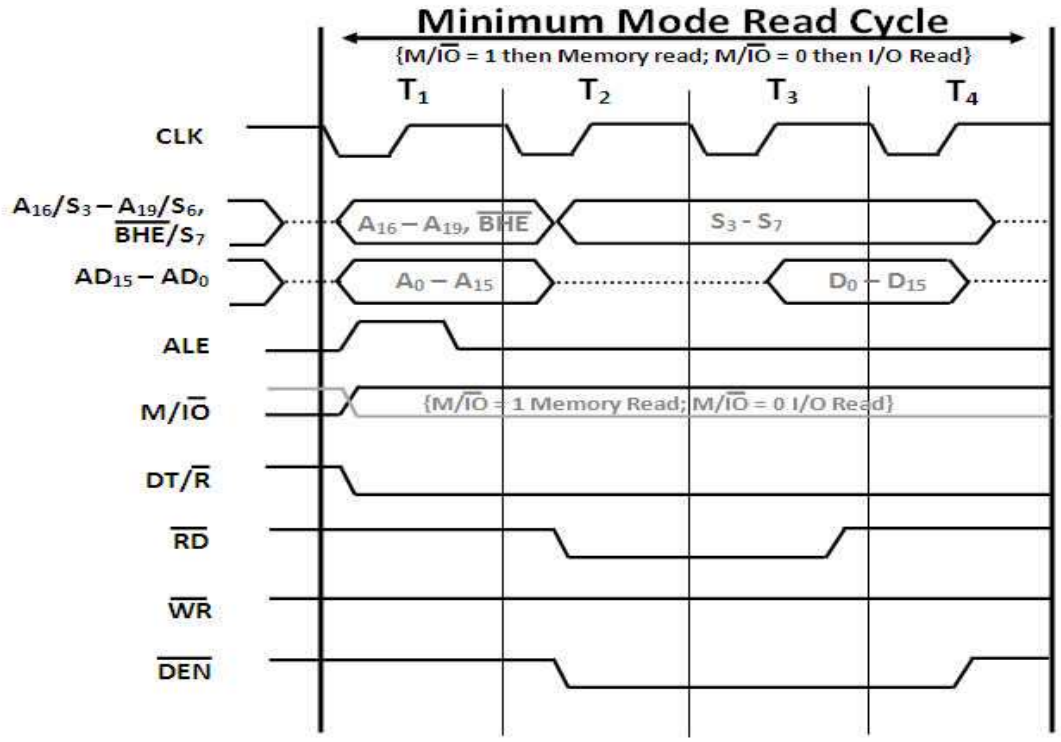
7) **M/ $\overline{IO}$, $\overline{RD}$, $\overline{WR}$** are **decoded by a 3:8 decoder like IC 74138.**

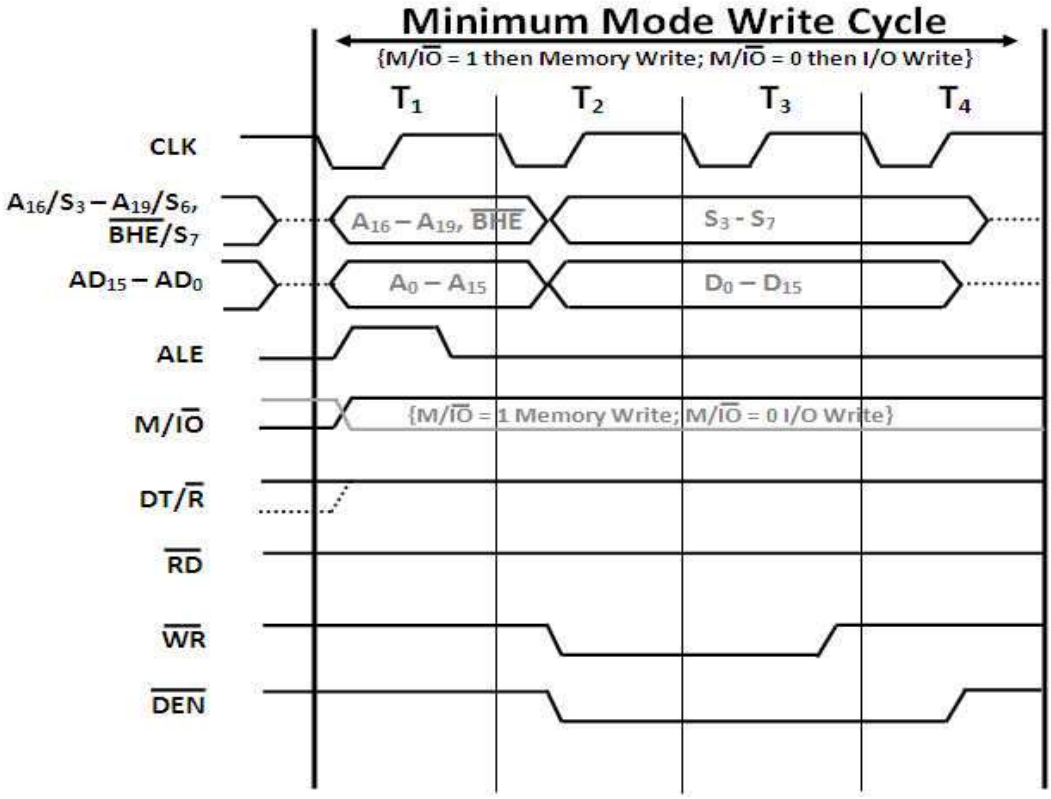
8) **Bus Request (DMA) is done using the HOLD and HLDA signals.**

9) **$\overline{INTA}$ is given by 8086, in response to an interrupt on INTR line.**

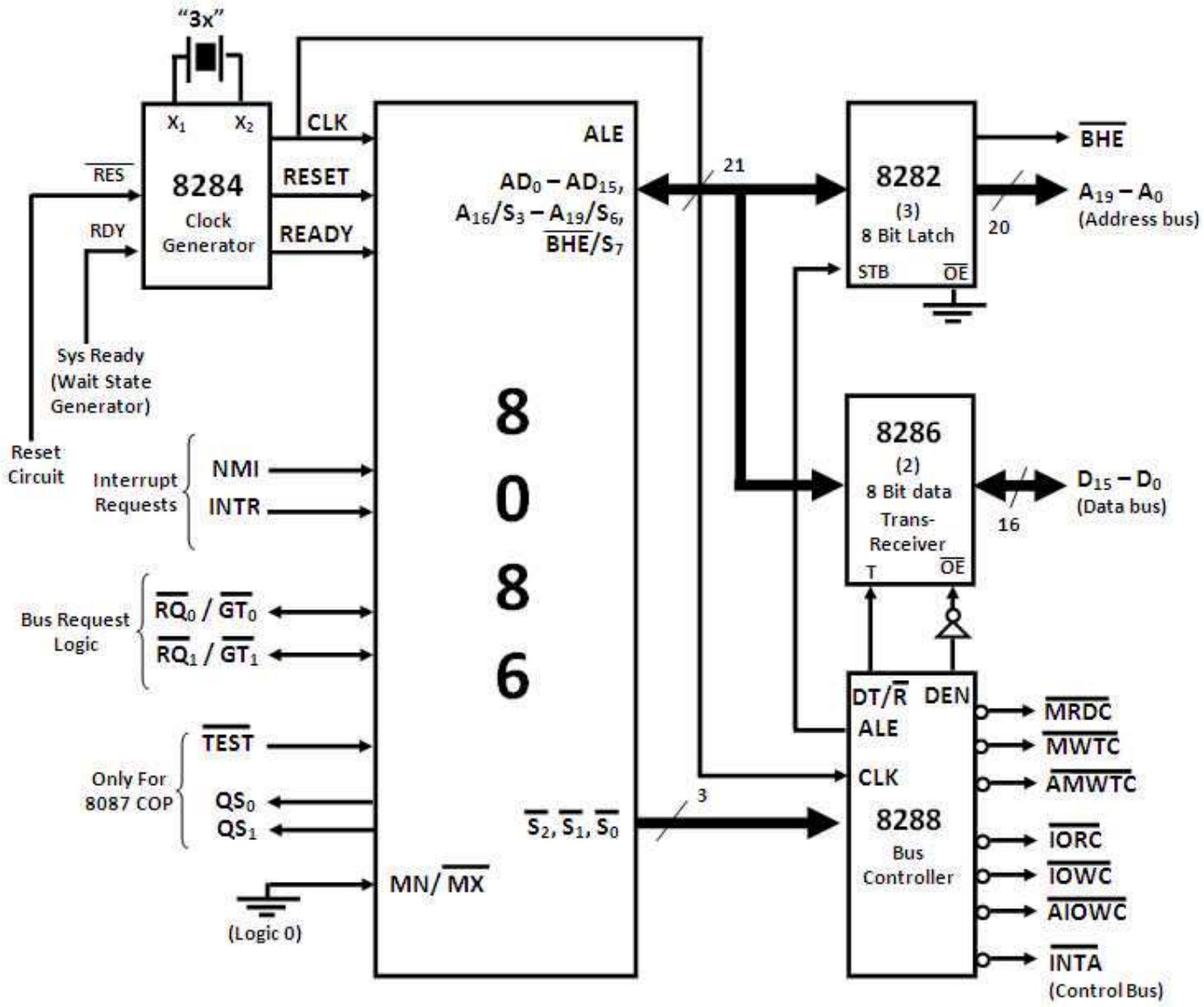
10) **The Circuit is simpler than Maximum Mode but does not support multiprocessing.**

Timing Diagrams:





8086 MAXIMUM MODE CONFIGURATION



1) **8086 works in Maximum Mode, when MN/ $\overline{MX}$ = 0.**

2) **In Maximum Mode, we can connect more processors to 8086 (8087/8089).**
The Maximum Mode circuit of 8086 is as shown above.

3) Clock is provided by the 8284 Clock Generator.

4) The most significant part of the Maximum Mode circuit is the 8288 Bus Controller.
Instead of 8086, the Bus Controller provides the various control signals as explained below.

5) Address form the address bus is latched into 8282 8-bit latch.
Three such latches are needed, as address bus is 20-bit.
This ALE is connected to STB of the latch.
The ALE for this latch is given by 8288 Bus Controller.

6) The data bus is driven through 8286 8-bit transreceiver.
Two such transreceivers are needed, as the data bus is 16-bit.
The transreceivers are enabled through the DEN signal, while the direction of data is controlled by the **DT/ $\overline{R}$** signal.

DEN is connected to **$\overline{OE}$** and **DT/ $\overline{R}$** is connected to T.

Both DEN and DT/ $\overline{R}$ are given by 8288 Bus Controller.

DEN (Of 8288)	DT/ $\overline{R}$	Action
0	X	Transreceiver is disabled
1	0	Receive data
1	1	Transmit data

7) **Control signals for all operations are generated by decoding $\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$ signals.** For doubts contact Bharat Sir on 98204 08217

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State (What the µP wants to do)	8288 Active Output (What Control signal should 8288 generate)
0	0	0	Int. Acknowledge	**$\overline{INTA}$**
0	0	1	Read I/O Port	**$\overline{IORC}$**
0	1	0	Write I/O Port	**$\overline{IOWC}$** and **$\overline{AIOWC}$**
0	1	1	Halt	None
1	0	0	Instruction Fetch	**$\overline{MRDC}$**
1	0	1	Memory Read	**$\overline{MRDC}$**
1	1	0	Memory Write	**$\overline{MWTC}$** and **$\overline{AMWTC}$**
1	1	1	Inactive	None

8) $\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$ are decoded using 8288 bus controller.

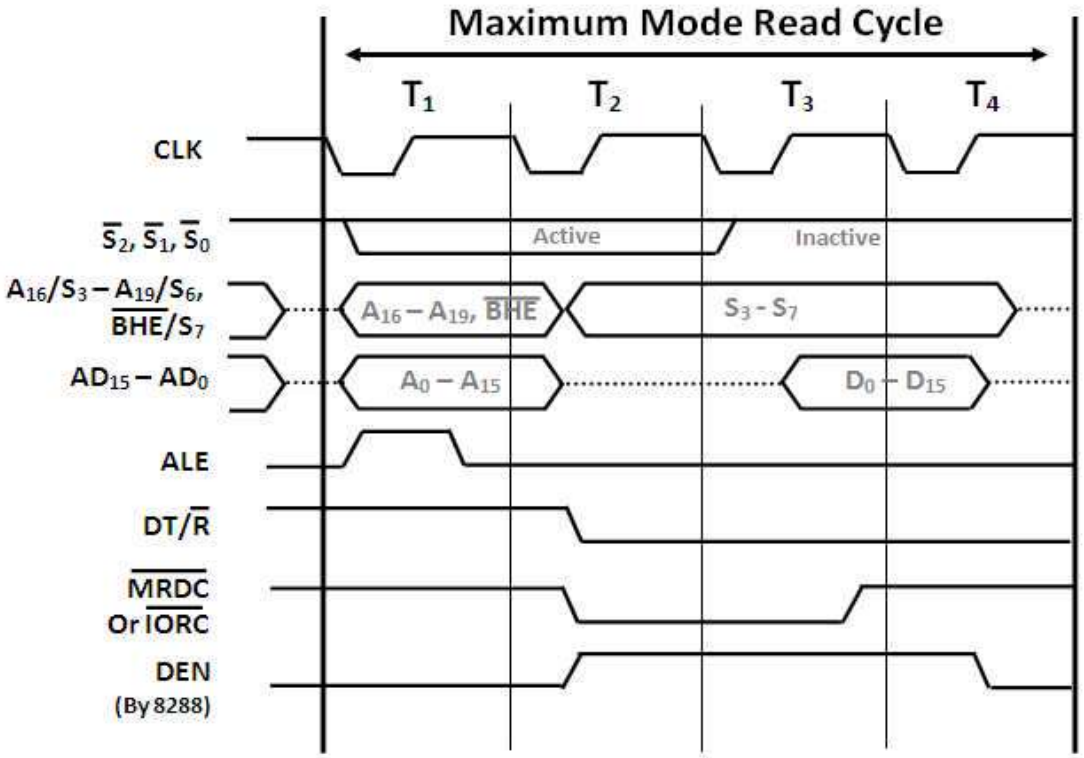
9) Bus request is done using $\overline{RQ}$ / $\overline{GT}$ lines interfaced with 8086.
RQ_0/GT_0 has higher priority than RQ_1/GT_1. ☺ For doubts contact Bharat Sir on 98204 08217

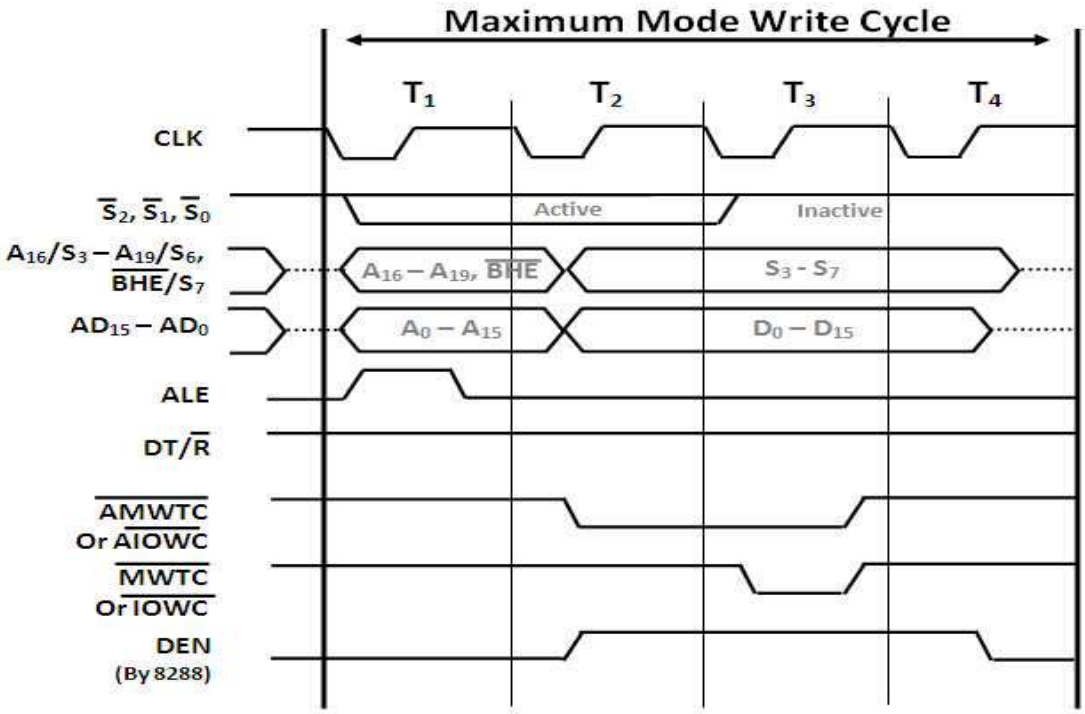
10) $\overline{INTA}$ is given by 8288 Bus Controller, in response to an int. on INTR line of 8086.

11) Max mode circuit is more complex than Min mode but supports multiprocessing hence gives better performance.

12) In max mode, the advanced write signals get activated one T-State in advance as compared to normal write signals. This gives slower devices more time to get ready to accept the data (as µP is writing), and hence reduces the number of "wait states".

TIMING DIAGRAMS





Differentiate between

	MIN MODE	MAX MODE
1	It is a **uniprocessor mode.** 8086 is the only processor in the circuit.	It is a **multiprocessor mode.** Along with 8086, there can be other processors like 8087 and 8089 in the circuit.
2	Here **MN/ $\overline{\text{MX}}$** is connected to **Vcc.**	Here **MN/ $\overline{\text{MX}}$** is connected to **Ground.**
3	**ALE** for the latch is **given by 8086** itself.	As there are multiple processors, **ALE** for the latch is **given by 8288 bus controller**.
4	**$\overline{\text{DEN}}$** and **DT/ $\overline{\text{R}}$** for the transreceivers **are given by 8086 itself.**	As there are multiple processors, **DEN** and **DT/ $\overline{\text{R}}$** for the transreceivers is **given by 8288 bus controller**.
5	Direct control signals like **M/ $\overline{\text{IO}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are produced by 8086 itself.**	Instead of control signals, all processors produce status signals **$\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$**
6	Control signals **M/ $\overline{\text{IO}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are decocded by a 3:8 decoder IC 74138.**	Status signals **$\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$ require special decoding** are decoded by **8288 bus controller**.
7	**$\overline{\text{INTA}}$** for interrupt acknowledgement **is produced by 8086.**	**$\overline{\text{INTA}}$** for interrupt acknowledgement **is produced by 8288 Bus Controller.**
8	**Bus request are grant** is handled using **HOLD and HLDA** signals.	**Bus request are grant** is handled using **$\overline{\text{RQ}}$ / $\overline{\text{GT}}$** signals.
9	Since **74138** does not independently generate any signals, it **does not need a CLK.**	Since **8288** independently generates control signals, it **needs a CLK from 8284** clock generator.
10	The circuit is **simpler but does not support multiprocessing**.	The circuit is **more complex but supports multiprocessing**.