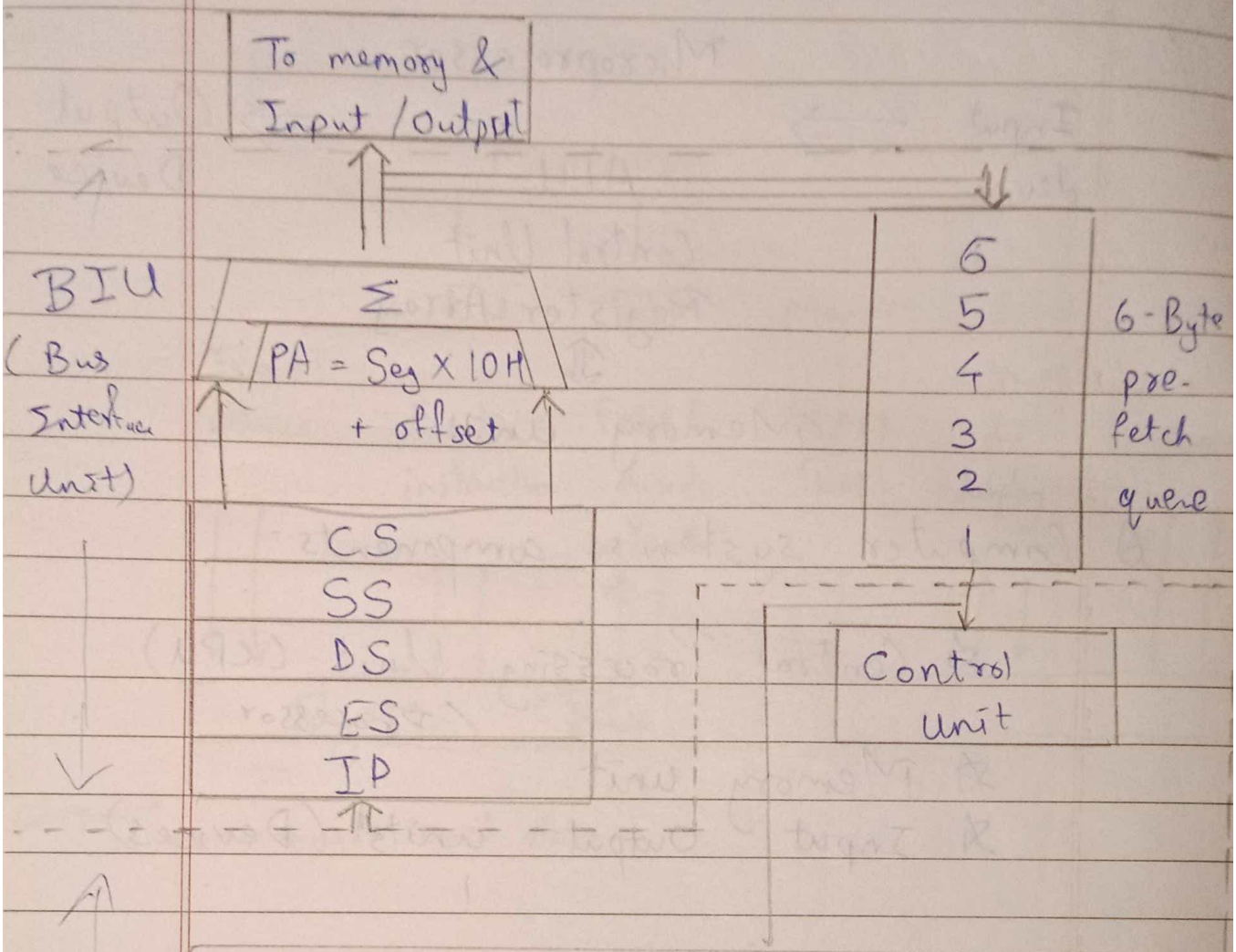
FS19C0042

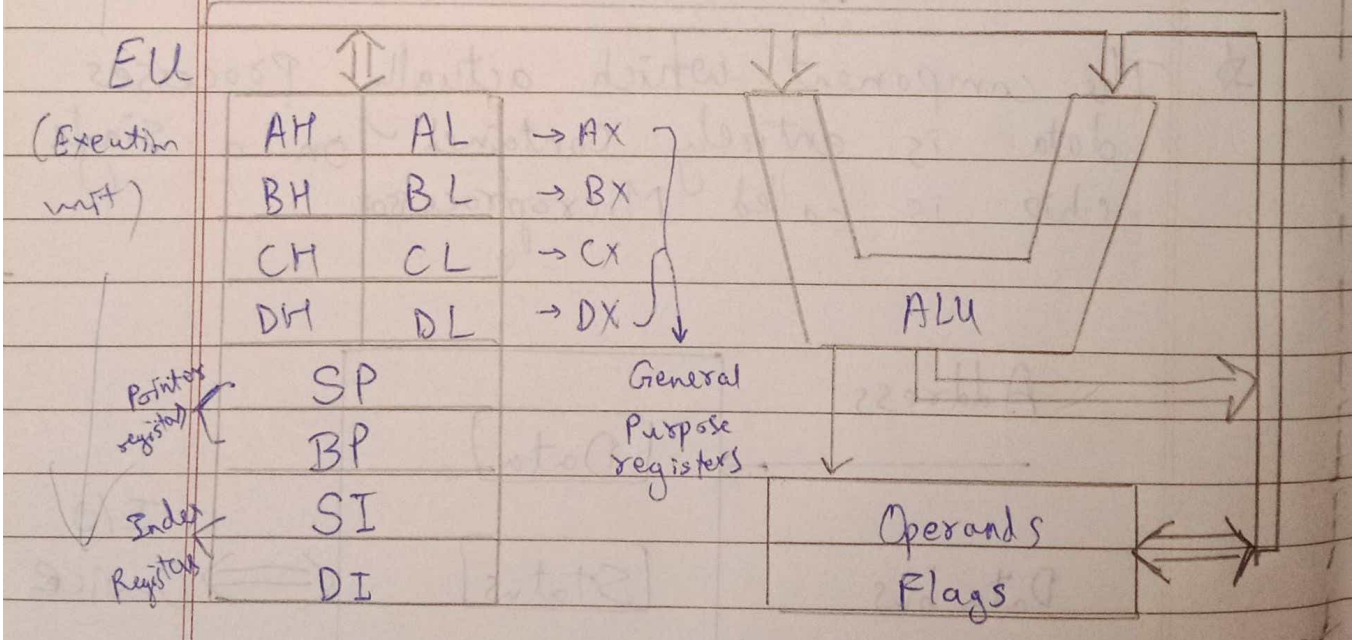
Q.B Unit 1

1. List any 4 features of 8086

→ • It has an instruction queue which is capable of storing six instruction bytes from the memory resulting in faster processing.
• It uses 2 stages of pipelining i.e. Fetch Stage & Execute stage which improves performance
• It has 256 vectored interrupts
• It consists of 29000 transistors

2. Draw functional block diagram of 8086





Flag Register; (16-bit, ~~8-bit~~. 7 bits unused)

				OF	DF	IF	TF	SF	ZF		AF		PF		CF

3. State the System Bus with its types

→ A System bus is a single computer bus that connects the major components of a computer system, combining the functions of a data bus to carry information, an address bus to determine memory addresses and a control

→ The connecting channel between CPU, ~~the~~ main memory, various components on motherboard and other peripheral devices is known as system bus

Types of System bus:

① Address bus - Carries Memory address between processor & other components
Width of address bus determines amount of physical address addressable by processor

② Data bus - Width of data bus determines the size of data transferred between two components

③ Control bus - Carries control signals that indicate type of action going to occur

4. List & explain elements of Computer

→ Computer has 3 following main elements:

- Central Processing unit - Performs all the operations for computer
- Memory unit - It stores necessary data
  It is of 2 types:
  - RAM - For storing temporary data
  - ROM - For storing reliable data
- Input / Output devices - These devices provide a user interface to users. Some I/O devices also store data

5. ~~Hab~~ Elaborate evolution of Microprocessor

6. Give the limitations of 8 bit microprocessor

→ · 8 bit microprocessors ~~can~~ has only 8 bit data bus, ~~hence~~ and 16 bit address line which limits data ~~transfer~~ transfer rate
· Only 64kB of memory can be used
· It has only 5 flags
· It has no MIN or MAX mode.
· Doesn't support Memory Segmentation or Pipelining
~~· Do~~

Unit 2

1 List Maskable & Non-Maskable interrupts of 8086

→ ~~Non~~ NMI (Non-maskable interrupt) - It is of type 2 interrupt
INTR - It is a maskable interrup

2. Describe register organization of 8086

→ · 8086 has a powerful set of registers known as general purpose registers & special purpose registers.
· All of them are 16 bit registers
· General purpose registers
  · Usable as 8-bit or 16-bit registers
  · They may hold data as variables & store intermediate results or to store offset address
· Special purpose registers
  · These registers are used as segment registers, pointers, index registers or as offset storage registers for particular addressing modes
· 8086 registers:
  · General data registers
  · Segment Registers
  · Pointers & index registers
  · Flag register

3. Describe concept of memory segmentation of 8086

→ - The CPU 8086 is able to access 1MB of physical memory. The complete 1MB of memory can be divided into 16 segments, each of 64 kB size and is addressed by one of the segment register.

- The 16-bit contents of segment register actually Point to the starting location of particular segment. The address of segments may be assigned as 0000H to F000H respectively
- To address a specific memory location ~~while~~ ~~whi~~ within a segment, we need an offset address. The offset address values are from 0000H to FFFFH so that the physical addresses range from 00000H to FFFFFH

4. Draw labeled flag ~~regist~~ register of 8086 & explain function of all flags.

→

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AF	U	PF	U	CF

Undefined

Overflow flag

Direction flag for string instruction

Interrupt enable flag

Trap flag for single step

Sign flag - MSB of result

Zero flag, if result = 0

Auxiliary carry flag for BCD

Parity flag - set if result has even parity

Carry flag set by carry out of MSB

Flags are of 2 types:

- Status flags:
  1. Carry flag - Set whenever there is carry or borrow out of MSB
  2. Parity flag - Set if result has even parity
  3. Auxiliary carry flag - Set if carry generated out of lower nibble
  4. Zero flag - Set if result is 0
  5. Sign flag - Set is MSB of result is 1
  6. Overflow flag - Set if result of signed operation is too large to fit.
- Control flags
  1. Trap flag - Set trace mode i.e. start single stepping mode. MP is interrupted after each instruction to debug program
  2. Interrupt enable flag - Disable / enable INTR interrupt
  3. Direction flag - If it is set, SI & DI are auto-decrementing mode in string operations

5. State all control signal generated by S_0, S_1, S_2 with their function of 8086

→ Control signals generated by S_0, S_1 & S_2 are as follows:

S_2	S_1	S_0	Function
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive (in active)

6.

6. With help of diagram describe physical memory address generation of 8086

→ Formula for physical memory address generation of 8086:

Physical address = Segment address * 10H + Offset address

For example, Segment address → 1005H
Offset address → 5555H
Segment address → 1005H
* (0001 0000 0000 0101)

Shifted left by 4 positions → 0001 0000 0000 0101 0000
+
Offset address (5555H) 0101 0101 0101 0101
Physical address (15A5AH) → 0001 0101 0101 1010 0101

7. Describe concept of pipelining in 8086

→ Following are features of 8086 pipelining

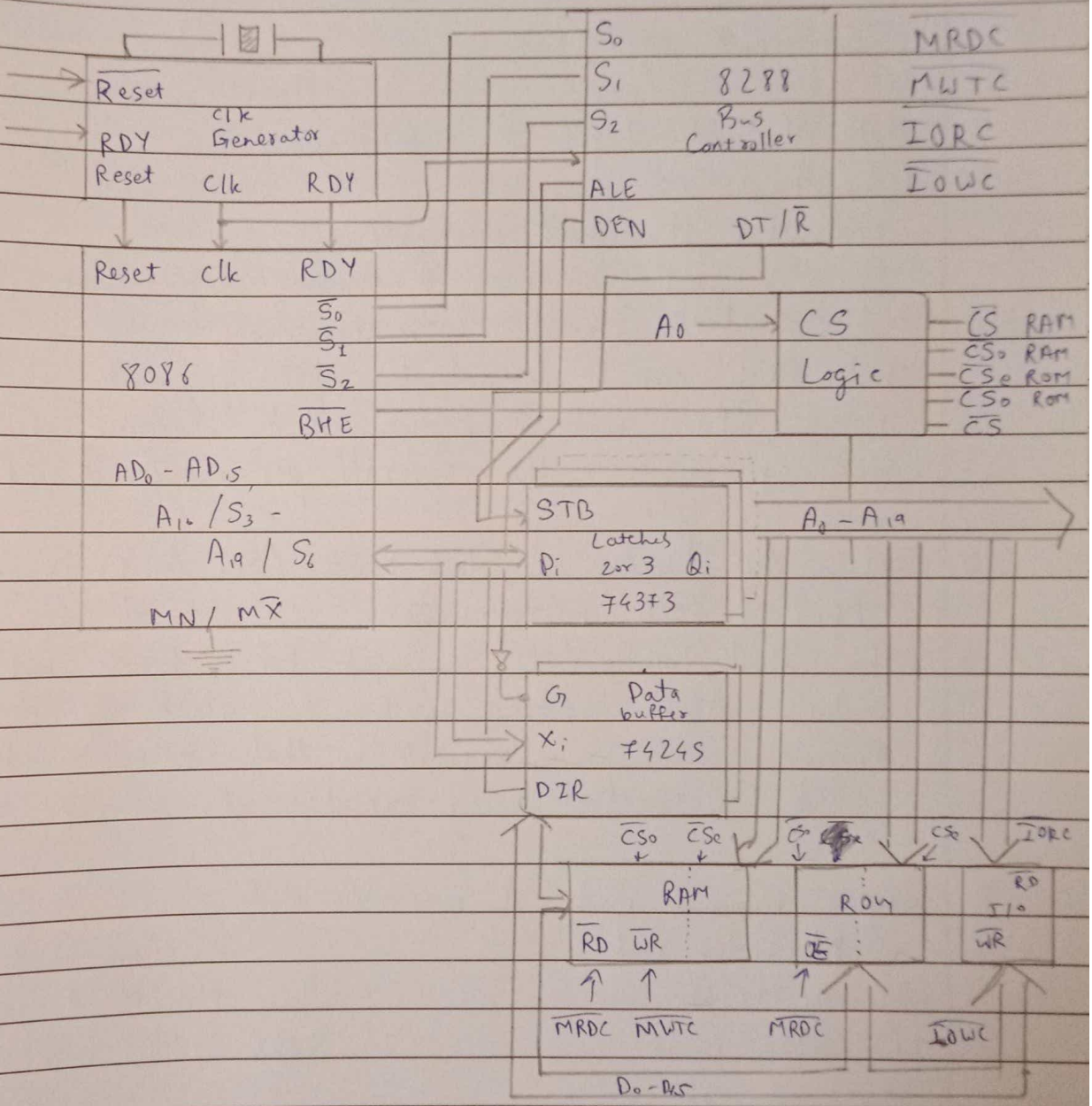
- While EU is decoding or executing an instruction, which doesn't require use of buses, BIU fetches up to six instruction bytes for following instructions.
- The BIU stores these pre-fetched bytes in first-in-first-out register set called a queue.
- When EU is ready for its next instruction from the queue in the BIU.
- Except in case of JMP & CALL instructions where queue is dumped & then reloaded starting from a new address, this pre-fetch & queue scheme greatly speeds up processing.

∴ Fetching the next instruction while current instruction executes is called pipeling

8. With diagram explain Maximum mode 8086 configuration

→ • In maximum mode, 8086 is operated by strapping MN/MX' pin to ground. In this mode, processor derives status signals S2', S1' & S0'. Another chip called bus controller derives the control signals using status information

- In the maximum mode, there may be more than one microprocessor in the system configuration. The other components in the system are same as in minimum mode system.
- Basic functions of bus controller chip IC8288, is to derive control signals like RD' & WR' (for memory & I/O devices) DEN, DT/R', ALE, etc using information made available by processor on status lines $\overline{INTA}$



- $\overline{IORC}$, $\overline{IOWC}$ are I/O read command & I/O write command signals respectively. These signals enable an I/O interface to read or write the data for or to addressed port. The $\overline{MRDC}$, $\overline{MWTC}$ are memory read command & memory write command signals respectively & may

be used as memory read & write signals. All these commands signals instruct the memory to accept or send data from or to the bus

- The maximum mode system timing diagrams are also divided in 2 portions as read (input) & write (output) timing diagrams. The address/data & address/status timings are similar to minimum mode. ALE is asserted in T1, just like minimum mode. The only difference lies in the status signals used & the available control & advanced command signals.

9. State the advantages & pipelining.

→ Advantages:

- Instruction throughput increases
- Increase in the number of pipeline stages increases number of instructions executed simultaneously.
- Faster ALU can be designed when pipelining is used.
- Pipelined CPU's work at higher clock frequencies than RAM
- Pipelining increases the overall performance of CPU.

10. Explain the function of Stack pointer (SP) & program Counter (PC) of 8085 microprocessor

→ - The Stack Pointer (SP) is ~~used to indicate~~ register contains offset address within the stack segment.
- Program counter is a register ~~is~~ that contains address of instruction being executed at current time

11. Compare minimum mode & maximum mode

→

Maximum mode	Minimum mode
• When MN/MX' is low, 8086 is in Maximum mode	• When MN/MX' is high, 8086 is in minimum mode
• In this mode, 8086 generates QS_1, QS_0, $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$, $\overline{Lock}$, $\overline{RQ}$, GT1, $\overline{RG}$, GT0 control signals	• In this mode, 8086 generates $\overline{INTA}$, ALE, $\overline{DEN}$, $\overline{DT/R}$, $M/\overline{IO}$ HLDA, HOLD & $\overline{WR}$ control signals

Maximum mode	Minimum mode
- There are multiple processes in the System - In maximum mode, master/ slave & multiplexing & several such control signals are required	- There is only one processor in system - In minimum mode, no interfacing or master/slave signal is required.

12. State the function of BHE & A_0 pins of 8086

→ - The BHE (Bus High enable) is used to indicate transfer of data using data bus D8-D15.
- A_0 is analogous to BHE for lower byte of data bus. 8-bit oriented devices tied to lower half use A_0 to condition chip select functions

These lines are active high & float to tri-state during interrupt acknowledge & local bus "Hold acknowledge"

5. Elaborate evolution of Microprocessor

Year	Name	Transistors	Data Width	Clock Speed
1974	8080	6000	8 bits	2 MHz
1976	8085	65,000	8 bits	5 MHz
1978	8086	29,000	16 bits	5 MHz
1982	80286	134,000	16 bits	6 MHz
1985	80386	275,000	32 bits	16 MHz
1989	80486	1,200,000	32 bits	25 MHz
1993	Pentium	3,100,000	32/64 bits	60 MHz
1997	Pentium II	7,500,000	64 bits	233 MHz
1999	Pentium III	9,500,000	64 bits	450 MHz
2000	Pentium IV	42,000,000	64 bits	1.5 GHz
2003	Pentium M	140,000,000	64 bits	2.13 GHz
2005	Pentium D	376,000,000	64 bits	3.73 GHz
2006	Core 2 Duo	291,000,000	64 bits	1.2 GHz - 3 GHz
2007	Core2 Quad	410,000,000	64 bits	2.4 GHz
2009	Intel core i5 - 750	774,000,000	64 bits	2.6 GHz
2010	Intel core i5 - 430M	382,000,000	64 bits	2.6 GHz
2010	Intel core i3 - 530	382,000,000	64 bits	2.93 GHz

Page No.
Date

Year	Name	Transistors	Data width	Clock Speed
2010	Intel Core i3-330M	382,000,000	64 bits	2.13 GH
2017	Intel Core i9-7940X	-	64 bits	4.30 GH
2017	Intel Core i9-8950HX	-	64 bits	4.80 GHz
2019	Intel Core i5-10210u	-	64 bits	4.2 GHz
2019	Intel Core i3-1005G1	-	64 bits	3.6 GHz
2019	Intel Core i3-9100F	-	64 bits	4.2 GHz
2019	Intel Core i5-9300H	189,000,000	64 bits	3.80 GH
2020	Intel Core i7-10700	-	64 bits	4.80 GHz