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DELHI***

**Department
of
Electronics & Communication Engineering**

Embedded Logic Design(ECE270)

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Lab_5: Design and implement a GCD
Module

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2020220

25-10-2021

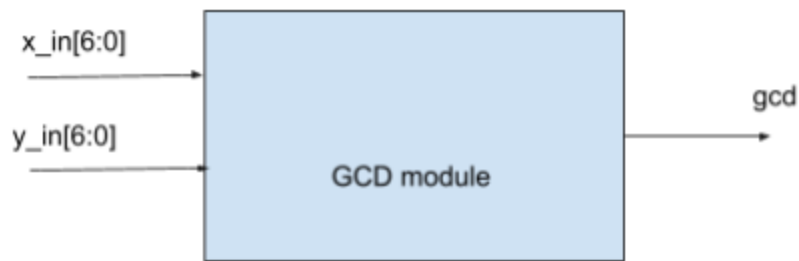
OBJECTIVE:

- GCD code implementation on Vivado

Theory:

GCD Explanation : GCD stands for Greater common divisor. Example : $\text{GCD}(12,8)$, $\text{GCD}(35,49) = 7$

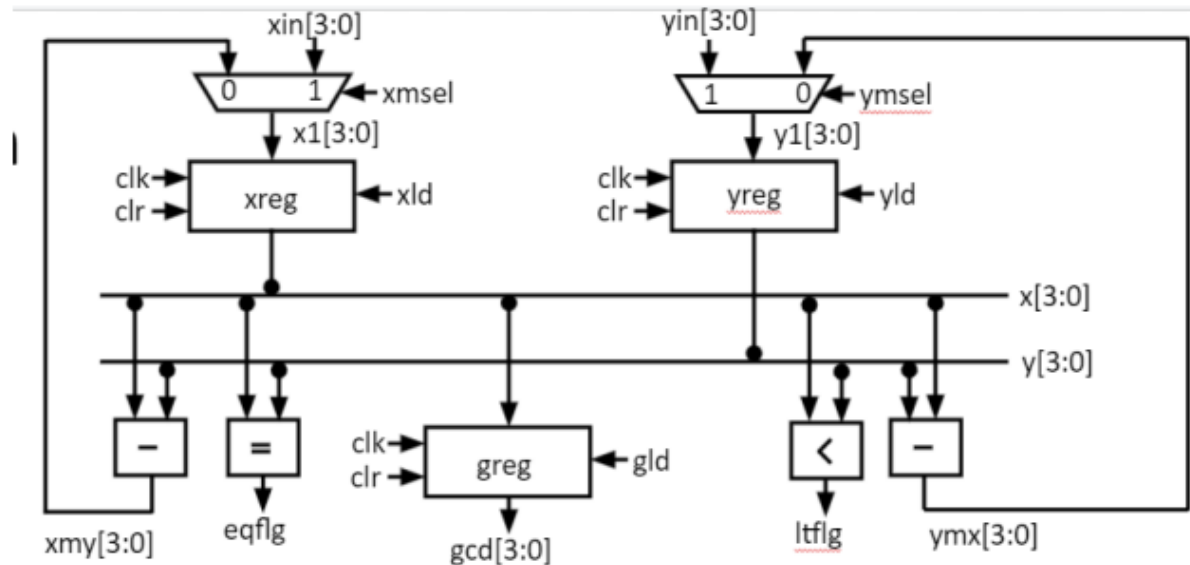
GCD calculation is done by subtracting larger numbers with smaller ones and replacing the larger number with the result of subtraction. Repeat this and stop when both the numbers become equal.



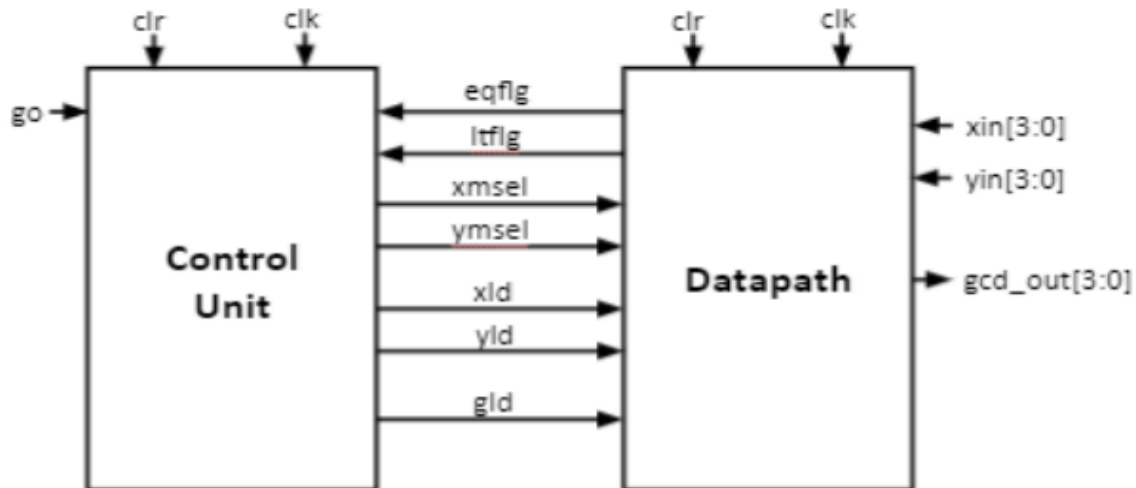
Data Path: Data Processing and operations are done here

Control Path: Gives the control logic signals and makes the Data Path do the tasks needed. The control path is the FSM.

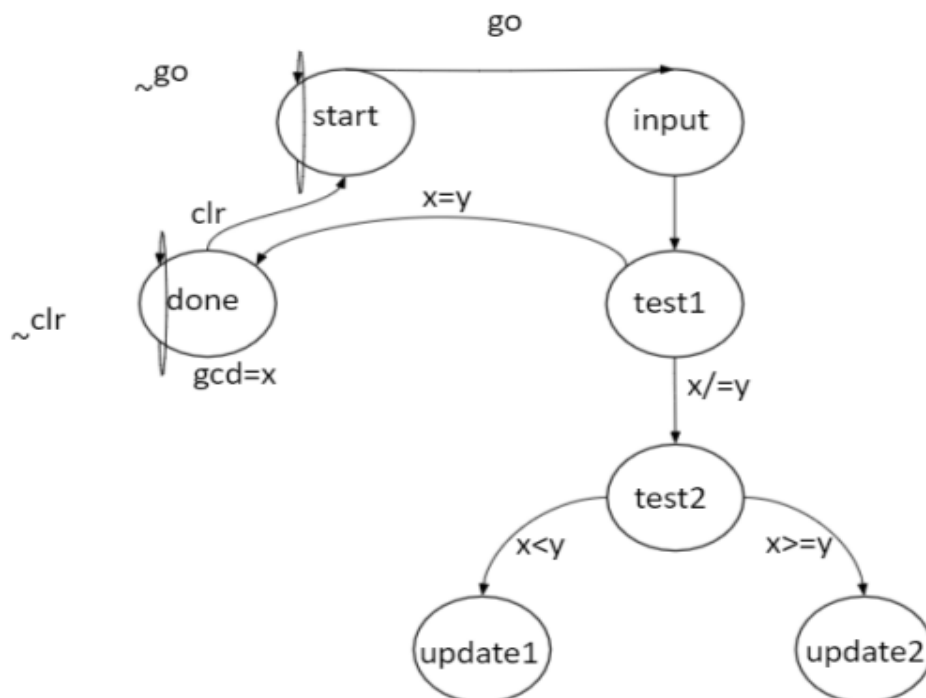
1. We have the registers for both inputs and outputs in the code. They are declared as xreg, yreg and greg. The former two are 3 bits wide, and the latter are one bit wide.
2. Connection of the register is given to the logical and arithmetic operations.
3. Following is the block diagram of the code that we are going to implement in Verilog.



4. To decide the values of xld , yld , clk , clr and gld , we will also make a control unit.

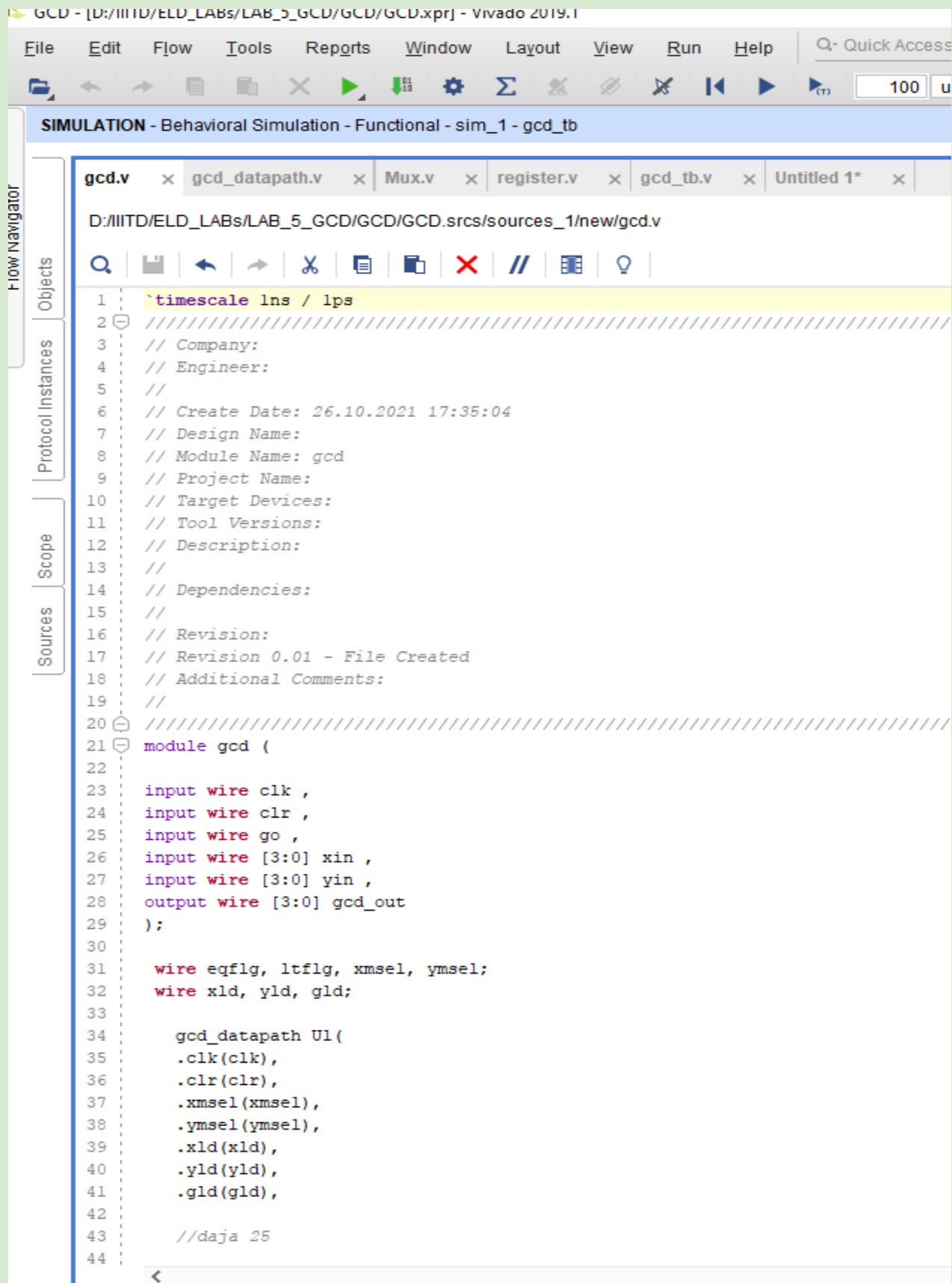


5. The above figure shows the overall control and data transfer
 - a. When `go` is one then data `xin` and `yin` will be loaded into the data path
 - b. If $x=y$ then the controller makes the `gld` = 1 and `x` passed to the output
 - c. if $x < y$ then $y = y - x$ will be loaded to the `yreg` and the other way around for the condition of $x > y$
6. Following is the FSM that we will be implementing for the GCD controller block:-



Observations:

programme for the functionality of GCD



The screenshot displays the Vivado 2019.1 IDE interface. The top menu bar includes File, Edit, Flow, Tools, Reports, Window, Layout, View, Run, and Help. Below the menu is a toolbar with various icons for file operations and simulation. The main window title is "SIMULATION - Behavioral Simulation - Functional - sim_1 - gcd_tb". The left sidebar shows the "Flow Navigator" with tabs for Objects, Protocol Instances, Scope, and Sources. The main editor area shows the source file "gcd.v" with the following code:

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date: 26.10.2021 17:35:04
7  // Design Name:
8  // Module Name: gcd
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////
21 module gcd (
22
23     input wire clk ,
24     input wire clr ,
25     input wire go ,
26     input wire [3:0] xin ,
27     input wire [3:0] yin ,
28     output wire [3:0] gcd_out
29 );
30
31     wire eqflg, ltflg, xmsel, ymsel;
32     wire xld, yld, gld;
33
34     gcd_datapath U1(
35         .clk(clk),
36         .clr(clr),
37         .xmsel(xmsel),
38         .ymsel(ymsel),
39         .xld(xld),
40         .yld(yld),
41         .gld(gld),
42
43         //daja 25
44     )
```

SIMULATION - Behavioral Simulation - Functional - sim_1 - gcd_tb

Flow Navigator

Objects


Protocol Instances

Scope

Sources

gcd.v x gcd_datapath.v x Mux.v x register.v x gcd_tb.v x Untitled 1* x

D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.srscs/sources_1/new/gcd.v



```
36     .clr(clr),
37     .xmsel(xmsel),
38     .ymsel(ymsel),
39     .xld(xld),
40     .yld(yld),
41     .gld(gld),
42
43     //daja 25
44
45     .xin(xin),
46     .yin(yin),
47     .gcd(gcd_out),
48
49     // flags to determine the weather we obtained the GCD or shoukld we keep on going.
50
51     .eqflg(eqflg),
52     .ltflg(ltflg)
53 );
54
55 gcd_control U2(
56
57     .clk(clk),
58     .clr(clr),
59     .go(go),
60
61     //flags to determine whether we obtained the GCD or should we keep going
62
63     .eqflg(eqflg),
64     .ltflg(ltflg),
65
66     // Select line for loading data into reg MUX
67     .xmsel(xmsel),
68     .ymsel(ymsel),
69
70     // load signals
71     .xld(xld),
72     .yld(yld),
73     .gld(gld)
74
75 );
76
77
78 endmodule
```

program for GCD_datapath

GCD - [D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Run Help Q- Quick Access

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SIMULATION - Behavioral Simulation - Functional - sim_1 - gcd_tb

gcd.v x gcd_datapath.v x Mux.v x register.v x gcd_tb.v x Untitled 1* x

D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.srscs/sources_1/new/gcd_datapath.v

Flow Navigator

Objects

Protocol Instances

Scope

Sources

```
19 //
20 //////////////////////////////////////////////////
21
22 module gcd_datapath (
23     input wire clk ,
24     input wire clr ,
25     input wire xmsel ,
26     input wire ymsel,
27     input wire xld ,
28     input wire yld ,
29     input wire gld ,
30     input wire [3:0] xin ,
31     input wire [3:0] yin ,
32     output wire [3:0] gcd ,
33     output reg eqflg = 0,
34     output reg ltflg = 0
35
36 );
37
38
39     wire [3:0] xmy, ymx, gcd_out;
40     wire [3:0] x, y, xl, yl;
41
42     assign xmy = x - y;
43     assign ymx = y - x;
44
45     always @(*)
46     begin
47         if(x == y)
48             eqflg = 1;
49
50         else
51             eqflg=0;
52     end
53
54     mux2g #(
55         .N(4))
56
57     M1(.a(xmy),
58         .b(xin),
59         .s(xmsel),
60         .y(xl)
61     );
62     mux2g #(
```

SIMULATION - Behavioral Simulation - Functional - sim_1 - gcd_tb

gcd.v x gcd_datapath.v x Mux.v x register.v x gcd_tb.v x Untitled 1* x

D:/IITD/ELD_LABs/LAB_5_GCD/GCD/GCD.srscs/sources_1/new/gcd_datapath.v



```
60         .y(x1)
61     );
62     mux2g #(
63         .N(4))
64
65     M2(.a(ymx),
66        .b(yin),
67        .s(ymse1),
68        .y(y1)
69     );
70
71     register #(
72         .N(4))
73     R1 (.load(xld),
74         .clk(clk),
75         .clr(clr),
76         .d(x1),
77         .q(x)
78     );
79
80     register #(
81         .N(4))
82     R2 (.load(yld),
83         .clk(clk),
84         .clr(clr),
85         .d(y1),
86         .q(y)
87     );
88
89     register #(
90         .N(4))
91     R3 (.load(gld),
92         .clk(clk),
93         .clr(clr),
94         .d(x),
95         .q(gcd_out)
96     );
97
98
99
100     assign gcd= gcd_out;
101
102 endmodule
```


program for MUX

GCD - [D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.xpr] - Vivado 2019.1

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SIMULATION - Behavioral Simulation - Functional - sim_1 - gcd_tb

Flow Navigator

Objects

Protocol Instances

Scope

Sources

gcd.v x gcd_datapath.v x **Mux.v** x register.v x gcd_tb.v x Untitled 1* x

D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.srscs/sources_1/new/Mux.v

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date: 26.10.2021 23:17:28
7  // Design Name:
8  // Module Name: mux2g
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
22
23 module mux2g
24
25     #(parameter N=4)
26     (
27     input wire [N-1:0] a,
28     input wire [N-1:0] b,
29     input wire s,
30     output reg [N-1:0] y=0
31
32     );
33
34     always@(*)
35     begin
36         if (s==0)
37             y=a;
38         else
39             y=b;
40     end
41
42 endmodule
```

program for Register

GCD - [D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Run Help

SIMULATION - Behavioral Simulation - Functional - sim_1 - gcd_tb

Flow Navigator

gcd.v x gcd_datapath.v x Mux.v x **register.v** x gcd_tb.v x

D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.srscs/sources_1/new/register.v

Q [Save] [Undo] [Redo] [Cut] [Copy] [Paste] [Delete] [Comment] [Uncomment] [Find]

```
1 timescale 1ns / 1ps
2 //////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 26.10.2021 23:13:36
7 // Design Name:
8 // Module Name: register
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////
21
22
23 module register
24 #(parameter N=8)
25 (input wire load,
26 input wire clk,
27 input wire clr,
28 input wire [N-1:0] d,
29 output reg [N-1:0] q=0
30 );
31
32 always @(posedge clk or posedge clr)
33 begin
34     if (clr == 1)
35         q<=0;
36     else if (load == 1)
37         q<=d;
38     end
39
40 endmodule
41
```

Testbench for GCD

GCD - [D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.xpr] - Vivado 2019.1

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100 us

SIMULATION - Behavioral Simulation - Functional - sim_1 - gcd_tb

gcd.v x gcd_datapath.v x Mux.v x register.v x gcd_tb.v x Untitled 1* x

D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.srscs/sim_1/new/gcd_tb.v

Q [Icons]

```
1 timescale 1ns / 1ps
2 //////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 26.10.2021 23:23:43
7 // Design Name:
8 // Module Name: gcd_tb
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////
21
22
23 module gcd_tb(
24
25     );
26
27     reg clk, clr , go ;
28     reg [3:0] xin ,yin;
29     wire [3:0] gcd_out;
30
31     gcd U4(
32         .clk(clk),
33         .go(go),
34         .xin(xin),
35         .yin(yin),
36         .gcd_out(gcd_out)
37
38     );
39
40
41     initial
42     begin
43         clk =1'b0;
44         clr= 1'b0;
```



SIMULATION - Behavioral Simulation - Functional - sim_1 - gcd_tb

Flow Navigator

Objects

Protocol Instances

Scope

Sources

gcd.v x gcd_datapath.v x Mux.v x register.v x gcd_tb.v

D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.srscs/sim_1/new/gcd_tb.v



```
36      .gcd_out(gcd_out)
37
38
39  );
40
41  initial
42  begin
43      clk = 1'b0;
44      clr = 1'b0;
45      go = 1'b0;
46      xin = 4'b0000;
47      yin = 4'b0000;
48  end
49
50  always #10 clk = ~clk;
51
52  initial
53  begin
54      @(negedge clk);
55      clr = 1;
56      @(negedge clk);
57      clr = 1'b0;
58      go = 1'b1;
59      xin = 4'b0011;
60      yin = 4'b0110;
61      @(negedge clk);
62      @(negedge clk);
63      @(negedge clk);
64      @(negedge clk);
65      @(negedge clk);
66      @(negedge clk);
67      @(negedge clk);
```

GCD - [D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.xpr] - Vivado 2019.1

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SIMULATION - Behavioral Simulation - Functional - sim_1 - gcd_tb

gcd.v x gcd_datapath.v x Mux.v x register.v x gcd_tb.v x

D:/IIITD/ELD_LABs/LAB_5_GCD/GCD/GCD.srscs/sim_1/new/gcd_tb.v

Flow Navigator

Objects

Protocol Instances

Scope

Sources

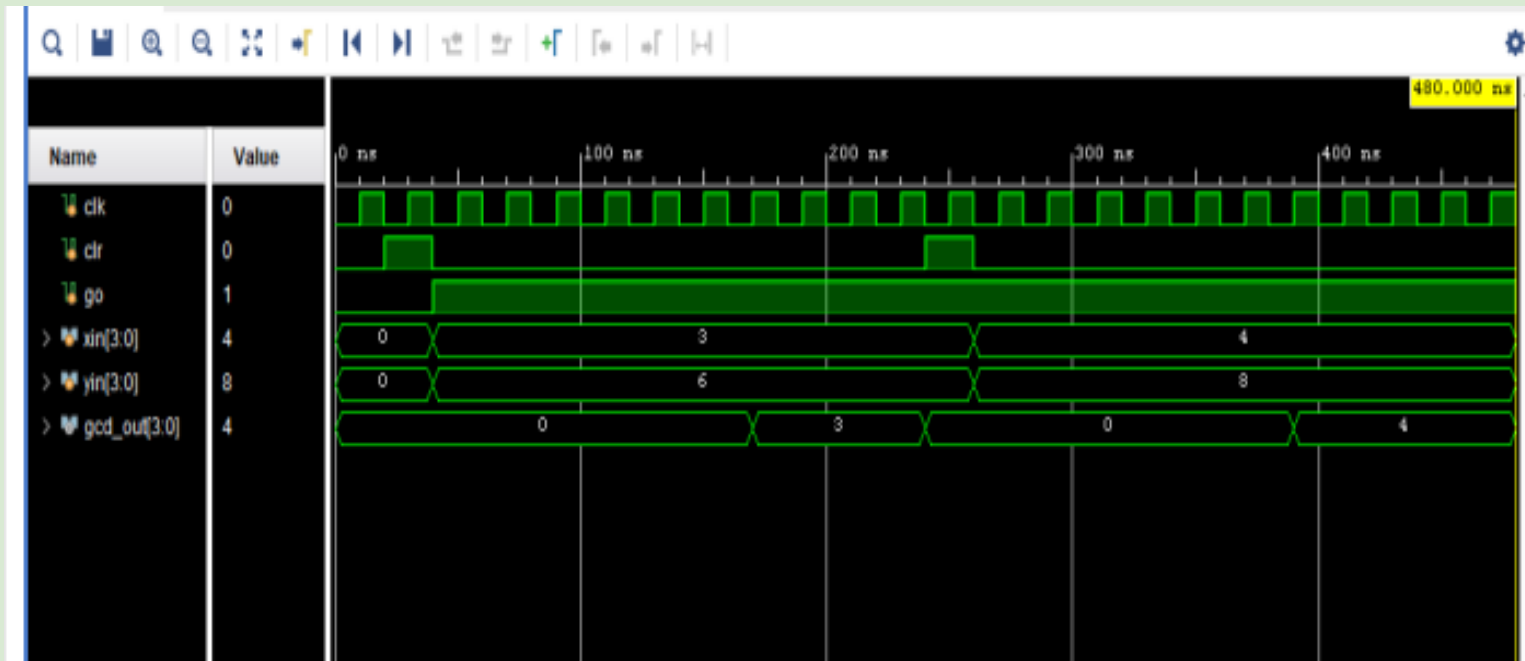
```

54      ○      @(negedge clk);
55      ○      clr = 1 ;
56      ○      @(negedge clk);
57      ○      clr = 1'b0;
58      ○      go = 1'b1;
59      ○      xin = 4'b0011;
60      ○      yin = 4'b0110;
61      ○      @(negedge clk);
62      ○      @(negedge clk);
63      ○      @(negedge clk);
64      ○      @(negedge clk);
65      ○      @(negedge clk);
66      ○      @(negedge clk);
67      ○      @(negedge clk);
68      ○      @(negedge clk);
69      ○      @(negedge clk);
70
71      ○
72      ○      @(negedge clk);
73      ○      clr = 1'b1 ;
74      ○      @(negedge clk);
75      ○      clr = 1'b0;
76      ○      go = 1'b1;
77      ○      xin = 4'b0100;
78      ○      yin = 4'b1000;
79      ○      @(negedge clk);
80      ○      @(negedge clk);
81      ○      @(negedge clk);
82      ○      @(negedge clk);
83      ○      @(negedge clk);
84      ○      @(negedge clk);
85      ○      @(negedge clk);
86      ○      @(negedge clk);
87      ○      @(negedge clk);
88      ○      @(negedge clk);
89      ○      @(negedge clk);
90
91      ○      $finish;
92
93      ○      end
94
95      ○      endmodule
96

```

@negedge is for delay purpose

Results for automated testbench:



Conclusion:

GCD_module has been implemented successfully on vivado.