INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

Department
of
Electronics & Communication Engineering

Embedded Logic Design(ECE270)

Dr. Sumit J Darak

Lab_1: Vivado Design Flow Using 4:2 Encoder

Mohammad Shariq
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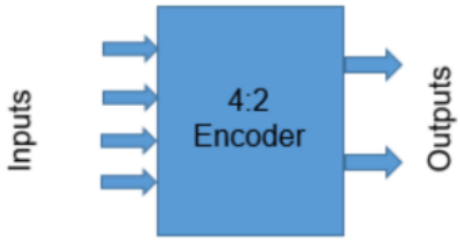
Objective: To implement 4:2 Encoder and verify the functionality

Design FLow:

Theory:

4:2 Encoder



Block Diagram

Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

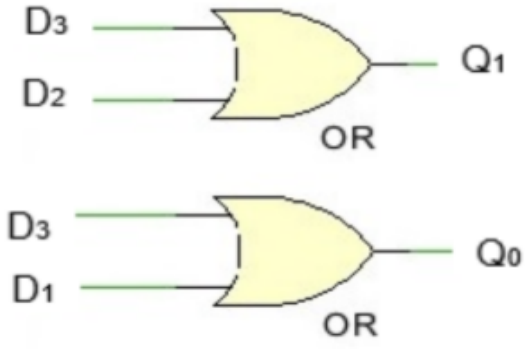
Truth Table

$Q_1 = D_3 + D_2$

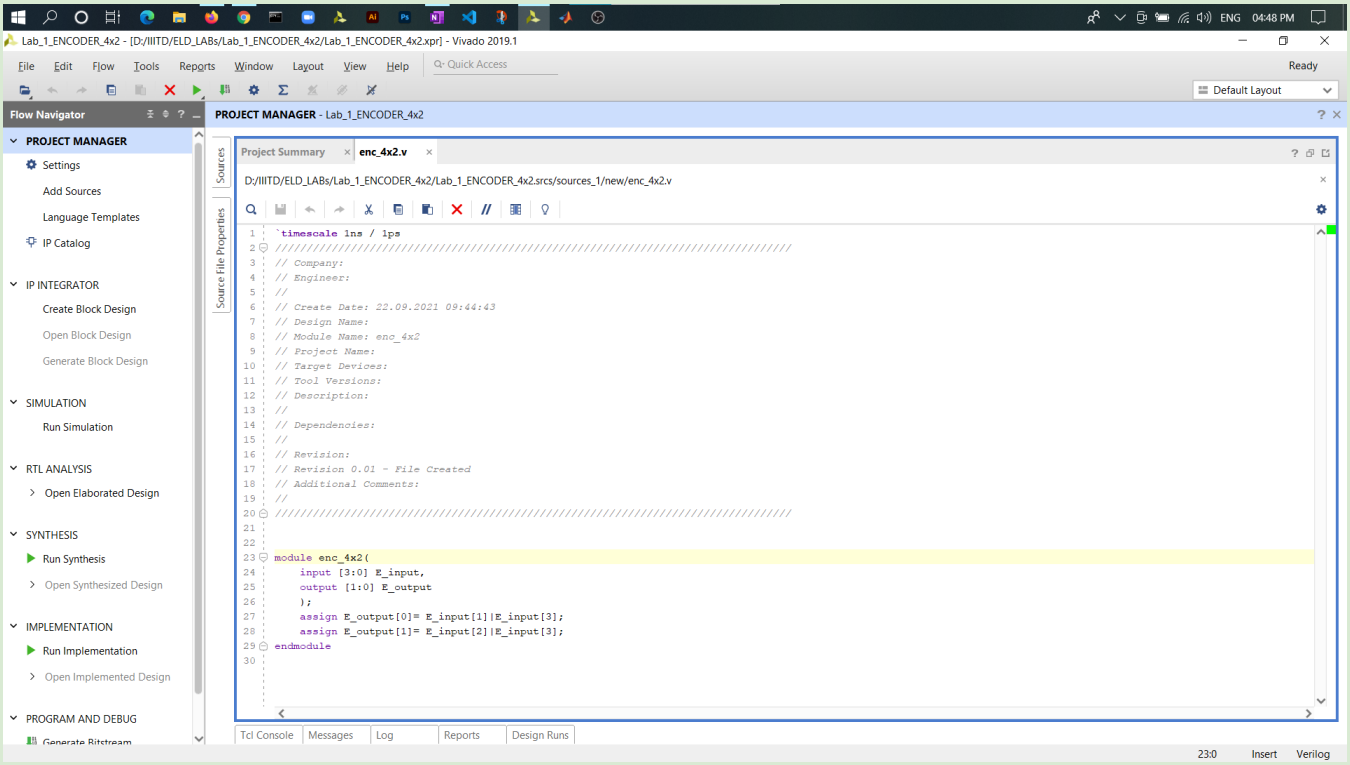
$Q_0 = D_3 + D_1$

An "n-bit" binary encoder has 2^n input lines and n-bit output lines with common types that include 4-to-2, 8-to-3 and 16-to-4 line configurations.

Circuit Diagram:



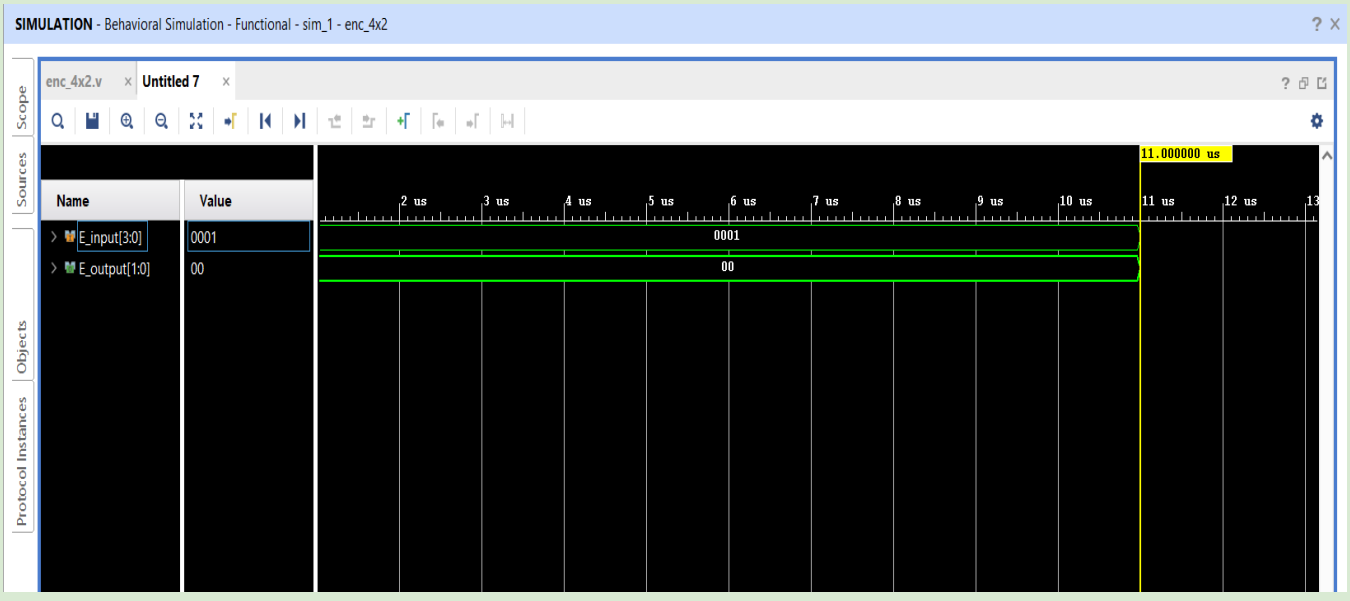
Observations:

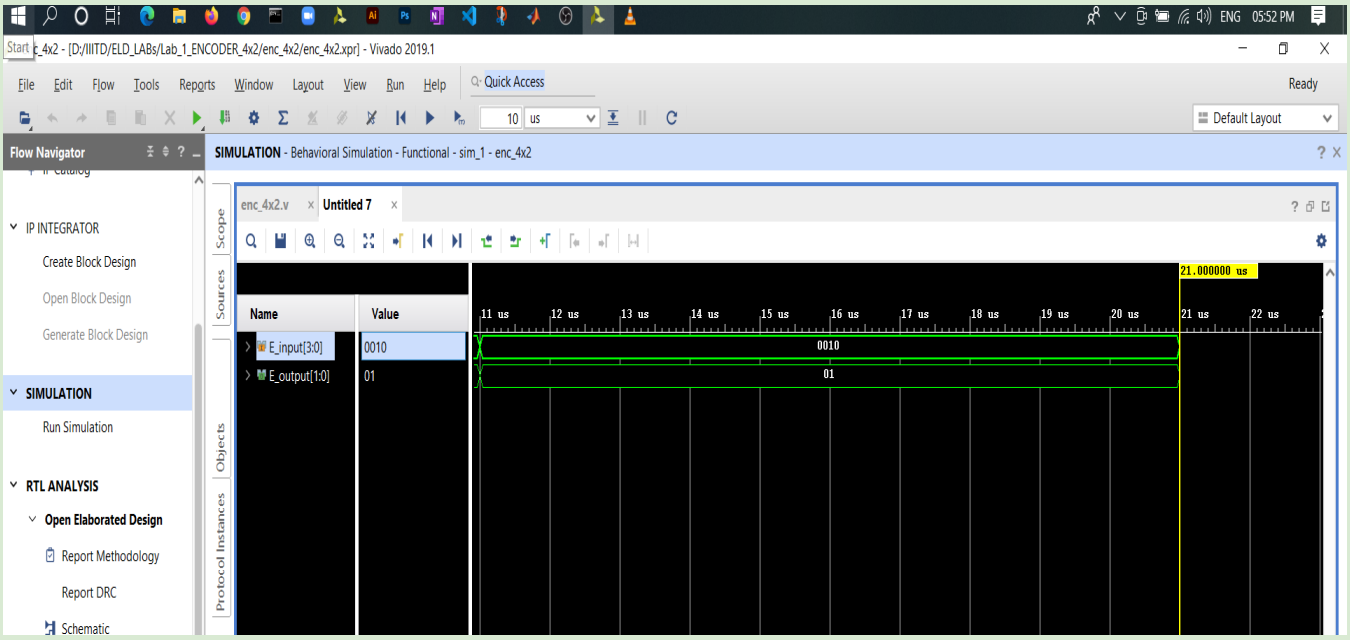


- Since we know that keyword ***input*** in verilog which is a ***reg*** data type and output data type is shown via ***output*** keyword which is a ***wire*** data type.

- In the above Verilog code we designed a 4x2 encoder in the module ***enc_4x2*** declared variable E_input for taking input from users manually or automated. Similarly we declared a variable E_output for showing our output.

For Manual Input:



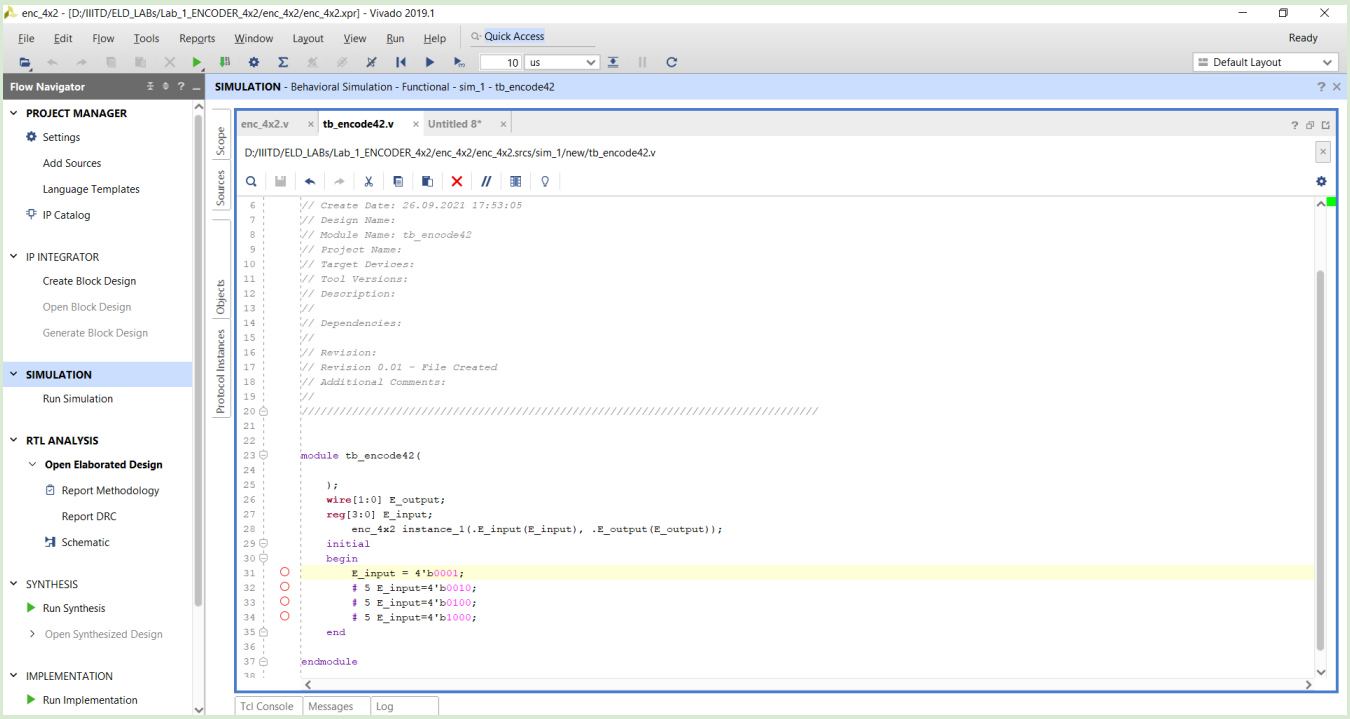


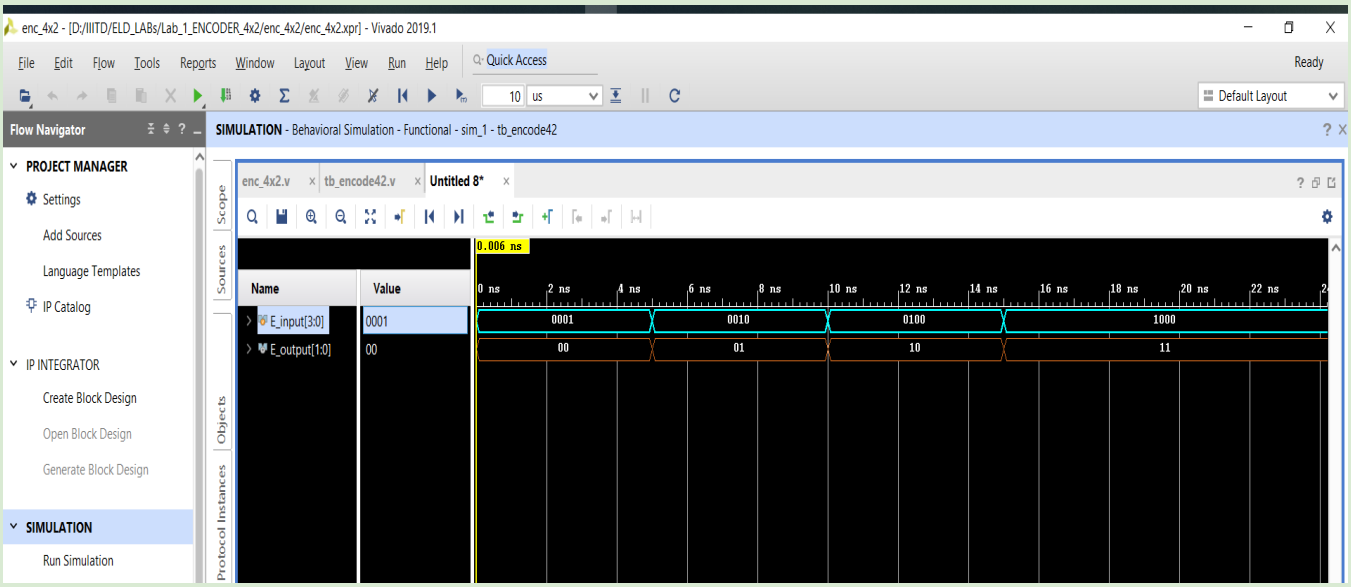
We manually input our data by forcing constants in the verilog code in the simulation and running the simulation for a period of time.

For Testbench:

- We can manually give inputs for testing for a short data,but for a large data we like to automate it using a testbench file.

- for the above verilog code we created a testbench file in the simulation folder using add sources and tested our verilog code for inputs *0001,0010,0100,1000* after creating a *instance for enc_4x2* source code module after creating a *tb_encode42* module in our testbench file.





Conclusion:

- In the manual input testing when we force constant 0001 we get output as 00 and for 0010 we get 01 which satisfies the conditions according to the truth table above and our logic expression.

- In the automated testing we get outputs 00,01,10,11 for 0001,0010,0100,1000 respectively which satisfies the conditions of our logical expression and truth-table.