ECE270: Embedded Logic Design

End-Semester Lab Exam

Date: 29/12/2021

Time: 1 pm – 4.45 pm

Deadline-> Between 4.45 pm : 5 pm (Google Classroom) : **Submissions after 5 pm will NOT be accepted**

Plagiarism: F grade for first instance as per the Institute policy

Submission Requirements: Submit single PDF with all the solutions.

Total Marks: 15 Marks + 2 Bonus Marks

Question 1. Consider the design of accelerator which take input X and produces the output Y. The relationship between X and Y is given as:

$$Y = \left(\ln\left(\frac{1}{\sqrt{X}}\right)\right)$$

Design the accelerator for realization in FPGA, integrate it with the Microblaze processor using direct memory access (DMA).

Demonstrate the functionality of the accelerator which receives the input from DMA and send the processed data back to DMA. The DMA is configured via Microblaze. The DMA reads the data from Block RAM and stores the processed data back to same Block RAM. The size of an input data is 10 elements with arbitrarily chosen positive integer values.

Submit the PDF containing following details:

1) Explanation of accelerator design
2) Block diagram in Vivado (screenshot)
3) C-Code in SDK with comments (screenshot)
4) Testbench with comments (screenshot)
5) Simulation waveforms demonstrating DMA configuration by Microblaze processor (screenshot)
6) Simulation waveforms demonstrating DMA to Accelerator transactions (screenshot)
7) Simulation waveforms demonstrating Accelerator to DMA transactions (screenshot)

Your solution will not be evaluated if any of these deliverables are missing.

10 Marks

Question 2. Modify the design in Question 1 as per the following requirements and submit the solution in the same format as Question 1:

- Use separate Block RAM to send the data to DMA and accelerator and another block RAM to store the processed data from accelerator and DMA.

5 Marks

Question 3. Modify the design in Question 2 as per the following requirements and submit the solution in the same format as Question 1:

- The relationship between input and output is

$$Y = \left(\ln\left(\frac{1}{\sqrt{X}}\right)\right) + 10$$

2 Marks