



***INDRAPRASTHA INSTITUTE of  
INFORMATION TECHNOLOGY  
DELHI***

**Department  
of  
Electronics & Communication Engineering**

Embedded Logic Design(ECE270)

Dr. Sumit J Darak

**Lab\_7:** FFT IP Implementation and test bench.

**Mohammad Shariq**

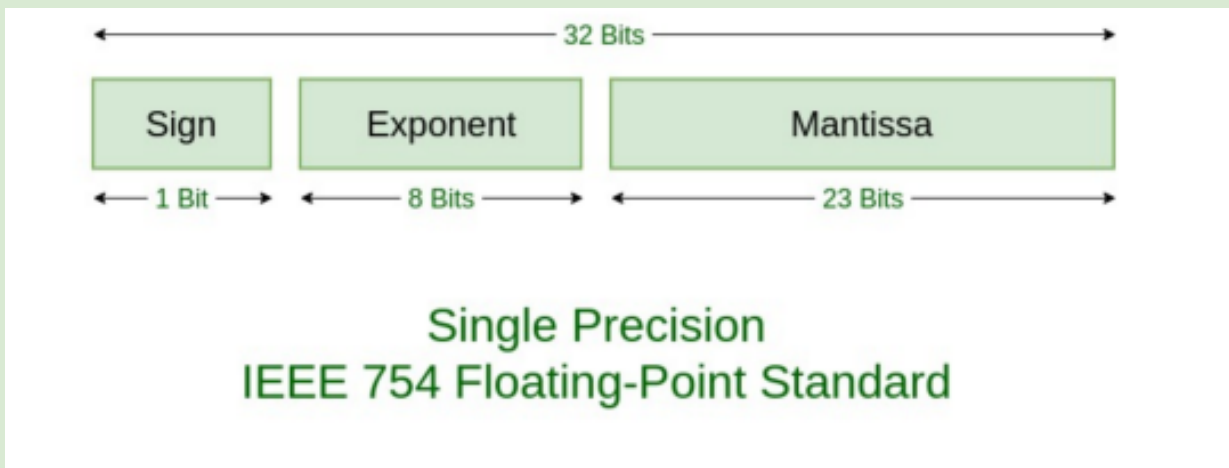
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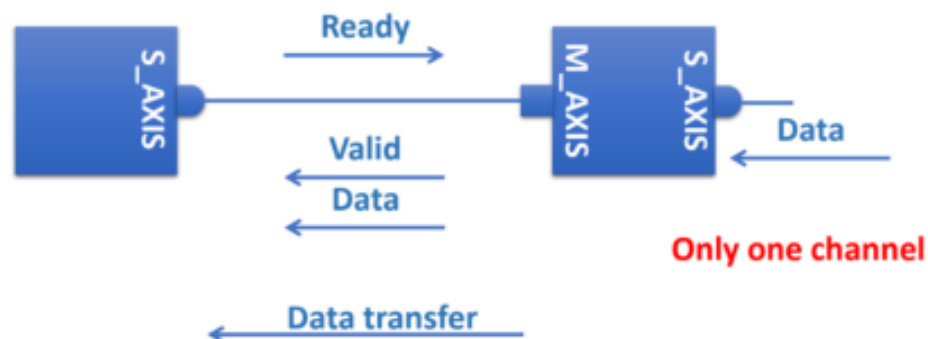
## OBJECTIVE:

- AXI Stream Protocol Use
- Floating Point IP usage
- FFT IP Implementation and test bench.

## Theory:



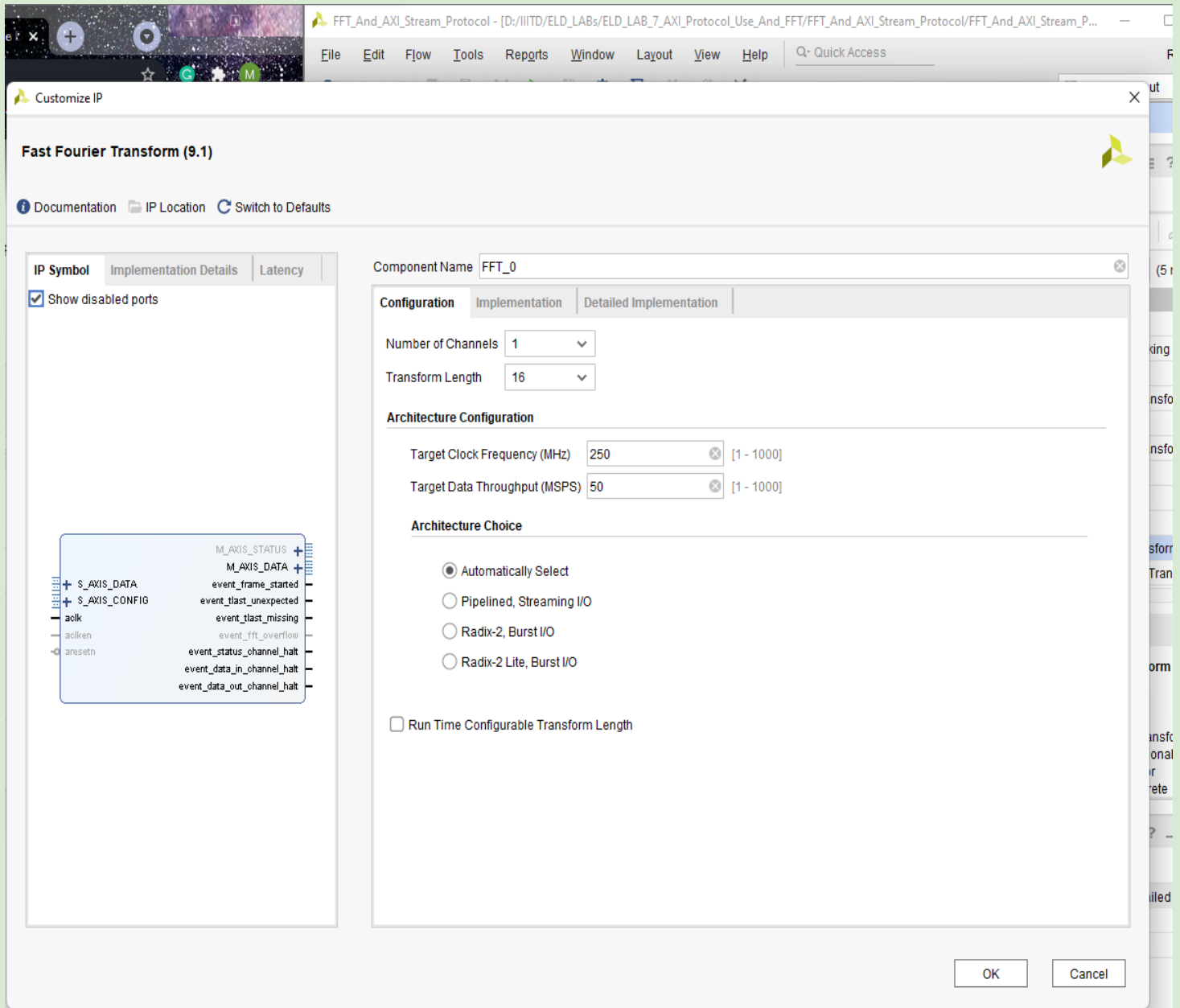
The Floating-point IP will be using the AXI Protocols (AXI Stream in particular). Two concepts that will be useful in this Lab are Master-Slave and Valid Ready Signals. In AXI, the transactions take place between Master and Slave, as shown below:



The AXI Master initiates the transactions, and the slave responds to it. Many signals are associated with a transaction out of which the valid and ready signals are useful for this Lab. More information on these signals is covered in the Lab tutorial video.

### Observations:

### ### *FFT IP Wizard :*



## Fast Fourier Transform (9.1)

[Documentation](#) [IP Location](#) [Switch to Defaults](#)

## IP Symbol

## Implementation Details

## Latency

☒ Show disabled ports

Component Name FFT\_0

## Configuration

## Implementation

## Detailed Implementation

Data Format Floating Point

Scaling Options Scaled

Rounding Modes Truncation

## Precision Options

Input Data Width 32

Phase Factor Width 24

## Control Signals

☐ ACLKEN ☒ ARESETn (active low)

ARESETn must be asserted for a minimum of 2 cycles

## Output Ordering Options

Output Ordering Natural Order

☐ Cyclic Prefix Insertion

## Optional Output Fields

## Throttle Scheme

☐ XK\_INDEX ☐ OVFO☒ Non Real Time ☐ Real Time

OK

Cancel

Fast Fourier Transform (9.1)

[Documentation](#) [IP Location](#) [Switch to Defaults](#)

IP Symbol

Implementation Details

Latency

Information

implementation :  
                    Pipelined, Streaming I/O

Transform Size

Largest :  
Smallest :  
Output Data Width :

16  
16  
32

Resource Estimates Group

DSP48 Slices :  
Block RAMs :

8  
2

AXI4 Stream Port Structure

S\_AXIS\_DATA - TDATA

Transaction	Field	Type
0	CHAN_0_XN_IM_0(63:32)	float_single
	CHAN_0_XN_RE_0(31:0)	float_single
1	CHAN_0_XN_IM_1(63:32)	float_single
	CHAN_0_XN_RE_1(31:0)	float_single
2	CHAN_0_XN_IM_2(63:32)	float_single
	CHAN_0_XN_RE_2(31:0)	float_single
3	CHAN_0_XN_IM_3(63:32)	float_single
	CHAN_0_XN_RE_3(31:0)	float_single
...		
15	CHAN_0_XN_IM_15(63:32)	float_single
	CHAN_0_XN_RE_15(31:0)	float_single

S\_AXIS\_CONFIG - TDATA

Component Name FFT\_0

Configuration

Implementation

Detailed Implementation

Number of Channels

1

Transform Length

16

Architecture Configuration

Target Clock Frequency (MHz)

250

[1 - 1000]

Target Data Throughput (MSPS)

50

[1 - 1000]

Architecture Choice

☒ Automatically Select

☐ Pipelined, Streaming I/O

☐ Radix-2, Burst I/O

☐ Radix-2 Lite, Burst I/O

☐ Run Time Configurable Transform Length

# Fast Fourier Transform (9.1)

[Documentation](#)
[IP Location](#)
[Switch to Defaults](#)

IP Symbol	Implementation Details	Latency
2	CHAN_0_XN_IM_2(63:32)	float_single
	CHAN_0_XN_RE_2(31:0)	float_single
3	CHAN_0_XN_IM_3(63:32)	float_single
	CHAN_0_XN_RE_3(31:0)	float_single
...		
15	CHAN_0_XN_IM_15(63:32)	float_single
	CHAN_0_XN_RE_15(31:0)	float_single

**S\_AXIS\_CONFIG - TDATA**

Transaction	Field	Type
0	SCALE_SCH_0(4:1)	bit4
	FWD_INV_0(0:0)	bit1

**M\_AXIS\_DATA - TDATA**

Transaction	Field	Type
0	CHAN_0_XN_IM_0(63:32)	float_single
	CHAN_0_XN_RE_0(31:0)	float_single
1	CHAN_0_XN_IM_1(63:32)	float_single
	CHAN_0_XN_RE_1(31:0)	float_single
2	CHAN_0_XN_IM_2(63:32)	float_single
	CHAN_0_XN_RE_2(31:0)	float_single
3	CHAN_0_XN_IM_3(63:32)	float_single
	CHAN_0_XN_RE_3(31:0)	float_single
...		
15	CHAN_0_XN_IM_15(63:32)	float_single
	CHAN_0_XN_RE_15(31:0)	float_single

Component Name
 FFT\_0

Configuration	Implementation	Detailed Implementation
---------------	----------------	-------------------------

Number of Channels
 1

Transform Length
 16

**Architecture Configuration**

Target Clock Frequency (MHz)
 250
 [1 - 1000]

Target Data Throughput (MSPS)
 50
 [1 - 1000]

**Architecture Choice**

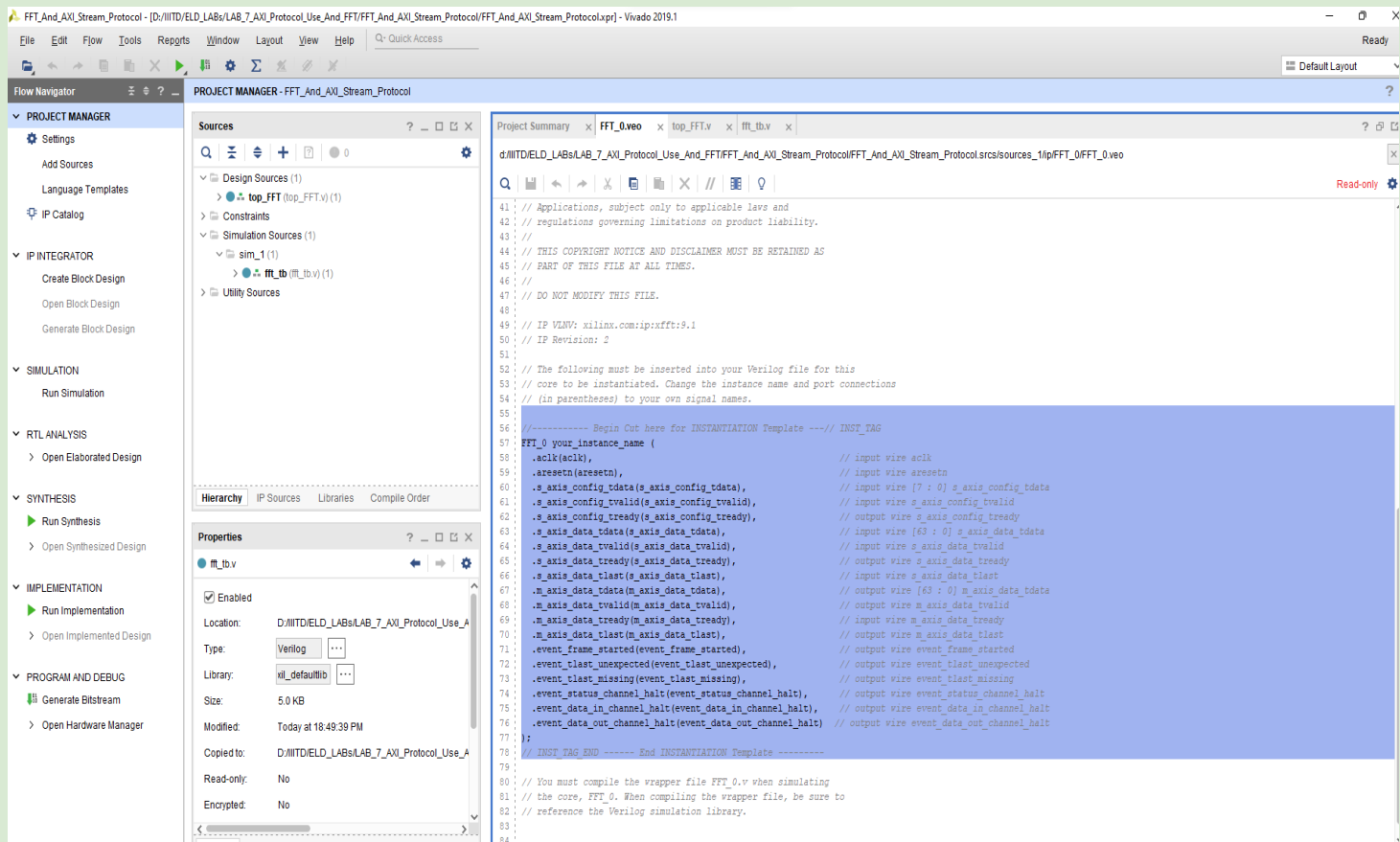
☒ Automatically Select

☐ Pipelined, Streaming I/O

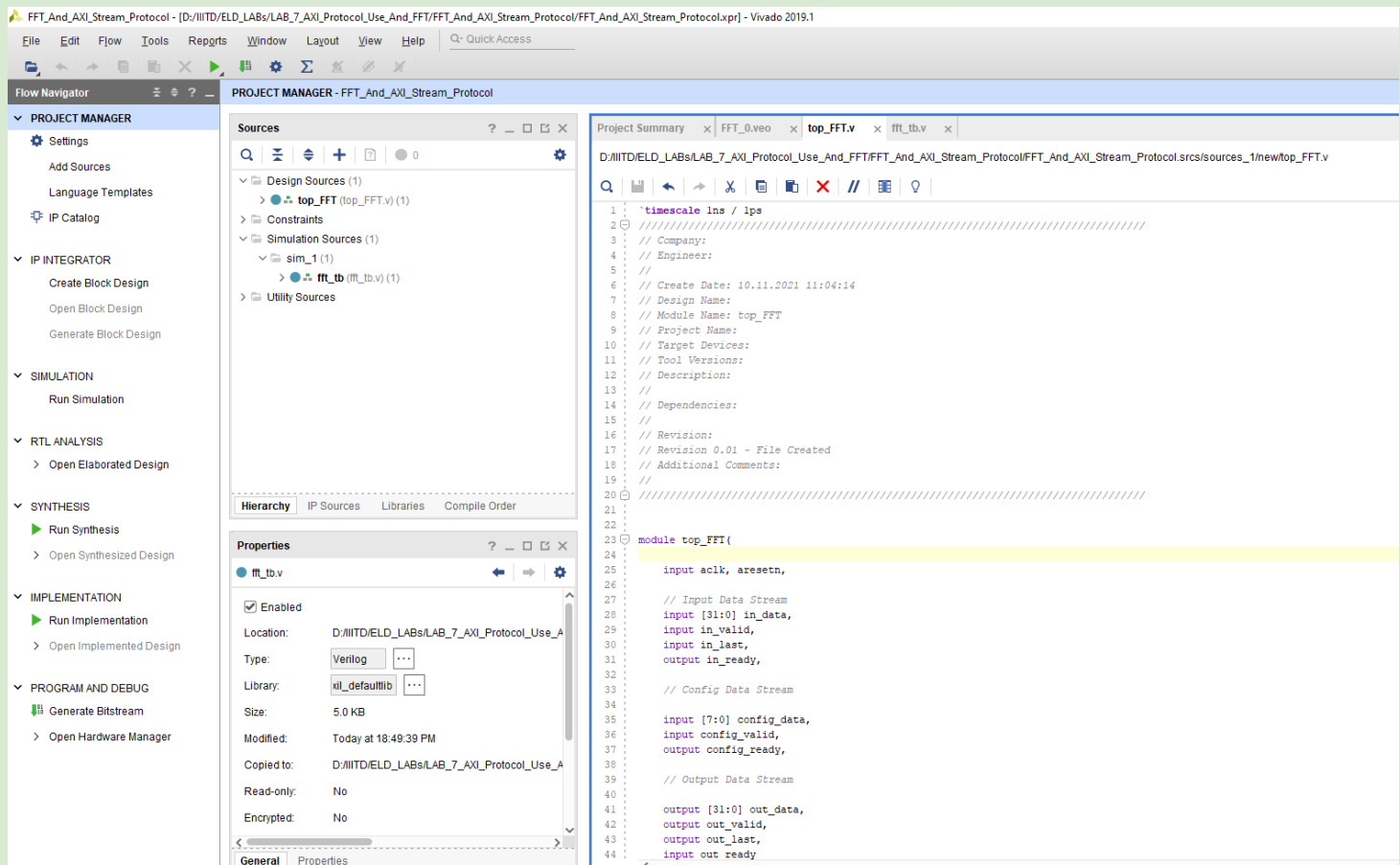
☐ Radix-2, Burst I/O

☐ Radix-2 Lite, Burst I/O

☐ Run Time Configurable Transform Length



## # programme for the functionality of FFT (FastFourier Transform)



## PROJECT MANAGER

- Settings
  - Add Sources
  - Language Templates
- IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

## Sources

- Design Sources (1)
  - top\_FFT (top\_FFT.v) (1)
- Constraints
- Simulation Sources (1)
  - sim\_1 (1)
    - fft\_tb (fft\_tb.v) (1)
- Utility Sources

## Hierarchy

## IP Sources

## Libraries

## Compile Order

## Properties

## fft\_tb.v

## Enabled

Location: D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_A

Type: Verilog

Library: xil\_defaultlib

Size: 5.0 KB

Modified: Today at 18:49:39 PM

Copied to: D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_A

Read-only: No

Encrypted: No

## Project Summary

## FFT\_0.veo

## top\_FFT.v

## fft\_tb.v

## D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_And\_FFT/FFT\_And\_AXI\_Stream\_Protocol/FFT\_And\_AXI\_Stream\_Protocol.srscs/sources\_1/newtop\_FFT.v

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40
41     output [31:0] out_data,
42     output out_valid,
43     output out_last,
44     input out_ready
45
46
47 ):
48
49
50 wire [63:0] data_fft; // FFT IP takes 64 bit data, so padding the upper 32 bit's with 0's
51
52 assign data_fft[63:0] = 32'd0;
53 assign data_fft[31:0] = in_data; // Read data from the user using input stream
54
55 wire [63:0] out_fft; // Output of FFT is 64 bit
56
57
58 // Additional Event Signals
59 wire
60     event_frame_started,
61     event_tlast_unexpected,
62     event_tlast_missing,
63     event_status_channel_halt,
64     event_data_in_channel_halt,
65     event_data_out_channel_halt ;
66
67
68
69 //----- Begin Cut here for INSTANTIATION Template ----- INST_TAG
70 FFT_0 fft0 (
71     .aclk(aclk), // input wire aclk
72     .aresetn(aresetn), // input wire aresetn
73
74     .s_axis_config_tdata(config_data), // input wire [7 : 0] s_axis_config_tdata
75     .s_axis_config_tvalid(config_valid), // input wire s_axis_config_tvalid
76     .s_axis_config_tready(config_ready), // output wire s_axis_config_tready
77
78     .s_axis_data_tdata(data_fft), // input wire [63 : 0] s_axis_data_tdata
79     .s_axis_data_tvalid(in_valid), // input wire s_axis_data_tvalid
80     .s_axis_data_tready(in_ready), // output wire s_axis_data_tready
81     .s_axis_data_tlast(in_last), // input wire s_axis_data_tlast
82
```

## PROJECT MANAGER

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## fft\_tb.v

## Enabled

Location: D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_A

Type: Verilog

Library: xil\_defaultlib

Size: 5.0 KB

Modified: Today at 18:49:39 PM

Copied to: D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_A

Read-only: No

Encrypted: No

## Project Summary

## FFT\_0.veo

## top\_FFT.v

## fft\_tb.v

## D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_And\_FFT/FFT\_And\_AXI\_Stream\_Protocol/FFT\_And\_AXI\_Stream\_Protocol.srscs/sources\_1/newtop\_FFT.v

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```
60     event_frame_started,
61     event_tlast_unexpected,
62     event_tlast_missing,
63     event_status_channel_halt,
64     event_data_in_channel_halt,
65     event_data_out_channel_halt ;
66
67
68
69 //----- Begin Cut here for INSTANTIATION Template ----- INST_TAG
70 FFT_0 fft0 (
71     .aclk(aclk), // input wire aclk
72     .aresetn(aresetn), // input wire aresetn
73
74     .s_axis_config_tdata(config_data), // input wire [7 : 0] s_axis_config_tdata
75     .s_axis_config_tvalid(config_valid), // input wire s_axis_config_tvalid
76     .s_axis_config_tready(config_ready), // output wire s_axis_config_tready
77
78     .s_axis_data_tdata(data_fft), // input wire [63 : 0] s_axis_data_tdata
79     .s_axis_data_tvalid(in_valid), // input wire s_axis_data_tvalid
80     .s_axis_data_tready(in_ready), // output wire s_axis_data_tready
81     .s_axis_data_tlast(in_last), // input wire s_axis_data_tlast
82
83     .m_axis_data_tdata(out_fft), // output wire [63 : 0] m_axis_data_tdata
84     .m_axis_data_tvalid(out_valid), // output wire m_axis_data_tvalid
85     .m_axis_data_tready(out_ready), // input wire m_axis_data_tready
86     .m_axis_data_tlast(out_last), // output wire m_axis_data_tlast
87
88     .event_frame_started(event_frame_started), // output wire event_frame_started
89     .event_tlast_unexpected(event_tlast_unexpected), // output wire event_tlast_unexpected
90     .event_tlast_missing(event_tlast_missing), // output wire event_tlast_missing
91     .event_status_channel_halt(event_status_channel_halt), // output wire event_status_channel_halt
92     .event_data_in_channel_halt(event_data_in_channel_halt), // output wire event_data_in_channel_halt
93     .event_data_out_channel_halt(event_data_out_channel_halt) // output wire event_data_out_channel_halt
94 );
95 // INST_TAG_END ----- End INSTANTIATION Template -----
96
97 assign out_data = out_fft[31:0]; // Lower 32 bits being dispalyed.As real Part is needed
98
99
100
101 endmodule
102
```



# Testbench for FFT:

FFT\_And\_Axi\_Stream\_Protocol - [D:/IITD/ELD\_LABs/LAB\_7\_Axi\_Protocol\_Use\_And\_FFT/FFT\_And\_Axi\_Stream\_Protocol/FFT\_And\_Axi\_Stream\_Protocol.xpr] - Vivado 2019.1

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Flow Navigator PROJECT MANAGER - FFT\_And\_Axi\_Stream\_Protocol

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Sources

- Design Sources (1)
  - top\_FFT (top\_FFT.v) (1)
- Constraints
- Simulation Sources (1)
  - sim\_1 (1)
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- Utility Sources

Hierarchy IP Sources Libraries Compile Order

Properties

fft\_tb.v

- Enabled
- Location: D:/IITD/ELD\_LABs/LAB\_7\_Axi\_Protocol\_Use\_A
- Type: Verilog
- Library: xil\_defaultlib
- Size: 5.0 KB
- Modified: Today at 18:49:39 PM
- Copied to: D:/IITD/ELD\_LABs/LAB\_7\_Axi\_Protocol\_Use\_A
- Read-only: No
- Encrypted: No

Project Summary x FFT\_0.vco x top\_FFT.v x fft\_tb.v x

D:/IITD/ELD\_LABs/LAB\_7\_Axi\_Protocol\_Use\_And\_FFT/FFT\_And\_Axi\_Stream\_Protocol/FFT\_And\_Axi\_Stream\_Protocol.srcs/sim\_1/new/fft\_tb.v

```
1 timescale 1ns / 1ps
2 // Company:
3 // Engineer:
4 //
5 // Create Date: 16.11.2021 17:58:29
6 // Design Name:
7 // Module Name: fft_tb
8 // Project Name:
9 // Target Devices:
10 // Tool Versions:
11 // Description:
12 //
13 // Dependencies:
14 //
15 // Revision:
16 // Revision 0.01 - File Created
17 // Additional Comments:
18 //
19 //
20 //
21
22
23 module fft_tb();
24
25     reg aclk, aresetn;
26
27     // making reg types for Inputs
28     reg [31:0] in_data;
29     reg in_valid;
30     reg in_last;
31     wire in_ready; // wire for outputs for all groups of streams Signals
32
33
34     reg [7:0] config_data;
35     reg config_valid;
36     wire config_ready;
37
38
39
40     wire [31:0] out_data;
41     wire out_valid;
42     wire out_last;
43     reg out_ready;
```

FFT\_And\_Axi\_Stream\_Protocol - [D:/IITD/ELD\_LABs/LAB\_7\_Axi\_Protocol\_Use\_And\_FFT/FFT\_And\_Axi\_Stream\_Protocol/FFT\_And\_Axi\_Stream\_Protocol.xpr] - Vivado 2019.1

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Flow Navigator PROJECT MANAGER - FFT\_And\_Axi\_Stream\_Protocol

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- Location: D:/IITD/ELD\_LABs/LAB\_7\_Axi\_Protocol\_Use\_A
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- Encrypted: No

Project Summary x FFT\_0.vco x top\_FFT.v x fft\_tb.v x

D:/IITD/ELD\_LABs/LAB\_7\_Axi\_Protocol\_Use\_And\_FFT/FFT\_And\_Axi\_Stream\_Protocol/FFT\_And\_Axi\_Stream\_Protocol.srcs/sim\_1/new/fft\_tb.v

```
37
38
39     wire [31:0] out_data;
40     wire out_valid;
41     wire out_last;
42     reg out_ready;
43
44
45     reg [31:0] input_data [15:0]; // creating a ROM , for the input data to the FFT IP
46
47     integer i;
48
49
50     // instantiating top_FFT module
51
52     top_FFT in0(
53         .aclk(aclk),
54         .aresetn(aresetn),
55
56         .in_data(in_data),
57         .in_valid(in_valid),
58         .in_ready(in_ready),
59         .in_last(in_last),
60
61         .config_data(config_data),
62         .config_valid(config_valid),
63         .config_ready(config_ready),
64
65         .out_data(out_data),
66         .out_valid(out_valid),
67         .out_last(out_last),
68         .out_ready(out_ready)
69     );
70
71
72
73     always
74     begin
75         #5 aclk<=aclk; // clock with time period of 10 units
76     end
77
78
```

FFT\_And\_AXI\_Stream\_Protocol - [D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_And\_FFT/FFT\_And\_AXI\_Stream\_Protocol/FFT\_And\_AXI\_Stream\_Protocol.xpr] - Vivado 2019.1

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Flow Navigator PROJECT MANAGER - FFT\_And\_AXI\_Stream\_Protocol

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fft\_tb.v

Enabled

Location: D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_A

Type: Verilog

Library: xil\_defaultlib

Size: 5.0 KB

Modified: Today at 18:49:39 PM

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Read-only: No

Encrypted: No

Project Summary x FFT\_0.vco x top\_FFT.v x fft\_tb.v x

D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_And\_FFT/FFT\_And\_AXI\_Stream\_Protocol/FFT\_And\_AXI\_Stream\_Protocol.srcs/sim\_1/new/fft\_tb.v

```
79 initial
80 begin
81     aclk=0;
82     aresetn=0;
83
84     in_valid = 1'b0;
85     in_data= 32'd0 ;
86     in_last = 1'b0;
87
88
89
90     /* Initialising OUT_READY to 1 , inorder to tell FFT
91        that outputs can be generated whenever ready
92        failure to do so leads to " Back-Pressure"
93    */
94
95     out_ready = 1'b1;
96
97
98     config_data = 8'd0;
99     config_valid= 1'b0;
100
101 end
102
103
104 initial
105 begin
106     #70 // As Reset needs to be activated for atleast 2 cycles we have given 70 units of delay
107     aresetn = 1;
108
109     // input data entered using python
110     input_data[0]= 32'b00100101100010100110001001100101;
111     input_data[1]= 32'b00111110011110001111010111101;
112     input_data[2]= 32'b0011111011110100110001111101;
113     input_data[3]= 32'b001111100010110011100010001;
114     input_data[4]= 32'b001111001010100111001011001101;
115     input_data[5]= 32'b00111110101101010100111010111;
116     input_data[6]= 32'b001111101110011011100001110001;
117     input_data[7]= 32'b001111011010000000111111001001;
118     input_data[8]= 32'b001111011010000000111111001001;
119     input_data[9]= 32'b00111110110011011100001110001;
120     input_data[10]=32'b001111010101010100111010111;
121     input_data[11]=32'b00111100101001110011011001101;
```

FFT\_And\_AXI\_Stream\_Protocol - [D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_And\_FFT/FFT\_And\_AXI\_Stream\_Protocol/FFT\_And\_AXI\_Stream\_Protocol.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

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Hierarchy IP Sources Libraries Compile Order

Properties

fft\_tb.v

Enabled

Location: D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_A

Type: Verilog

Library: xil\_defaultlib

Size: 5.0 KB

Modified: Today at 18:49:39 PM

Copied to: D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_A

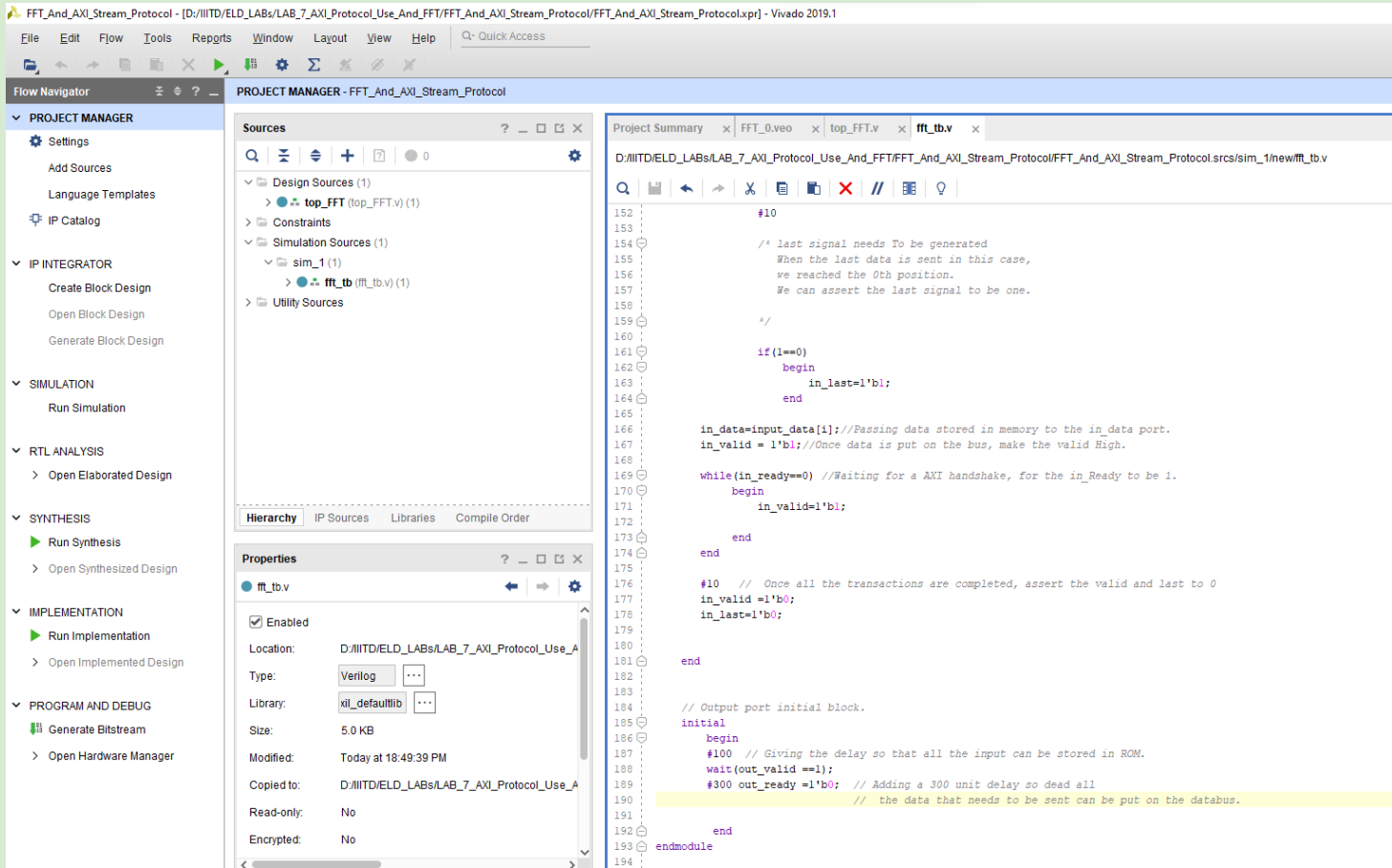
Read-only: No

Encrypted: No

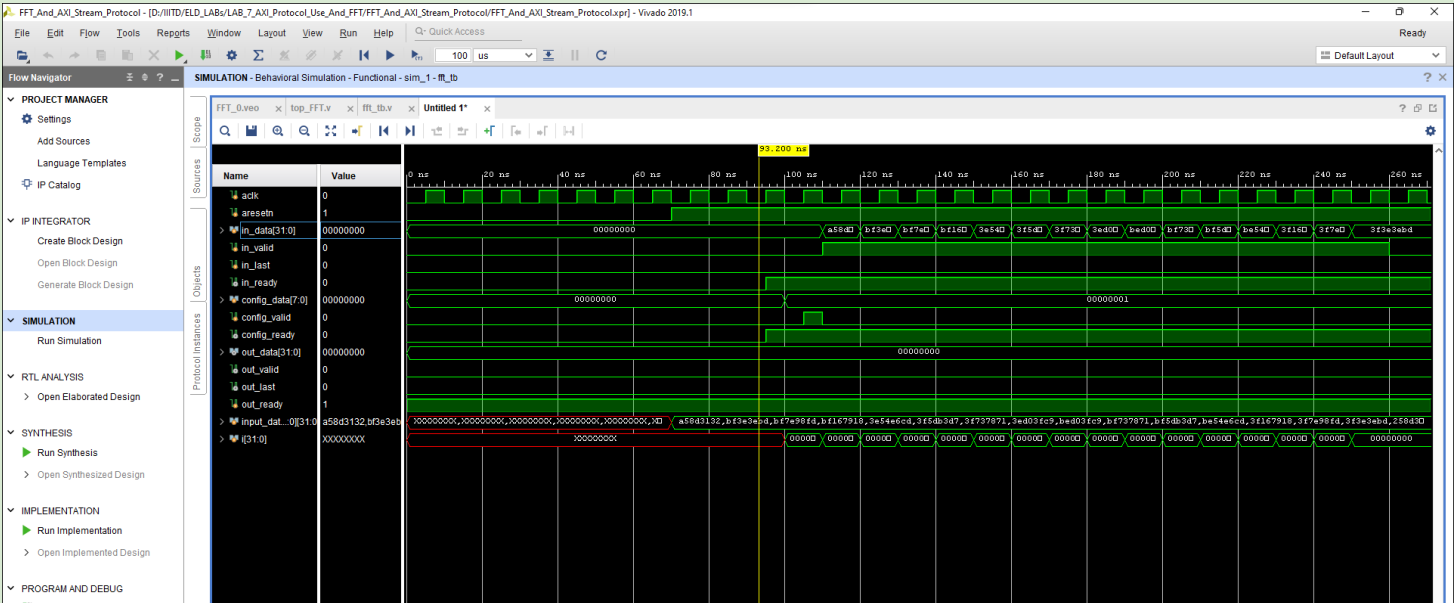
Project Summary x FFT\_0.vco x top\_FFT.v x fft\_tb.v x

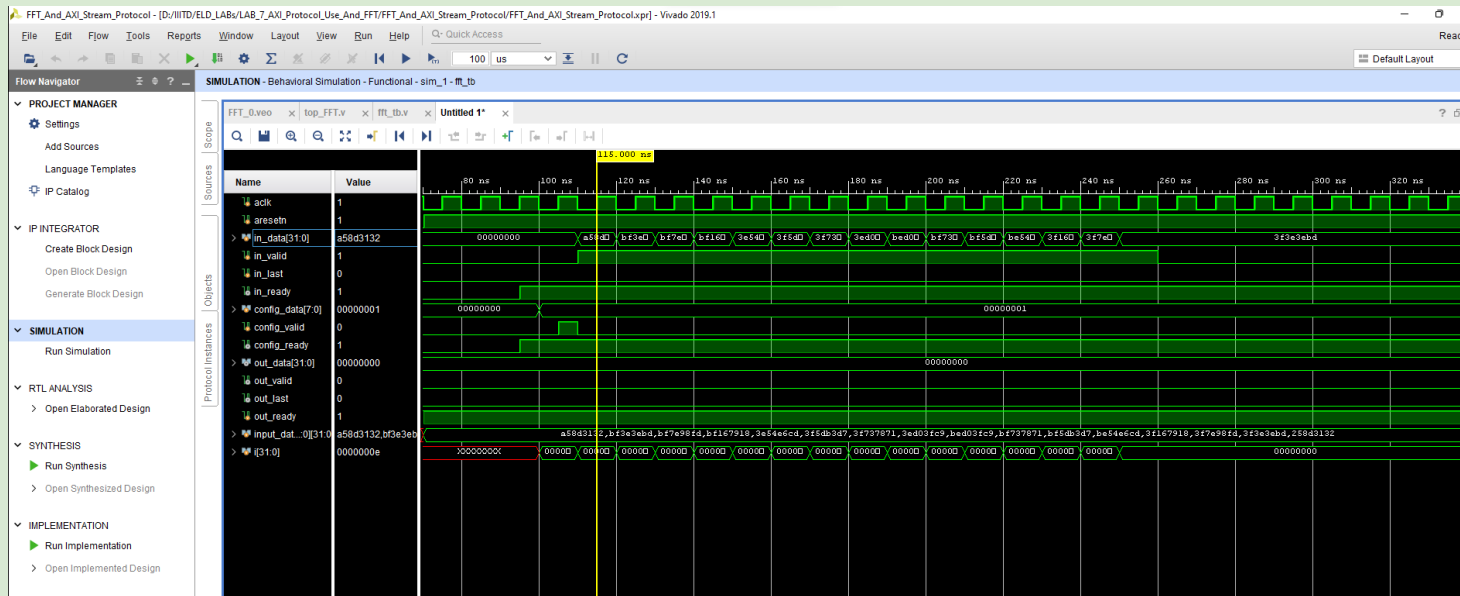
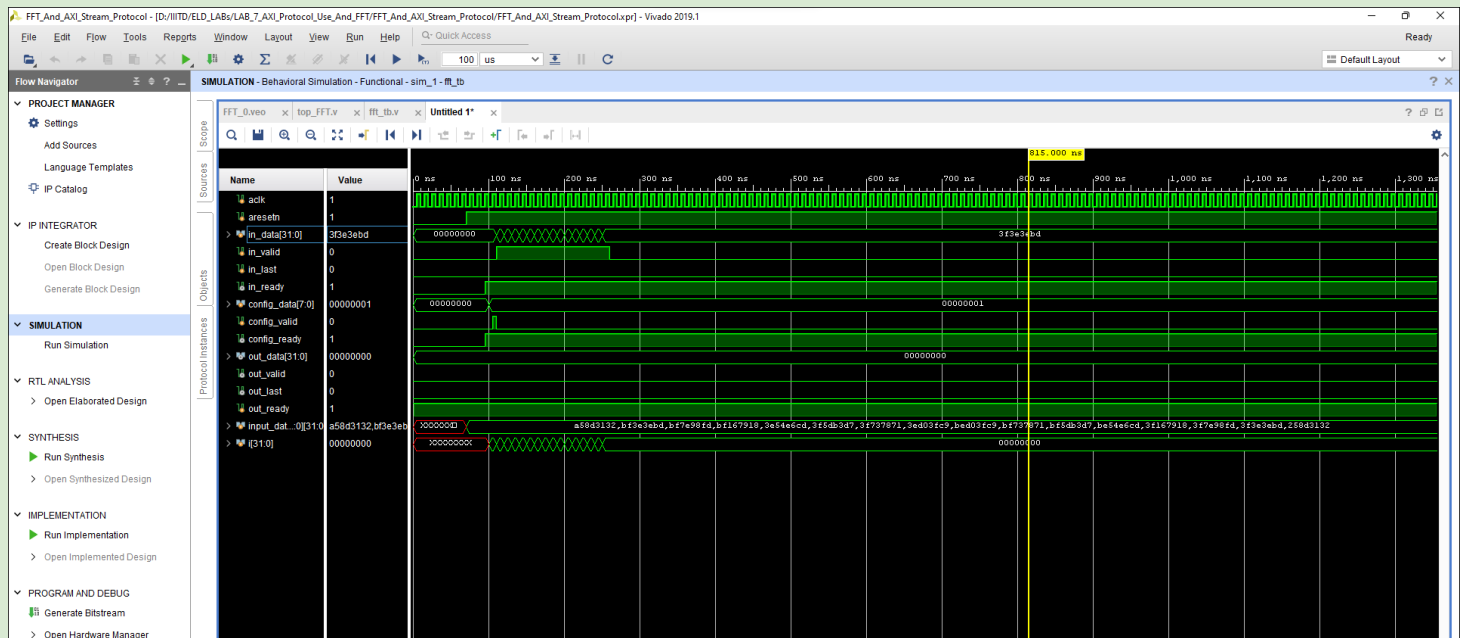
D:/IITD/ELD\_LABs/LAB\_7\_AXI\_Protocol\_Use\_And\_FFT/FFT\_And\_AXI\_Stream\_Protocol/FFT\_And\_AXI\_Stream\_Protocol.srcs/sim\_1/new/fft\_tb.v

```
118 input_data[8]= 32'b001111101010000001111111001001;
119 input_data[9]= 32'b001111101110011011100001110001;
120 input_data[10]=32'b0011111010110101001111010111;
121 input_data[11]=32'b001111001010100111001011001101;
122 input_data[12]=32'b001111100010110011100100011000;
123 input_data[13]=32'b00111110111101001100011111101;
124 input_data[14]=32'b0011111001111000111101011101;
125 input_data[15]=32'b00100101100011010011000100110010;
126
127 end
128
129 // Configuring Data initial Block
130 initial
131 begin
132     #100 config_data =1;
133     #5 config_valid =1;
134
135     while (config_ready == 0)
136     begin
137         config_valid =1;
138     end
139
140     #5 config_valid=0;
141
142 end
143
144
145 // Input Port Initialisation Block
146 initial
147 begin
148
149     #100
150     for(i =15 ; i>0 ; i=i-1)
151     begin
152         #10
153
154         /* last signal needs To be generated
155            When the last data is sent in this case,
156            we reached the 0th position.
157            We can assert the last signal to be one.
158        */
159     end
160 end
```



*Results for automated testbench of FFT :*





## Conclusion:

Successfully designed and implemented FFT IP and its Testbench.