INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

Department
of
Electronics & Communication Engineering

Embedded Logic Design(ECE270)

Dr. Sumit J Darak

Lab_8

Mohammad Shariq
2020220
20-11-2021

OBJECTIVE:

Tasks to be done in this Lab:

1. Create block design in Vivado using the IP Integrator and configure the Zynq IP according to our needs.

2. Create a Hello World application in Xilinx SDK for the ARM processor and learn how to display different kinds of data and take user input using JTAG Terminal.

3. Write a C application to compute the following expression.

X/T + SQRT(2*LogN/T)

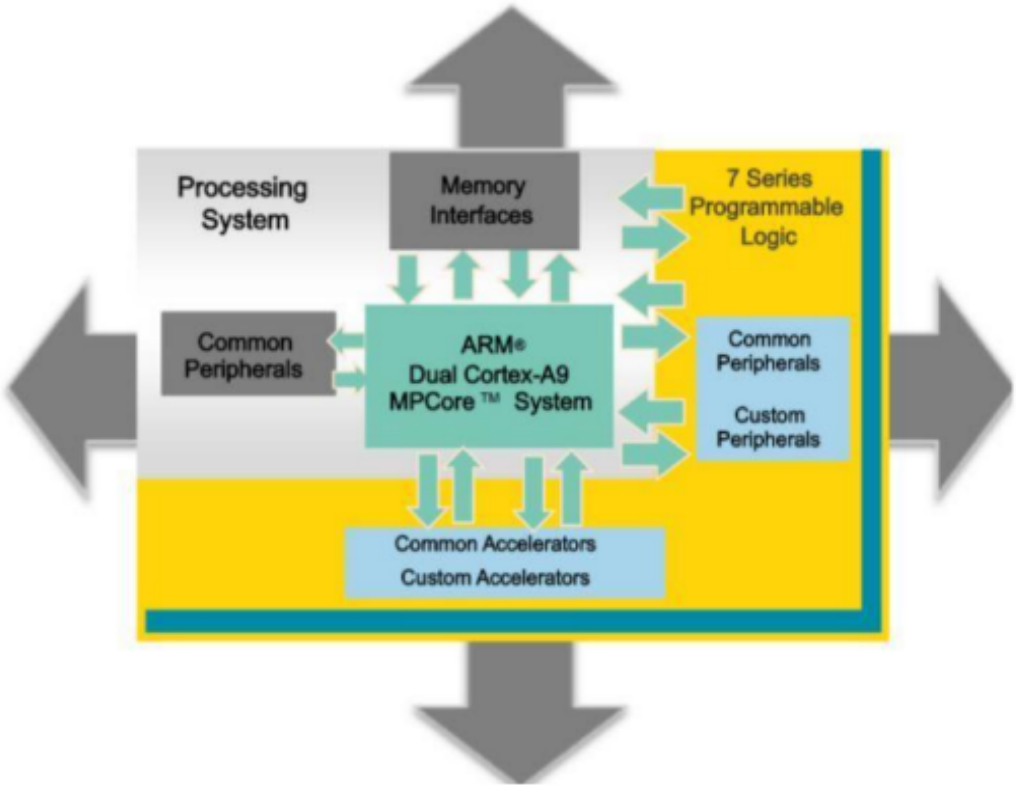
4. Write a C application to compute 8-point FFT.

Topics to explore:

1) Vivado's IP Integrator
2) Zynq Architecture
3) SDK design flow
4) JTAG terminal
5) Integer and floating point number handling
6) 8-point FFT

Theory:

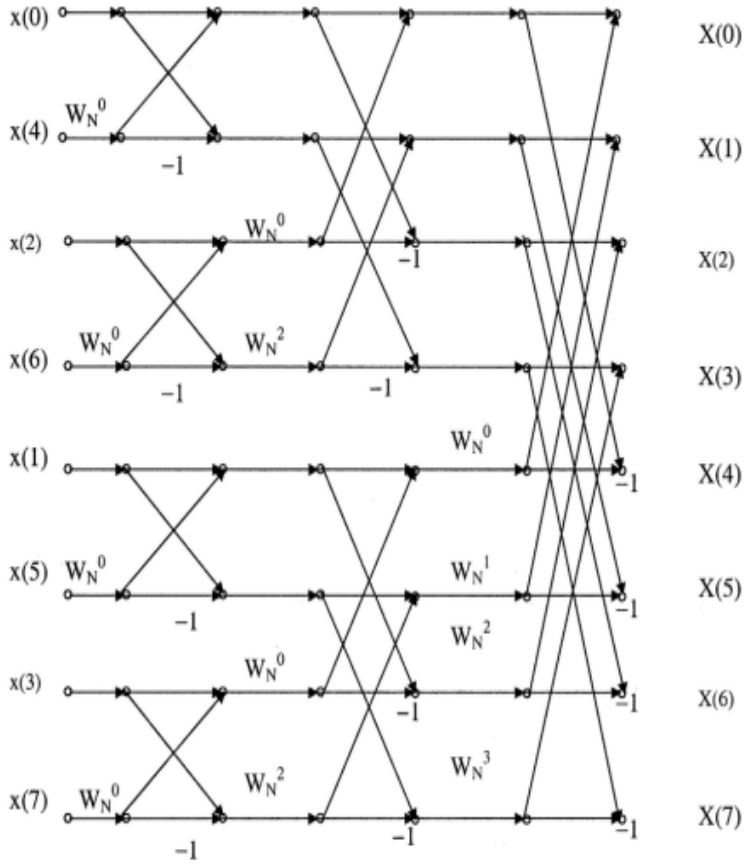
In this part, we will learn how to use IP Integrator to create a processing system-based design consisting of ARM cortex A9 cores. An abstract view of the Zynq architecture is given below. We will need the DDR3 controller for external DDR3 memory. As we are accessing the Zybo board remotely, we will be using the JTAG terminal instead of UART for the STDIN and STDOUT.



Part-4:

- **8-point FFT**

1. Create a new application project name FFT and modify the BSP settings as we did in Part-2.
2. Given below is the flow diagram of 8-point FFT

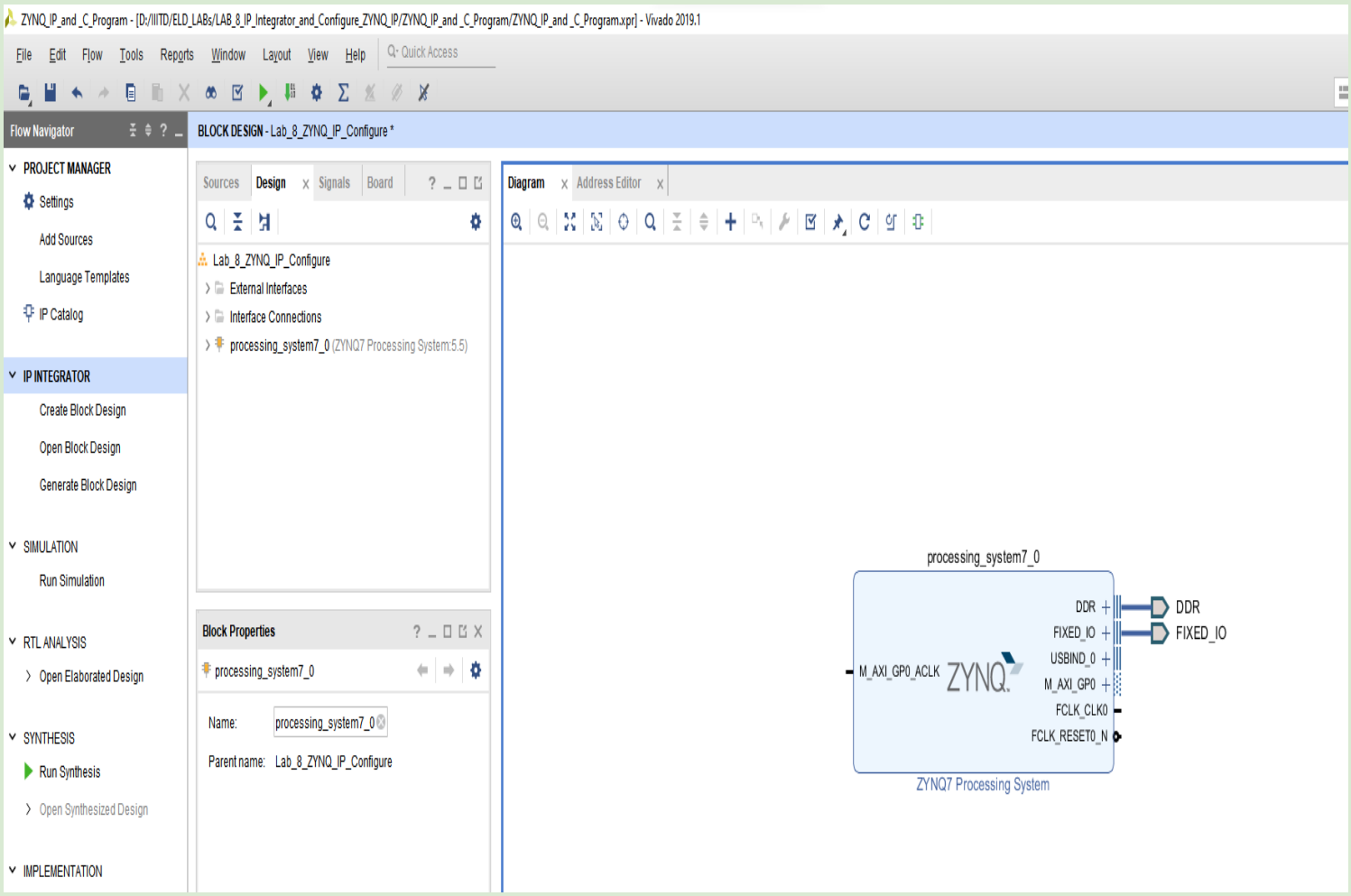


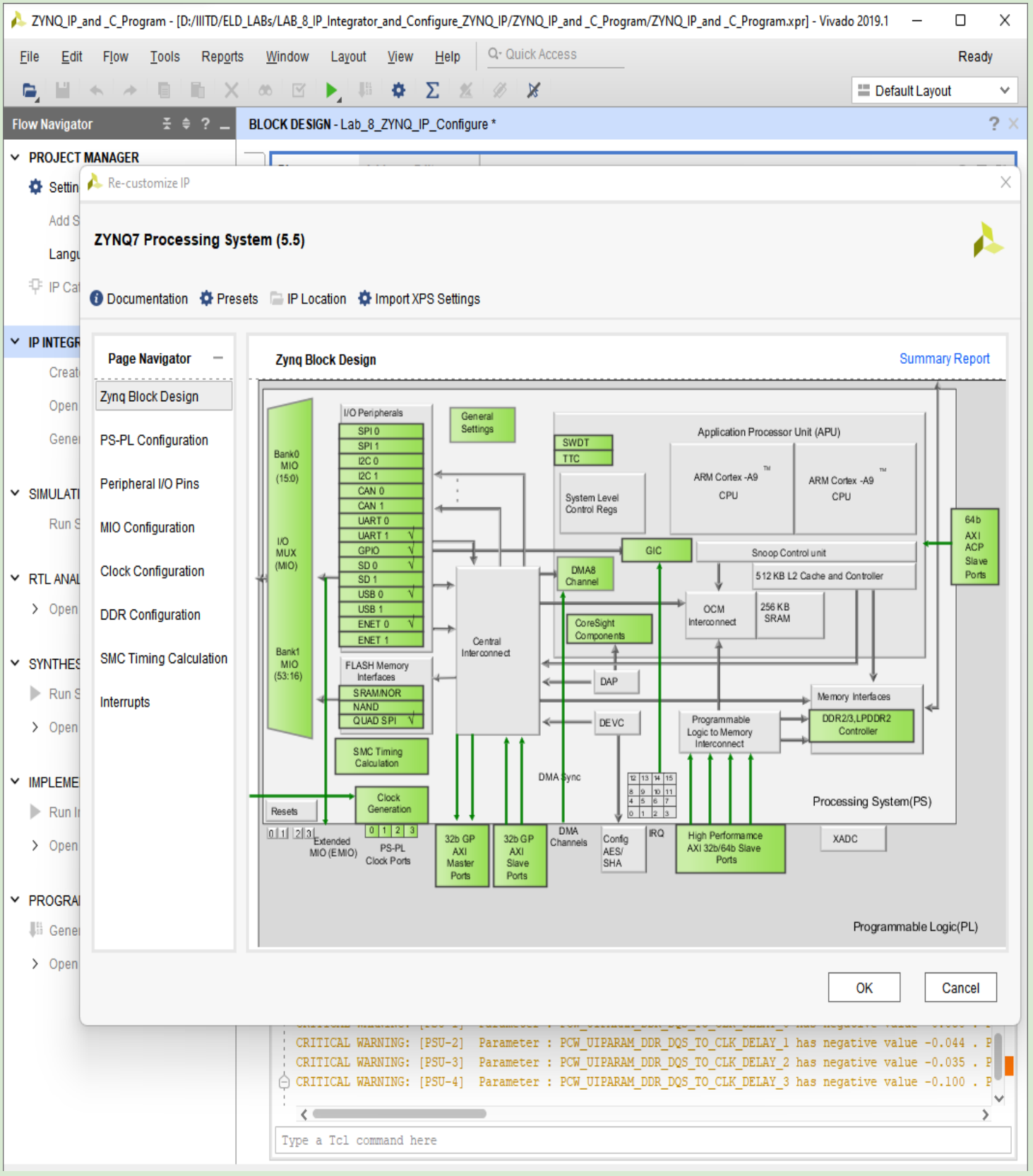
$W_N^0 = 1$, $W_N^1 = (1-j)/\sqrt{2}$, $W_N^2 = -j$, $W_N^3 = -(1+j)/\sqrt{2}$

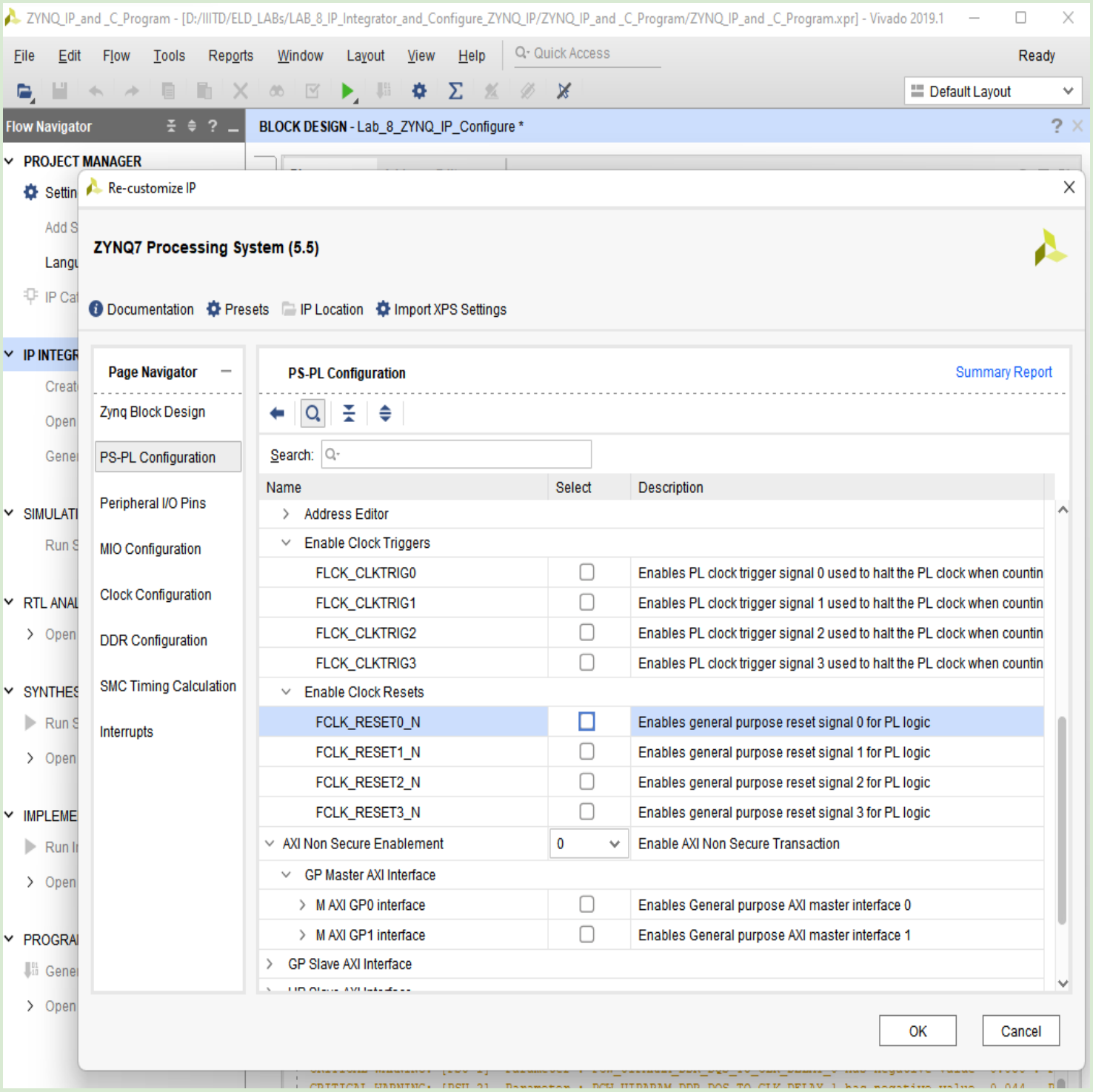
3. Write the following code for 8-point FFT.

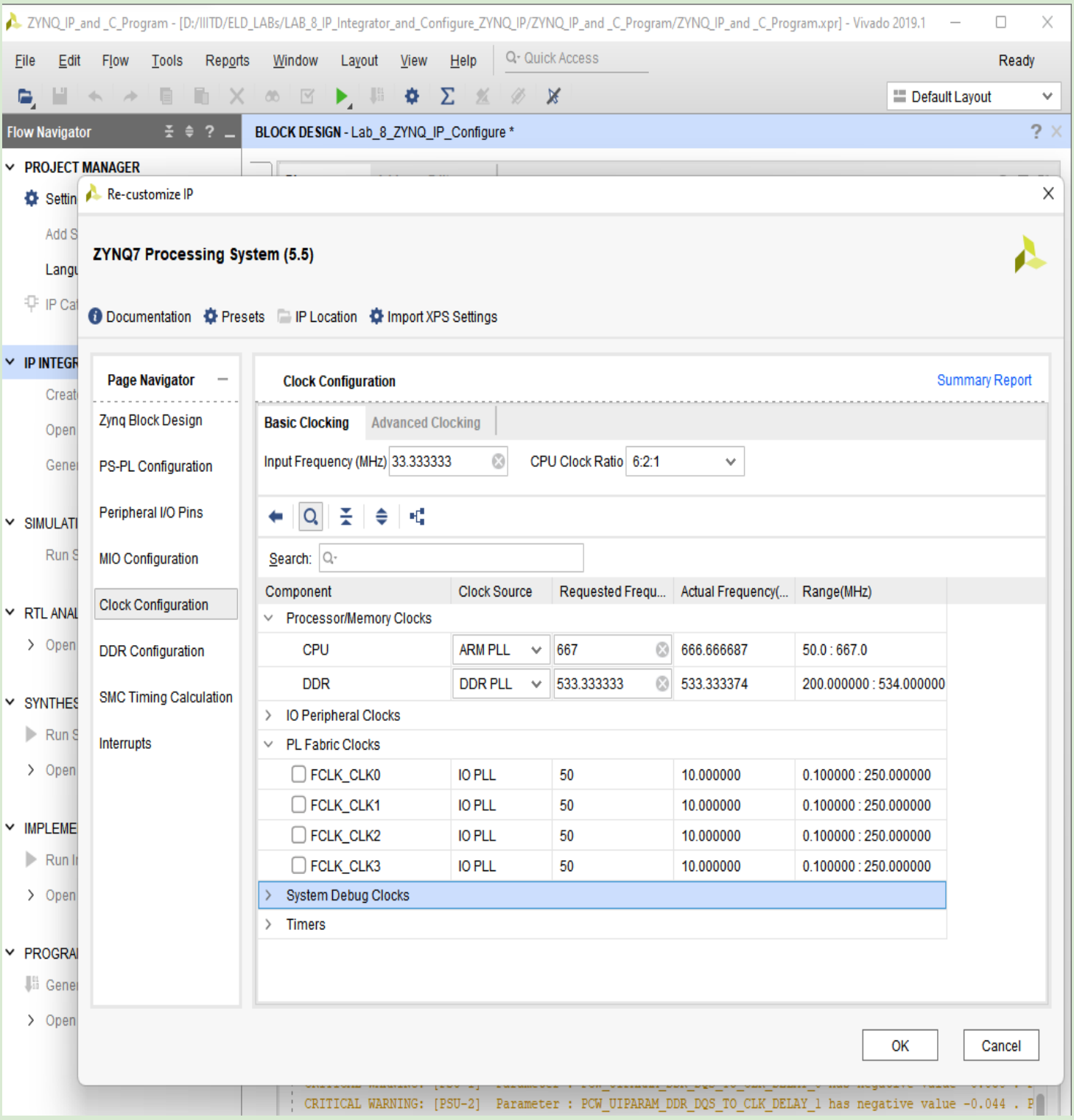
Observations:

ZYNQ_processing_System_Block_Design :

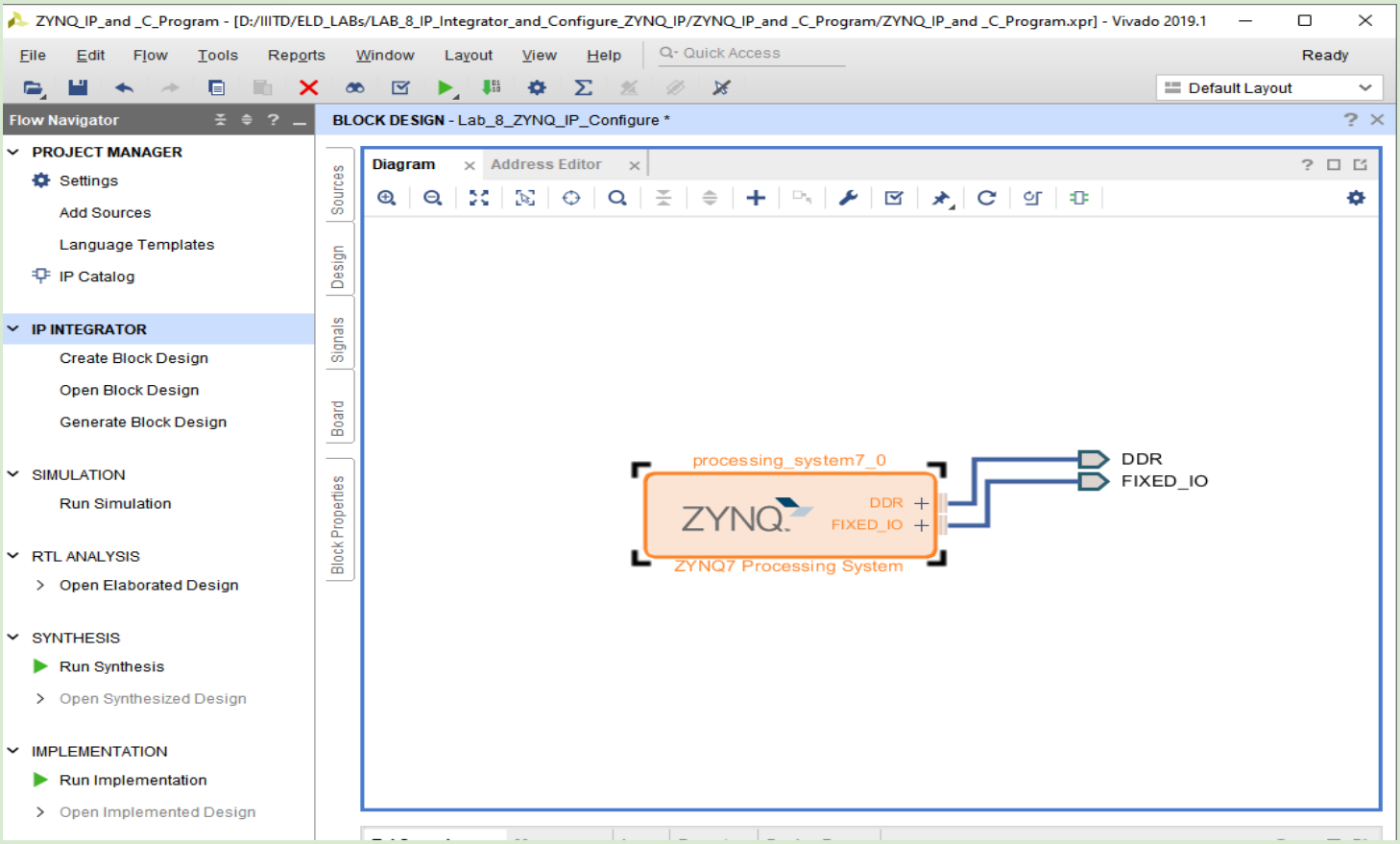


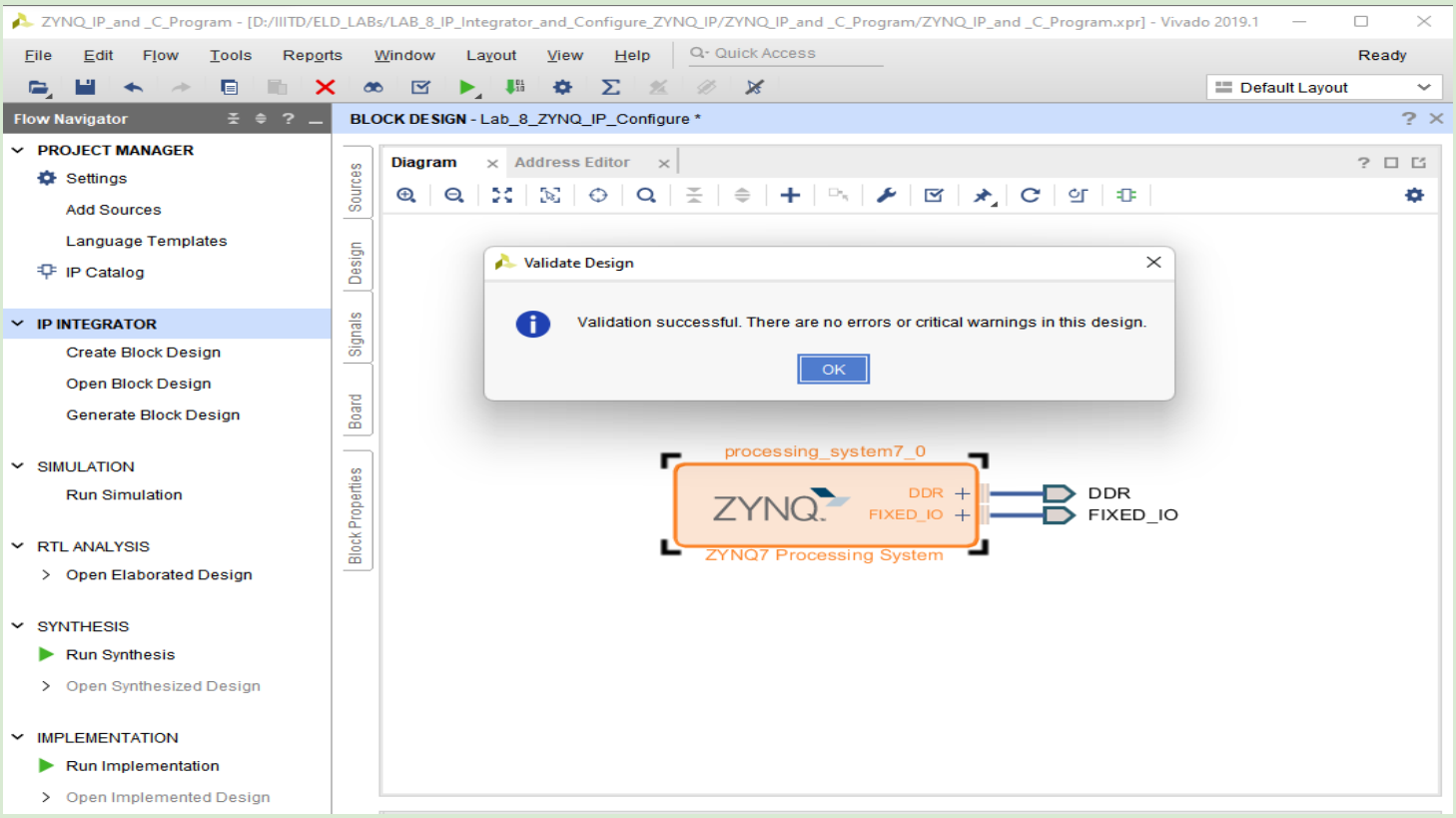

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_IP_Integrator_and_Configure_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
BLOCK DESIGN - Lab_8_ZYNQ_IP_Configure *
PROJECT MANAGER
IP INTEGR
SIMULATI
RTL ANAL
SYNTHES
IMPLEME
PROGRA
Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
Zynq Block Design
Summary Report
I/O Peripherals
SPI 0
SPI 1
I2C 0
I2C 1
CAN 0
CAN 1
UART 0
UART 1
GPIO
SD 0
SD 1
USB 0
USB 1
ENET 0
ENET 1
Bank0 MIO (15:0)
I/O MUX (MIO)
Bank1 MIO (53:16)
FLASH Memory Interfaces
SRAM/NOR
NAND
QUAD SPI
General Settings
SWDT
TTC
System Level Control Regs
Application Processor Unit (APU)
ARM Cortex -A9 CPU
ARM Cortex -A9 CPU
GIC
Snoop Control unit
512 KB L2 Cache and Controller
64b AXI ACP Slave Ports
DMA8 Channel
OCM Interconnect
256 KB SRAM
CoreSight Components
Central Interconnect
DAP
DEVC
Memory Interfaces
DDR2/3,LPDDR2 Controller
Programmable Logic to Memory Interconnect
SMC Timing Calculation
DMA Sync
Resets
Clock Generation
Extended MIO (EMIO)
PS-PL Clock Ports
32b GP AXI Master Ports
32b GP AXI Slave Ports
DMA Channels
Config AES/ SHA
IRQ
High Performance AXI 32b/64b Slave Ports
XADC
Processing System(PS)
Programmable Logic(PL)
OK
Cancel
CRITICAL WARNING: [PSU-2] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1 has negative value -0.044 . P
CRITICAL WARNING: [PSU-3] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2 has negative value -0.035 . P
CRITICAL WARNING: [PSU-4] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3 has negative value -0.100 . P
Type a Tcl command here

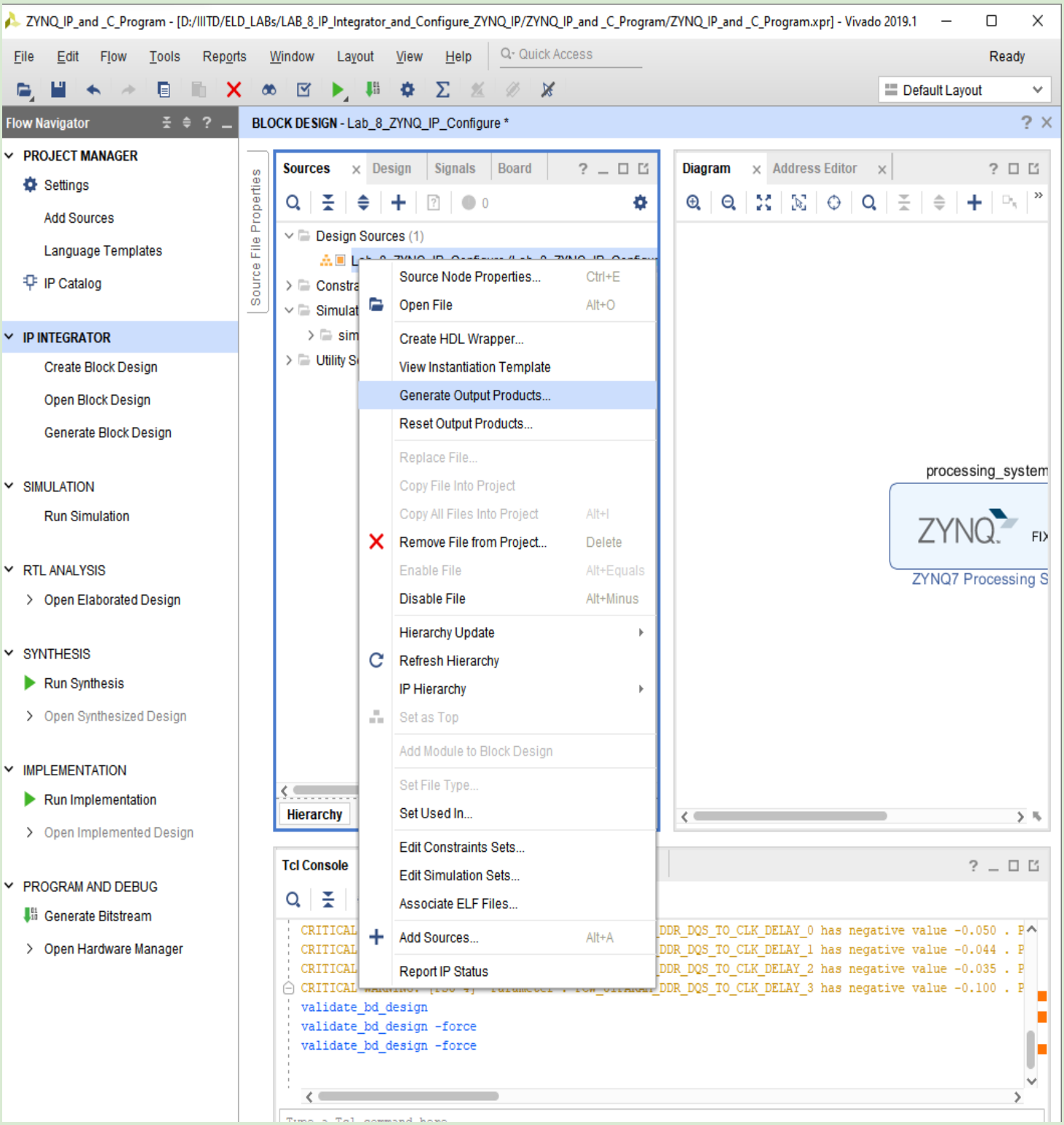

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_IP_Integrator_and_Configure_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
BLOCK DESIGN - Lab_8_ZYNQ_IP_Configure *
PROJECT MANAGER
IP INTEGR
SIMULATI
RTL ANAL
SYNTHES
IMPLEME
PROGRA
Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
PS-PL Configuration
Summary Report
Search:
Name
Select
Description
Address Editor
Enable Clock Triggers
FLCK_CLKTRIG0
Enables PL clock trigger signal 0 used to halt the PL clock when countin
FLCK_CLKTRIG1
Enables PL clock trigger signal 1 used to halt the PL clock when countin
FLCK_CLKTRIG2
Enables PL clock trigger signal 2 used to halt the PL clock when countin
FLCK_CLKTRIG3
Enables PL clock trigger signal 3 used to halt the PL clock when countin
Enable Clock Resets
FCLK_RESET0_N
Enables general purpose reset signal 0 for PL logic
FCLK_RESET1_N
Enables general purpose reset signal 1 for PL logic
FCLK_RESET2_N
Enables general purpose reset signal 2 for PL logic
FCLK_RESET3_N
Enables general purpose reset signal 3 for PL logic
AXI Non Secure Enablement
0
Enable AXI Non Secure Transaction
GP Master AXI Interface
M AXI GP0 interface
Enables General purpose AXI master interface 0
M AXI GP1 interface
Enables General purpose AXI master interface 1
GP Slave AXI Interface
OK
Cancel

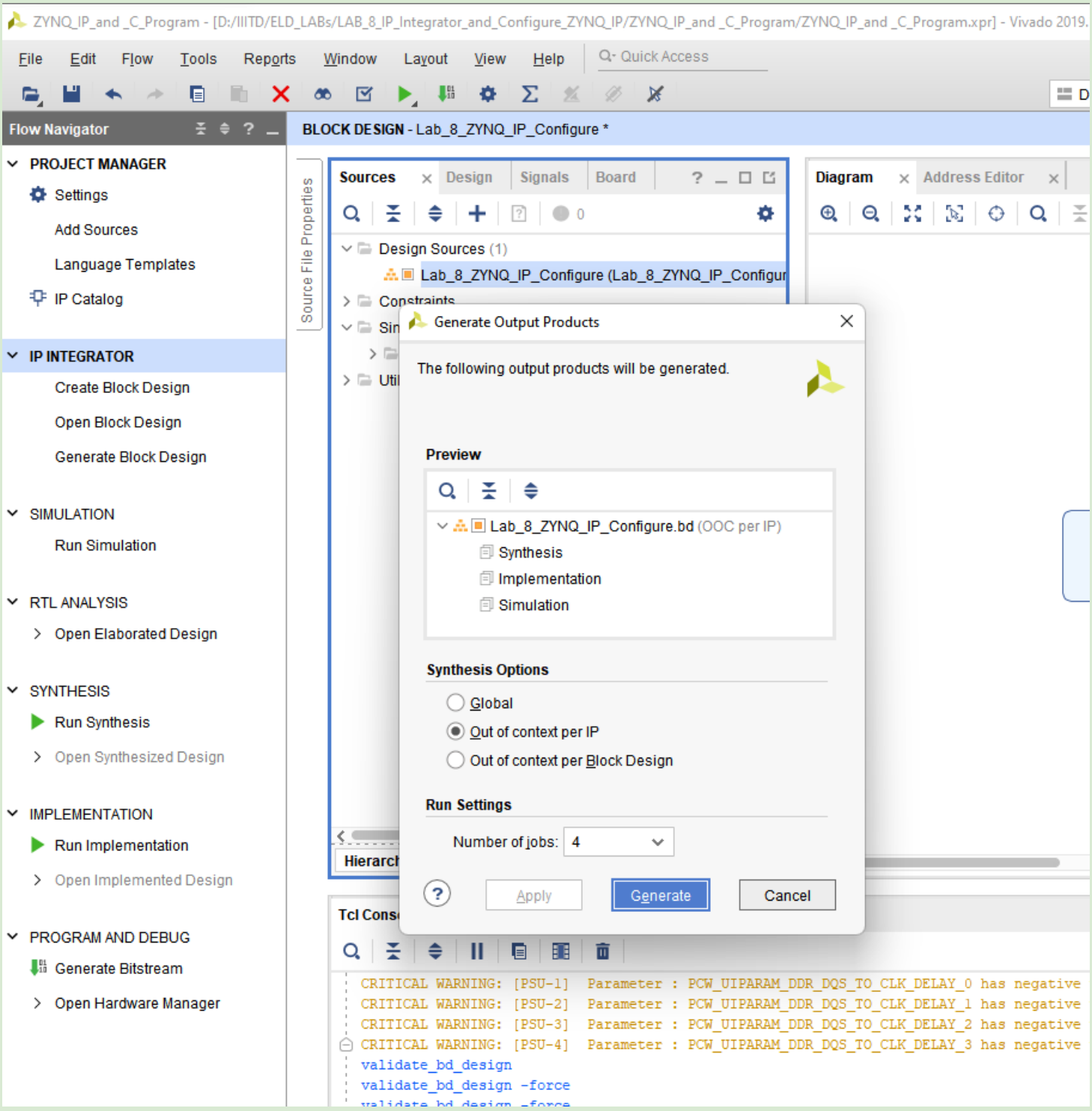

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_IP_Integrator_and_Configure_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
BLOCK DESIGN - Lab_8_ZYNQ_IP_Configure *
PROJECT MANAGER
IP INTEGR
SIMULATI
RTL ANAL
SYNTHES
IMPLEME
PROGRA
Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
Clock Configuration
Summary Report
Basic Clocking
Advanced Clocking
Input Frequency (MHz) 33.333333
CPU Clock Ratio 6:2:1
Search:
Component
Clock Source
Requested Frequ...
Actual Frequency(...
Range(MHz)
Processor/Memory Clocks
CPU
ARM PLL
667
666.666687
50.0 : 667.0
DDR
DDR PLL
533.333333
533.333374
200.000000 : 534.000000
IO Peripheral Clocks
PL Fabric Clocks
FCLK_CLK0
IO PLL
50
10.000000
0.100000 : 250.000000
FCLK_CLK1
IO PLL
50
10.000000
0.100000 : 250.000000
FCLK_CLK2
IO PLL
50
10.000000
0.100000 : 250.000000
FCLK_CLK3
IO PLL
50
10.000000
0.100000 : 250.000000
System Debug Clocks
Timers
OK
Cancel
CRITICAL WARNING: [PSU-2] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1 has negative value -0.044 . P

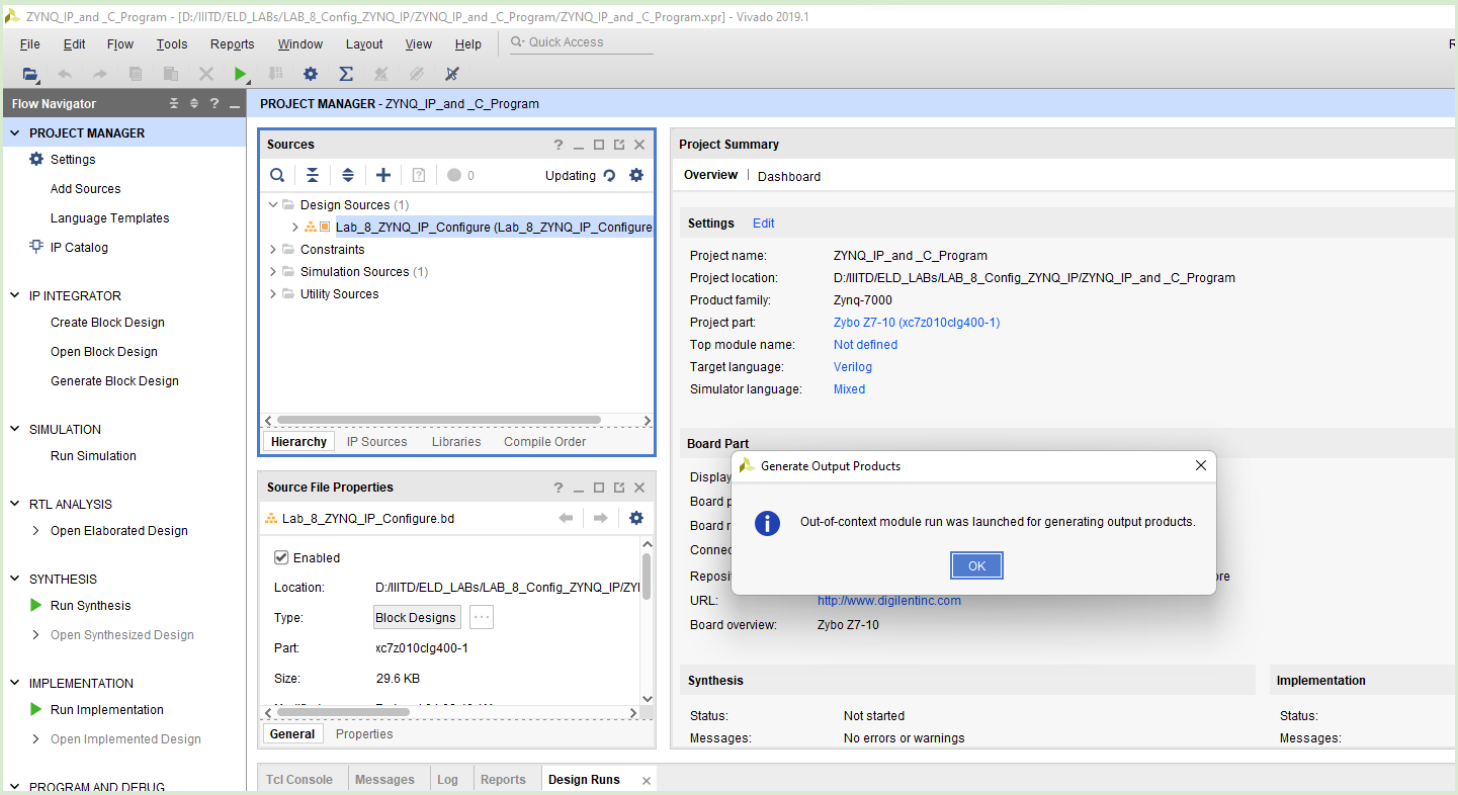
Validate the design, generate output product, and create HDL wrapper. DO NOT ever miss these steps.

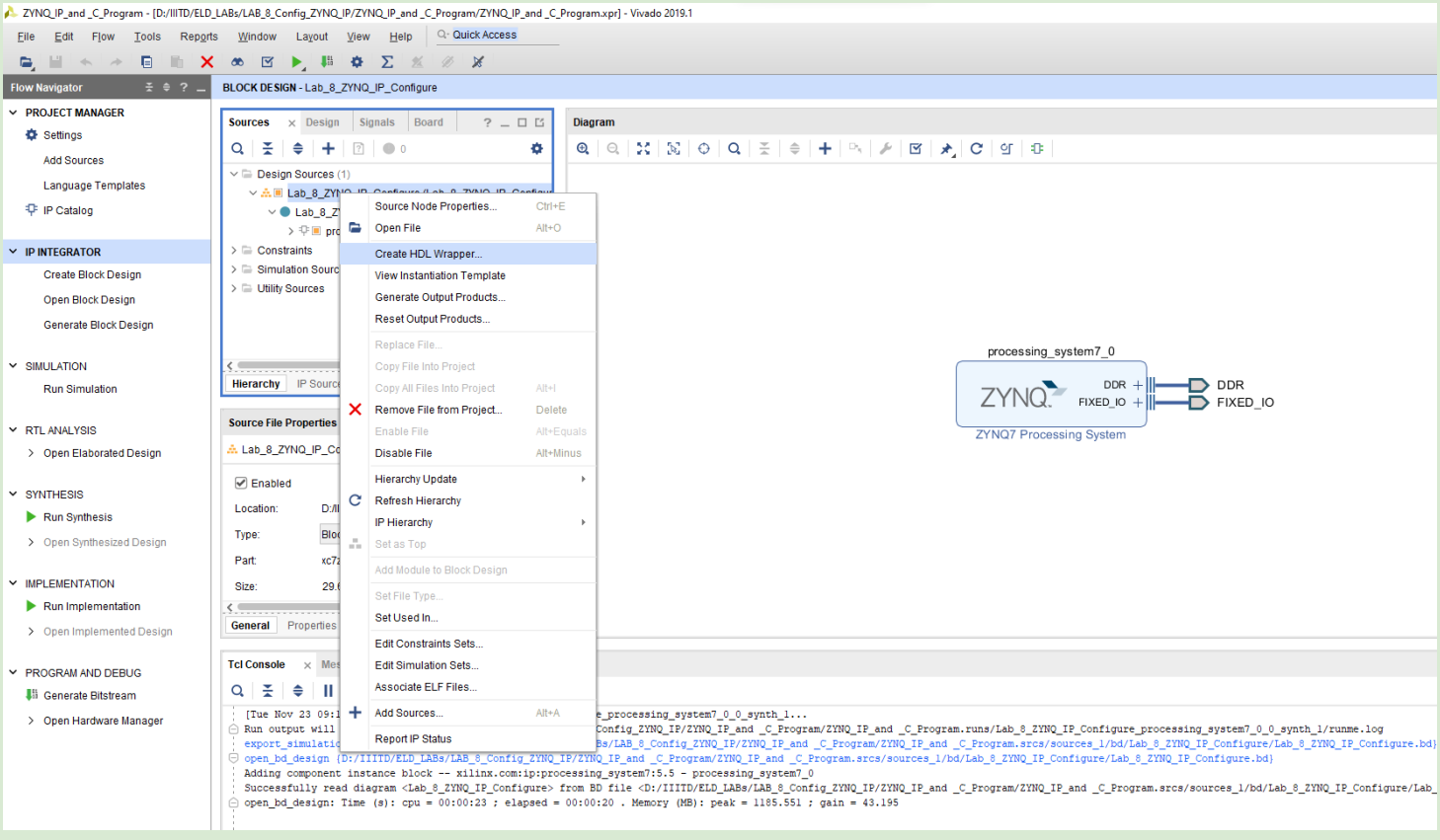




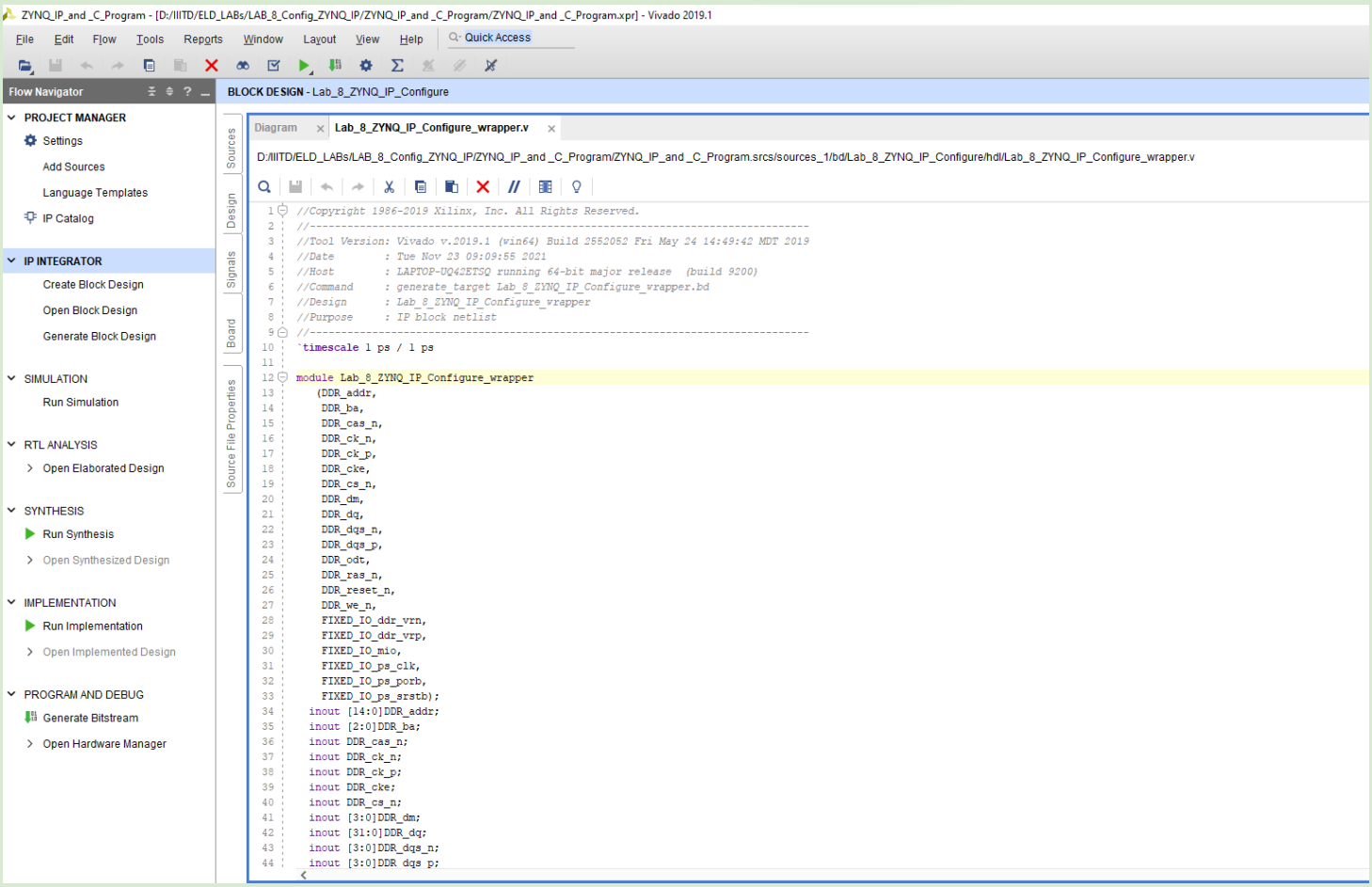

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_IP_Integrator_and_Configure_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - Lab_8_ZYNQ_IP_Configure *
Source File Properties
Sources
Design
Signals
Board
Design Sources (1)
Source Node Properties... Ctrl+E
Open File Alt+O
Create HDL Wrapper...
View Instantiation Template
Generate Output Products...
Reset Output Products...
Replace File...
Copy File Into Project
Copy All Files Into Project Alt+I
Remove File from Project... Delete
Enable File Alt+Equals
Disable File Alt+Minus
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Set as Top
Add Module to Block Design
Set File Type...
Set Used In...
Edit Constraints Sets...
Edit Simulation Sets...
Associate ELF Files...
Add Sources... Alt+A
Report IP Status
Hierarchy
Diagram
Address Editor
processing_system
ZYNQ
ZYNQ7 Processing S
Tcl Console
validate_bd_design
validate_bd_design -force
validate_bd_design -force

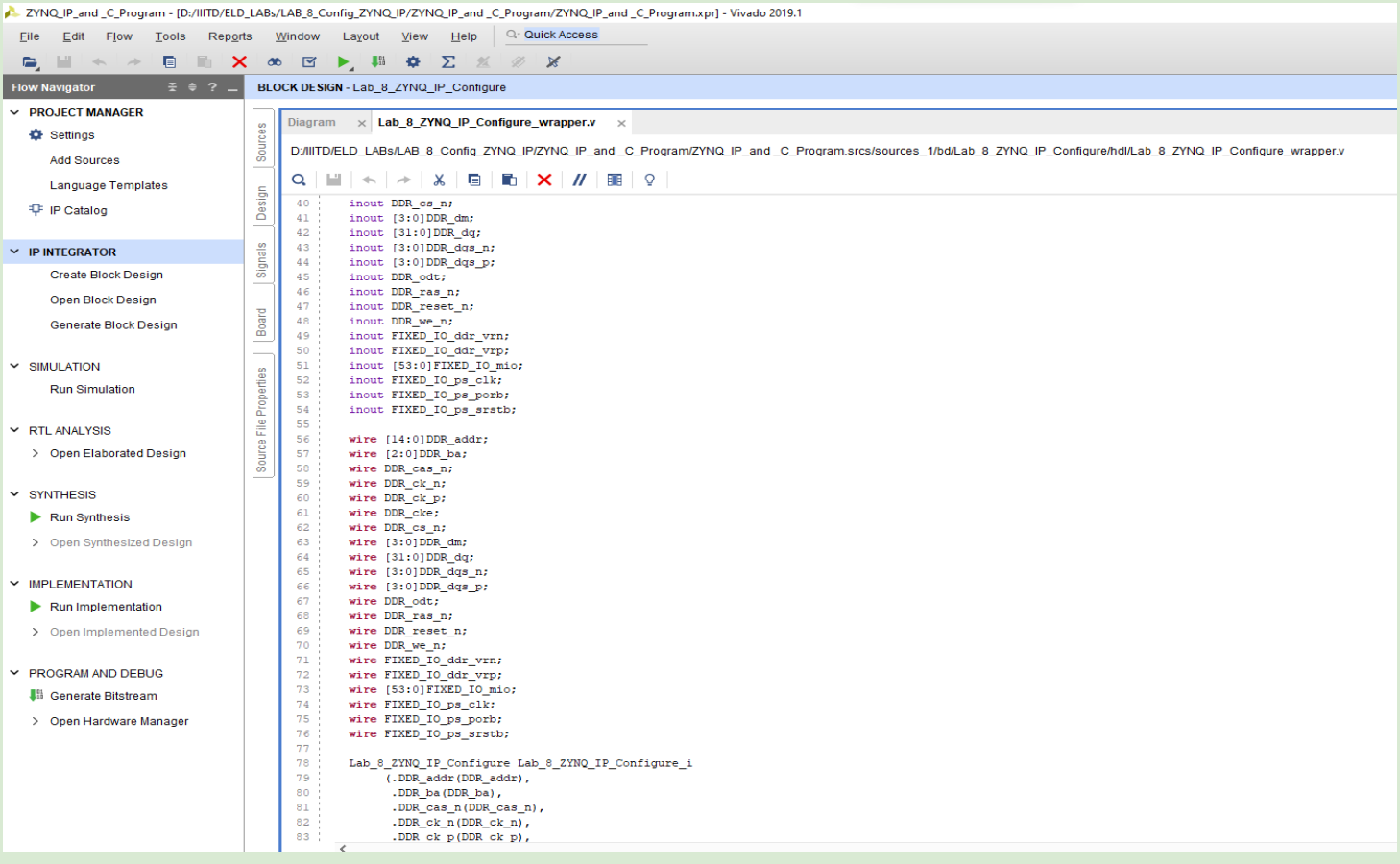

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_IP_Integrator_and_Configure_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - Lab_8_ZYNQ_IP_Configure *
Source File Properties
Sources
Design
Signals
Board
Design Sources (1)
Lab_8_ZYNQ_IP_Configure (Lab_8_ZYNQ_IP_Configur
Constraints
Diagram
Address Editor
Generate Output Products
The following output products will be generated.
Preview
Lab_8_ZYNQ_IP_Configure.bd (OOC per IP)
Synthesis
Implementation
Simulation
Synthesis Options
Global
Out of context per IP
Out of context per Block Design
Run Settings
Number of jobs: 4
Apply
Generate
Cancel
Tcl Cons
CRITICAL WARNING: [PSU-1] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_0 has negative
CRITICAL WARNING: [PSU-2] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_1 has negative
CRITICAL WARNING: [PSU-3] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_2 has negative
CRITICAL WARNING: [PSU-4] Parameter : PCW_UIPARAM_DDR_DQS_TO_CLK_DELAY_3 has negative
validate_bd_design
validate_bd_design -force

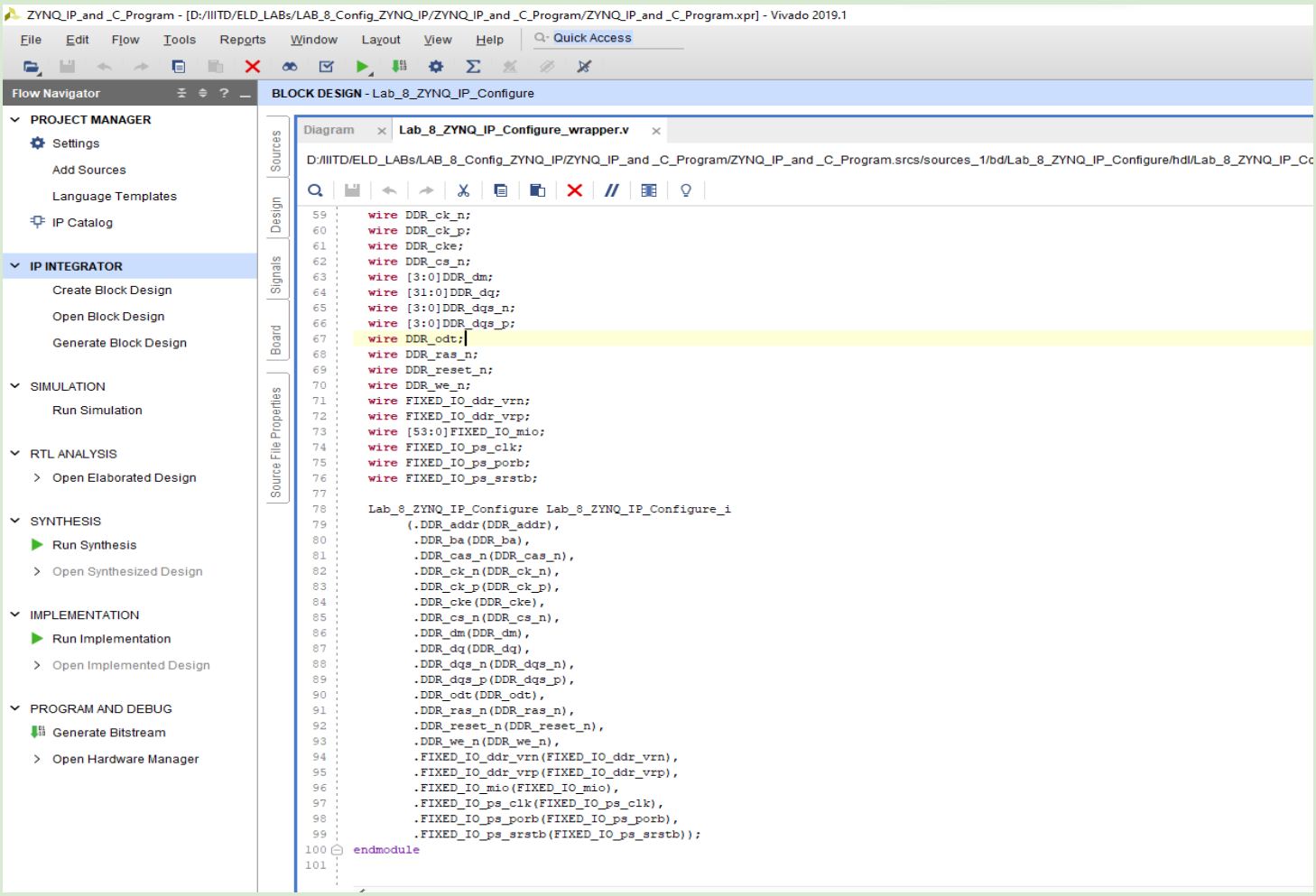

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
PROJECT MANAGER - ZYNQ_IP_and _C_Program
Sources
Updating
Design Sources (1)
Lab_8_ZYNQ_IP_Configure (Lab_8_ZYNQ_IP_Configure
Constraints
Simulation Sources (1)
Utility Sources
Hierarchy IP Sources Libraries Compile Order
Source File Properties
Lab_8_ZYNQ_IP_Configure.bd
Enabled
Location: D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYI
Type: Block Designs
Part: xc7z010clg400-1
Size: 29.6 KB
General Properties
Project Summary
Overview | Dashboard
Settings Edit
Project name: ZYNQ_IP_and _C_Program
Project location: D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program
Product family: Zynq-7000
Project part: Zybo Z7-10 (xc7z010clg400-1)
Top module name: Not defined
Target language: Verilog
Simulator language: Mixed
Board Part
Generate Output Products
Out-of-context module run was launched for generating output products.
OK
URL: http://www.digilentinc.com
Board overview: Zybo Z7-10
Synthesis
Status: Not started
Messages: No errors or warnings
Implementation
Status:
Messages:
Tcl Console Messages Log Reports Design Runs

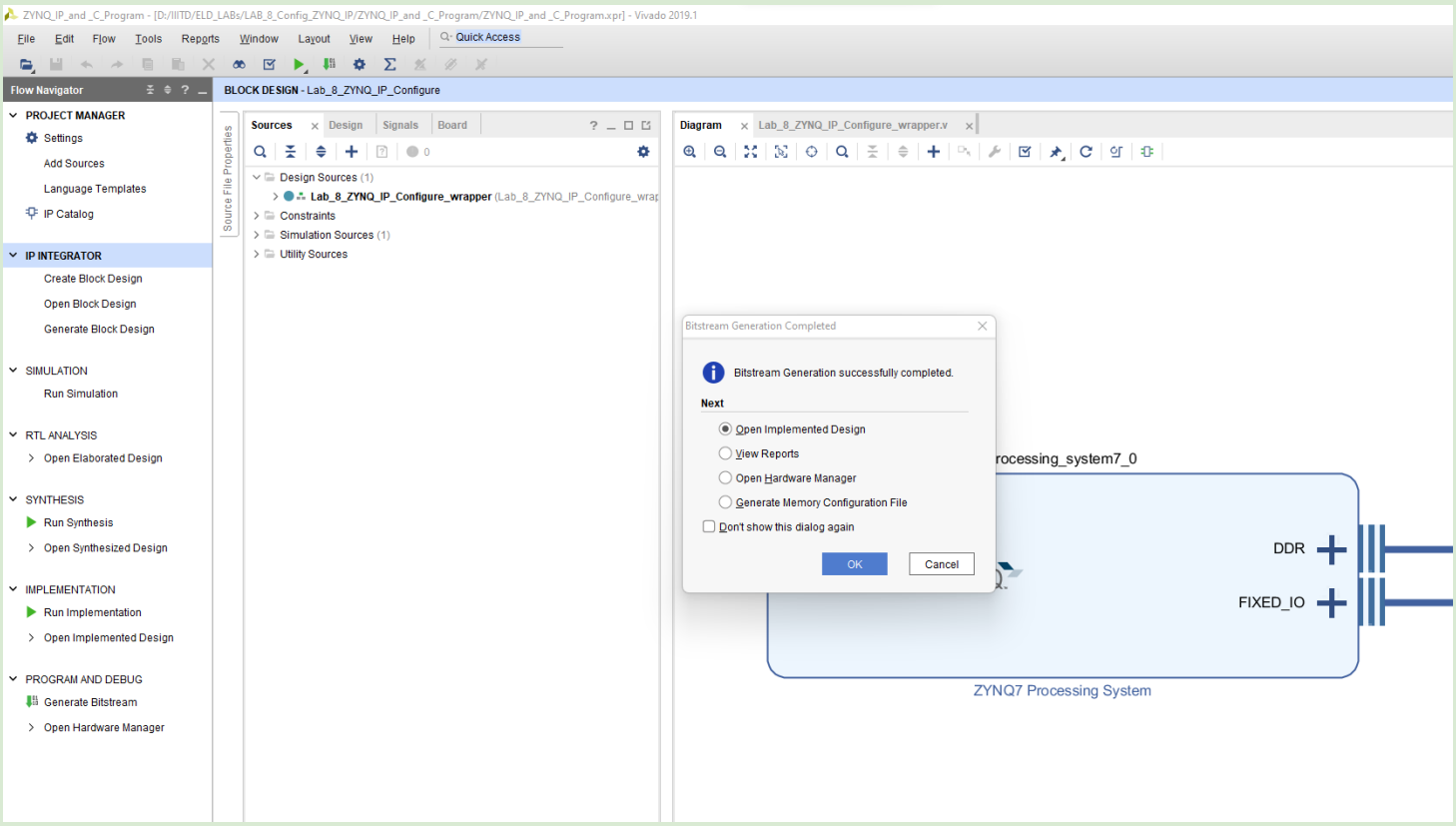

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - Lab_8_ZYNQ_IP_Configure
Sources Design Signals Board
Design Sources (1)
Constraints
Simulation Sources
Utility Sources
Hierarchy
Source File Properties
Enabled
Location:
Type:
Part:
Size:
General Properties
Source Node Properties... Ctrl+E
Open File Alt+O
Create HDL Wrapper...
View Instantiation Template
Generate Output Products...
Reset Output Products...
Replace File...
Copy File Into Project
Copy All Files Into Project Alt+I
Remove File from Project... Delete
Enable File Alt+Equals
Disable File Alt+Minus
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Set as Top
Add Module to Block Design
Set File Type...
Set Used In...
Edit Constraints Sets...
Edit Simulation Sets...
Associate ELF Files...
Add Sources... Alt+A
Report IP Status
Diagram
processing_system7_0
ZYNQ
DDR
FIXED_IO
ZYNQ7 Processing System
Tcl Console
open_bd_design {D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.srcs/sources_1/bd/Lab_8_ZYNQ_IP_Configure/Lab_8_ZYNQ_IP_Configure.bd}
Adding component instance block -- xilinx.com:ip:processing_system7:5.5 - processing_system7_0
Successfully read diagram <Lab_8_ZYNQ_IP_Configure> from BD file <D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.srcs/sources_1/bd/Lab_8_ZYNQ_IP_Configure/Lab_
open_bd_design: Time (s): cpu = 00:00:23 ; elapsed = 00:00:20 . Memory (MB): peak = 1185.551 ; gain = 43.195

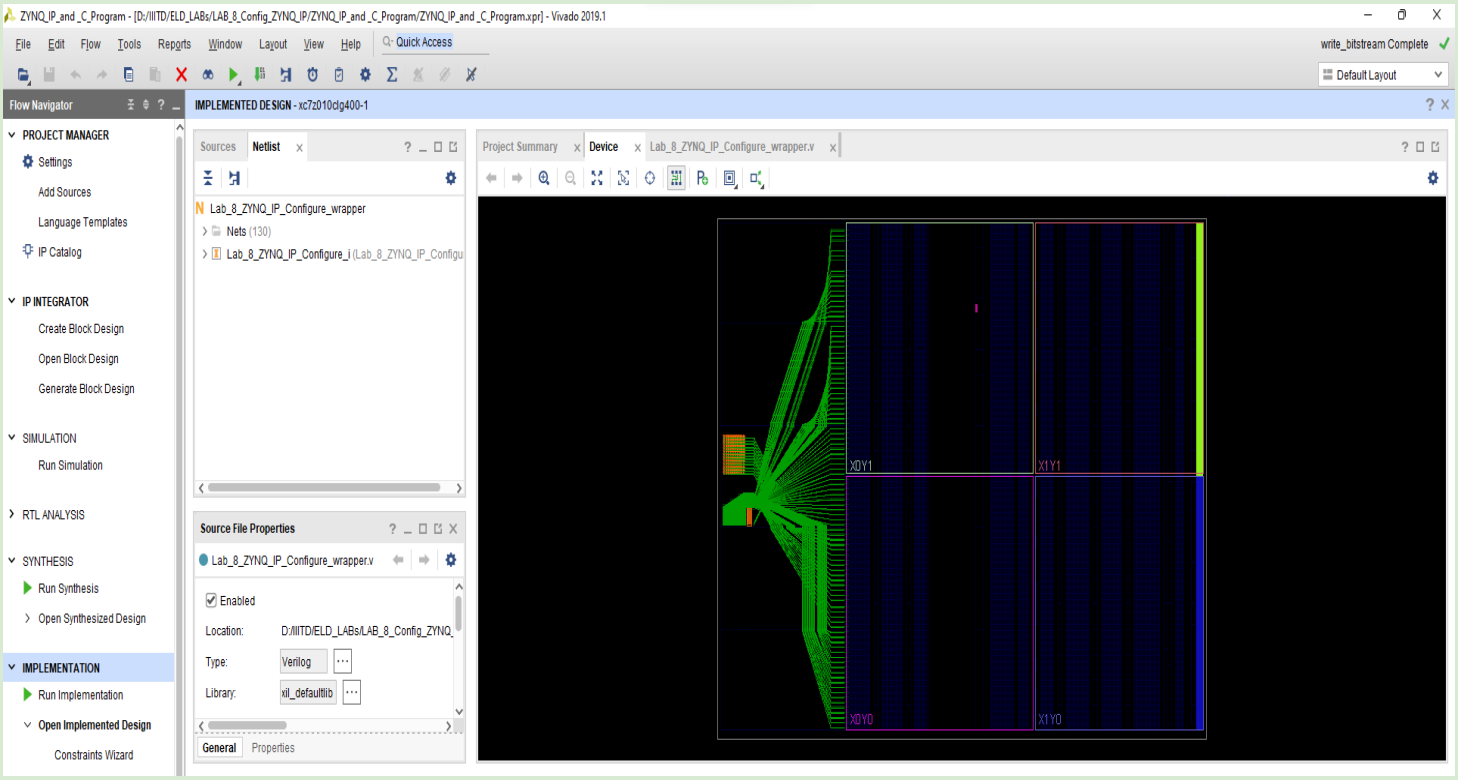
Auto_Generated_HDL_Wrapper

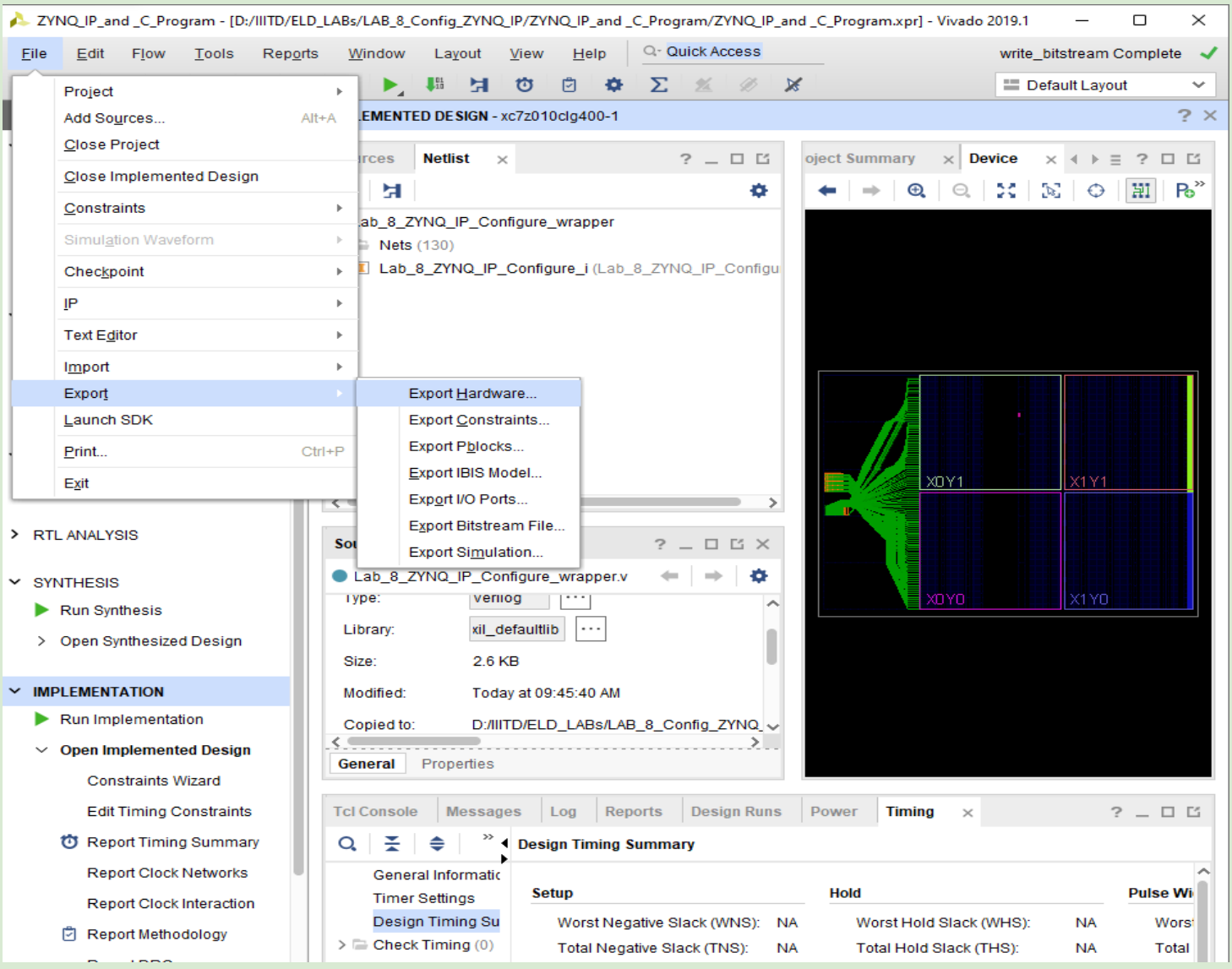


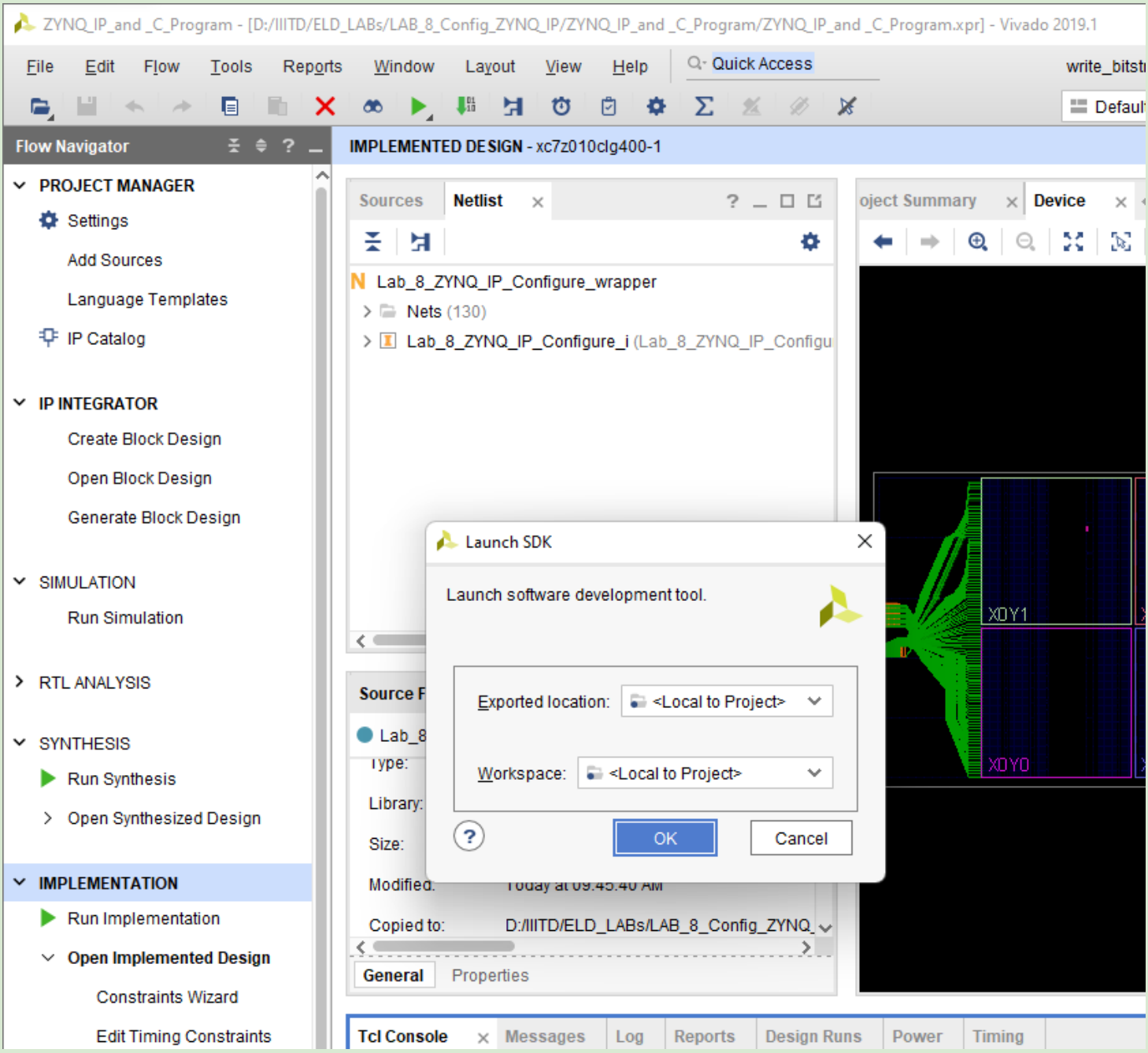



ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - Lab_8_ZYNQ_IP_Configure
Diagram
Lab_8_ZYNQ_IP_Configure_wrapper.v
D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.srcs/sources_1/bd/Lab_8_ZYNQ_IP_Configure/hdl/Lab_8_ZYNQ_IP_Co
Sources
Design
Signals
Board
Source File Properties
59 wire DDR_ck_n;
60 wire DDR_ck_p;
61 wire DDR_cke;
62 wire DDR_cs_n;
63 wire [3:0]DDR_dm;
64 wire [31:0]DDR_dq;
65 wire [3:0]DDR_dqs_n;
66 wire [3:0]DDR_dqs_p;
67 wire DDR_odt;
68 wire DDR_ras_n;
69 wire DDR_reset_n;
70 wire DDR_we_n;
71 wire FIXED_IO_ddr_vrn;
72 wire FIXED_IO_ddr_vrp;
73 wire [53:0]FIXED_IO_mio;
74 wire FIXED_IO_ps_clk;
75 wire FIXED_IO_ps_porb;
76 wire FIXED_IO_ps_srstb;
77
78 Lab_8_ZYNQ_IP_Configure Lab_8_ZYNQ_IP_Configure_i
79 (.DDR_addr(DDR_addr),
80 .DDR_ba(DDR_ba),
81 .DDR_cas_n(DDR_cas_n),
82 .DDR_ck_n(DDR_ck_n),
83 .DDR_ck_p(DDR_ck_p),
84 .DDR_cke(DDR_cke),
85 .DDR_cs_n(DDR_cs_n),
86 .DDR_dm(DDR_dm),
87 .DDR_dq(DDR_dq),
88 .DDR_dqs_n(DDR_dqs_n),
89 .DDR_dqs_p(DDR_dqs_p),
90 .DDR_odt(DDR_odt),
91 .DDR_ras_n(DDR_ras_n),
92 .DDR_reset_n(DDR_reset_n),
93 .DDR_we_n(DDR_we_n),
94 .FIXED_IO_ddr_vrn(FIXED_IO_ddr_vrn),
95 .FIXED_IO_ddr_vrp(FIXED_IO_ddr_vrp),
96 .FIXED_IO_mio(FIXED_IO_mio),
97 .FIXED_IO_ps_clk(FIXED_IO_ps_clk),
98 .FIXED_IO_ps_porb(FIXED_IO_ps_porb),
99 .FIXED_IO_ps_srstb(FIXED_IO_ps_srstb));
100 endmodule
101

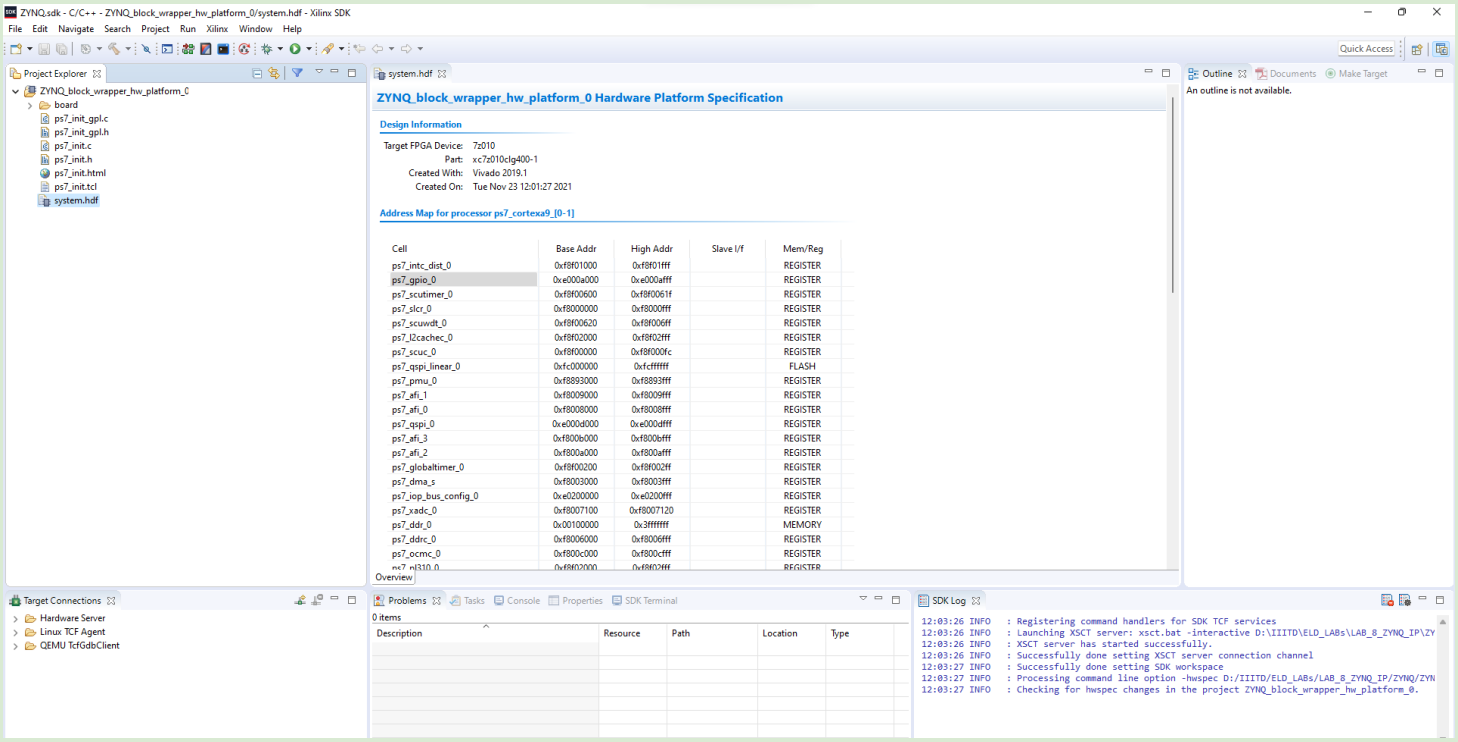

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help Quick Access
Flow Navigator
BLOCK DESIGN - Lab_8_ZYNQ_IP_Configure
Sources
Design
Signals
Board
Diagram
Lab_8_ZYNQ_IP_Configure_wrapper.v
Design Sources (1)
Lab_8_ZYNQ_IP_Configure_wrapper
Constraints
Simulation Sources (1)
Utility Sources
Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
Open Implemented Design
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel
DDR
FIXED_IO
ZYNQ7 Processing System


ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7z010clg400-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Sources
Netlist
Lab_8_ZYNQ_IP_Configure_wrapper
Nets (130)
Lab_8_ZYNQ_IP_Configure_i (Lab_8_ZYNQ_IP_Configu
Source File Properties
Lab_8_ZYNQ_IP_Configure_wrapper.v
Enabled
Location: D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_
Type: Verilog
Library: xil_defaultlib
General
Properties
Project Summary
Device
Lab_8_ZYNQ_IP_Configure_wrapper.v
X0Y1
X1Y1
X0Y0
X1Y0

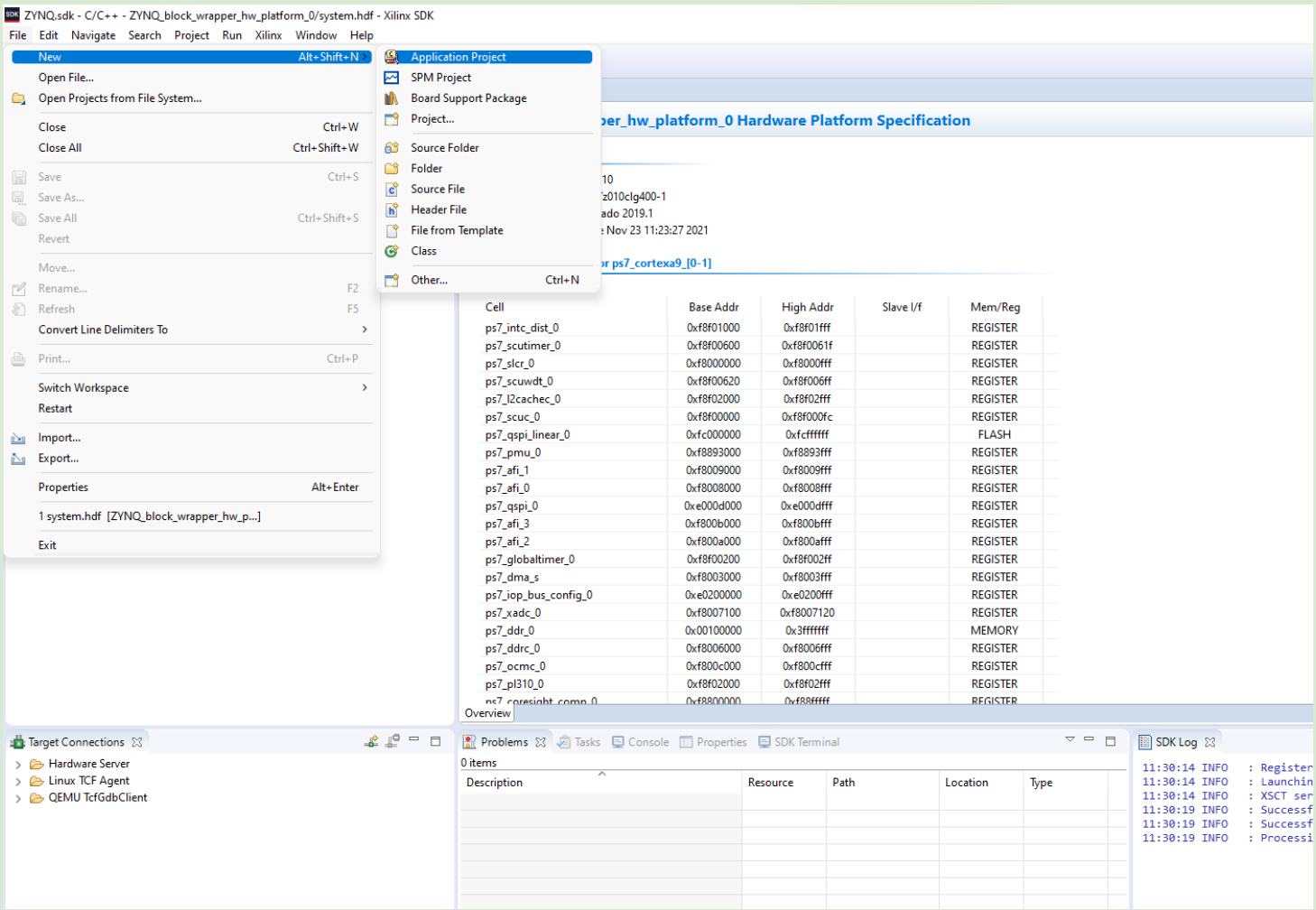

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Project
Add Sources... Alt+A
Close Project
Close Implemented Design
Constraints
Simulation Waveform
Checkpoint
IP
Text Editor
Import
Export
Launch SDK
Print... Ctrl+P
Exit
Export Hardware...
Export Constraints...
Export Pblocks...
Export IBIS Model...
Export I/O Ports...
Export Bitstream File...
Export Simulation...
Netlist
Lab_8_ZYNQ_IP_Configure_wrapper
Nets (130)
Lab_8_ZYNQ_IP_Configure_i (Lab_8_ZYNQ_IP_Configu
Device
X0Y1
X1Y1
X0Y0
X1Y0
Lab_8_ZYNQ_IP_Configure_wrapper.v
Library: xil_defaultlib
Size: 2.6 KB
Modified: Today at 09:45:40 AM
Copied to: D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_
General
Properties
RTL ANALYSIS
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Tcl Console
Messages
Log
Reports
Design Runs
Power
Timing
Design Timing Summary
General Informatic
Timer Settings
Design Timing Su
Check Timing (0)
Setup
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Hold
Worst Hold Slack (WHS): NA
Total Hold Slack (THS): NA
Pulse Wi
Worst
Total

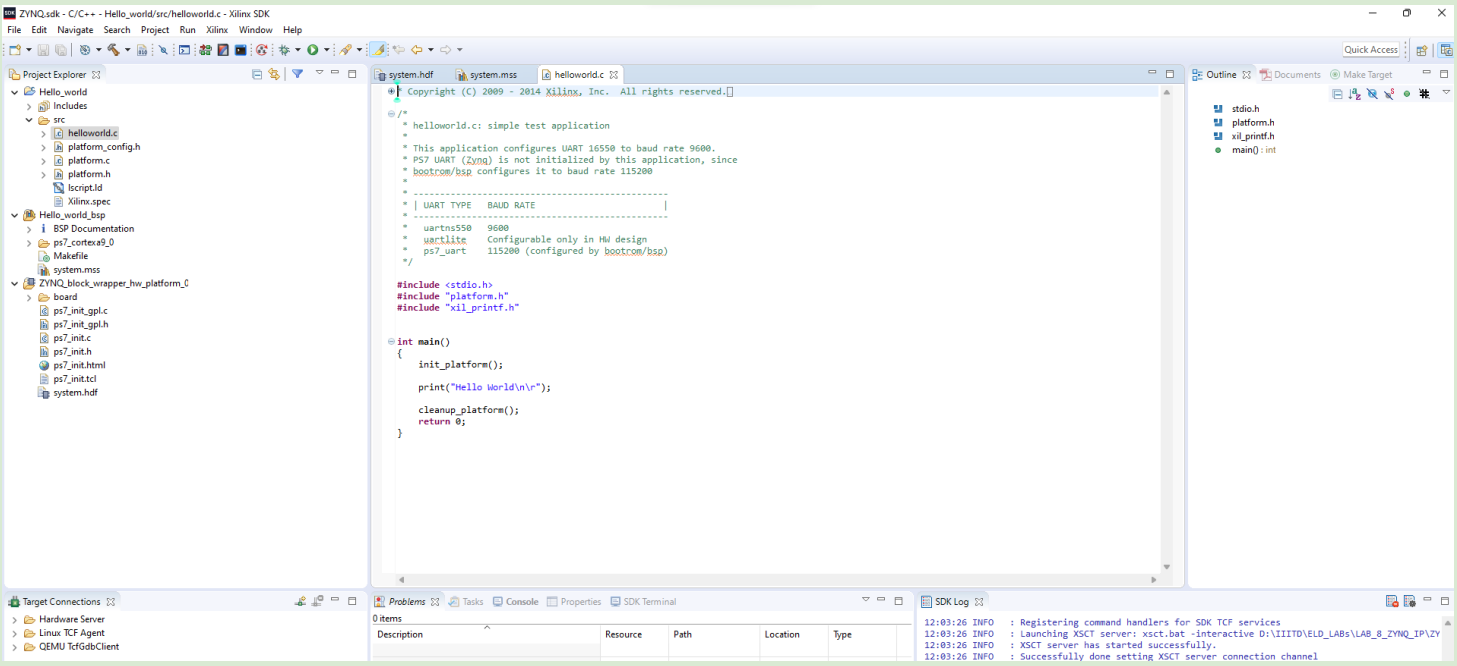

ZYNQ_IP_and _C_Program - [D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_IP/ZYNQ_IP_and _C_Program/ZYNQ_IP_and _C_Program.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
IMPLEMENTED DESIGN - xc7z010clg400-1
Sources
Netlist
Lab_8_ZYNQ_IP_Configure_wrapper
Nets (130)
Lab_8_ZYNQ_IP_Configure_i (Lab_8_ZYNQ_IP_Configu
Device
XOY1
XOY0
Launch SDK
Launch software development tool.
Exported location: <Local to Project>
Workspace: <Local to Project>
OK
Cancel
Source F
Type:
Library:
Size:
Modified:
Copied to: D:/IIITD/ELD_LABs/LAB_8_Config_ZYNQ_
General
Properties
Tcl Console
Messages
Log
Reports
Design Runs
Power
Timing

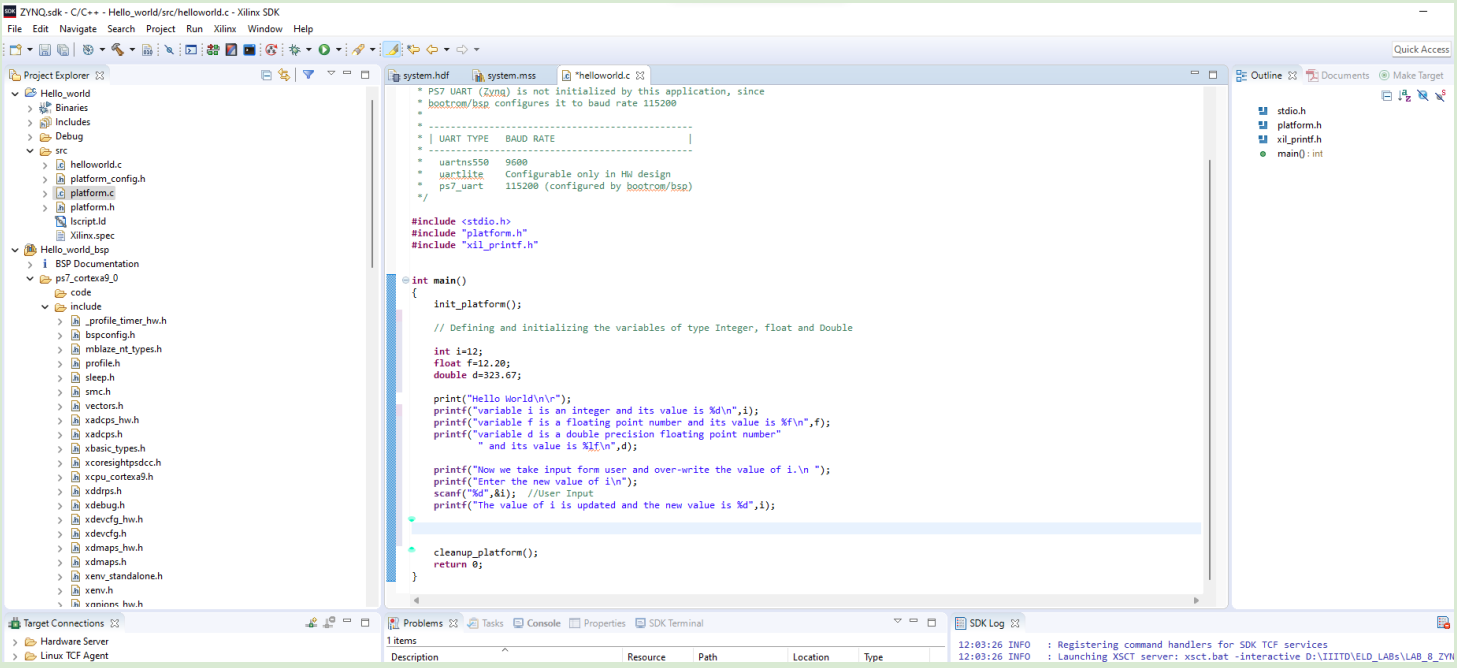
Launched_SDK_and_we seeauto-decompressed_.hdl_file_that we exported earlier

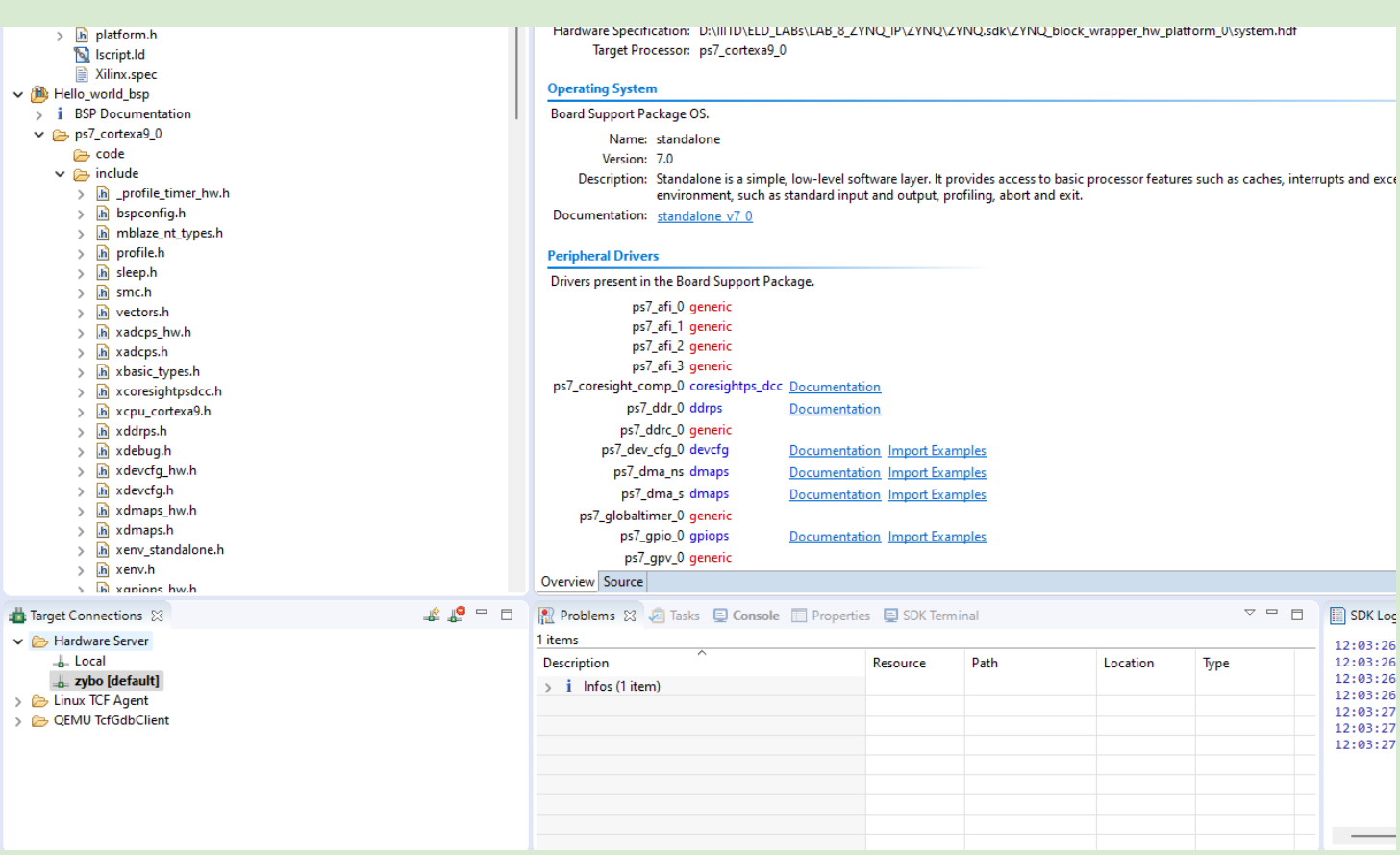


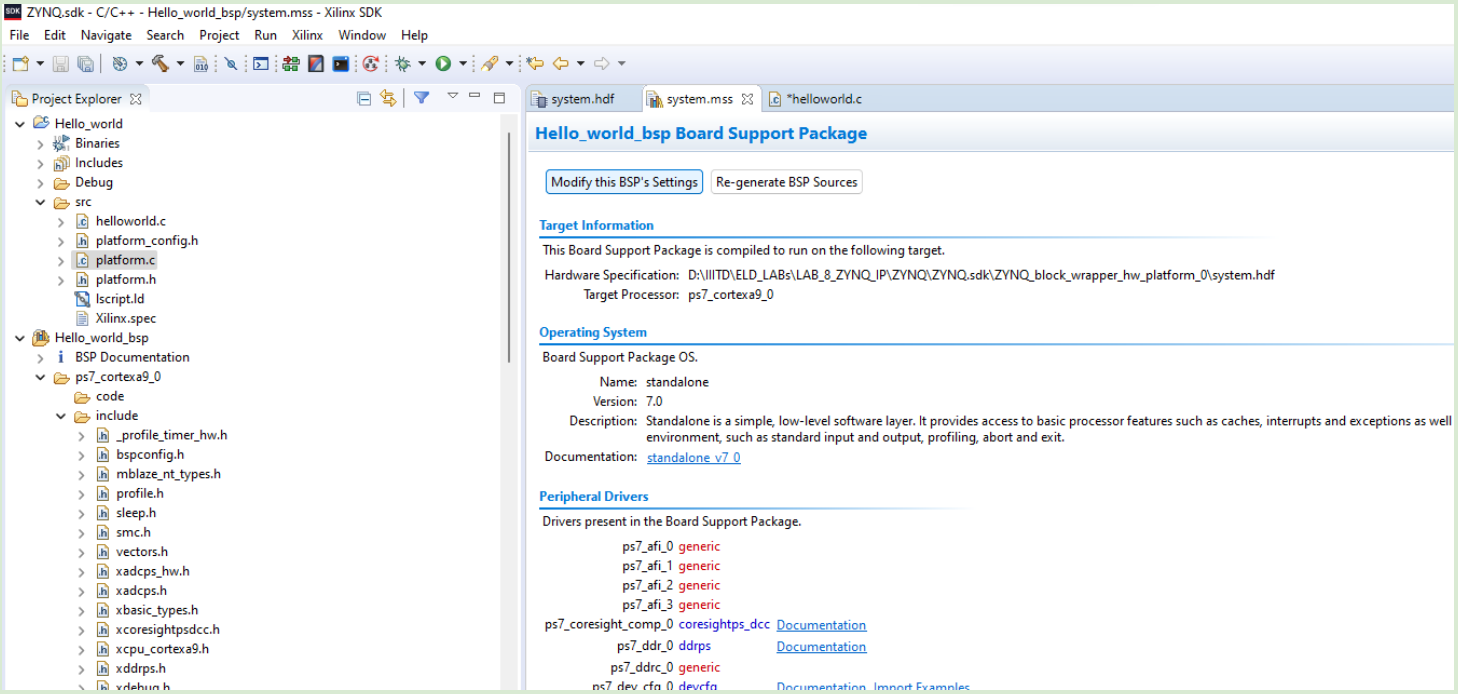
writing hello_world program in C

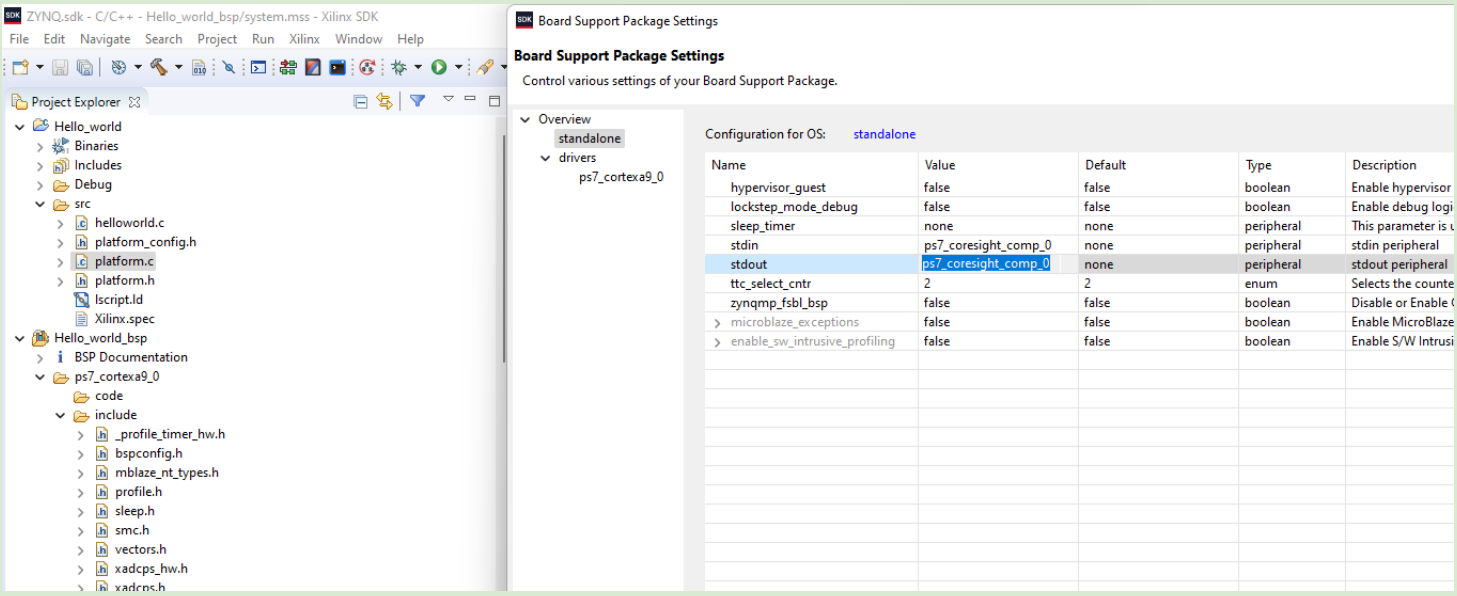



ZYNQ.sdk - C/C++ - Hello_world/src/helloworld.c - Xilinx SDK
File Edit Navigate Search Project Run Xilinx Window Help
Project Explorer
Hello_world
Includes
src
helloworld.c
platform_config.h
platform.c
platform.h
lscript.ld
Xilinx.spec
Hello_world_bsp
BSP Documentation
ps7_cortexa9_0
Makefile
system.mss
ZYNQ_block_wrapper_hw_platform_0
board
ps7_init_gpl.c
ps7_init_gpl.h
ps7_init.c
ps7_init.h
ps7_init.html
ps7_init.tcl
system.hdf
system.hdf
system.mss
helloworld.c
Copyright (C) 2009 - 2014 Xilinx, Inc. All rights reserved.
/*
* helloworld.c: simple test application
*
* This application configures UART 16550 to baud rate 9600.
* PS7 UART (Zynq) is not initialized by this application, since
* bootrom/bsp configures it to baud rate 115200
*
* --
* | UART TYPE BAUD RATE |
* --
* uartns550 9600
* uartlite Configurable only in HW design
* ps7_uart 115200 (configured by bootrom/bsp)
*/
#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"
int main()
{
init_platform();
print("Hello World\n\r");
cleanup_platform();
return 0;
}
Outline
Documents
Make Target
stdio.h
platform.h
xil_printf.h
main() : int
Target Connections
Hardware Server
Linux TCF Agent
QEMU TcfGdbClient
Problems
Tasks
Console
Properties
SDK Terminal
0 items
Description
Resource
Path
Location
Type
SDK Log
12:03:26 INFO : Registering command handlers for SDK TCF services
12:03:26 INFO : Launching XSCT server: xsct.bat -interactive D:\IIITD\ELD_LABs\LAB_8_ZYNQ_IP\ZY
12:03:26 INFO : XSCT server has started successfully.
12:03:26 INFO : Successfully done setting XSCT server connection channel

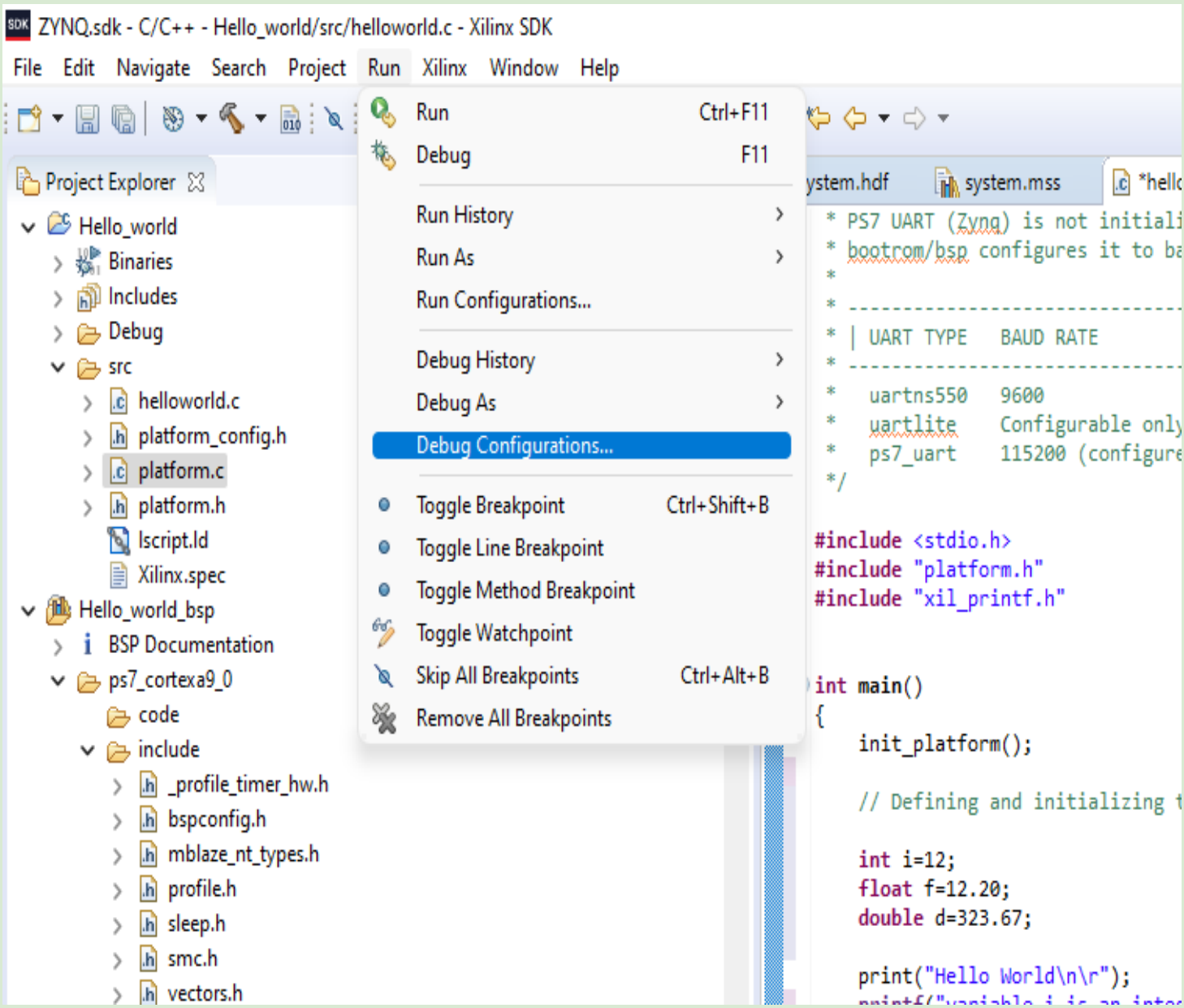

ZYNQ.sdk - C/C++ - Hello_world/src/helloworld.c - Xilinx SDK
File Edit Navigate Search Project Run Xilinx Window Help
Project Explorer
Hello_world
Binaries
Includes
Debug
src
helloworld.c
platform_config.h
platform.c
platform.h
lscript.ld
Xilinx.spec
Hello_world_bsp
BSP Documentation
ps7_cortexa9_0
code
include
_profile_timer_hw.h
bspconfig.h
mblaze_nt_types.h
profile.h
sleep.h
smc.h
vectors.h
xadcps_hw.h
xadcps.h
xbasic_types.h
xcoresightpsdcc.h
xcpu_cortexa9.h
xddrps.h
xdebug.h
xdevcfg_hw.h
xdevcfg.h
xdmaps_hw.h
xdmaps.h
xenv_standalone.h
xenv.h
system.hdf
system.mss
*helloworld.c
* PS7 UART (Zynq) is not initialized by this application, since
* bootrom/bsp configures it to baud rate 115200
*
* --
* | UART TYPE BAUD RATE |
* --
* uartns550 9600
* uartlite Configurable only in HW design
* ps7_uart 115200 (configured by bootrom/bsp)
*/
#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"
int main()
{
init_platform();
// Defining and initializing the variables of type Integer, float and Double
int i=12;
float f=12.20;
double d=323.67;
print("Hello World\n\r");
printf("variable i is an integer and its value is %d\n",i);
printf("variable f is a floating point number and its value is %f\n",f);
printf("variable d is a double precision floating point number"
" and its value is %lf\n",d);
printf("Now we take input form user and over-write the value of i.\n ");
printf("Enter the new value of i\n");
scanf("%d",&i); //User Input
printf("The value of i is updated and the new value is %d",i);
cleanup_platform();
return 0;
}
Outline
Documents
Make Target
stdio.h
platform.h
xil_printf.h
main() : int
Target Connections
Hardware Server
Linux TCF Agent
Problems
Tasks
Console
Properties
SDK Terminal
1 items
Description
Resource
Path
Location
Type
SDK Log
12:03:26 INFO : Registering command handlers for SDK TCF services
12:03:26 INFO : Launching XSCT server: xsct.bat -interactive D:\IIITD\ELD_LABs\LAB_8_ZYN

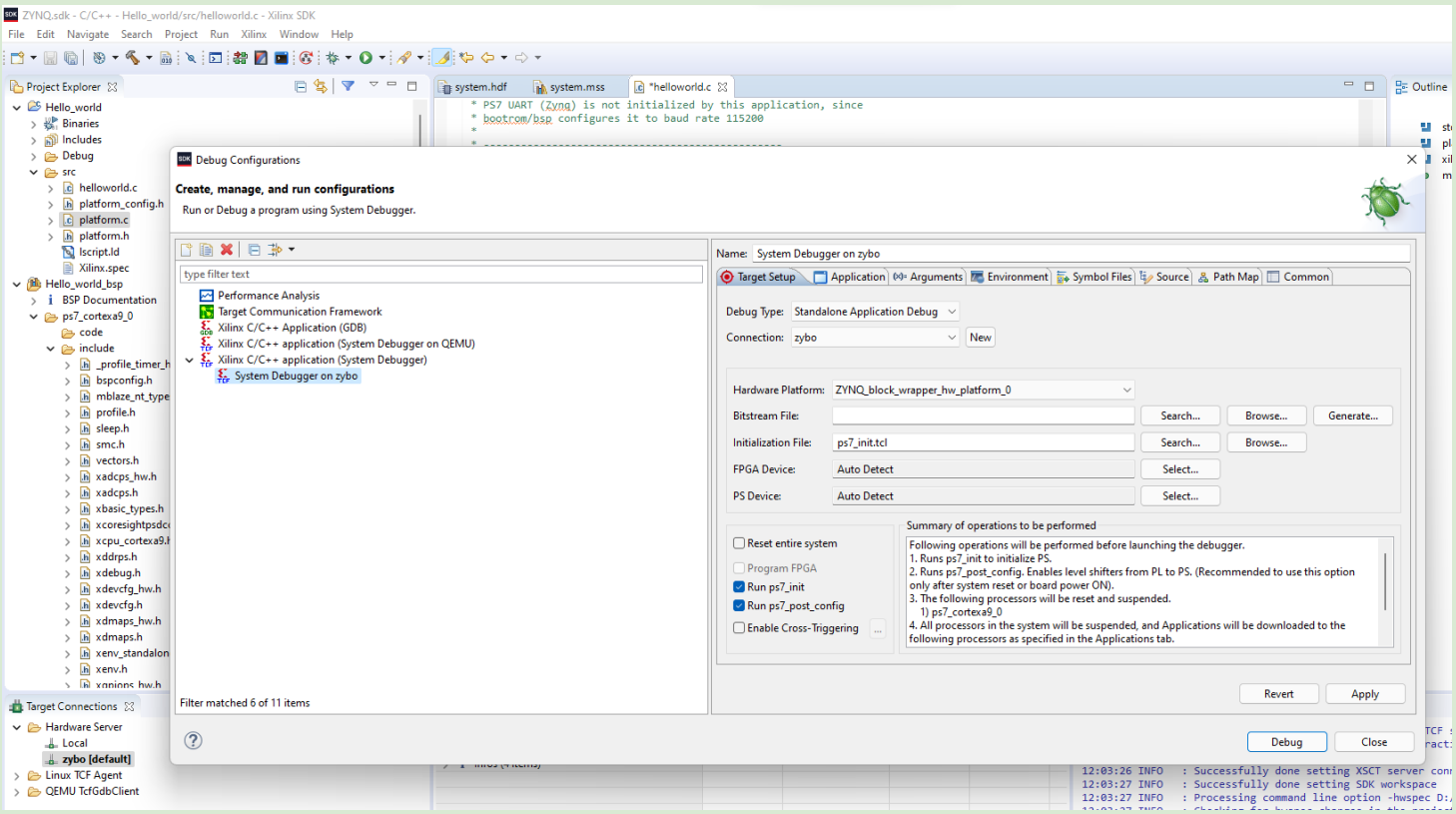

platform.h
lscript.ld
Xilinx.spec
Hello_world_bsp
BSP Documentation
ps7_cortexa9_0
code
include
_profile_timer_hw.h
bspconfig.h
mblaze_nt_types.h
profile.h
sleep.h
smc.h
vectors.h
xadcps_hw.h
xadcps.h
xbasic_types.h
xcoresightpsdcc.h
xcpu_cortexa9.h
xddrps.h
xdebug.h
xdevcfg_hw.h
xdevcfg.h
xdmaps_hw.h
xdmaps.h
xenv_standalone.h
xenv.h
Hardware Specification: D:\IIITD\ELD_LABs\LAB_8_ZYNQ_IP\ZYNQ\ZYNQ.sdk\ZYNQ_block_wrapper_hw_platform_0\system.hdf
Target Processor: ps7_cortexa9_0
Operating System
Board Support Package OS.
Name: standalone
Version: 7.0
Description: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exc
environment, such as standard input and output, profiling, abort and exit.
Documentation: standalone v7_0
Peripheral Drivers
Drivers present in the Board Support Package.
ps7_afi_0 generic
ps7_afi_1 generic
ps7_afi_2 generic
ps7_afi_3 generic
ps7_coresight_comp_0 coresightps_dcc Documentation
ps7_ddr_0 ddrps Documentation
ps7_ddrc_0 generic
ps7_dev_cfg_0 devcfg Documentation Import Examples
ps7_dma_ns dmaps Documentation Import Examples
ps7_dma_s dmaps Documentation Import Examples
ps7_globaltimer_0 generic
ps7_gpio_0 gpiops Documentation Import Examples
ps7_gpv_0 generic
Overview
Source
Target Connections
Hardware Server
Local
zybo [default]
Linux TCF Agent
QEMU TcfGdbClient
Problems
Tasks
Console
Properties
SDK Terminal
1 items
Description
Resource
Path
Location
Type
Infos (1 item)
SDK Log
12:03:26
12:03:26
12:03:26
12:03:26
12:03:27
12:03:27
12:03:27

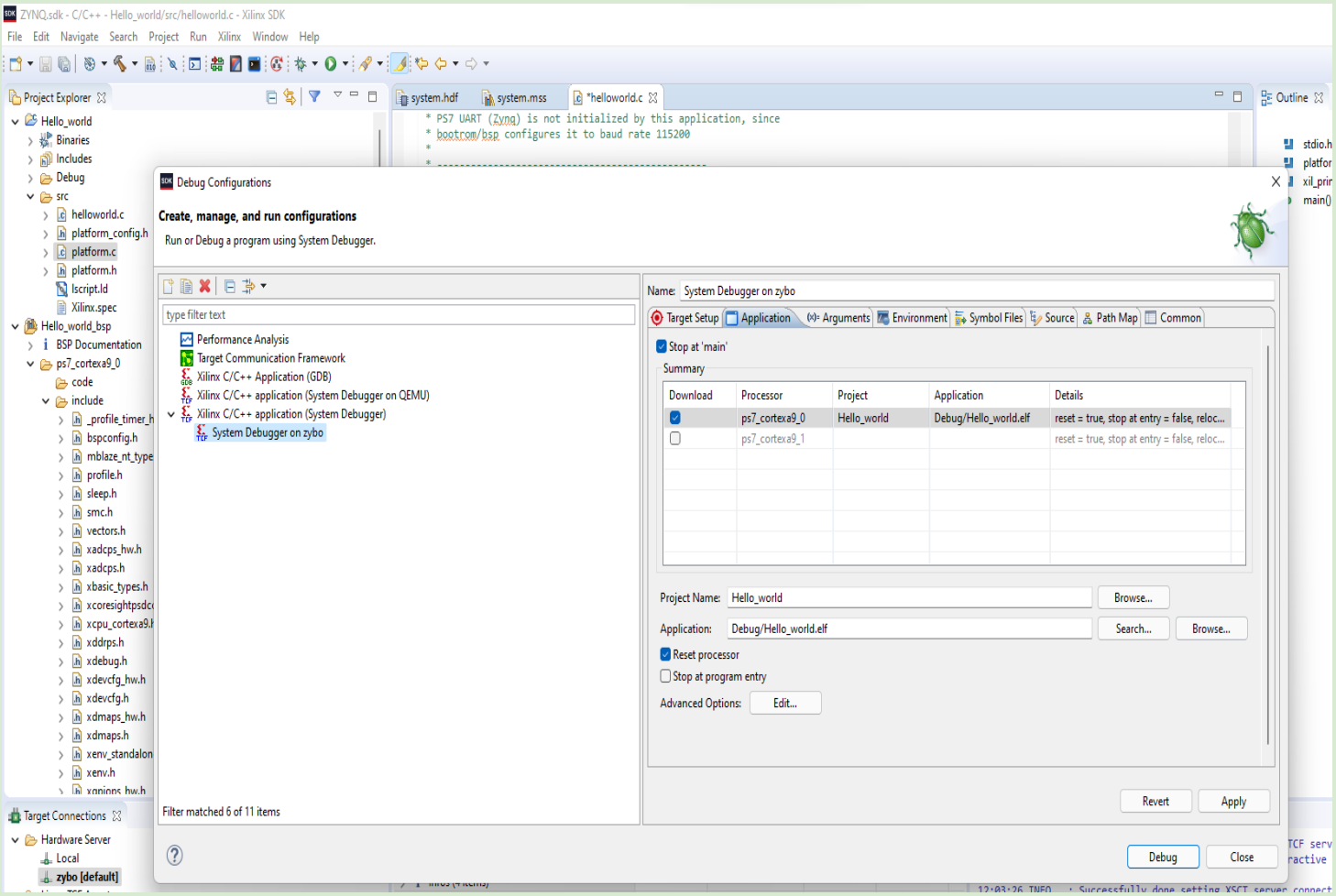

ZYNQ.sdk - C/C++ - Hello_world_bsp/system.mss - Xilinx SDK
File Edit Navigate Search Project Run Xilinx Window Help
Project Explorer
Hello_world
Binaries
Includes
Debug
src
helloworld.c
platform_config.h
platform.c
platform.h
lscript.ld
Xilinx.spec
Hello_world_bsp
BSP Documentation
ps7_cortexa9_0
code
include
_profile_timer_hw.h
bspconfig.h
mblaze_nt_types.h
profile.h
sleep.h
smc.h
vectors.h
xadcps_hw.h
xadcps.h
xbasic_types.h
xcoresightpsdcc.h
xcpu_cortexa9.h
xddrps.h
system.hdf
system.mss
*helloworld.c
Hello_world_bsp Board Support Package
Modify this BSP's Settings
Re-generate BSP Sources
Target Information
This Board Support Package is compiled to run on the following target.
Hardware Specification: D:\IIITD\ELD_LABs\LAB_8_ZYNQ_IP\ZYNQ\ZYNQ.sdk\ZYNQ_block_wrapper_hw_platform_0\system.hdf
Target Processor: ps7_cortexa9_0
Operating System
Board Support Package OS.
Name: standalone
Version: 7.0
Description: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well
environment, such as standard input and output, profiling, abort and exit.
Documentation: standalone v7_0
Peripheral Drivers
Drivers present in the Board Support Package.
ps7_afi_0 generic
ps7_afi_1 generic
ps7_afi_2 generic
ps7_afi_3 generic
ps7_coresight_comp_0 coresightps_dcc Documentation
ps7_ddr_0 ddrps Documentation
ps7_ddrc_0 generic

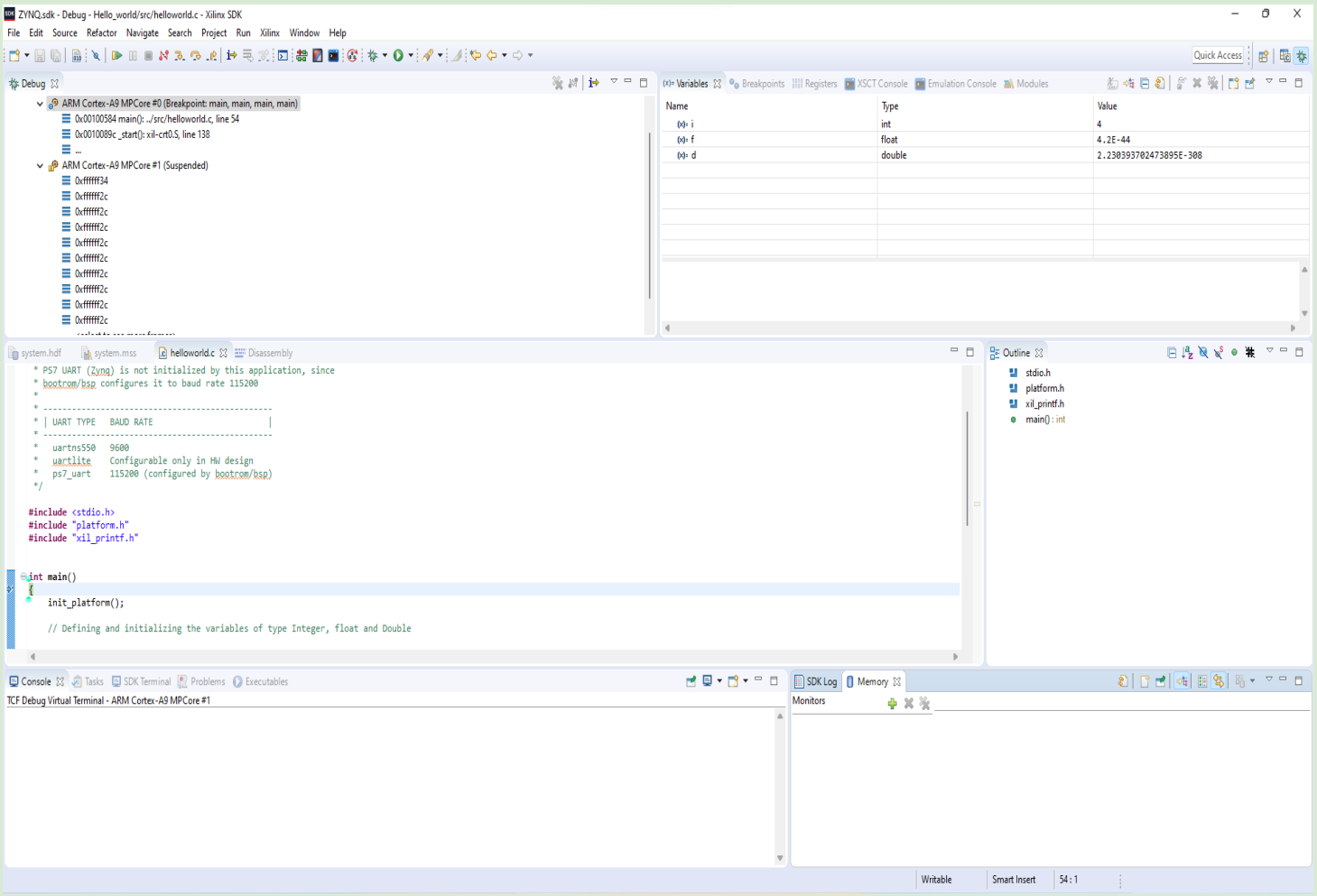


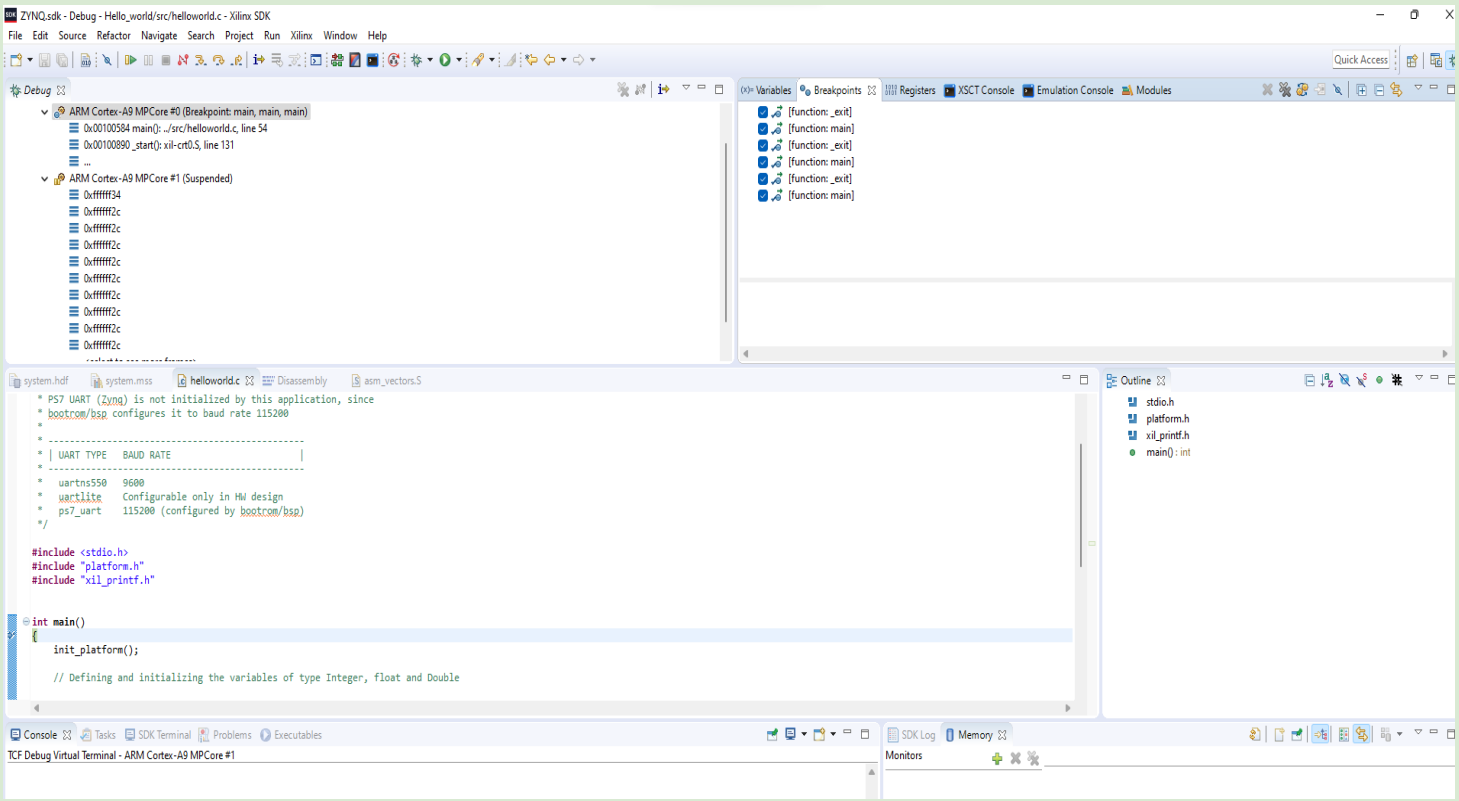
running program in debug mode



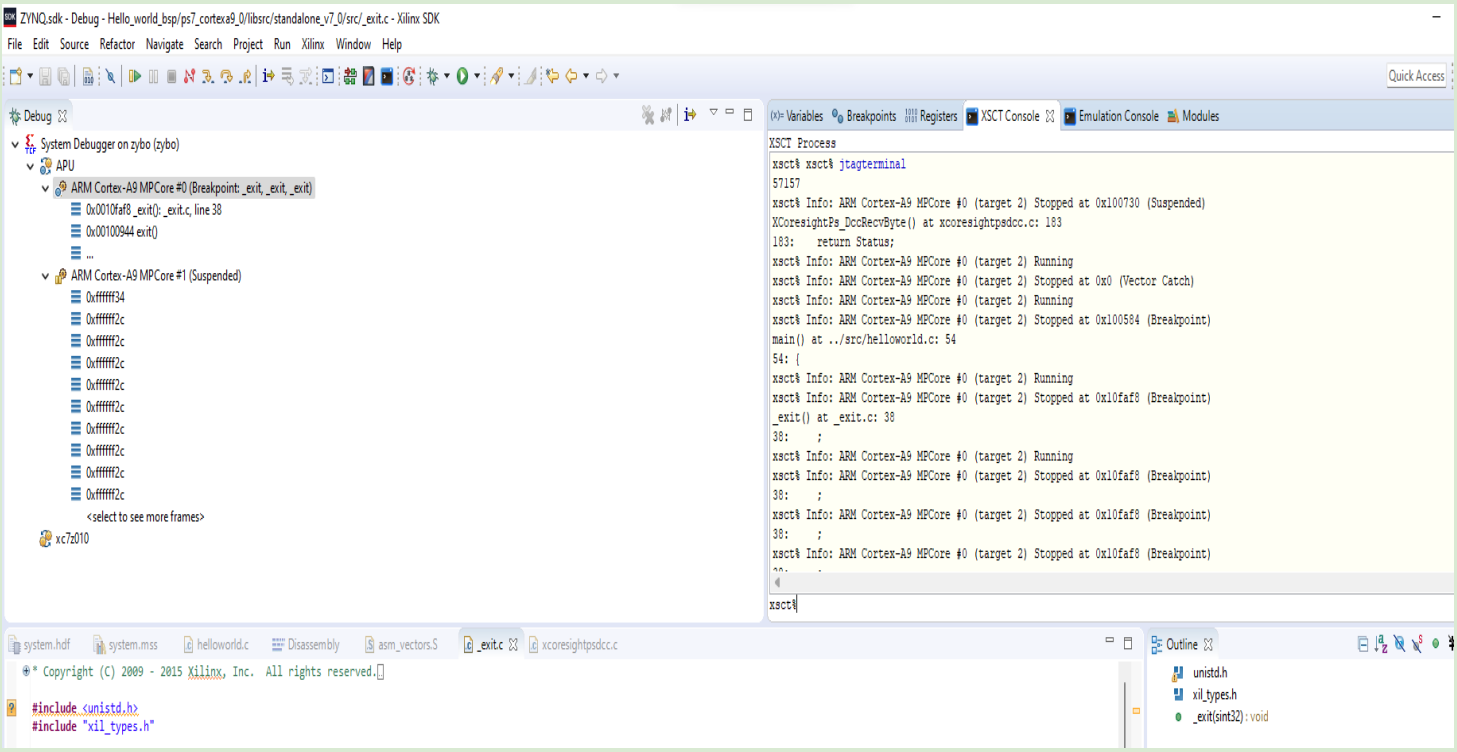

ZYNQ.sdk - C/C++ - Hello_world/src/helloworld.c - Xilinx SDK
File Edit Navigate Search Project Run Xilinx Window Help
Project Explorer
Hello_world
Binaries
Includes
Debug
src
helloworld.c
platform_config.h
platform.c
platform.h
lscript.ld
Xilinx.spec
Hello_world_bsp
BSP Documentation
ps7_cortexa9_0
code
include
system.hdf
system.mss
*helloworld.c
* PS7 UART (Zynq) is not initialized by this application, since
* bootrom/bsp configures it to baud rate 115200
Outline
Debug Configurations
Create, manage, and run configurations
Run or Debug a program using System Debugger.
type filter text
Performance Analysis
Target Communication Framework
Xilinx C/C++ Application (GDB)
Xilinx C/C++ application (System Debugger on QEMU)
Xilinx C/C++ application (System Debugger)
System Debugger on zybo
Filter matched 6 of 11 items
Name: System Debugger on zybo
Target Setup
Application
Arguments
Environment
Symbol Files
Source
Path Map
Common
Debug Type: Standalone Application Debug
Connection: zybo
New
Hardware Platform: ZYNQ_block_wrapper_hw_platform_0
Bitstream File:
Initialization File: ps7_init.tcl
FPGA Device: Auto Detect
PS Device: Auto Detect
Search...
Browse...
Generate...
Select...
Reset entire system
Program FPGA
Run ps7_init
Run ps7_post_config
Enable Cross-Triggering
Summary of operations to be performed
Following operations will be performed before launching the debugger.
1. Runs ps7_init to initialize PS.
2. Runs ps7_post_config. Enables level shifters from PL to PS. (Recommended to use this option only after system reset or board power ON).
3. The following processors will be reset and suspended.
1) ps7_cortexa9_0
4. All processors in the system will be suspended, and Applications will be downloaded to the following processors as specified in the Applications tab.
Revert
Apply
Debug
Close
Target Connections
Hardware Server
Local
zybo [default]
Linux TCF Agent
QEMU TcfGdbClient
12:03:26 INFO : Successfully done setting XSCT server
12:03:27 INFO : Successfully done setting SDK workspace
12:03:27 INFO : Processing command line option -hwspec

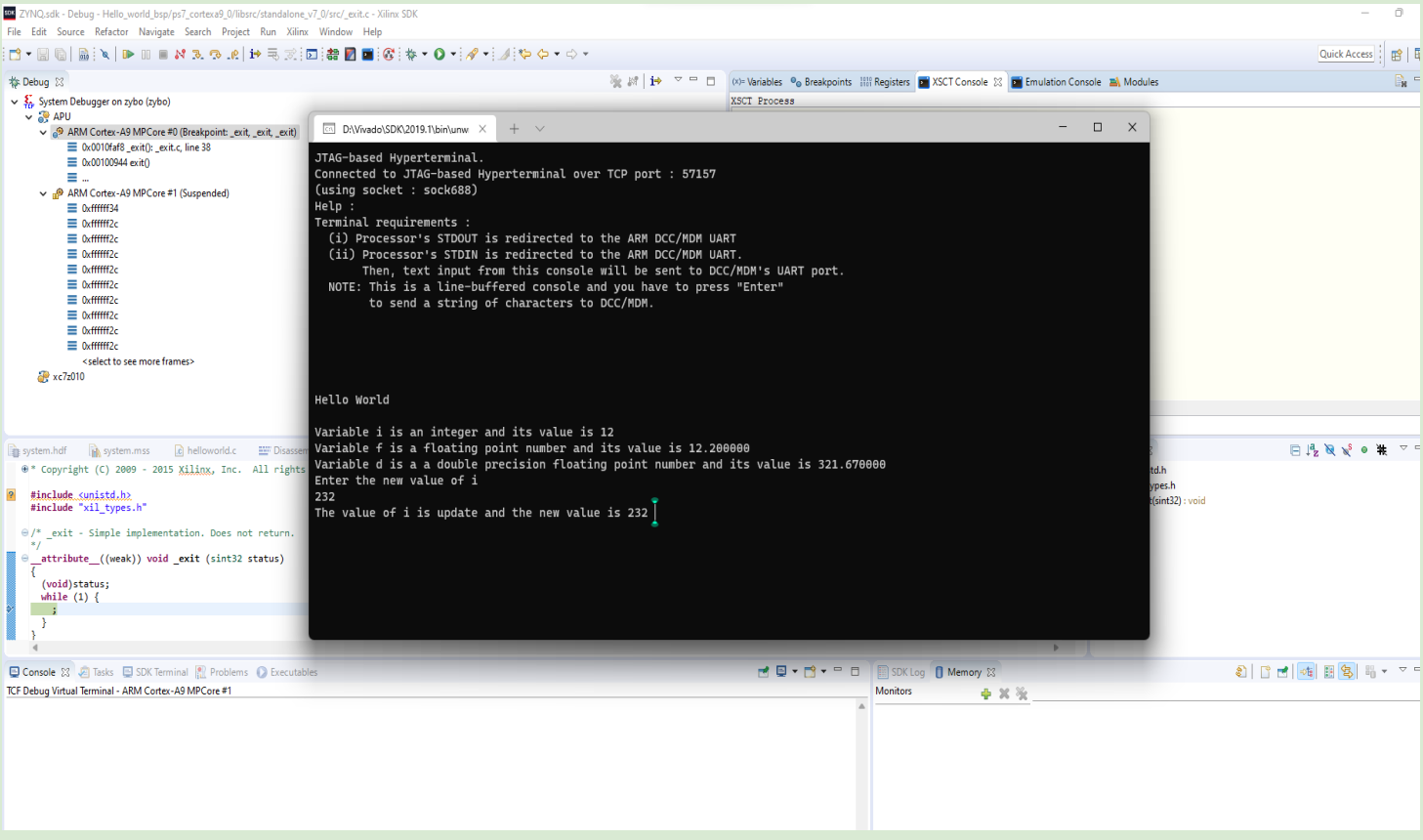

ZYNQ.sdk - C/C++ - Hello_world/src/helloworld.c - Xilinx SDK
File Edit Navigate Search Project Run Xilinx Window Help
Project Explorer
Hello_world
Binaries
Includes
Debug
src
helloworld.c
platform_config.h
platform.c
platform.h
lscript.ld
Xilinx.spec
Hello_world_bsp
BSP Documentation
ps7_cortexa9_0
code
include
system.hdf
system.mss
*helloworld.c
* PS7 UART (Zynq) is not initialized by this application, since
* bootrom/bsp configures it to baud rate 115200
Outline
stdio.h
main()
Debug Configurations
Create, manage, and run configurations
Run or Debug a program using System Debugger.
type filter text
Performance Analysis
Target Communication Framework
Xilinx C/C++ Application (GDB)
Xilinx C/C++ application (System Debugger on QEMU)
Xilinx C/C++ application (System Debugger)
System Debugger on zybo
Filter matched 6 of 11 items
Name: System Debugger on zybo
Target Setup
Application
Arguments
Environment
Symbol Files
Source
Path Map
Common
Stop at 'main'
Summary
Download
Processor
Project
Application
Details
ps7_cortexa9_0
Hello_world
Debug/Hello_world.elf
reset = true, stop at entry = false, reloc...
ps7_cortexa9_1
reset = true, stop at entry = false, reloc...
Project Name: Hello_world
Application: Debug/Hello_world.elf
Browse...
Search...
Reset processor
Stop at program entry
Advanced Options:
Edit...
Revert
Apply
Debug
Close
Target Connections
Hardware Server
Local
zybo [default]


ZYNQ.sdk - Debug - Hello_world/src/helloworld.c - Xilinx SDK
File Edit Source Refactor Navigate Search Project Run Xilinx Window Help
Quick Access
Debug
ARM Cortex-A9 MPCore #0 (Breakpoint: main, main, main)
0x00100584 main(): ../src/helloworld.c, line 54
0x0010089c _start(): xil-crt0.S, line 138
ARM Cortex-A9 MPCore #1 (Suspended)
0xffffff34
0xffffff2c
Variables
Breakpoints
Registers
XSCT Console
Emulation Console
Modules
Name
Type
Value
i
int
4
f
float
4.2E-44
d
double
2.2303937024738 95E-308
system.hdf
system.mss
helloworld.c
Disassembly
* PS7 UART (Zynq) is not initialized by this application, since
* bootrom/bsp configures it to baud rate 115200
* UART TYPE BAUD RATE
* uartns550 9600
* uartlite Configurable only in HW design
* ps7_uart 115200 (configured by bootrom/bsp)
#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"
int main()
{
init_platform();
// Defining and initializing the variables of type Integer, float and Double
Outline
stdio.h
platform.h
xil_printf.h
main() : int
Console
Tasks
SDK Terminal
Problems
Executables
TCF Debug Virtual Terminal - ARM Cortex-A9 MPCore #1
SDK Log
Memory
Monitors
Writable
Smart Insert
54 : 1


ZYNQ.sdk - Debug - Hello_world/src/helloworld.c - Xilinx SDK
File Edit Source Refactor Navigate Search Project Run Xilinx Window Help
Quick Access
Debug
ARM Cortex-A9 MPCore #0 (Breakpoint: main, main, main)
0x00100584 main(): ../src/helloworld.c, line 54
0x00100890 _start(): xil-crt0.S, line 131
ARM Cortex-A9 MPCore #1 (Suspended)
0xffffff34
0xffffff2c
Variables
Breakpoints
Registers
XSCT Console
Emulation Console
Modules
[function: _exit]
[function: main]
[function: _exit]
[function: main]
[function: _exit]
[function: main]
system.hdf
system.mss
helloworld.c
Disassembly
asm_vectors.S
* PS7 UART (Zynq) is not initialized by this application, since
* bootrom/bsp configures it to baud rate 115200
* UART TYPE BAUD RATE
* uartns550 9600
* uartlite Configurable only in HW design
* ps7_uart 115200 (configured by bootrom/bsp)
#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"
int main()
{
init_platform();
// Defining and initializing the variables of type Integer, float and Double
Outline
stdio.h
platform.h
xil_printf.h
main() : int
Console
Tasks
SDK Terminal
Problems
Executables
TCF Debug Virtual Terminal - ARM Cortex-A9 MPCore #1
SDK Log
Memory
Monitors

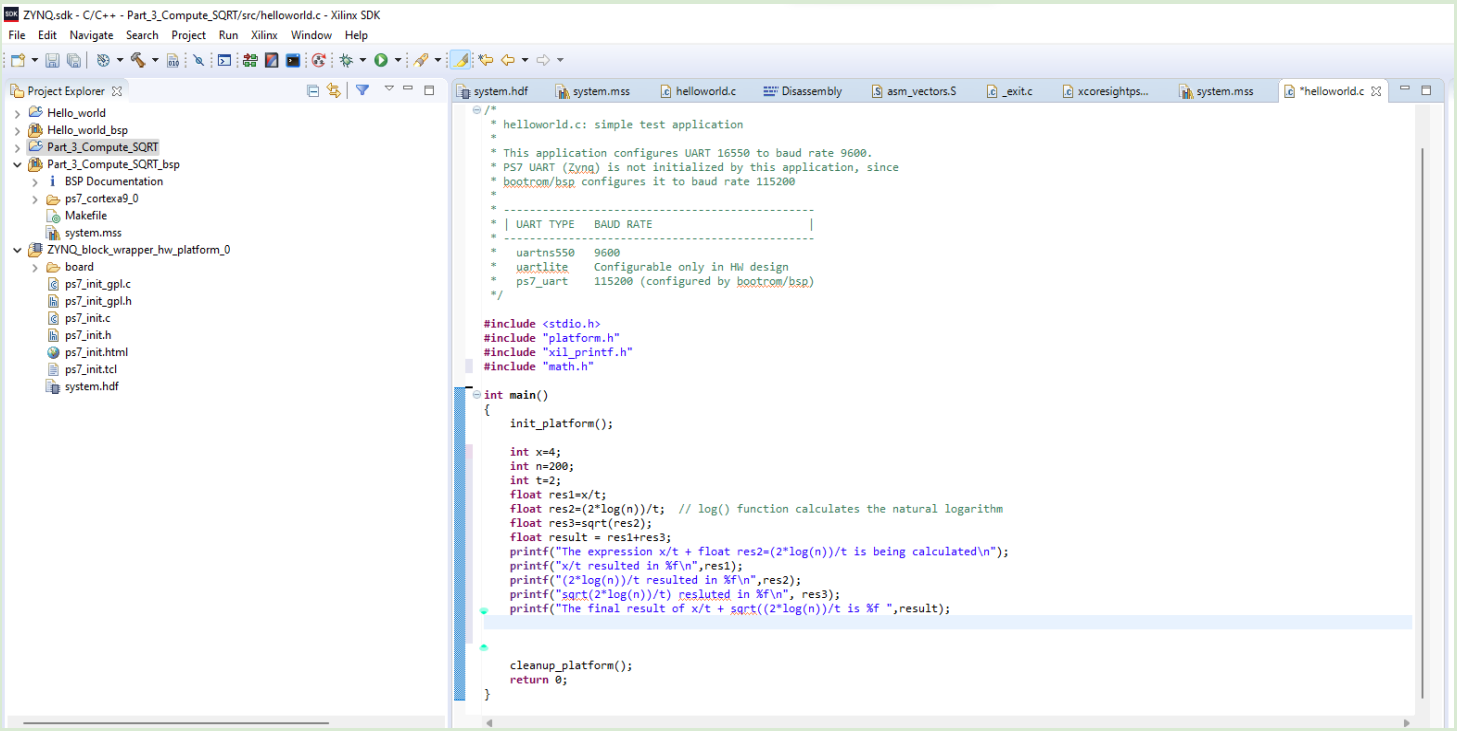
opening JTAG terminal and resuming our program

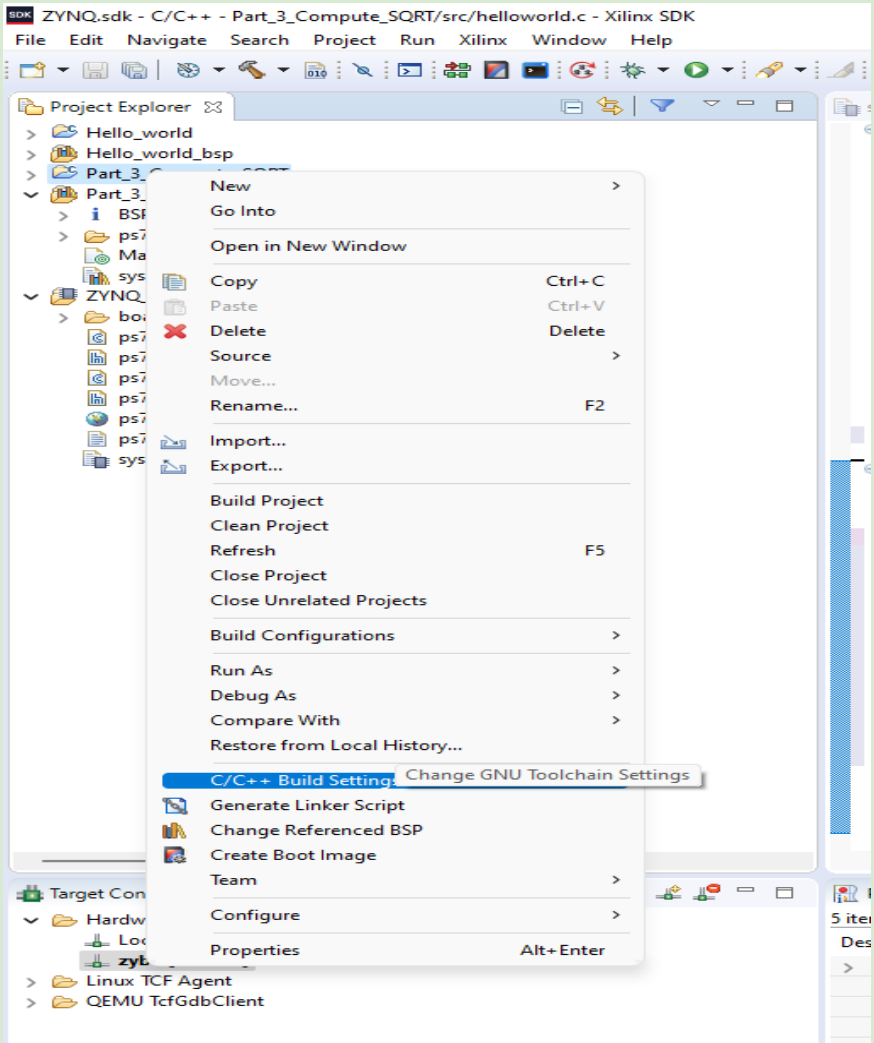


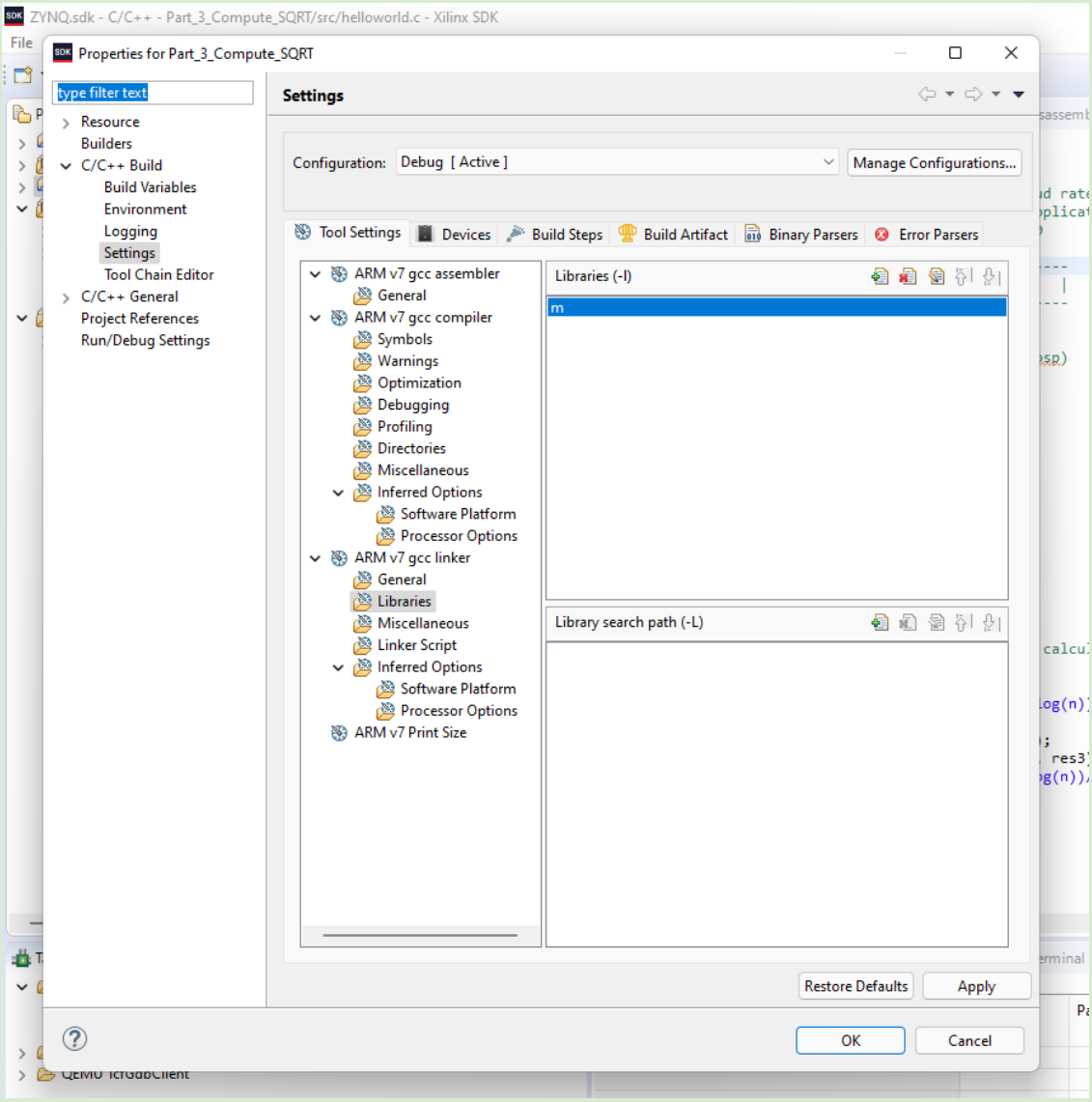


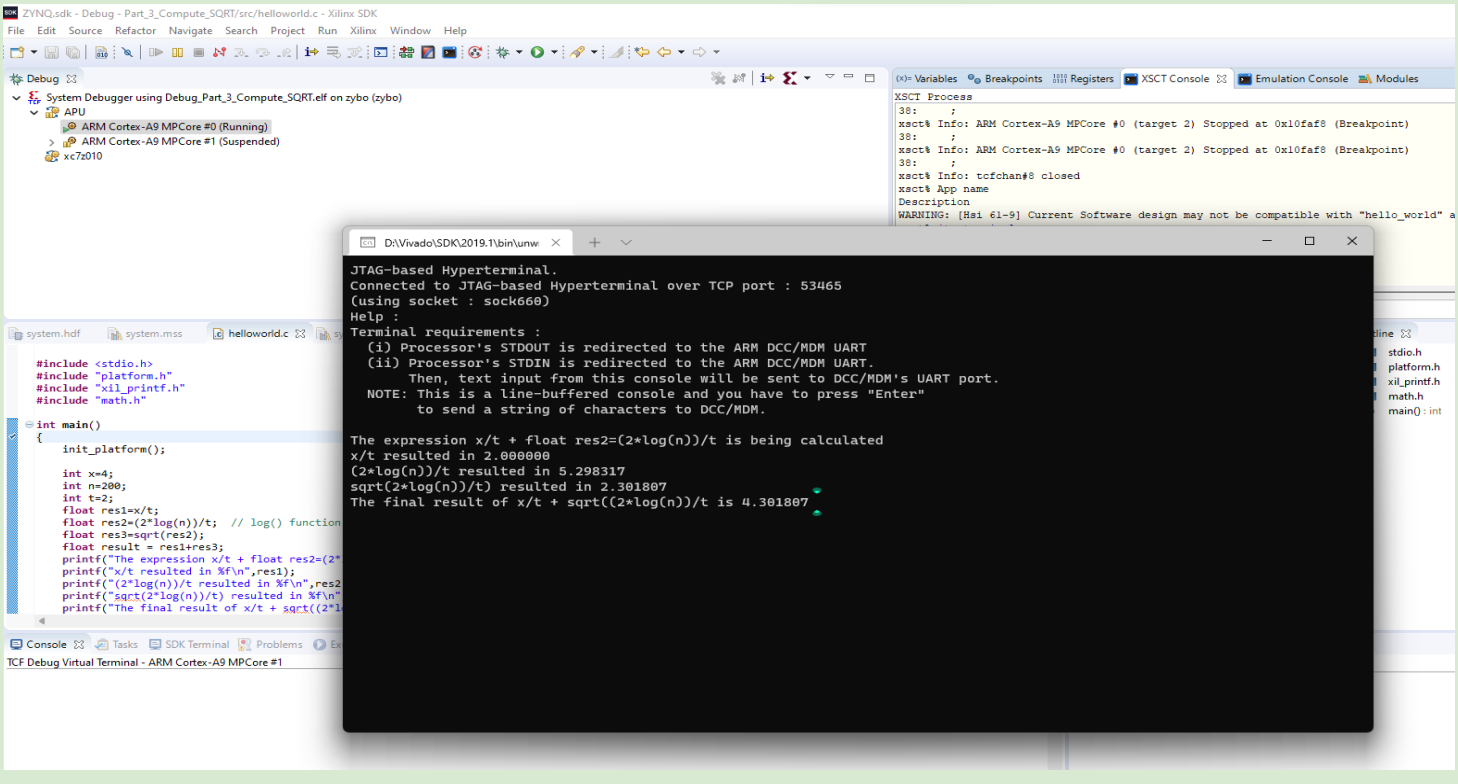
Writing a C application to compute the following expression.

*X/T +SQRT(2*LogN/T)*






ZYNQ.sdk - C/C++ - Part_3_Compute_SQRT/src/helloworld.c - Xilinx SDK
Properties for Part_3_Compute_SQRT
type filter text
Resource
Builders
C/C++ Build
Build Variables
Environment
Logging
Settings
Tool Chain Editor
C/C++ General
Project References
Run/Debug Settings
Settings
Configuration: Debug [Active]
Manage Configurations...
Tool Settings
Devices
Build Steps
Build Artifact
Binary Parsers
Error Parsers
ARM v7 gcc assembler
General
ARM v7 gcc compiler
Symbols
Warnings
Optimization
Debugging
Profiling
Directories
Miscellaneous
Inferred Options
Software Platform
Processor Options
ARM v7 gcc linker
General
Libraries
Miscellaneous
Linker Script
Inferred Options
Software Platform
Processor Options
ARM v7 Print Size
Libraries (-l)
m
Library search path (-L)
Restore Defaults
Apply
OK
Cancel


ZYNQ.sdk - Debug - Part_3_Compute_SQRT/src/helloworld.c - Xilinx SDK
System Debugger using Debug_Part_3_Compute_SQRT.elf on zybo (zybo)
APU
ARM Cortex-A9 MPCore #0 (Running)
ARM Cortex-A9 MPCore #1 (Suspended)
xc7z010
D:\Vivado\SDK\2019.1\bin\unw
JTAG-based Hyperterminal.
Connected to JTAG-based Hyperterminal over TCP port : 53465
(using socket : sock660)
Help :
Terminal requirements :
(i) Processor's STDOUT is redirected to the ARM DCC/MDM UART
(ii) Processor's STDIN is redirected to the ARM DCC/MDM UART.
Then, text input from this console will be sent to DCC/MDM's UART port.
NOTE: This is a line-buffered console and you have to press "Enter"
to send a string of characters to DCC/MDM.
The expression x/t + float res2=(2*log(n))/t is being calculated
x/t resulted in 2.000000
(2*log(n))/t resulted in 5.298317
sqrt(2*log(n))/t) resulted in 2.301807
The final result of x/t + sqrt((2*log(n))/t is 4.301807
#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"
#include "math.h"
int main()
{
init_platform();
int x=4;
int n=200;
int t=2;
float res1=x/t;
float res2=(2*log(n))/t;
float res3=sqrt(res2);
float result = res1+res3;
printf("The expression x/t + float res2=(2*
printf("x/t resulted in %f\n",res1);
printf("(2*log(n))/t resulted in %f\n",res2
printf("sqrt(2*log(n))/t) resulted in %f\n"
printf("The final result of x/t + sqrt((2*l
TCF Debug Virtual Terminal - ARM Cortex-A9 MPCore #1

ZYNQ.sdk - C/C++ - FFT8/src/helloworld.c - Xilinx SDK

File Edit Navigate Search Project Run Xilinx Window Help

helloworld.c | Disassembly | _exit.c | FFT8.elf

```
* Copyright (C) 2009 - 2014 Xilinx, Inc.  All rights reserved.

/*
 * helloworld.c: simple test application
 *
 * This application configures UART 16550 to baud rate 9600.
 * PS7 UART (Zynq) is not initialized by this application, since
 * bootrom/bsp configures it to baud rate 115200
 *
 * ------------------------------------------------
 * | UART TYPE   BAUD RATE                        |
 * ------------------------------------------------
 *   uartns550   9600
 *   uartlite    Configurable only in HW design
 *   ps7_uart    115200 (configured by bootrom/bsp)
 */

#include <stdio.h>
#include <stdlib.h>
#include <complex.h>


# define N 8

const int rev8[N] = {0,4,2,6,1,5,3,7};

const float complex W[N/2] = { 1-0*I, 0.7071067811865476 - 0.707106781165475*I, 0.0-1*I, -0.7071067811865475-0.7071067811865476*I };

void bitreverse(float complex dataIn[N], float complex dataOut[N])
{
       bit_reversal: for (int i=0 ; i<N ; i++)
       {
           dataOut[i]= dataIn[rev8[i]];
       }

}

void FFT_Stages(float complex FFT_Input[N], float complex FFT_Output[N])
{

    float complex temp1[N], temp2[N];
    stage1: for(int i=0 ; i<N ; i=i+2)
    {
        temp1[i]= FFT_Input[i]+FFT_Input[i+1];
        temp1[i+1]=FFT_Input[i]-FFT_Input[i+1];
    }

    stage2: for(int i=0 ; i<N ;i=i+4)
    {
        for(int j=0 ; j<2 ; ++j)
        {
            temp2[i+j]=temp1[i+j]+W[2*j]*temp1[i+j+2];
            temp2[i+j+2]= temp1[i+j]- W[2*j]*temp1[i+j+2];
        }
    }

    stage3: for (int i=0 ; i < N/2 ; i++)
    {
```

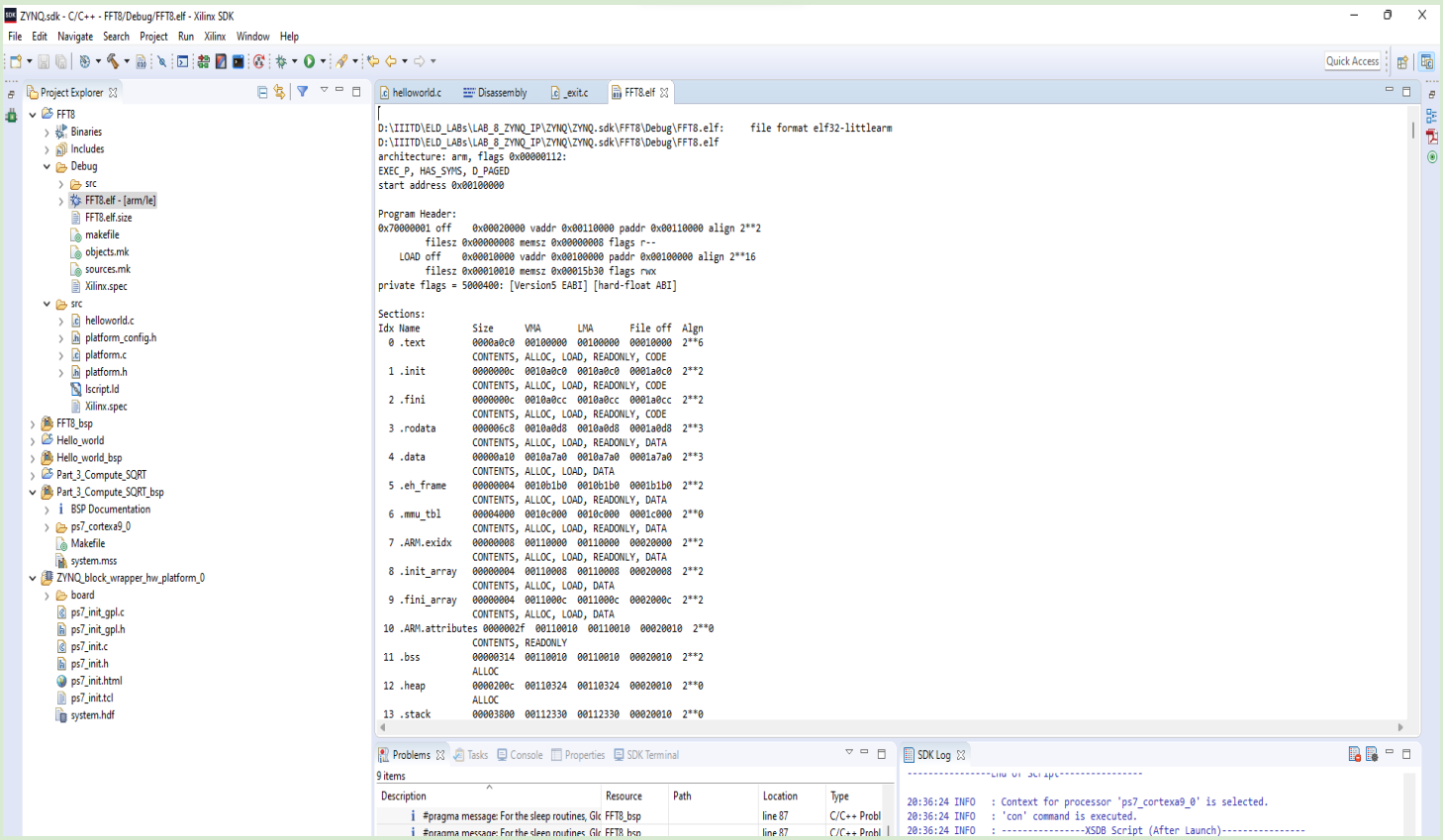
ZYNQ.sdk - C/C++ - FFT8/src/helloworld.c - Xilinx SDK

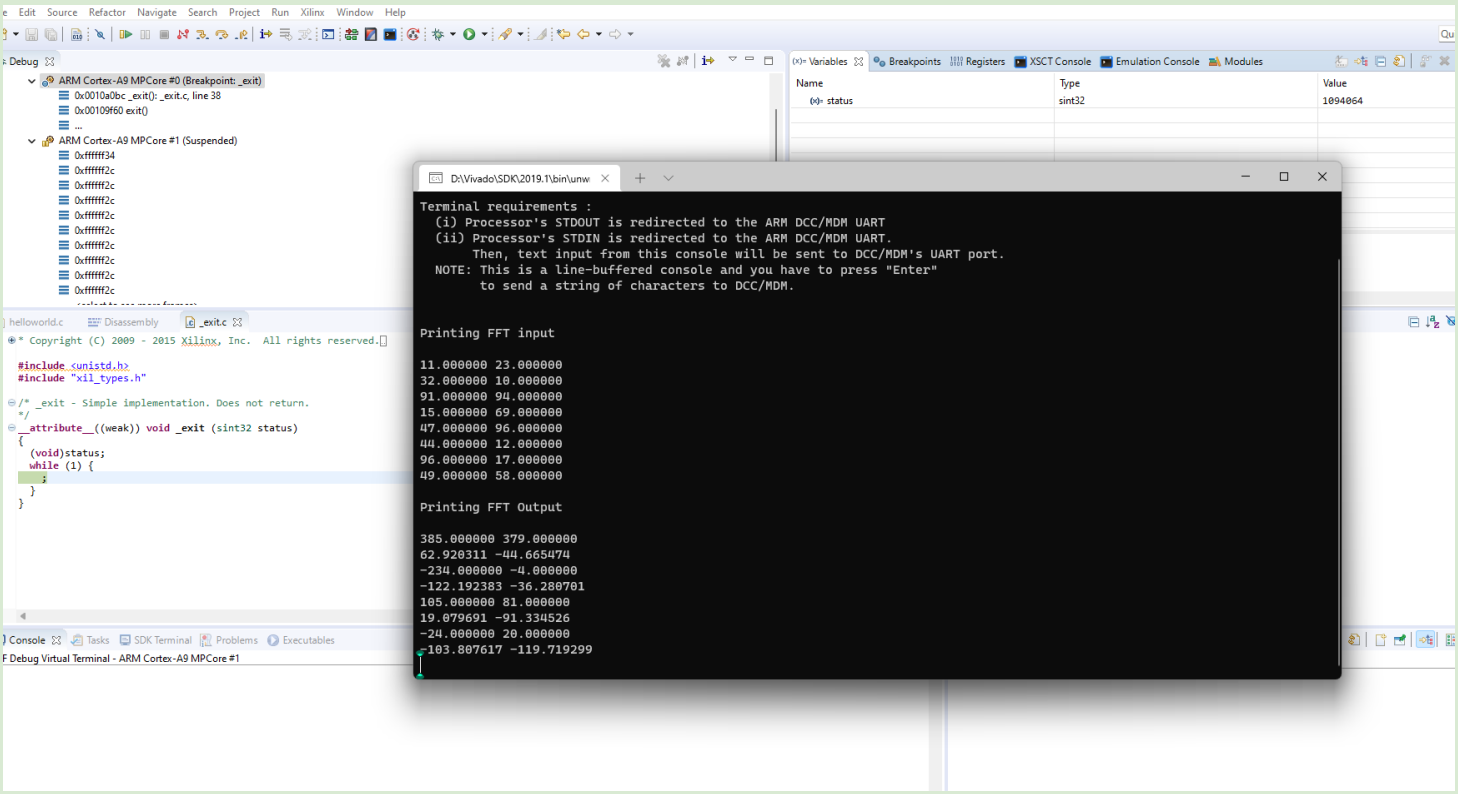
File Edit Navigate Search Project Run Xilinx Window Help

helloworld.c | Disassembly | _exit.c | FFT8.elf

```
        bit_reversal: for (int i=0 ; i<N ; i++)
        {
            dataOut[i]= dataIn[rev8[i]];
        }

}

void FFT_Stages(float complex FFT_Input[N], float complex FFT_Output[N])
{

    float complex temp1[N], temp2[N];
    stage1: for(int i=0 ; i<N ; i=i+2)
    {
        temp1[i]= FFT_Input[i]+FFT_Input[i+1];
        temp1[i+1]=FFT_Input[i]-FFT_Input[i+1];
    }

    stage2: for(int i=0 ; i<N ;i=i+4)
    {
        for(int j=0 ; j<2 ; ++j)
        {
            temp2[i+j]=temp1[i+j]+W[2*j]*temp1[i+j+2];
            temp2[i+j+2]= temp1[i+j]- W[2*j]*temp1[i+j+2];
        }
    }

    stage3: for (int i=0 ; i < N/2 ; i++)
    {
        FFT_Output[i]= temp2[i] + W[i]*temp2[i+4];
        FFT_Output[i+4]= temp2[i]- W[i]*temp2[i+4];
    }
}

int main()
{
    const float complex FFT_Input[N] = {11+23*I, 32+10*I, 91+94*I, 15+69*I, 47+96*I, 44+12*I, 96+17*I, 49+58*I};
    float complex FFT_Output[N];
    float complex FFT_rev[N];

    bitreverse(FFT_Input, FFT_rev);
    FFT_Stages(FFT_rev, FFT_Output);
    printf("\nPrinting FFT input\r\n");
    for (int i=0 ; i<N ; i++)
    {
        printf("%f %f \n", crealf(FFT_Input[i]),cimagf(FFT_Input[i]));
    }

    printf("\nPrinting FFT Output \r\n");
    for(int i =0; i<N ; i++)
    {
        printf("%f %f \n", crealf(FFT_Output[i]), cimagf(FFT_Output[i]));
    }

}
```

.elf files of the program in Debug folder (similar to byte code of java_program)





Conclusion:

Successfully created block design in Vivado using the IP Integrator and configure the Zynq IP according to our needs and wrote C programs for Standalone system and seen output using JTAG terminal.