INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

Department
of
Electronics & Communication Engineering

Embedded Logic Design(ECE270)

Dr. Sumit J Darak

Lab_7: FFT IP Implementation and test bench.

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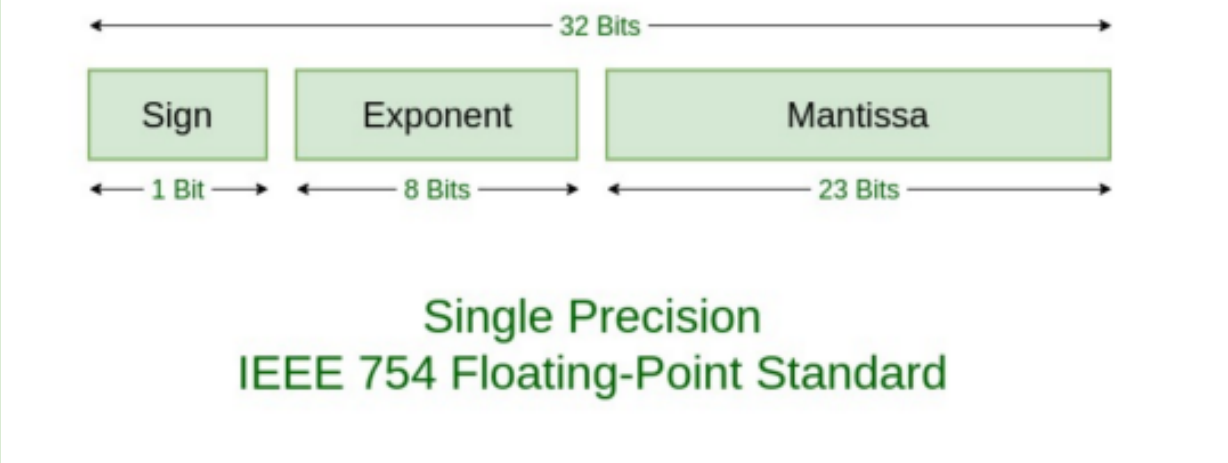
2020220

10-11-2021

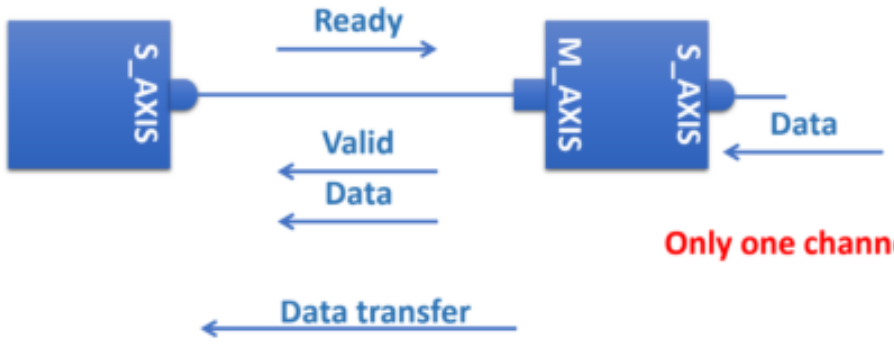
OBJECTIVE:

- AXI Stream Protocol Use
- Floating Point IP usage
- FFT IP Implementation and test bench.

Theory:



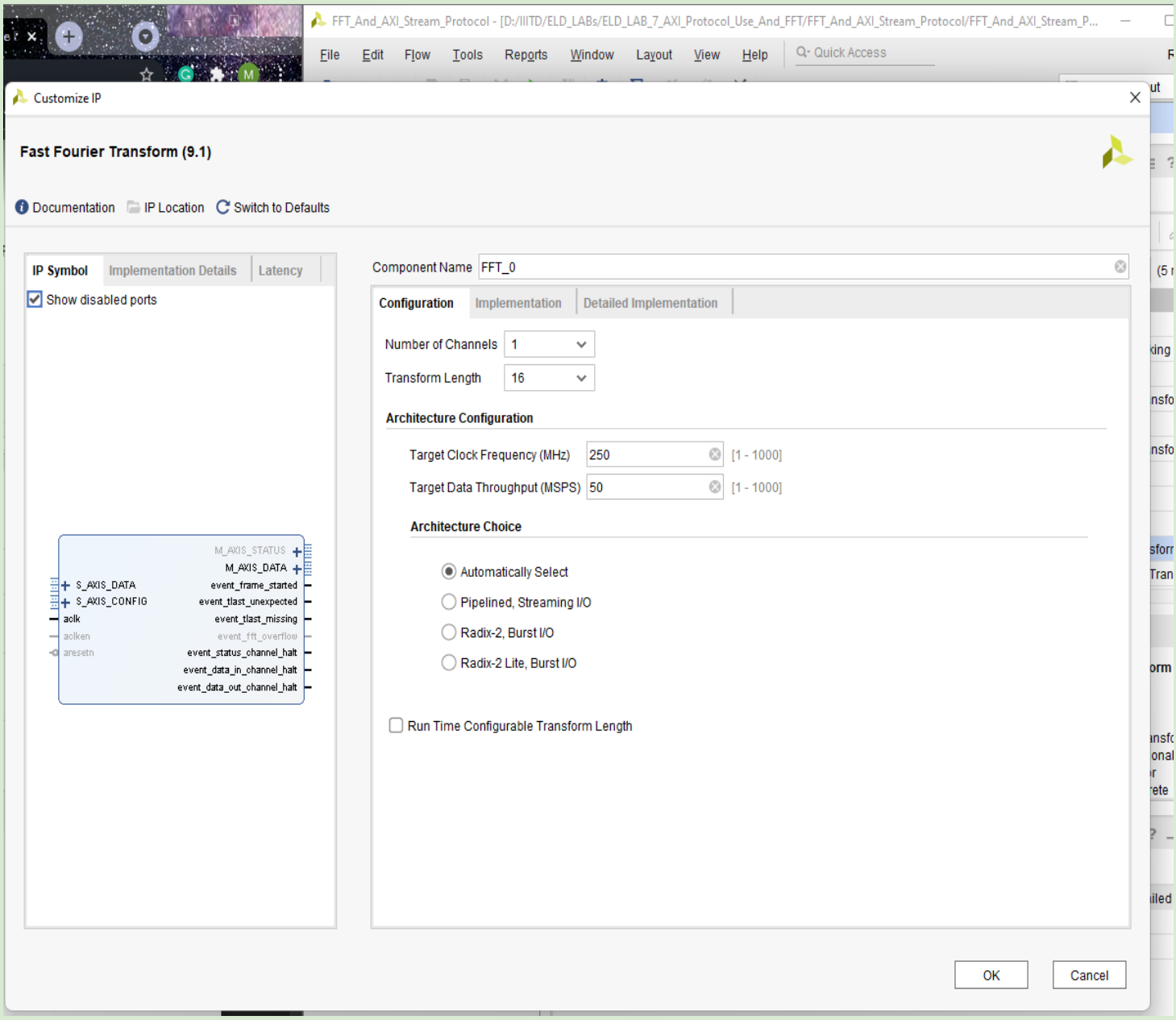
The Floating-point IP will be using the AXI Protocols (AXI Stream in particular). Two concepts that will be useful in this Lab are Master-Slave and Valid Ready Signals. In AXI, the transactions take place between Master and Slave, as shown below:



The AXI Master initiates the transactions, and the slave responds to it. Many signals are associated with a transaction out of which the valid and ready signals are useful for this Lab. More information on these signals is covered in the Lab tutorial video.

Observations:

FFT IP Wizard :



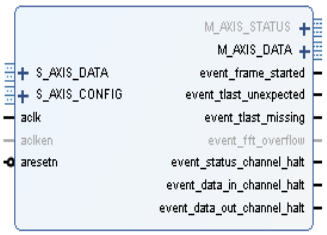
Customize IP

Fast Fourier Transform (9.1)

Documentation | IP Location | Switch to Defaults

IP Symbol | Implementation Details | Latency

Show disabled ports



Component Name: FFT_0

Configuration | **Implementation** | Detailed Implementation

Data Format: Floating Point

Scaling Options: Scaled

Rounding Modes: Truncation

Precision Options

Input Data Width: 32

Phase Factor Width: 24

Control Signals

ACLKEN | ARESETn (active low)

ARESETn must be asserted for a minimum of 2 cycles

Output Ordering Options

Output Ordering: Natural Order

Cyclic Prefix Insertion

Optional Output Fields

XK_INDEX | OVFLO

Throttle Scheme

Non Real Time | Real Time

OK | Cancel

Re-customize IP

Fast Fourier Transform (9.1)

Documentation | IP Location | Switch to Defaults

IP Symbol | **Implementation Details** | Latency

Information

implementation : Pipelined, Streaming I/O

Transform Size

Largest : 16
Smallest : 16
Output Data Width : 32

Resource Estimates Group

DSP48 Slices : 8
Block RAMs : 2

AXI4 Stream Port Structure

S_AXIS_DATA - TDATA

Transaction	Field	Type
0	CHAN_0_XN_IM_0(63:32)	float_single
	CHAN_0_XN_RE_0(31:0)	float_single
1	CHAN_0_XN_IM_1(63:32)	float_single
	CHAN_0_XN_RE_1(31:0)	float_single
2	CHAN_0_XN_IM_2(63:32)	float_single
	CHAN_0_XN_RE_2(31:0)	float_single
3	CHAN_0_XN_IM_3(63:32)	float_single
	CHAN_0_XN_RE_3(31:0)	float_single
...		
15	CHAN_0_XN_IM_15(63:32)	float_single
	CHAN_0_XN_RE_15(31:0)	float_single

S_AXIS_CONFIG - TDATA

Component Name: FFT_0

Configuration | Implementation | Detailed Implementation

Number of Channels: 1

Transform Length: 16

Architecture Configuration

Target Clock Frequency (MHz): 250 [1 - 1000]

Target Data Throughput (MSPS): 50 [1 - 1000]

Architecture Choice

- (•) Automatically Select
- ( ) Pipelined, Streaming I/O
- ( ) Radix-2, Burst I/O
- ( ) Radix-2 Lite, Burst I/O

[ ] Run Time Configurable Transform Length

Re-customize IP

Fast Fourier Transform (9.1)

Documentation | IP Location | Switch to Defaults

IP Symbol | **Implementation Details** | Latency

2	CHAN_0_XN_IM_2(63:32)	float_single
	CHAN_0_XN_RE_2(31:0)	float_single
3	CHAN_0_XN_IM_3(63:32)	float_single
	CHAN_0_XN_RE_3(31:0)	float_single
...		
15	CHAN_0_XN_IM_15(63:32)	float_single
	CHAN_0_XN_RE_15(31:0)	float_single

S_AXIS_CONFIG - TDATA

Transaction	Field	Type
0	SCALE_SCH_0(4:1)	bit4
	FWD_INV_0(0:0)	bit1

M_AXIS_DATA - TDATA

Transaction	Field	Type
0	CHAN_0_XN_IM_0(63:32)	float_single
	CHAN_0_XN_RE_0(31:0)	float_single
1	CHAN_0_XN_IM_1(63:32)	float_single
	CHAN_0_XN_RE_1(31:0)	float_single
2	CHAN_0_XN_IM_2(63:32)	float_single
	CHAN_0_XN_RE_2(31:0)	float_single
3	CHAN_0_XN_IM_3(63:32)	float_single
	CHAN_0_XN_RE_3(31:0)	float_single
...		
15	CHAN_0_XN_IM_15(63:32)	float_single
	CHAN_0_XN_RE_15(31:0)	float_single

Component Name: FFT_0

Configuration | Implementation | Detailed Implementation

Number of Channels: 1

Transform Length: 16

Architecture Configuration

Target Clock Frequency (MHz): 250 [1 - 1000]

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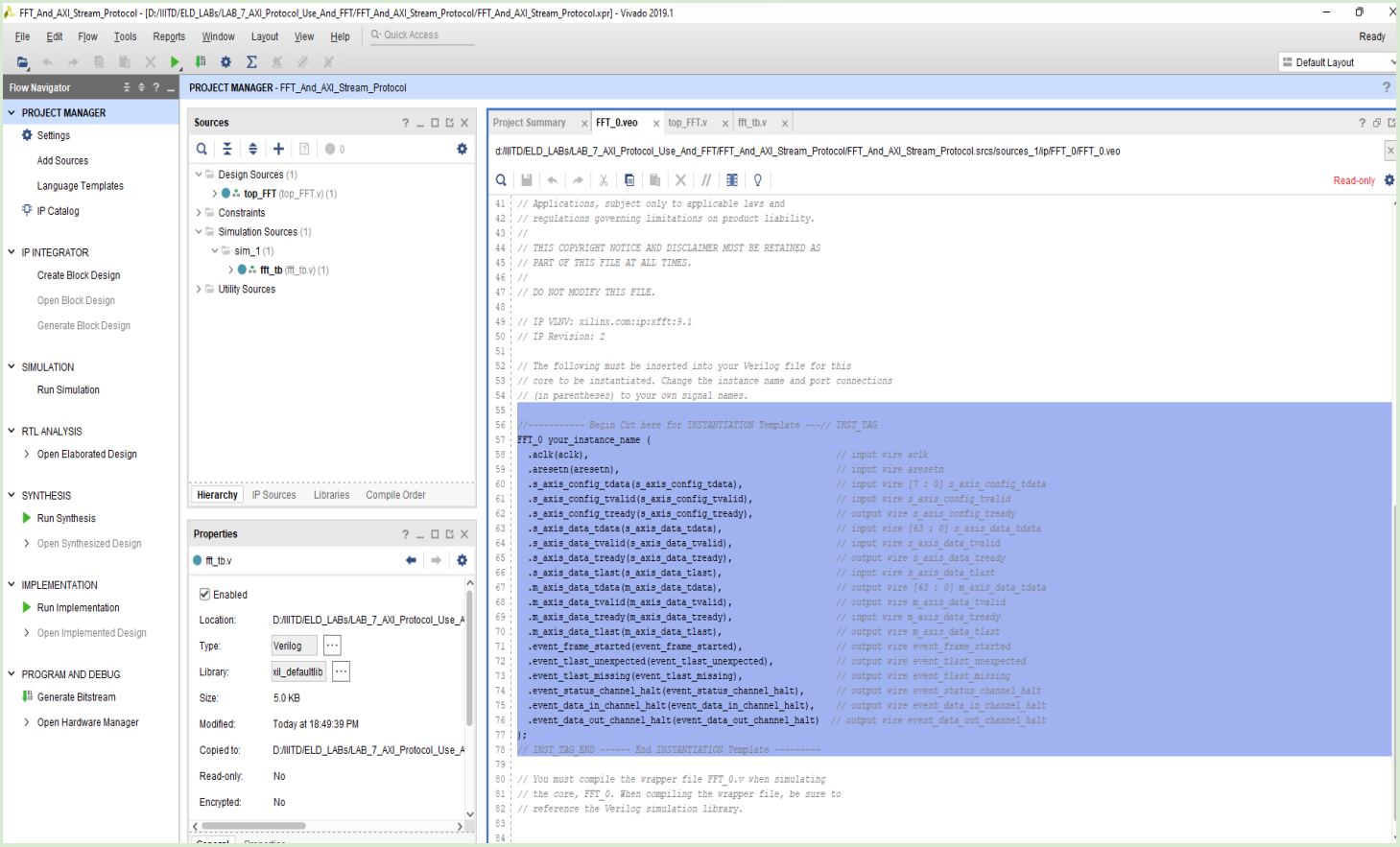
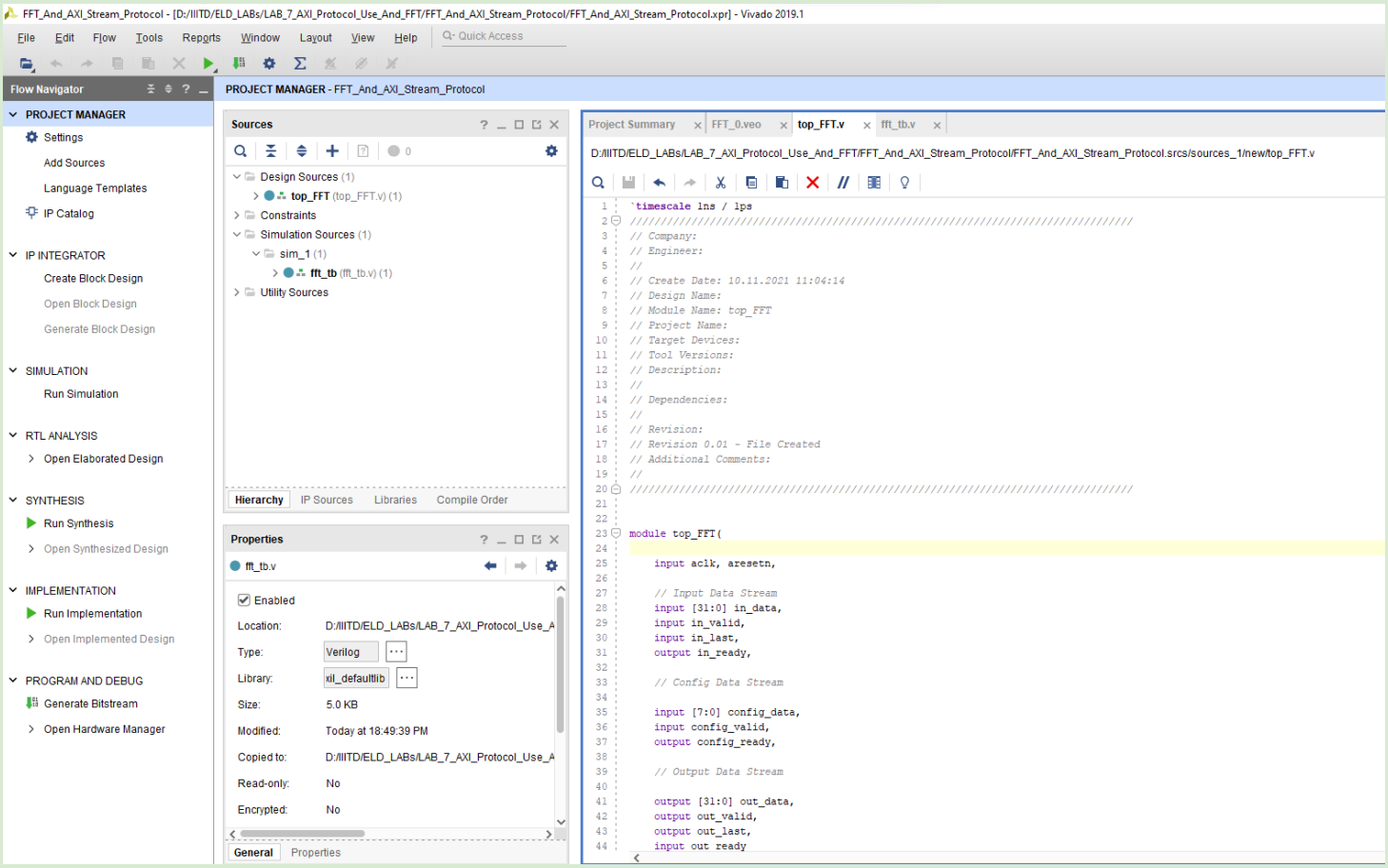
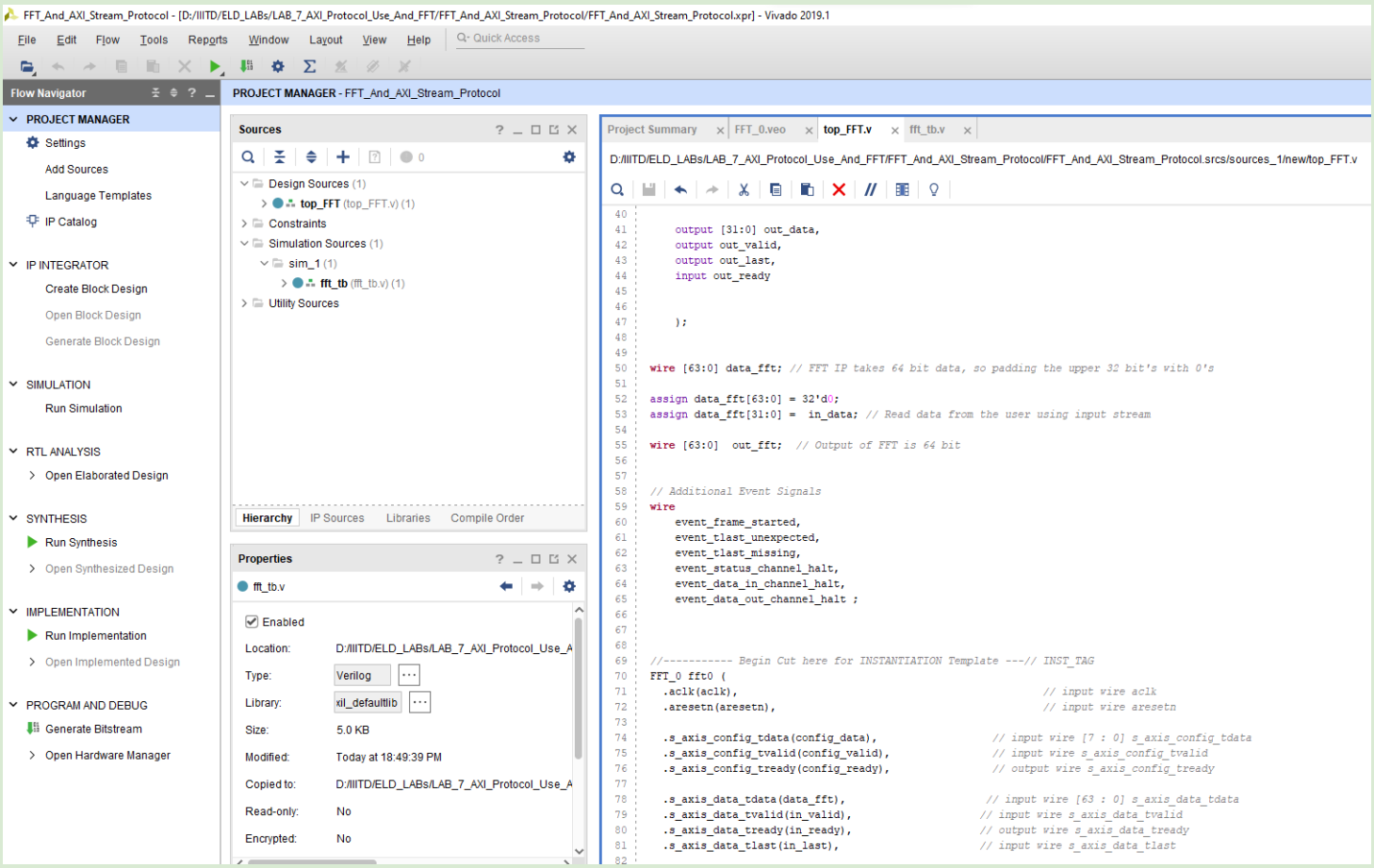
[ ] Run Time Configurable Transform Length



programme for the functionality of FFT (FastFourier Transform)




FFT_And_AXI_Stream_Protocol - [D:/IIITD/ELD_LABs/LAB_7_AXI_Protocol_Use_And_FFT/FFT_And_AXI_Stream_Protocol/FFT_And_AXI_Stream_Protocol.xpr] - Vivado 2019.1
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sim_1 (1)
fft_tb (fft_tb.v) (1)
Utility Sources
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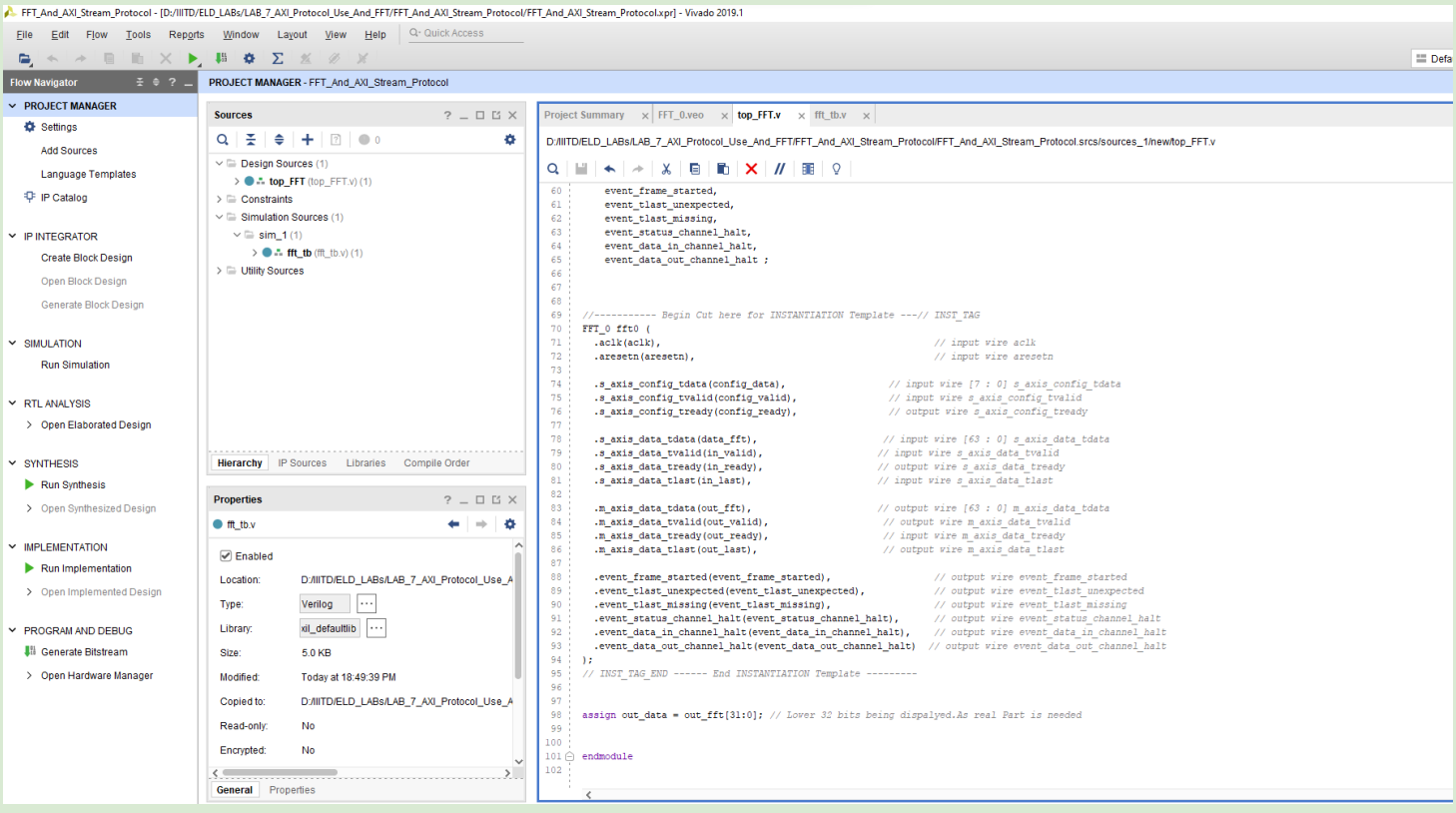
Properties
fft_tb.v
Enabled
Location: D:/IIITD/ELD_LABs/LAB_7_AXI_Protocol_Use_A
Type: Verilog
Library: xil_defaultlib
Size: 5.0 KB
Modified: Today at 18:49:39 PM
Copied to: D:/IIITD/ELD_LABs/LAB_7_AXI_Protocol_Use_A
Read-only: No
Encrypted: No
Project Summary
FFT_0.veo
top_FFT.v
fft_tb.v
D:/IIITD/ELD_LABs/LAB_7_AXI_Protocol_Use_And_FFT/FFT_And_AXI_Stream_Protocol/FFT_And_AXI_Stream_Protocol.srcs/sources_1/new/top_FFT.v
output [31:0] out_data,
output out_valid,
output out_last,
input out_ready
);
wire [63:0] data_fft; // FFT IP takes 64 bit data, so padding the upper 32 bit's with 0's
assign data_fft[63:0] = 32'd0;
assign data_fft[31:0] = in_data; // Read data from the user using input stream
wire [63:0] out_fft; // Output of FFT is 64 bit
// Additional Event Signals
wire
event_frame_started,
event_tlast_unexpected,
event_tlast_missing,
event_status_channel_halt,
event_data_in_channel_halt,
event_data_out_channel_halt ;
//----------- Begin Cut here for INSTANTIATION Template ---// INST_TAG
FFT_0 fft0 (
.aclk(aclk), // input wire aclk
.aresetn(aresetn), // input wire aresetn
.s_axis_config_tdata(config_data), // input wire [7 : 0] s_axis_config_tdata
.s_axis_config_tvalid(config_valid), // input wire s_axis_config_tvalid
.s_axis_config_tready(config_ready), // output wire s_axis_config_tready
.s_axis_data_tdata(data_fft), // input wire [63 : 0] s_axis_data_tdata
.s_axis_data_tvalid(in_valid), // input wire s_axis_data_tvalid
.s_axis_data_tready(in_ready), // output wire s_axis_data_tready
.s_axis_data_tlast(in_last), // input wire s_axis_data_tlast


FFT_And_AXI_Stream_Protocol - [D:/IIITD/ELD_LABs/LAB_7_AXI_Protocol_Use_And_FFT/FFT_And_AXI_Stream_Protocol/FFT_And_AXI_Stream_Protocol.xpr] - Vivado 2019.1
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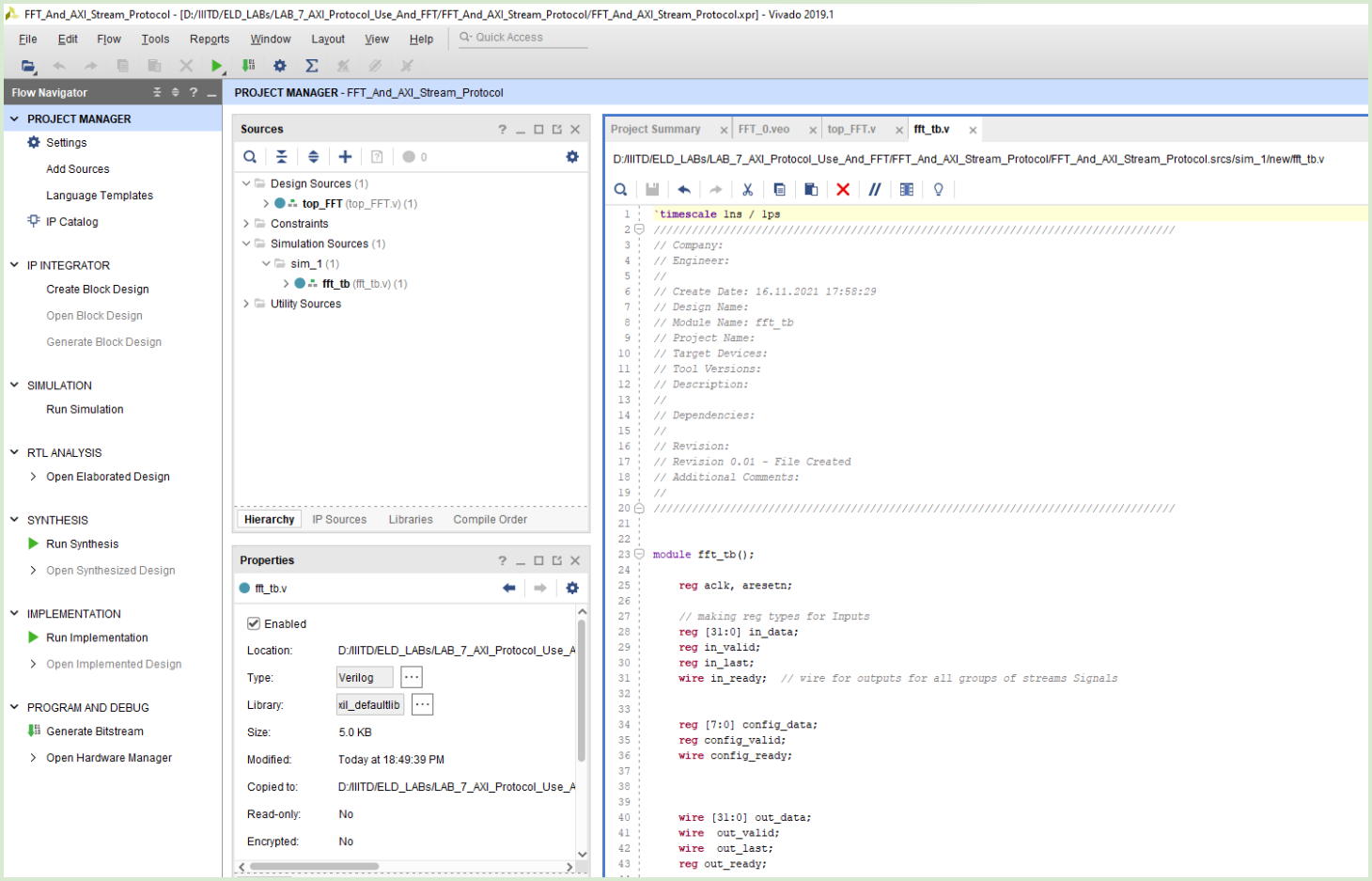
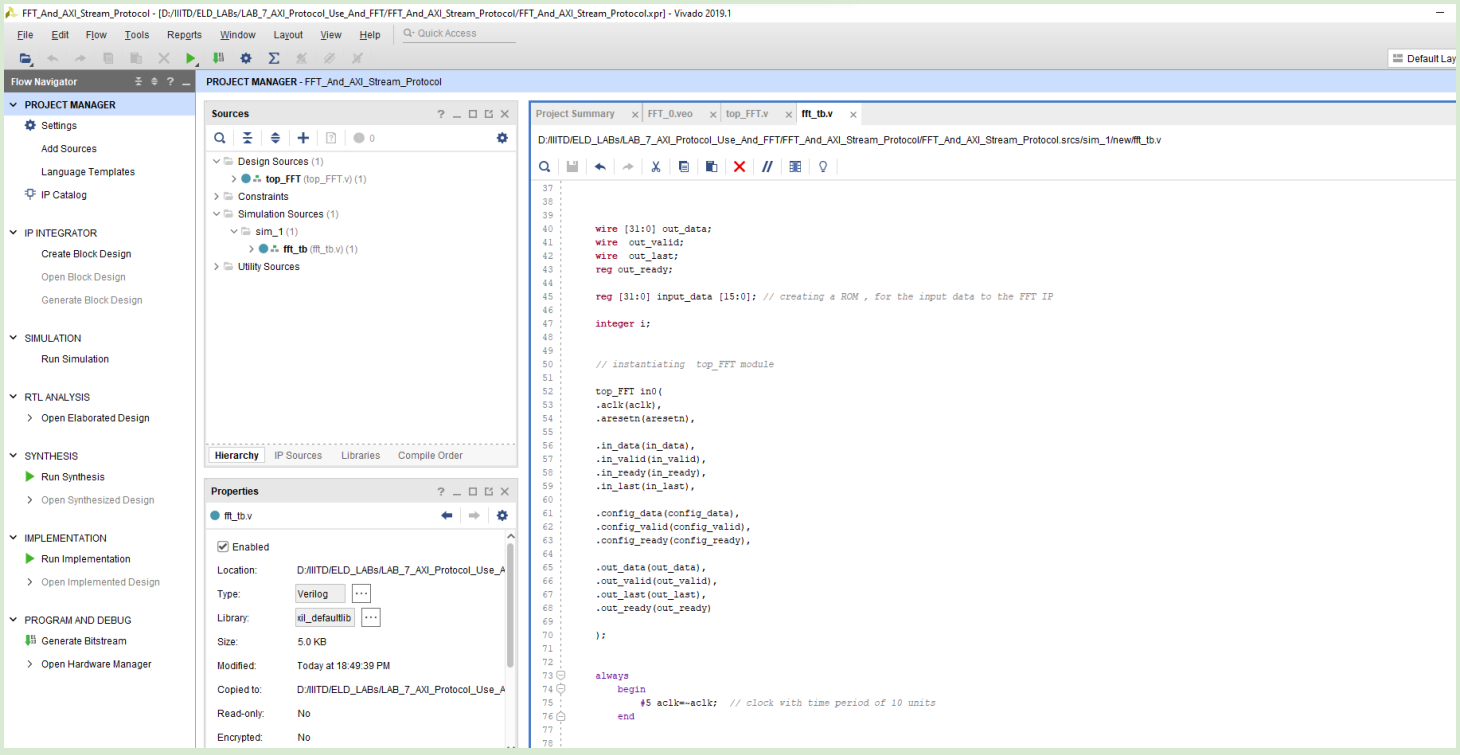
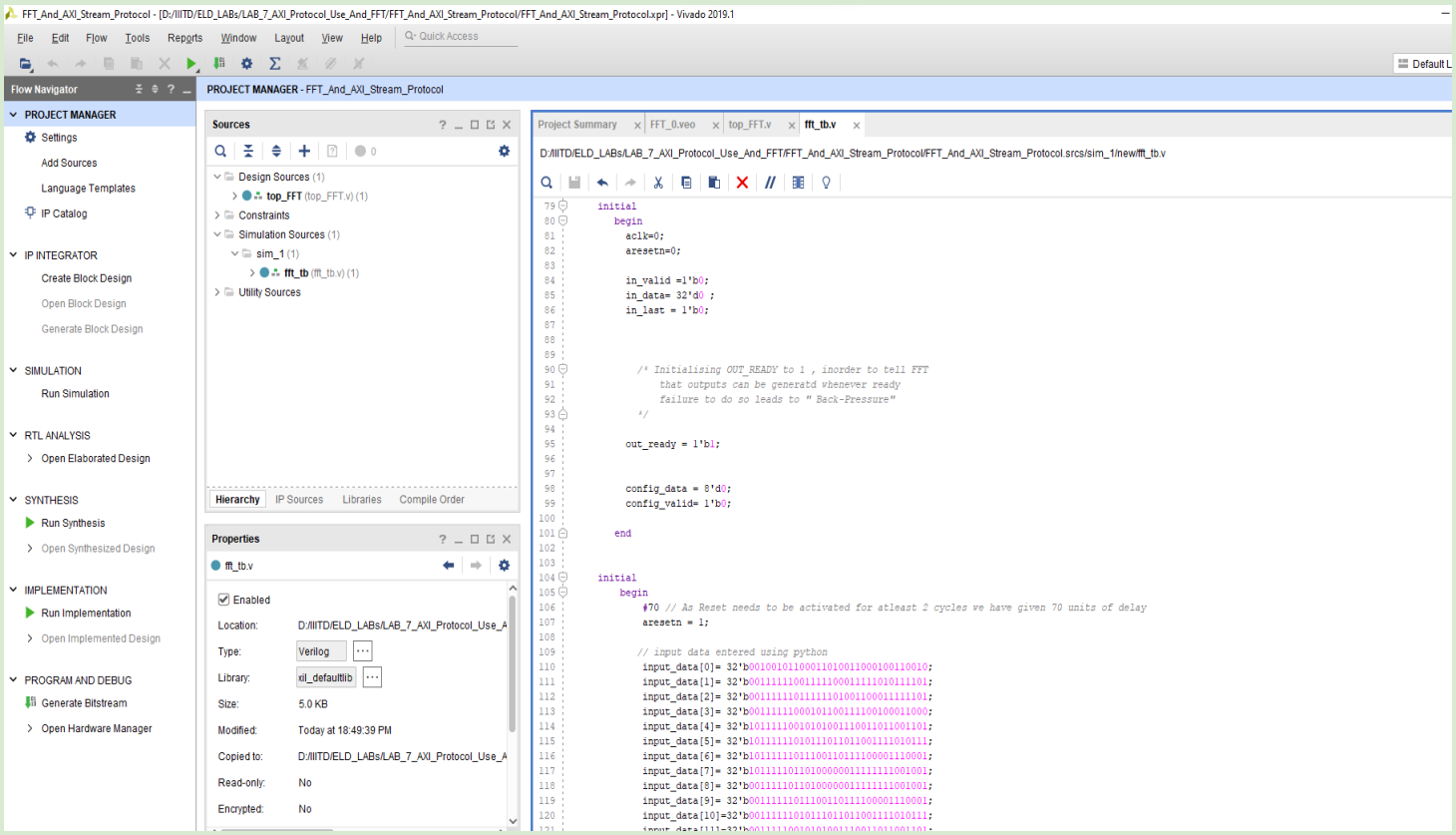
Properties
fft_tb.v
Enabled
Location: D:/IIITD/ELD_LABs/LAB_7_AXI_Protocol_Use_A
Type: Verilog
Library: xil_defaultlib
Size: 5.0 KB
Modified: Today at 18:49:39 PM
Copied to: D:/IIITD/ELD_LABs/LAB_7_AXI_Protocol_Use_A
Read-only: No
Encrypted: No
General Properties
Project Summary
FFT_0.veo
top_FFT.v
fft_tb.v
D:/IIITD/ELD_LABs/LAB_7_AXI_Protocol_Use_And_FFT/FFT_And_AXI_Stream_Protocol/FFT_And_AXI_Stream_Protocol.srcs/sources_1/new/top_FFT.v
event_frame_started,
event_tlast_unexpected,
event_tlast_missing,
event_status_channel_halt,
event_data_in_channel_halt,
event_data_out_channel_halt ;
//----------- Begin Cut here for INSTANTIATION Template ---// INST_TAG
FFT_0 fft0 (
.aclk(aclk), // input wire aclk
.aresetn(aresetn), // input wire aresetn
.s_axis_config_tdata(config_data), // input wire [7 : 0] s_axis_config_tdata
.s_axis_config_tvalid(config_valid), // input wire s_axis_config_tvalid
.s_axis_config_tready(config_ready), // output wire s_axis_config_tready
.s_axis_data_tdata(data_fft), // input wire [63 : 0] s_axis_data_tdata
.s_axis_data_tvalid(in_valid), // input wire s_axis_data_tvalid
.s_axis_data_tready(in_ready), // output wire s_axis_data_tready
.s_axis_data_tlast(in_last), // input wire s_axis_data_tlast
.m_axis_data_tdata(out_fft), // output wire [63 : 0] m_axis_data_tdata
.m_axis_data_tvalid(out_valid), // output wire m_axis_data_tvalid
.m_axis_data_tready(out_ready), // input wire m_axis_data_tready
.m_axis_data_tlast(out_last), // output wire m_axis_data_tlast
.event_frame_started(event_frame_started), // output wire event_frame_started
.event_tlast_unexpected(event_tlast_unexpected), // output wire event_tlast_unexpected
.event_tlast_missing(event_tlast_missing), // output wire event_tlast_missing
.event_status_channel_halt(event_status_channel_halt), // output wire event_status_channel_halt
.event_data_in_channel_halt(event_data_in_channel_halt), // output wire event_data_in_channel_halt
.event_data_out_channel_halt(event_data_out_channel_halt) // output wire event_data_out_channel_halt
);
// INST_TAG_END ------ End INSTANTIATION Template ---------
assign out_data = out_fft[31:0]; // Lower 32 bits being dispalyed.As real Part is needed
endmodule

Testbench for FFT:



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Read-only: No
Encrypted: No
Project Summary
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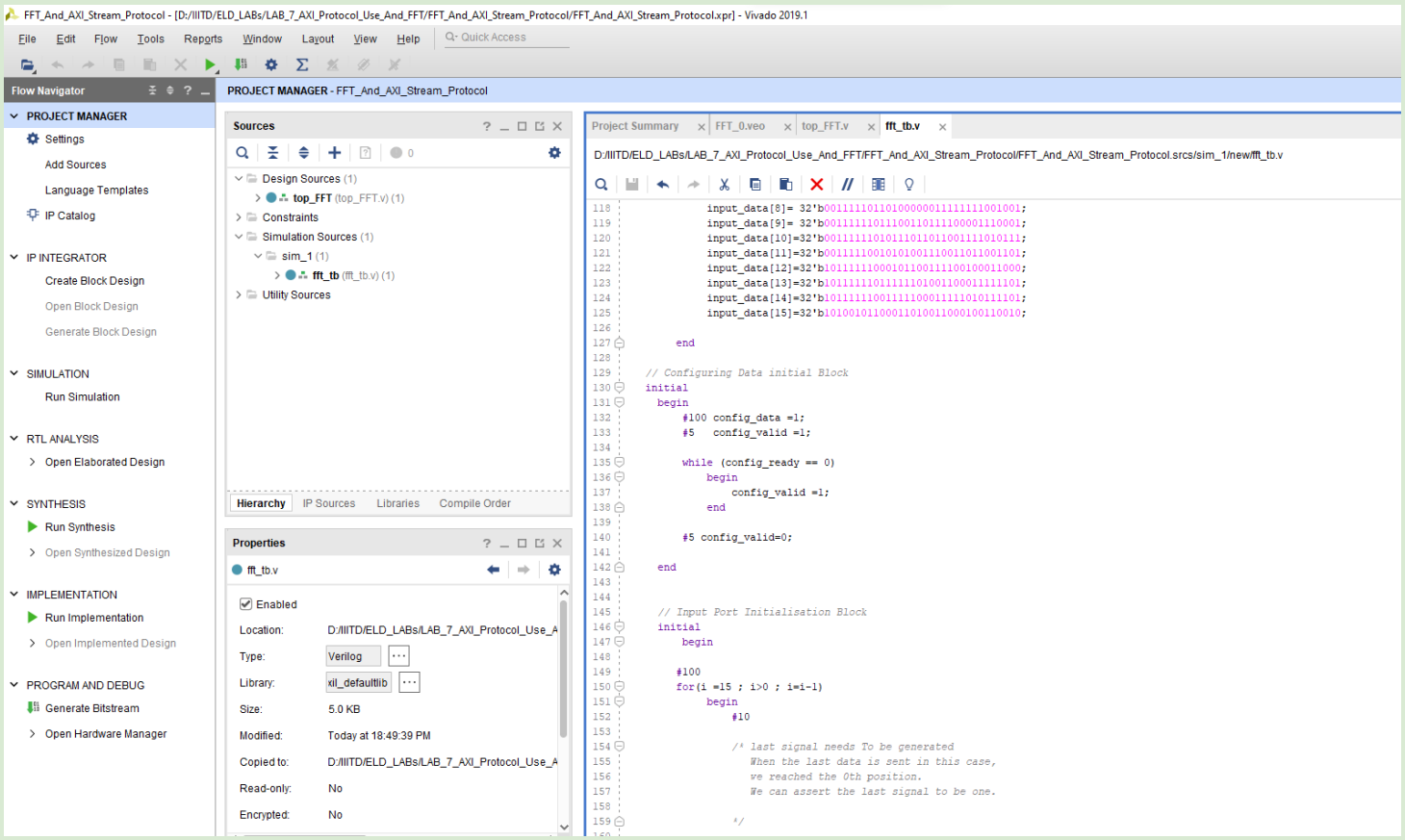
initial
begin
aclk=0;
aresetn=0;
in_valid =1'b0;
in_data= 32'd0 ;
in_last = 1'b0;
/* Initialising OUT_READY to 1 , inorder to tell FFT
that outputs can be generatd whenever ready
failure to do so leads to " Back-Pressure"
*/
out_ready = 1'b1;
config_data = 8'd0;
config_valid= 1'b0;
end
initial
begin
#70 // As Reset needs to be activated for atleast 2 cycles we have given 70 units of delay
aresetn = 1;
// input data entered using python
input_data[0]= 32'b00100101100011010011000100110010;
input_data[1]= 32'b00111111001111000111101011101;
input_data[2]= 32'b00111111011111101001100011111101;
input_data[3]= 32'b00111111000101100111100100011000;
input_data[4]= 32'b10111111001010011100110111001101;
input_data[5]= 32'b10111111010111011010011110101111;
input_data[6]= 32'b10111111011100110111100001110001;
input_data[7]= 32'b10111111011010000001111111001001;
input_data[8]= 32'b00111111011010000001111111001001;
input_data[9]= 32'b00111111011100110111100001110001;
input_data[10]=32'b00111111010111011010011110101111;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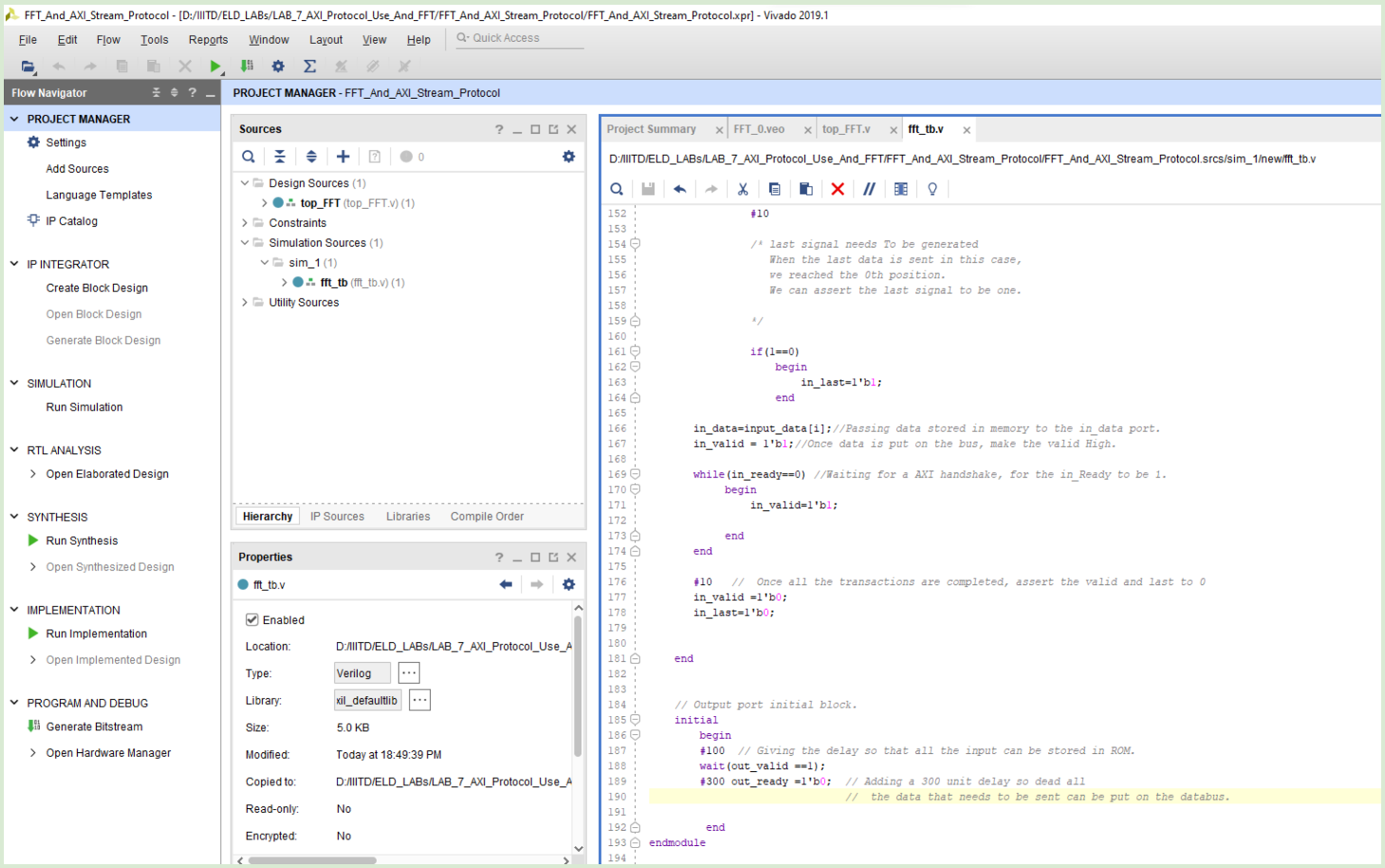
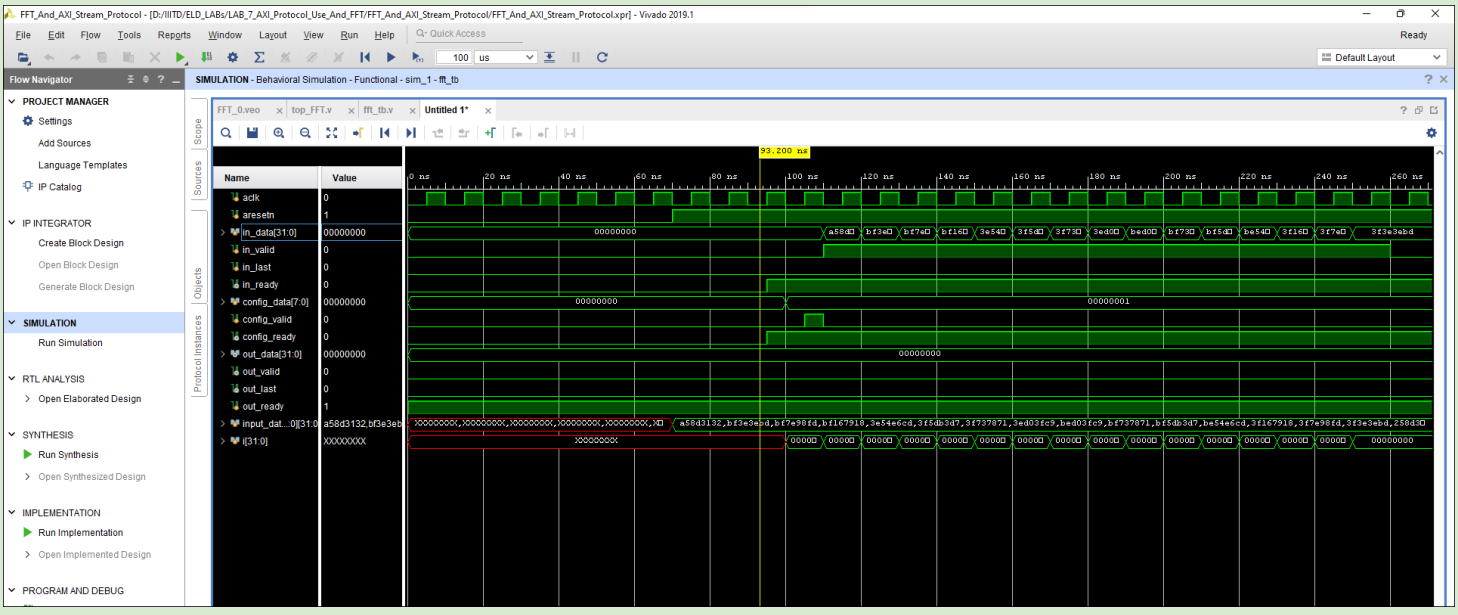
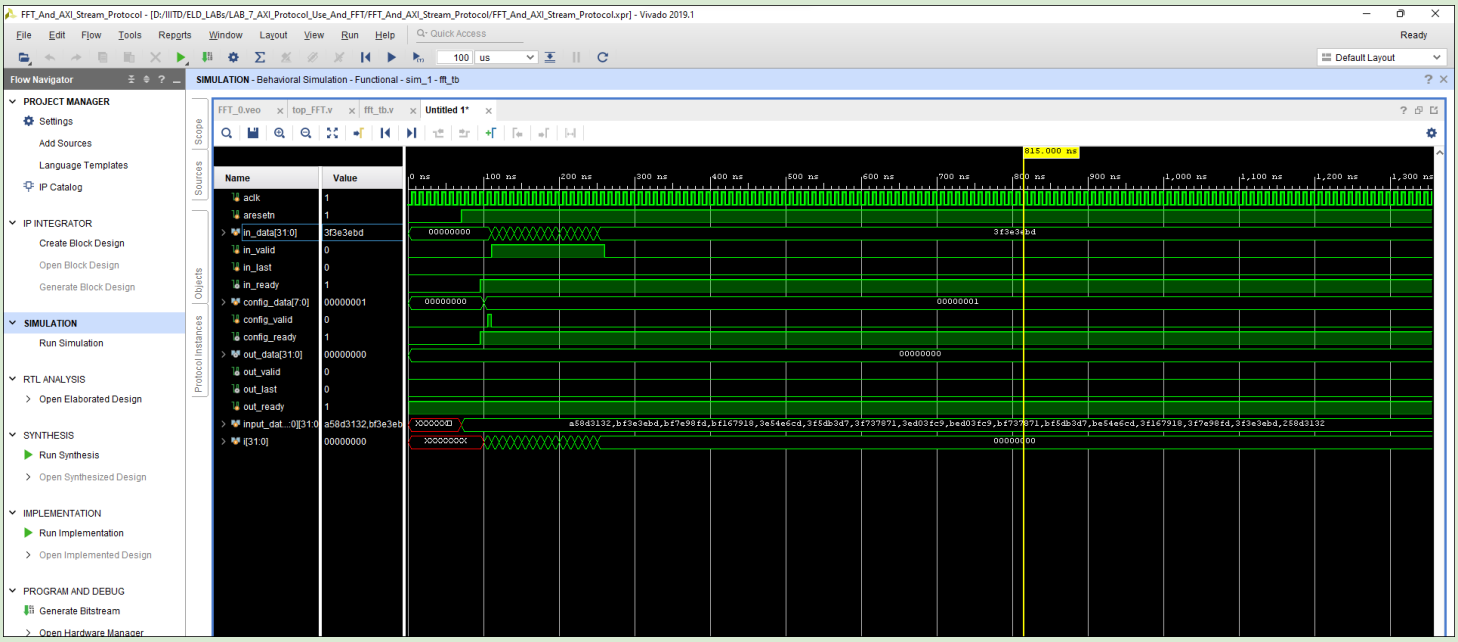
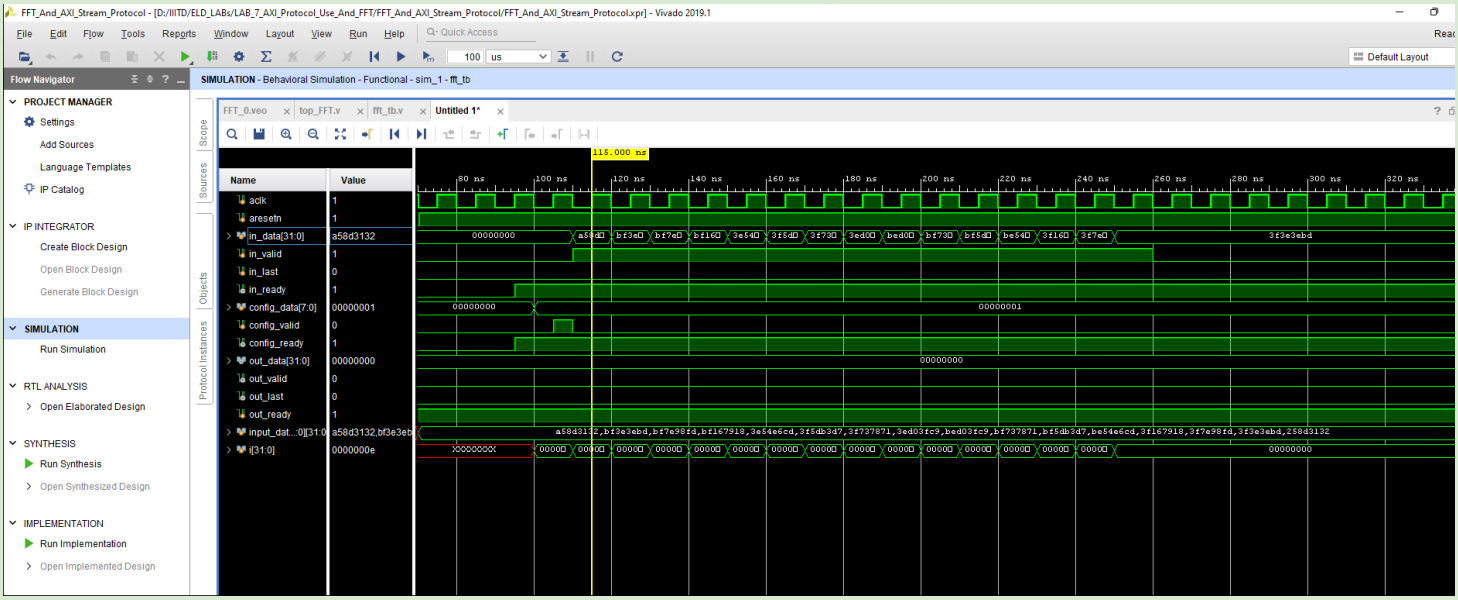
input_data[8]= 32'b00111111011010000001111111001001;
input_data[9]= 32'b00111111011100110111100001110001;
input_data[10]=32'b00111111010111011010011110101111;
input_data[11]=32'b00111111001010100111001101001101;
input_data[12]=32'b10111111000101100111001000011000;
input_data[13]=32'b10111111011111101001100011111101;
input_data[14]=32'b10111111001111000111101011101;
input_data[15]=32'b10100101100011010011000100110010;
end
// Configuring Data initial Block
initial
begin
#100 config_data =1;
#5 config_valid =1;
while (config_ready == 0)
begin
config_valid =1;
end
#5 config_valid=0;
end
// Input Port Initialisation Block
initial
begin
#100
for(i =15 ; i>0 ; i=i-1)
begin
#10
/* last signal needs To be generated
When the last data is sent in this case,
we reached the 0th position.
We can assert the last signal to be one.
*/



Results for automated testbench of FFT :







Conclusion:

Successfully designed and implemented FFT IP and its Testbench.