INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

Department
of
Electronics & Communication Engineering

Embedded Logic Design(ECE270)

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Lab_11

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OBJECTIVE:

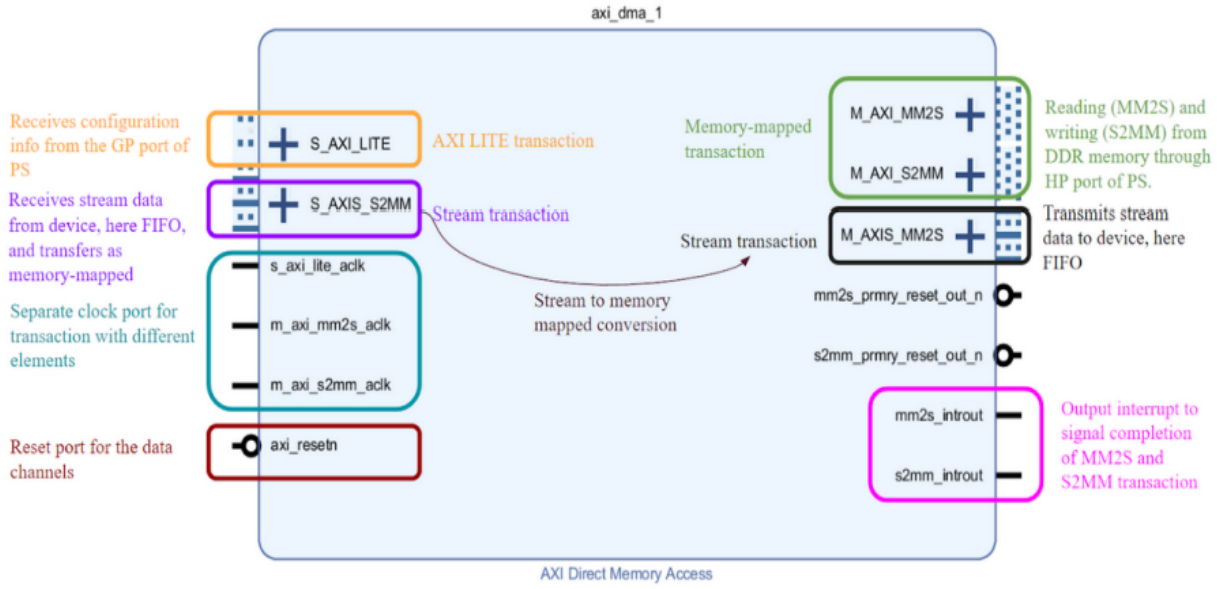
In this lab, we will be using FFT IP to perform the 8 points FFT. To perform data transfers between PS and PL, we will be using AXI DMA. First, some data will be stored in the DDR memory of the float complex data type. This data will be accessed by the DMA via the HP port of the Zynq Processing system. The DMA will then write this data to the FFT IP in the PL part. Then the DMA will read this data from the FFT, and write it back to the DDR memory again.

Theory:

Note: Float complex data type concatenates the real and imaginary part together with the upper 32 bits being imaginary and the lower 32 bits being real part of the complex number.

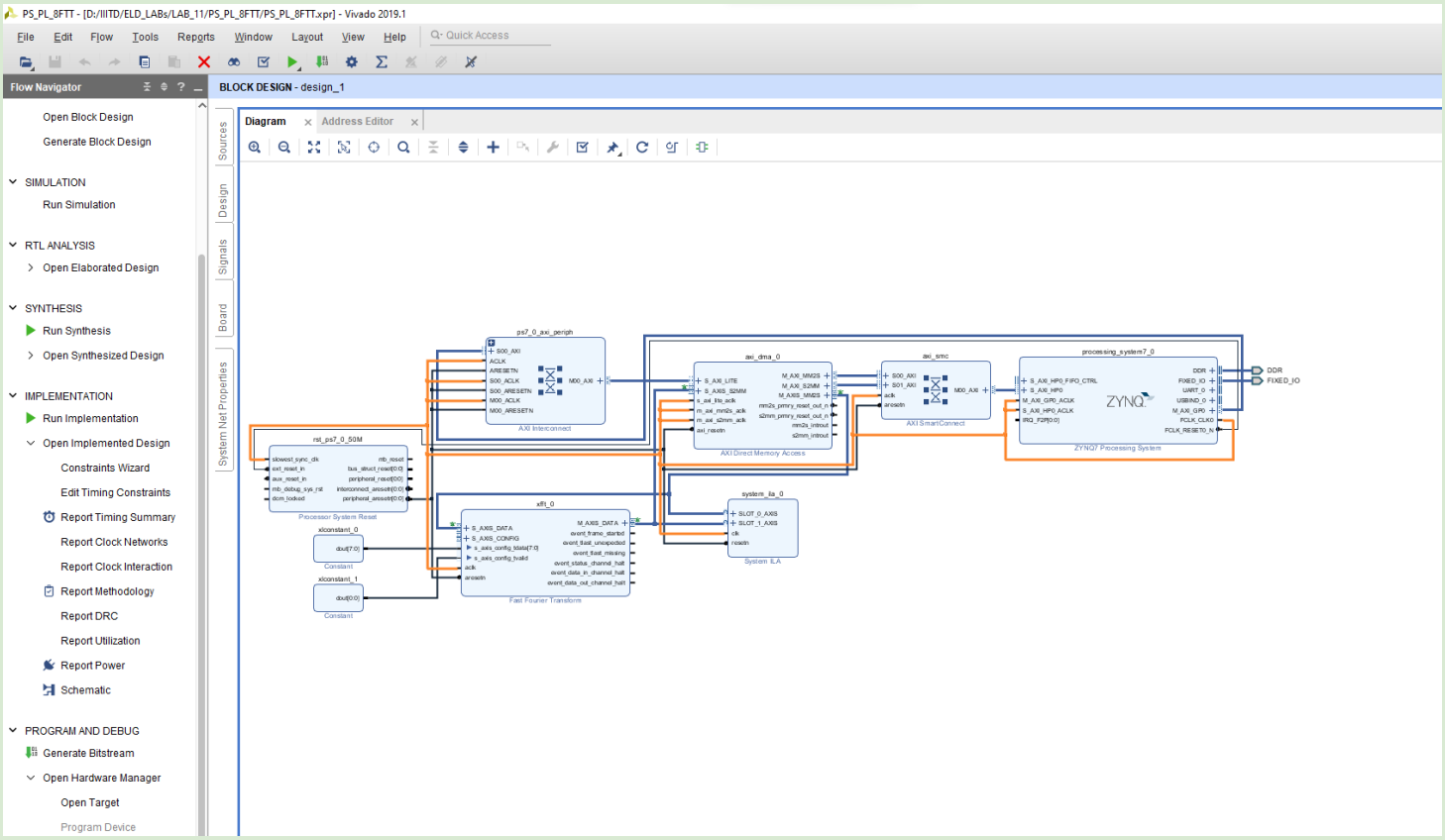
We will also perform the 8 Point FFT in PS using a testbench and then we will compare the software and hardware results.

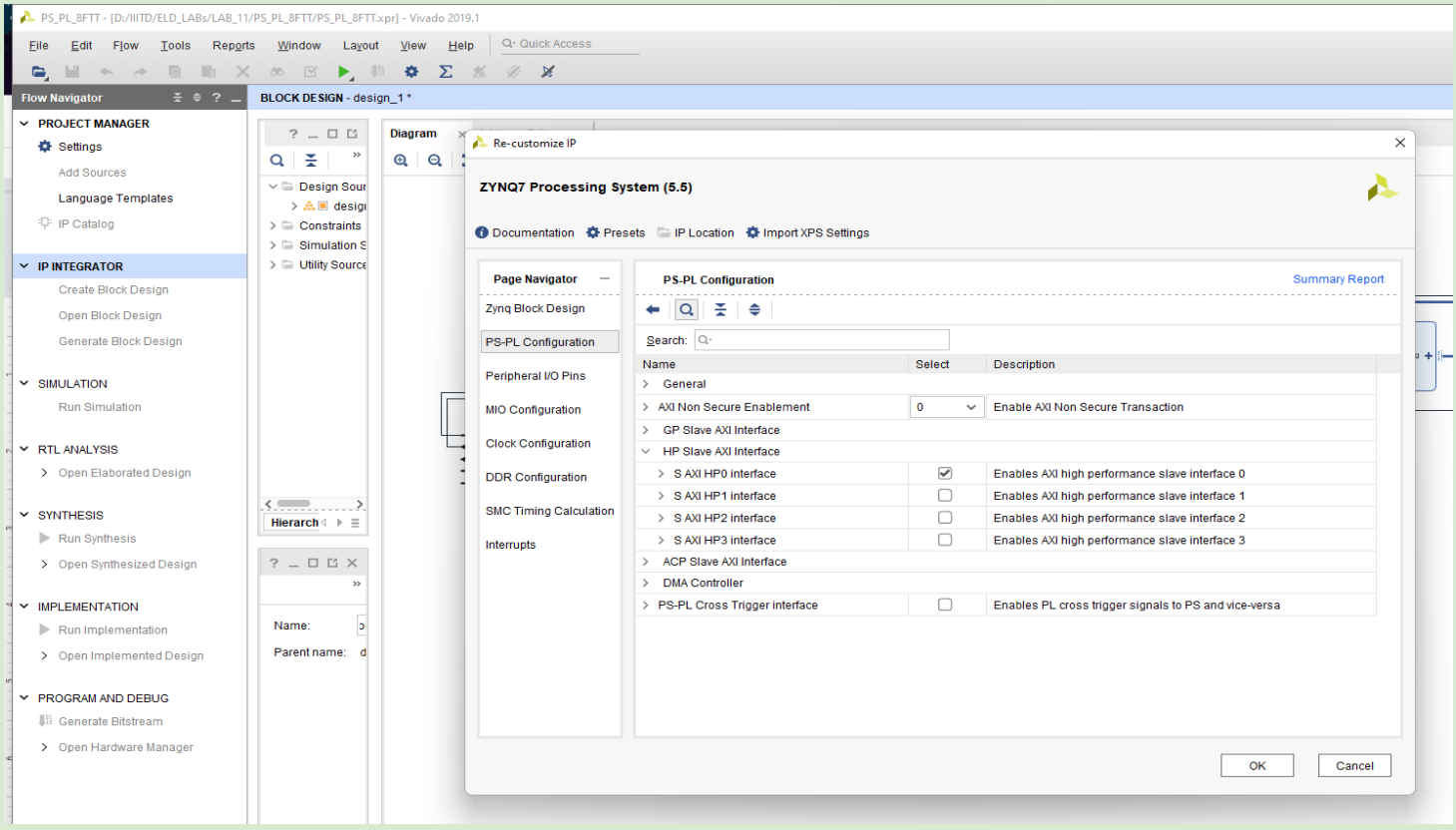
Before starting with the implementation, let's revise the various ports of DMA IP



Observations:

ZYNQ_processing_System_Block_Design :



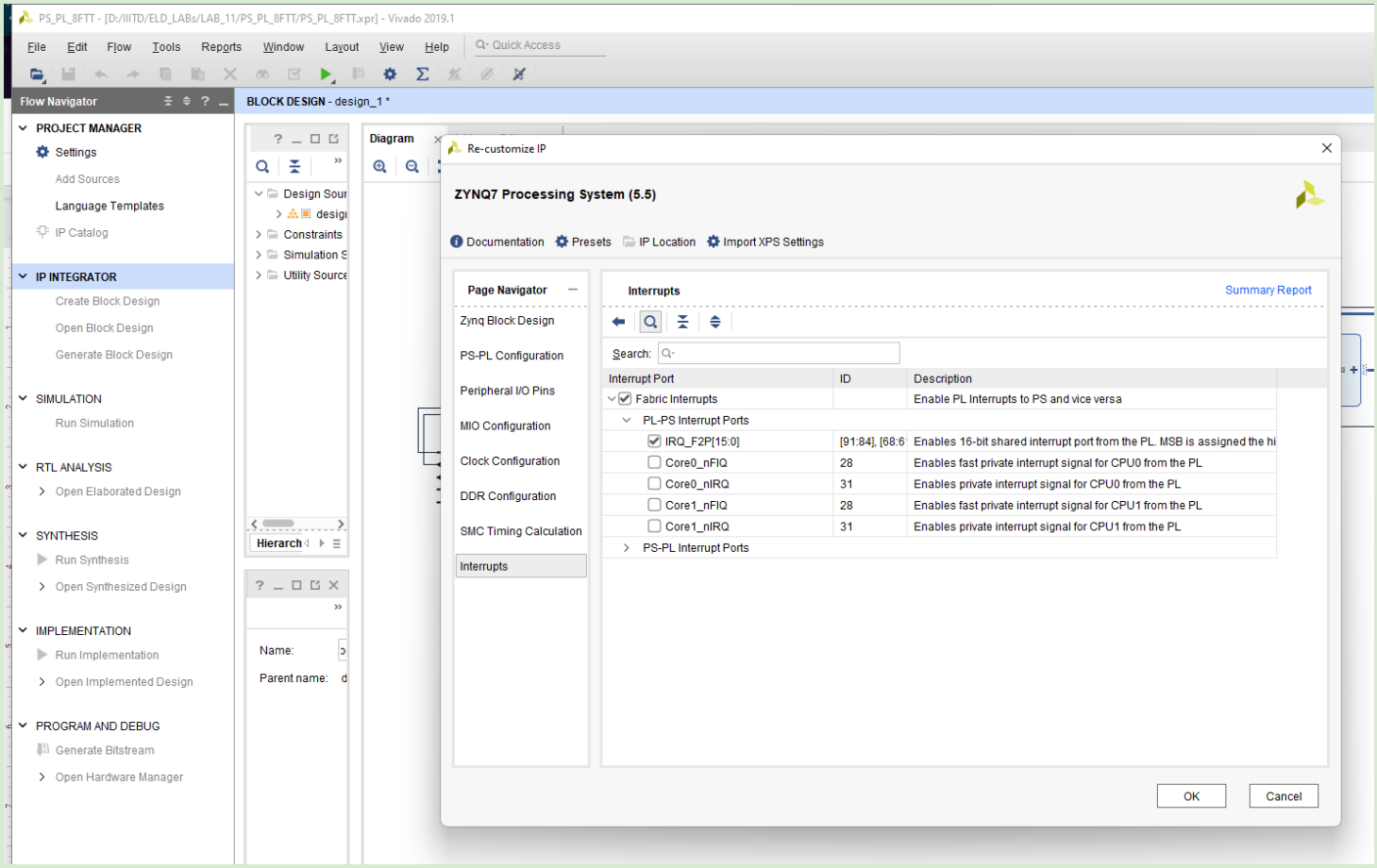


Open the customization window by double-clicking on the IP and make the following changes.

a. *In the PS-PL section, expand HP Slave AXI Interface and check the S AXI HP Interface to add a slave HP port to the Zynq IP. This port will be used by the DMA to access the DDR memory.*

b. *In the Interrupts section, expand the Fabric Interrupts, further expand the PL-PS Interrupt Ports, and check the IRQ_F2P[15:0]. This will add an interrupt port to the Zynq IP which will receive the interrupt signals from the DMA to indicate completion of the data transfers (only required if we want interrupt mode).*

c. *Click on Ok.*



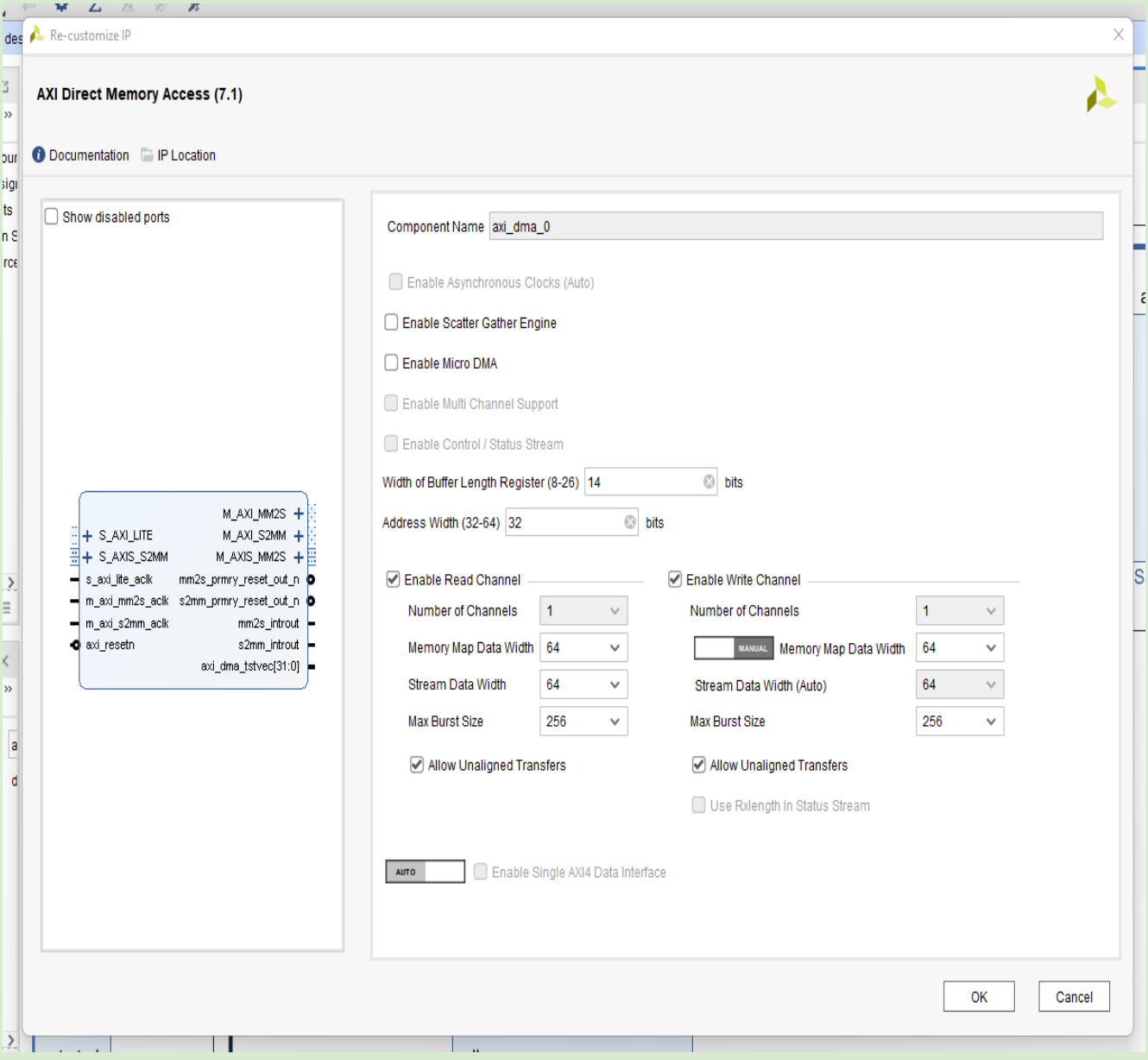
Now add AXI Direct Memory Access IP, and add it to the design.Open its configuration window and make the following changes

a. Deselect the "Enable Scatter/Gather mode"

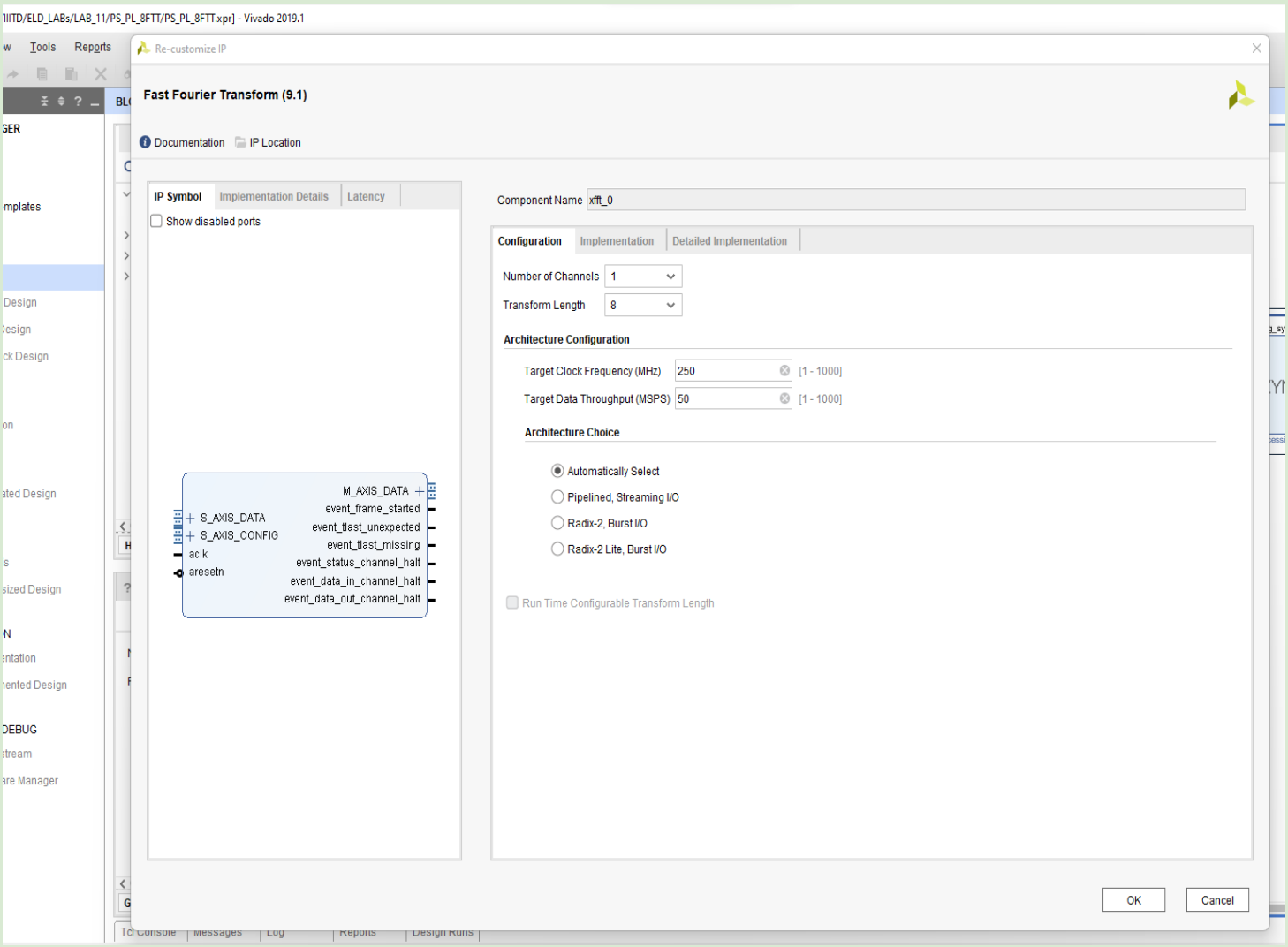
b. Increase the maximum burst size to 256

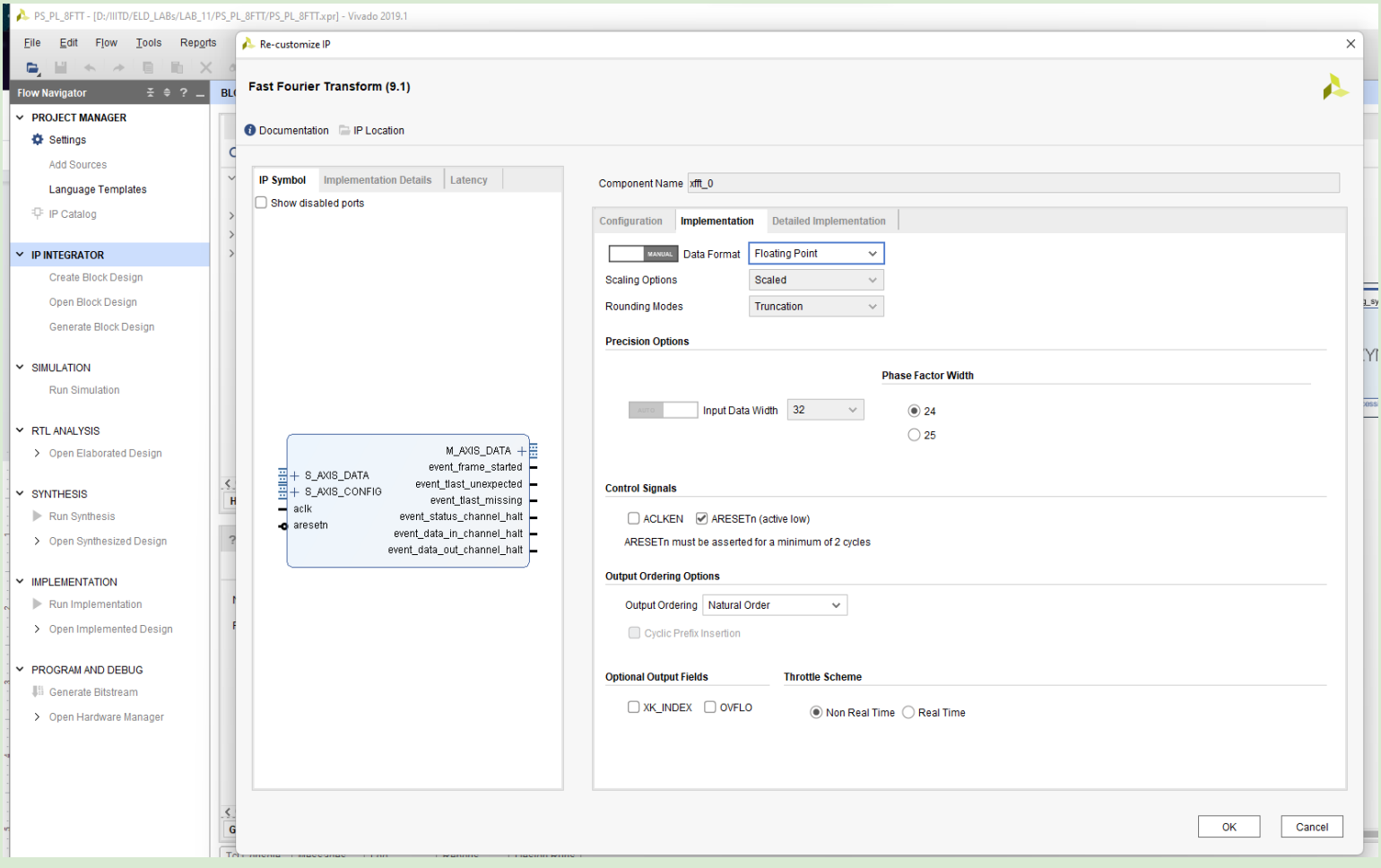
c. Increase the Memory Map data width and stream data width to 64

i. This is because now we are sending complex values which are of 64 bits (32 bits imaginary and 32 bits real concatenated)



Now add the Fast Fourier Transform IP and open its configuration window and Change the transform length to 8 since we are performing 8-point FFT


IIITD/ELD_LABs/LAB_11/PS_PL_8FTT/PS_PL_8FTT.xpr] - Vivado 2019.1
Tools
Reports
Re-customize IP
Fast Fourier Transform (9.1)
Documentation
IP Location
IP Symbol
Implementation Details
Latency
Show disabled ports
S_AXIS_DATA
S_AXIS_CONFIG
aclk
aresetn
M_AXIS_DATA
event_frame_started
event_tlast_unexpected
event_tlast_missing
event_status_channel_halt
event_data_in_channel_halt
event_data_out_channel_halt
Component Name
xfft_0
Configuration
Implementation
Detailed Implementation
Number of Channels
1
Transform Length
8
Architecture Configuration
Target Clock Frequency (MHz)
250
[1 - 1000]
Target Data Throughput (MSPS)
50
[1 - 1000]
Architecture Choice
Automatically Select
Pipelined, Streaming I/O
Radix-2, Burst I/O
Radix-2 Lite, Burst I/O
Run Time Configurable Transform Length
OK
Cancel


PS_PL_8FTT - [D:/IIITD/ELD_LABs/LAB_11/PS_PL_8FTT/PS_PL_8FTT.xpr] - Vivado 2019.1
File
Edit
Flow
Tools
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Flow Navigator
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Settings
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Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
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Run Simulation
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Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Fast Fourier Transform (9.1)
Documentation
IP Location
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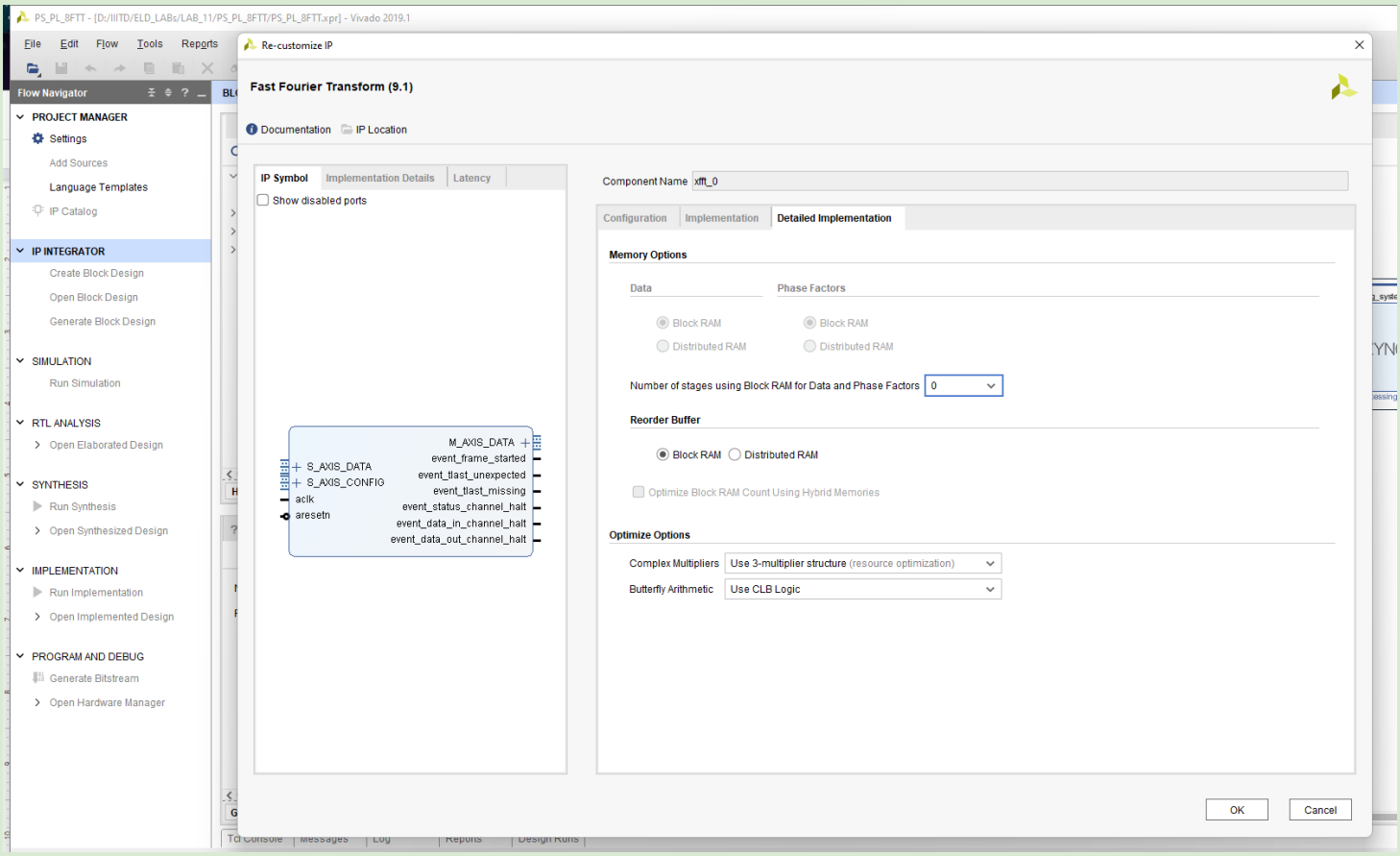
Implementation Details
Latency
Show disabled ports
S_AXIS_DATA
S_AXIS_CONFIG
aclk
aresetn
M_AXIS_DATA
event_frame_started
event_tlast_unexpected
event_tlast_missing
event_status_channel_halt
event_data_in_channel_halt
event_data_out_channel_halt
Component Name
xfft_0
Configuration
Implementation
Detailed Implementation
Data Format
Floating Point
Scaling Options
Scaled
Rounding Modes
Truncation
Precision Options
Phase Factor Width
Input Data Width
32
24
25
Control Signals
ACLKEN
ARESETn (active low)
ARESETn must be asserted for a minimum of 2 cycles
Output Ordering Options
Output Ordering
Natural Order
Cyclic Prefix Insertion
Optional Output Fields
XK_INDEX
OVFLO
Throttle Scheme
Non Real Time
Real Time
OK
Cancel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File Edit Flow Tools Reports
Re-customize IP
Fast Fourier Transform (9.1)
Documentation
IP Location
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Latency
Show disabled ports
S_AXIS_DATA
S_AXIS_CONFIG
aclk
aresetn
M_AXIS_DATA
event_frame_started
event_tlast_unexpected
event_tlast_missing
event_status_channel_halt
event_data_in_channel_halt
event_data_out_channel_halt
Component Name
xfft_0
Configuration
Implementation
Detailed Implementation
Memory Options
Data
Phase Factors
Block RAM
Distributed RAM
Number of stages using Block RAM for Data and Phase Factors
0
Reorder Buffer
Optimize Block RAM Count Using Hybrid Memories
Optimize Options
Complex Multipliers
Use 3-multiplier structure (resource optimization)
Butterfly Arithmetic
Use CLB Logic
OK
Cancel
Flow Navigator
PROJECT MANAGER
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Create Block Design
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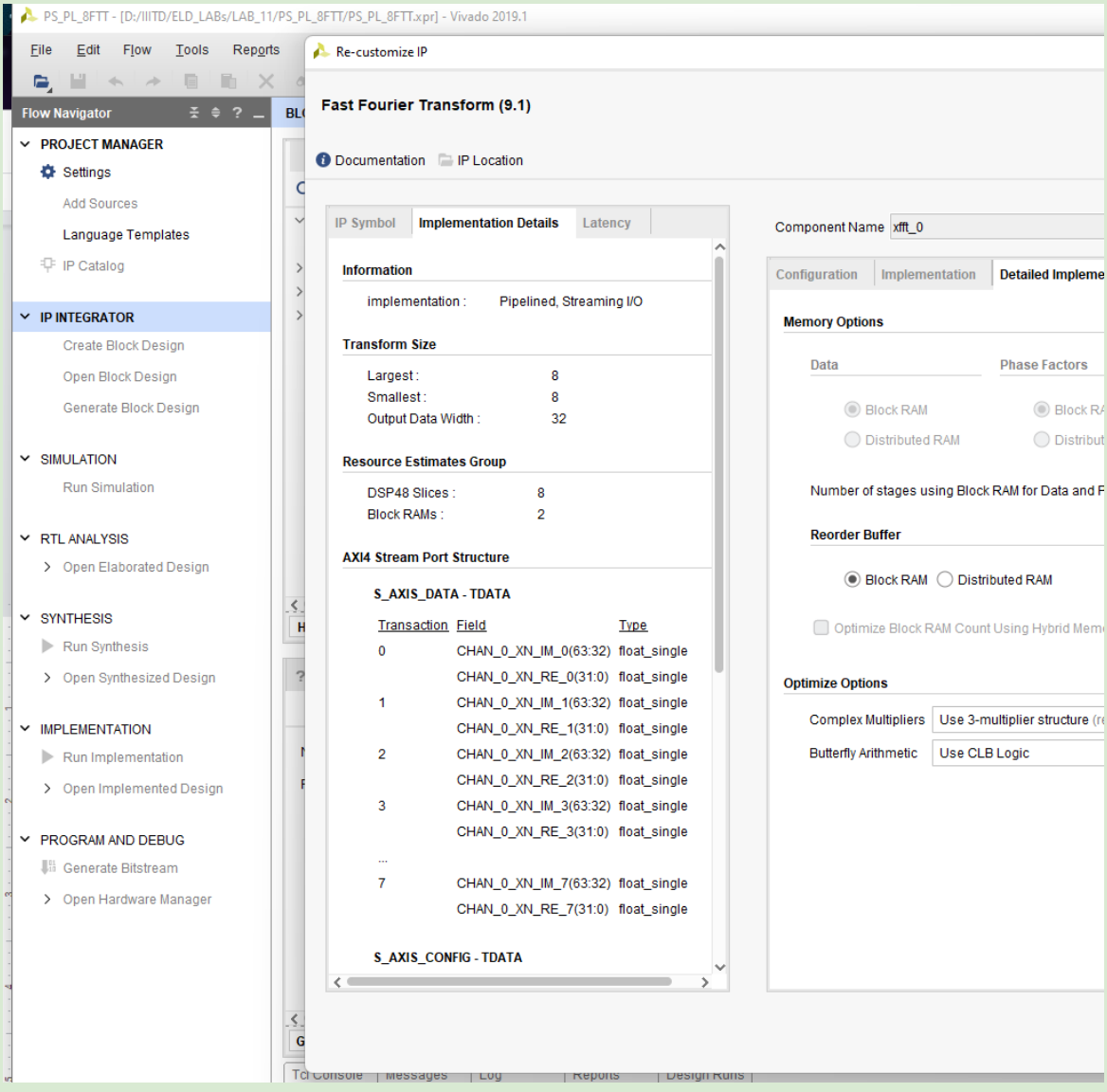
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager


PS_PL_8FTT - [D:/IIITD/ELD_LABs/LAB_11/PS_PL_8FTT/PS_PL_8FTT.xpr] - Vivado 2019.1
File Edit Flow Tools Reports
Re-customize IP
Fast Fourier Transform (9.1)
Documentation
IP Location
IP Symbol
Implementation Details
Latency
Information
implementation : Pipelined, Streaming I/O
Transform Size
Largest : 8
Smallest : 8
Output Data Width : 32
Resource Estimates Group
DSP48 Slices : 8
Block RAMs : 2
AXI4 Stream Port Structure
S_AXIS_DATA - TDATA
Transaction Field Type
0 CHAN_0_XN_IM_0(63:32) float_single
CHAN_0_XN_RE_0(31:0) float_single
1 CHAN_0_XN_IM_1(63:32) float_single
CHAN_0_XN_RE_1(31:0) float_single
2 CHAN_0_XN_IM_2(63:32) float_single
CHAN_0_XN_RE_2(31:0) float_single
3 CHAN_0_XN_IM_3(63:32) float_single
CHAN_0_XN_RE_3(31:0) float_single
...
7 CHAN_0_XN_IM_7(63:32) float_single
CHAN_0_XN_RE_7(31:0) float_single
S_AXIS_CONFIG - TDATA
Component Name
xfft_0
Configuration
Implementation
Memory Options
Data
Phase Factors
Reorder Buffer
Optimize Options
Complex Multipliers
Butterfly Arithmetic
Use CLB Logic
Flow Navigator
PROJECT MANAGER
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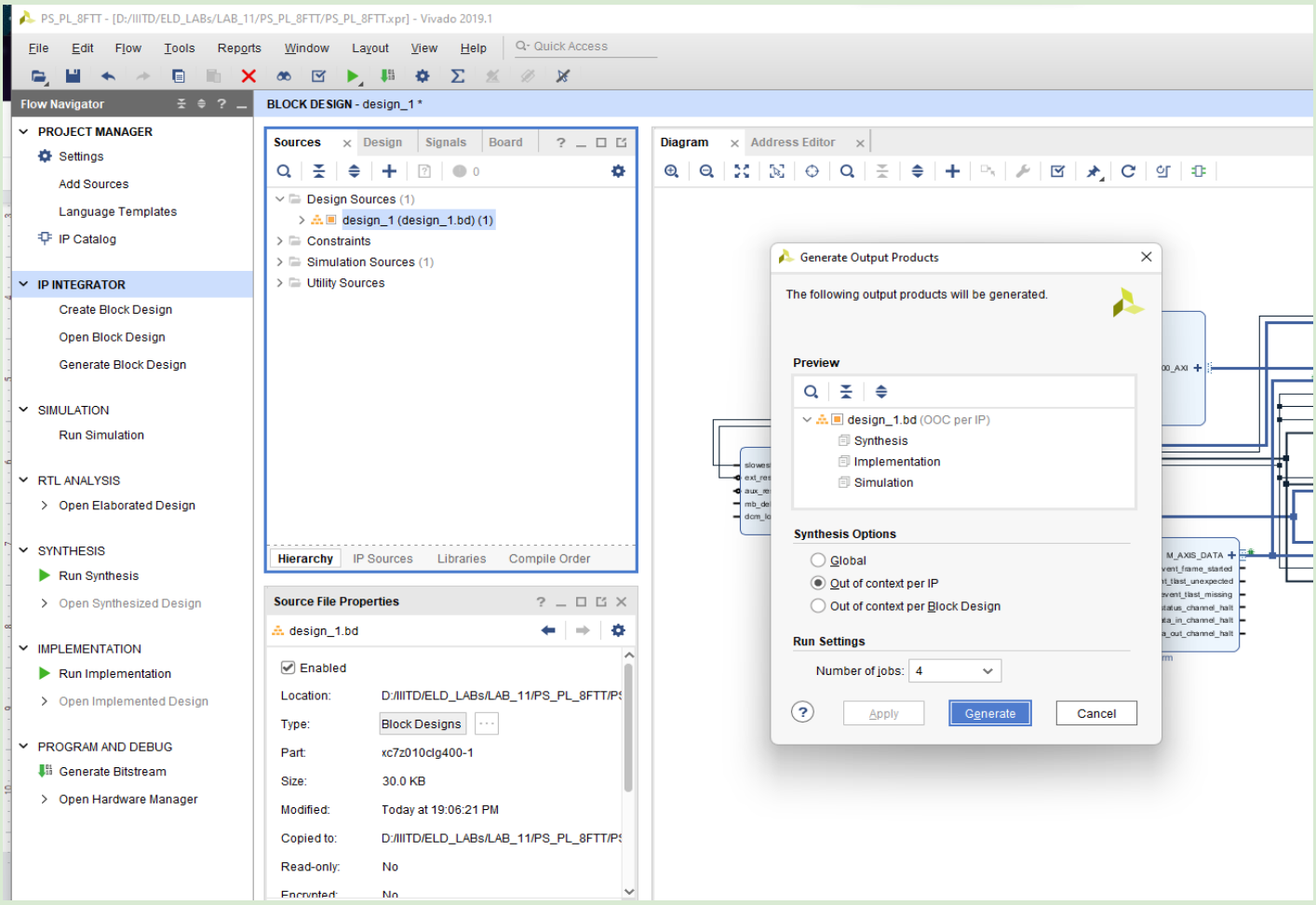
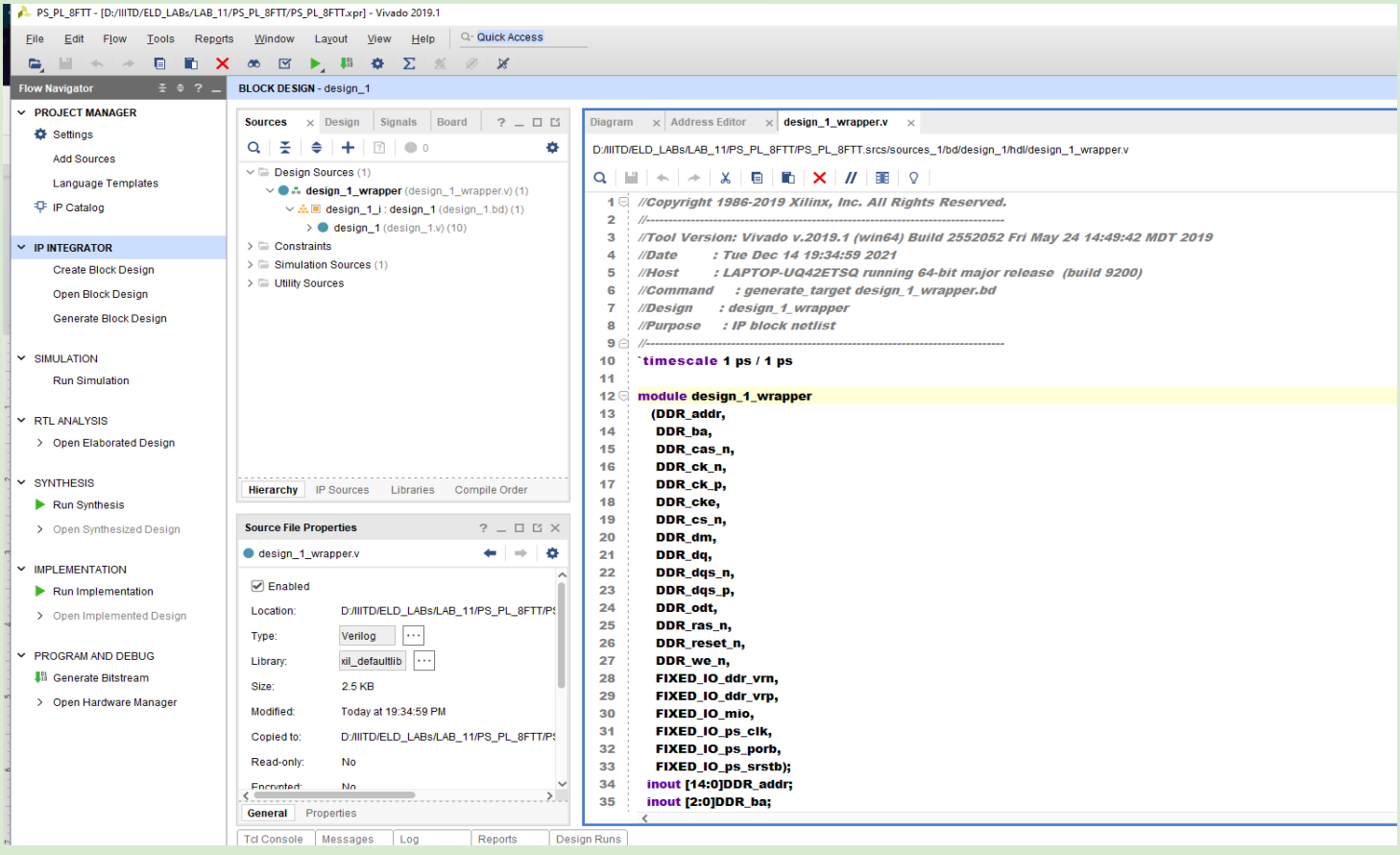
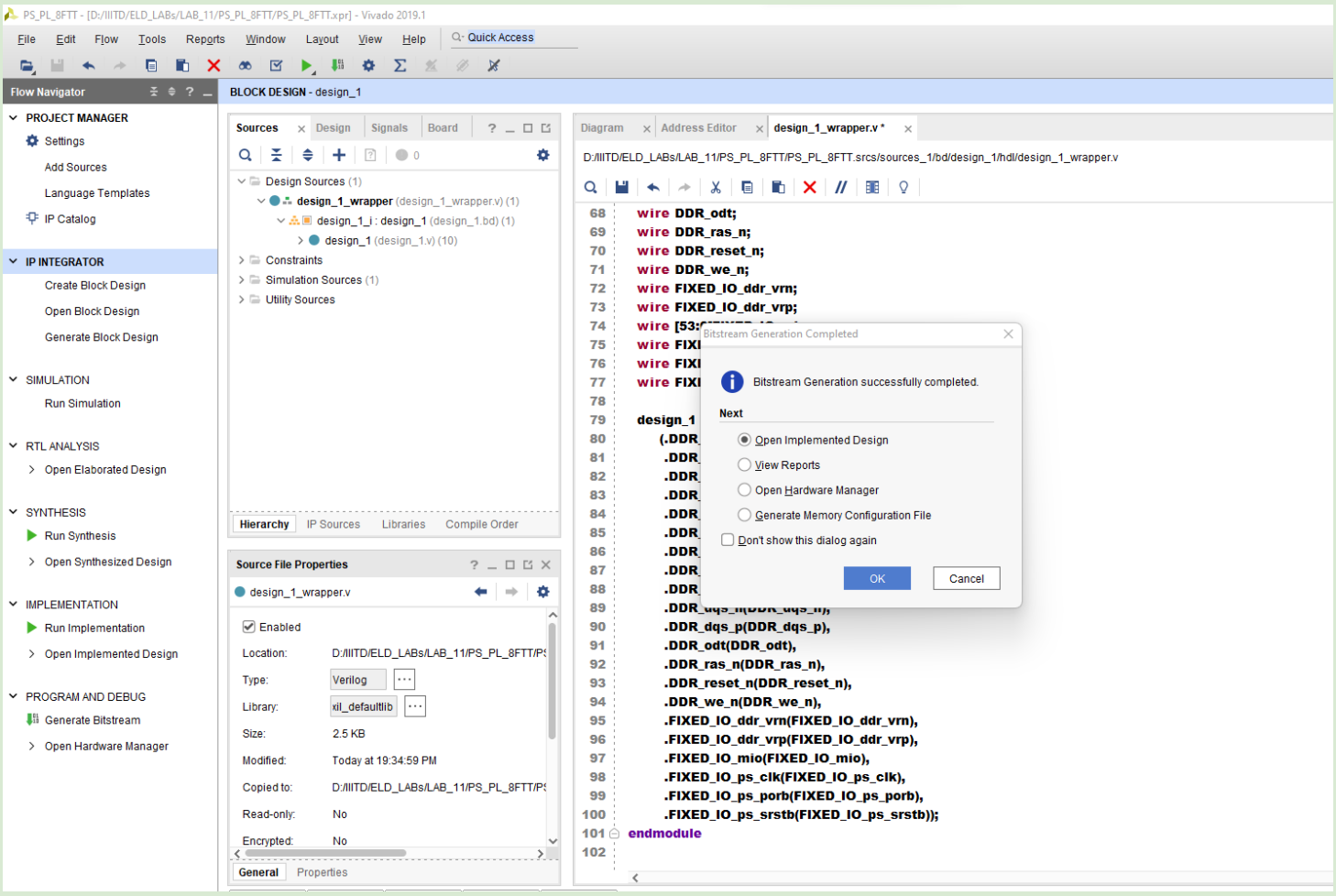
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager

Validate the design, generate output product, and create HDL wrapper. DO NOT ever miss these steps.



Auto_Generated_HDL_Wrapper




PS_PL_8FTT - [D:/IIITD/ELD_LABs/LAB_11/PS_PL_8FTT/PS_PL_8FTT.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Flow Navigator
PROJECT MANAGER
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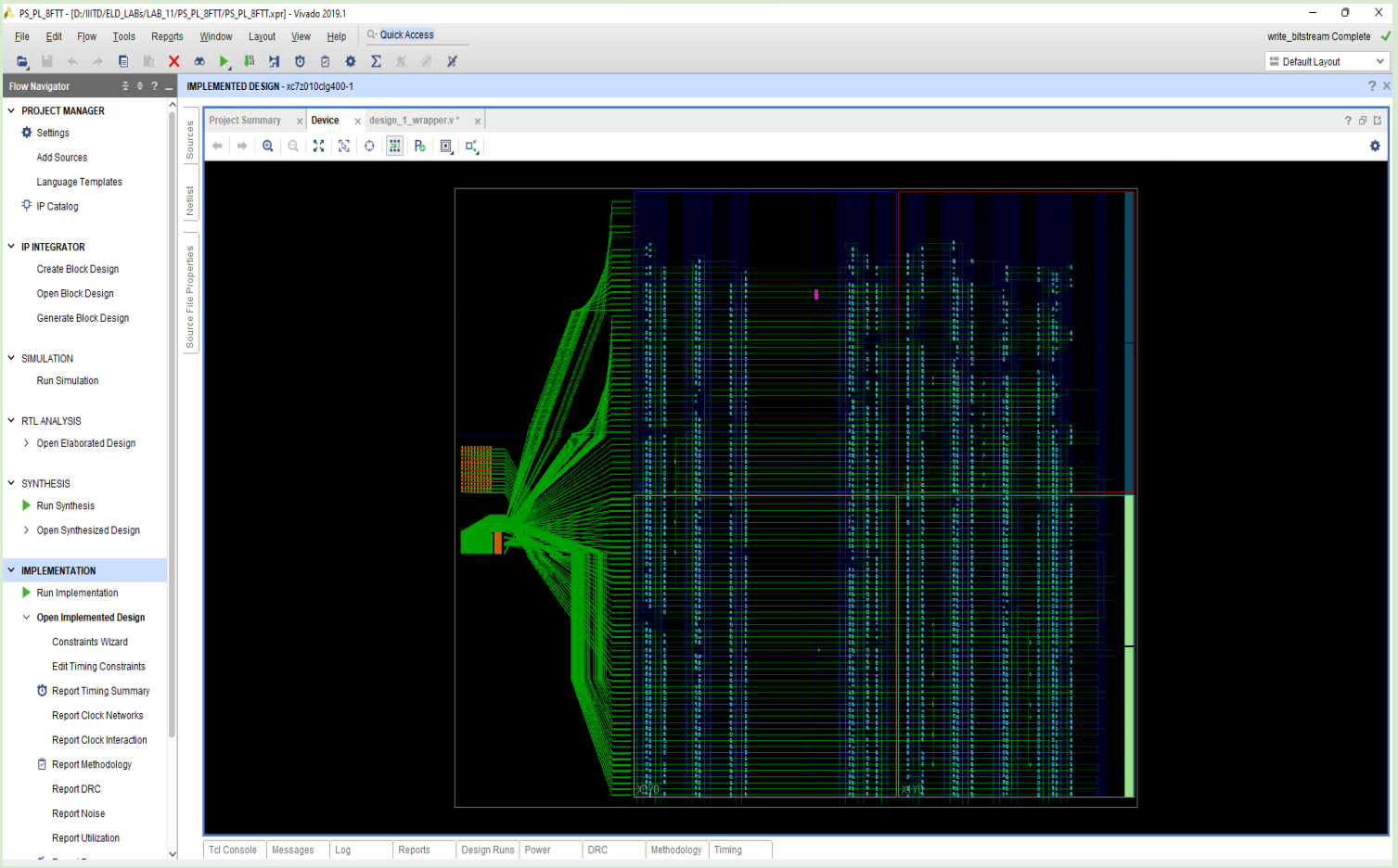
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - design_1
Sources
Design
Signals
Board
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
design_1_i : design_1 (design_1.bd) (1)
design_1 (design_1.v) (10)
Constraints
Simulation Sources (1)
Utility Sources
Hierarchy
IP Sources
Libraries
Compile Order
Source File Properties
design_1_wrapper.v
Enabled
Location: D:/IIITD/ELD_LABs/LAB_11/PS_PL_8FTT/PS
Type: Verilog
Library: xil_defaultlib
Size: 2.5 KB
Modified: Today at 19:34:59 PM
Copied to: D:/IIITD/ELD_LABs/LAB_11/PS_PL_8FTT/PS
Read-only: No
Encrypted: No
General
Properties
Diagram
Address Editor
design_1_wrapper.v *
D:/IIITD/ELD_LABs/LAB_11/PS_PL_8FTT/PS_PL_8FTT.srcs/sources_1/bd/design_1/hdl/design_1_wrapper.v
wire DDR_odt;
wire DDR_ras_n;
wire DDR_reset_n;
wire DDR_we_n;
wire FIXED_IO_ddr_vrn;
wire FIXED_IO_ddr_vrp;
design_1
.DDR_dqs_p(DDR_dqs_p),
.DDR_odt(DDR_odt),
.DDR_ras_n(DDR_ras_n),
.DDR_reset_n(DDR_reset_n),
.DDR_we_n(DDR_we_n),
.FIXED_IO_ddr_vrn(FIXED_IO_ddr_vrn),
.FIXED_IO_ddr_vrp(FIXED_IO_ddr_vrp),
.FIXED_IO_mio(FIXED_IO_mio),
.FIXED_IO_ps_clk(FIXED_IO_ps_clk),
.FIXED_IO_ps_porb(FIXED_IO_ps_porb),
.FIXED_IO_ps_srstb(FIXED_IO_ps_srstb));
endmodule
Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
Open Implemented Design
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel


PS_PL_8FTT - [D:/IIITD/ELD_LABs/LAB_11/PS_PL_8FTT/PS_PL_8FTT.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7z010clg400-1
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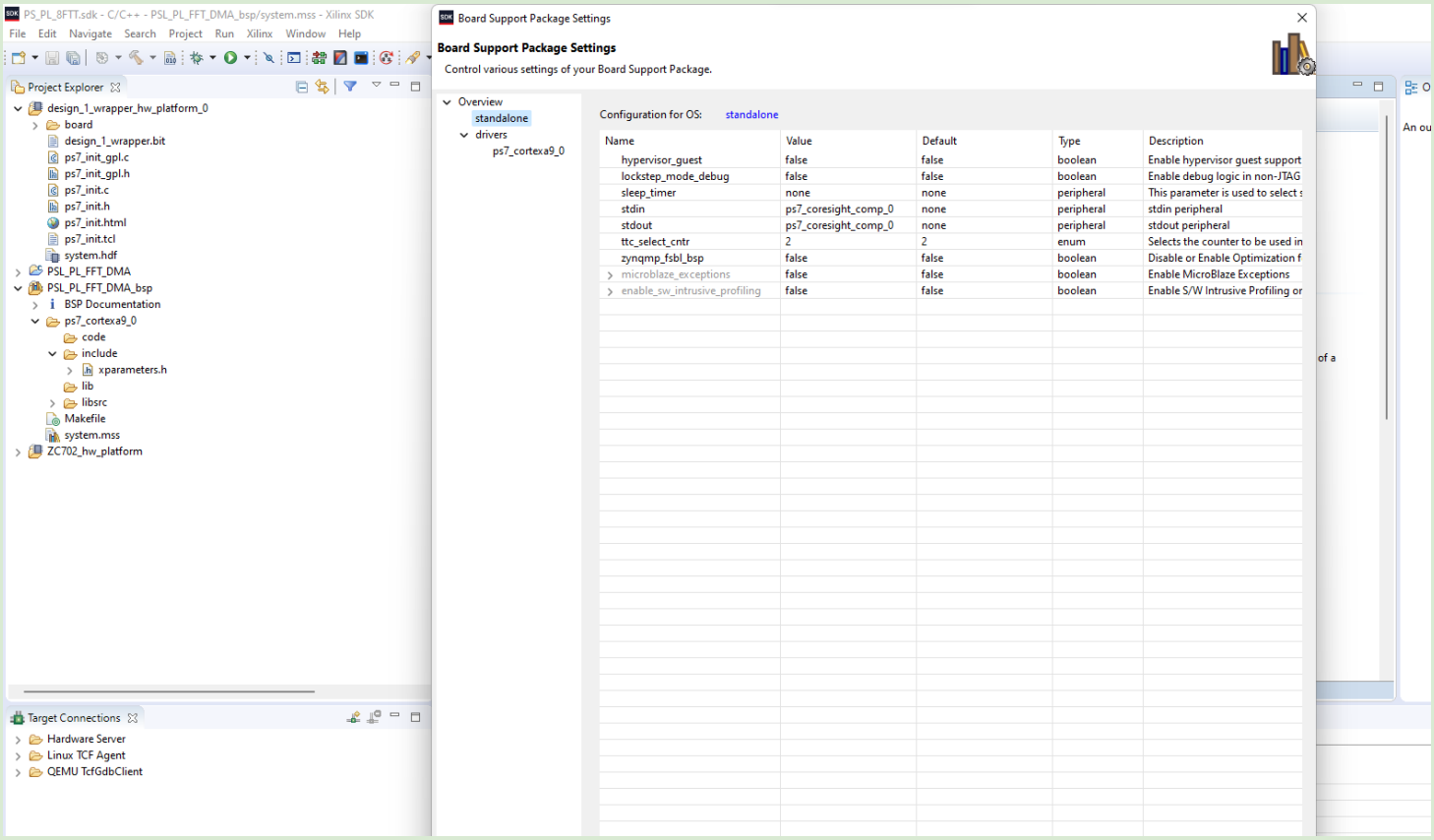
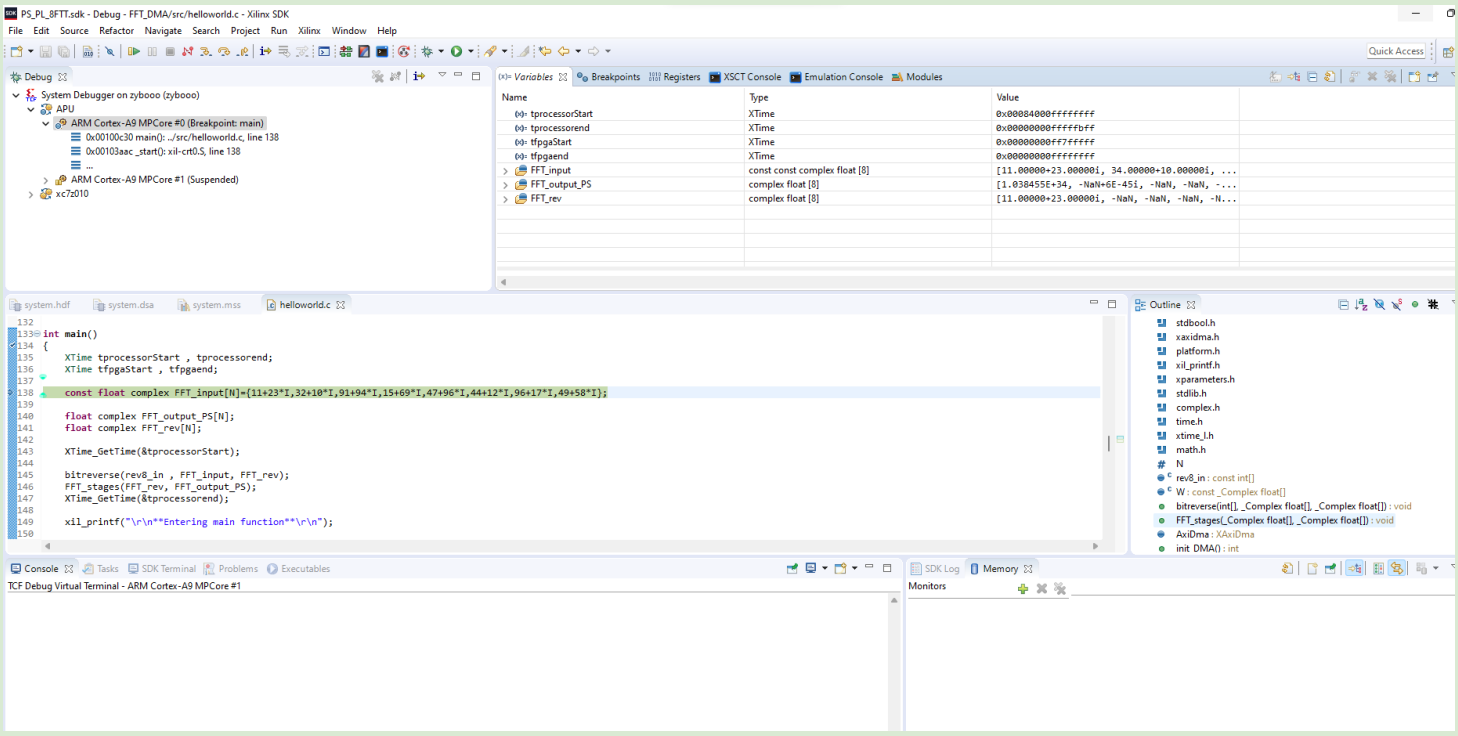
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Sources
Netlist
Source File Properties
Project Summary
Device
design_1_wrapper.v *
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing

Launching SDK and program in C and changing STDIN/OUT in BSP settings



running program in debug mode



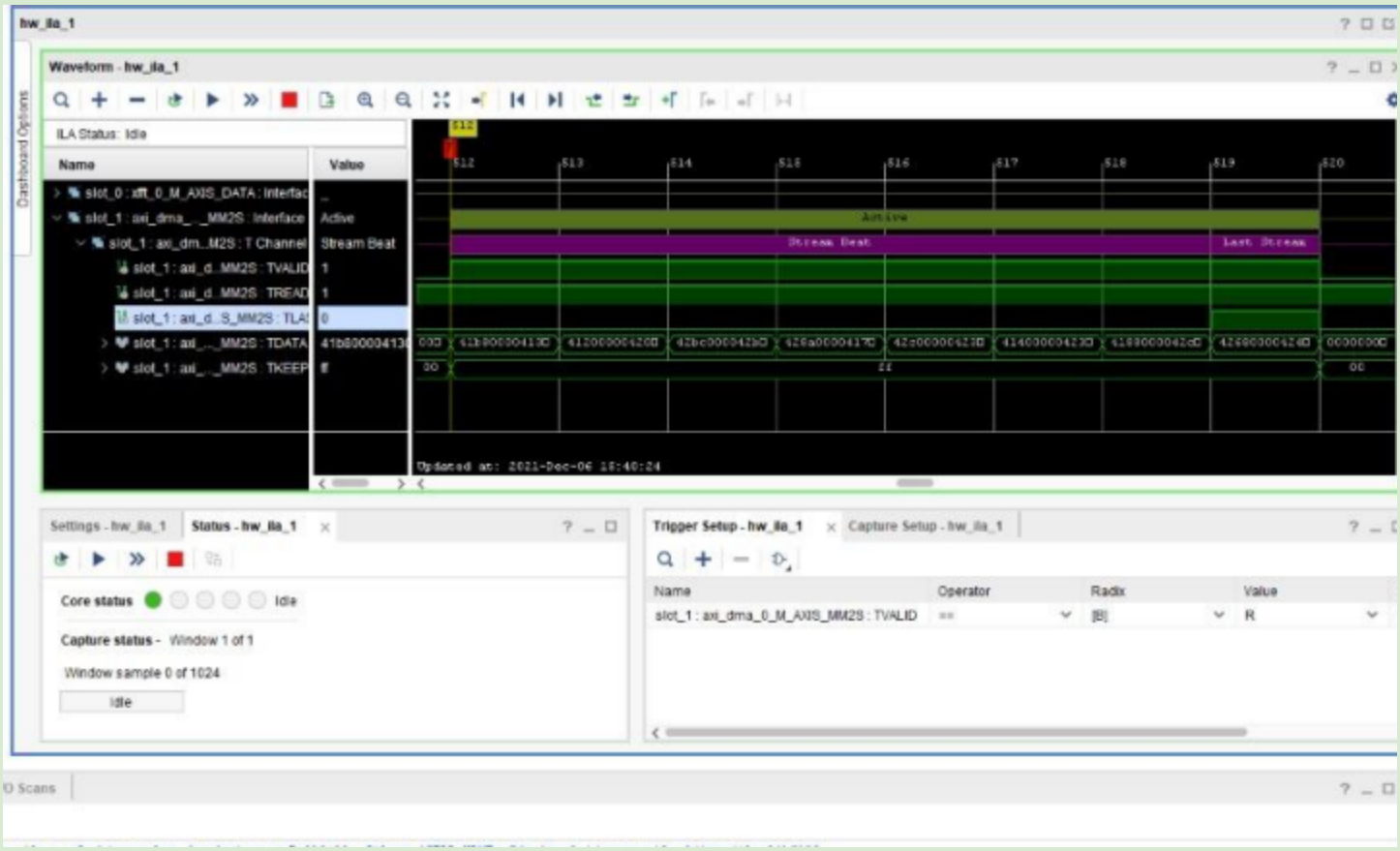
```
***Entering main function***

DMA status before transfer
DMA to Device: 0, Device to DMA:0

Starting Data Transfer---------->>>>>>>>>
DMA status between transfer
DMA to Device status: 0, Device to DMA status: 0
DMA status after transfer
DMA to Device status: 0, Device to DMA status: 0
DMA status after transfer
DMA to Device status: 2, Device to DMA status: 2

Comparing software FFT outputs and hardware FFT outputs via DMA
size of float complex : 8
PS Output : 385.000000 + I379.000000 , PL output : 385.000000 + I379.000000
 PS Output : 62.920311 + I-44.665474 , PL output : 62.920311 + I-44.665474
 PS Output : -234.000000 + I-4.000000 , PL output : -234.000000 + I-4.000000
 PS Output : -122.192383 + I-36.280701 , PL output : -122.192390 + I-36.280701
 PS Output : 105.000000 + I81.000000 , PL output : 105.000000 + I81.000000
 PS Output : 19.079691 + I-91.334526 , PL output : 19.079689 + I-91.334526
 PS Output : -24.000000 + I20.000000 , PL output : -24.000000 + I20.000000
 PS Output : -103.807617 + I-119.719299 , PL output : -103.807610 + I-119.719299

DMA ran successfully!! :)
-----------TIME COMPARISION--------------------
time for PS : 1517
time for PL : 2798330
```

Set the breakpoints properly and when we resume the program we will see the output.

Now to observe the AXI transactions, we will utilize the system ILA IP which was included when we added as debug.

- *Now go back to Vivado and open the hardware manager.*
- *Connect to the same Host IP as you did in SDK*
- *.Program the device*
- *Now, the waveform window will open up*
- *Add triggers for slot 1 and slot 2 for TVALID*

###Output-put ILA:



Conclusion:

Successfully created block design in Vivado and Compared the execution time for PS and PL.