INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

Department
of
Electronics & Communication Engineering

Embedded Logic Design(ECE270)

Dr. Sumit J Darak

Lab_9

Mohammad Shariq
2020220
29-11-2021

OBJECTIVE:

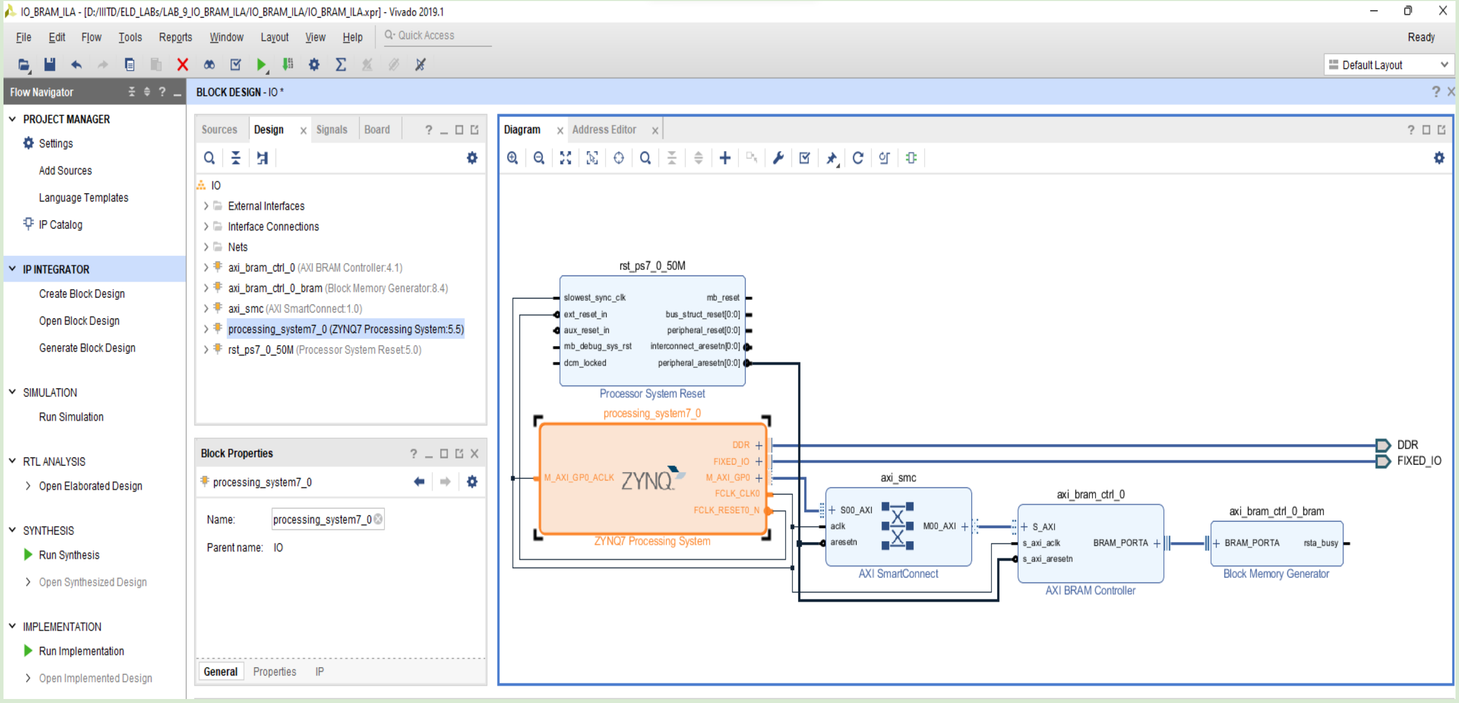
Tasks to be done in this Lab:

1) use the BRAM IP and create a ZYNQ block design to write and read data using BRAM through a driver code
2) Add ILA IP in the design to see the output waveforms and see the various handshakes taking pllace.

Observations:

### ZYNQ_processing_System_Block_Design :

for Part 1:



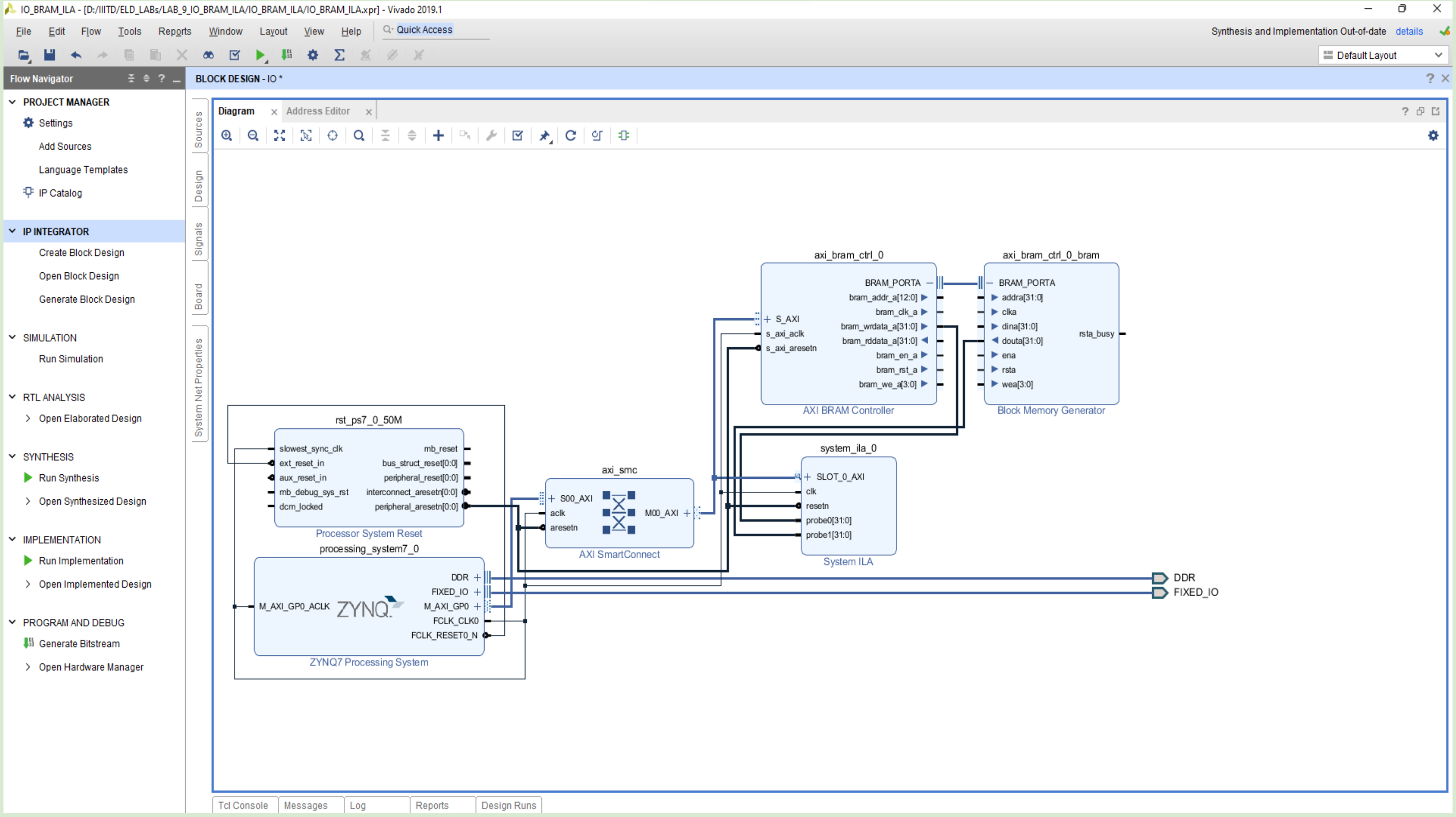
IO
- External Interfaces
- Interface Connections
- Nets
- axi_bram_ctrl_0 (AXI BRAM Controller:4.1)
- axi_bram_ctrl_0_bram (Block Memory Generator:8.4)
- axi_smc (AXI SmartConnect:1.0)
- processing_system7_0 (ZYNQ7 Processing System:5.5)
- rst_ps7_0_50M (Processor System Reset:5.0)

processing_system7_0

Name: processing_system7_0

Parent name: IO

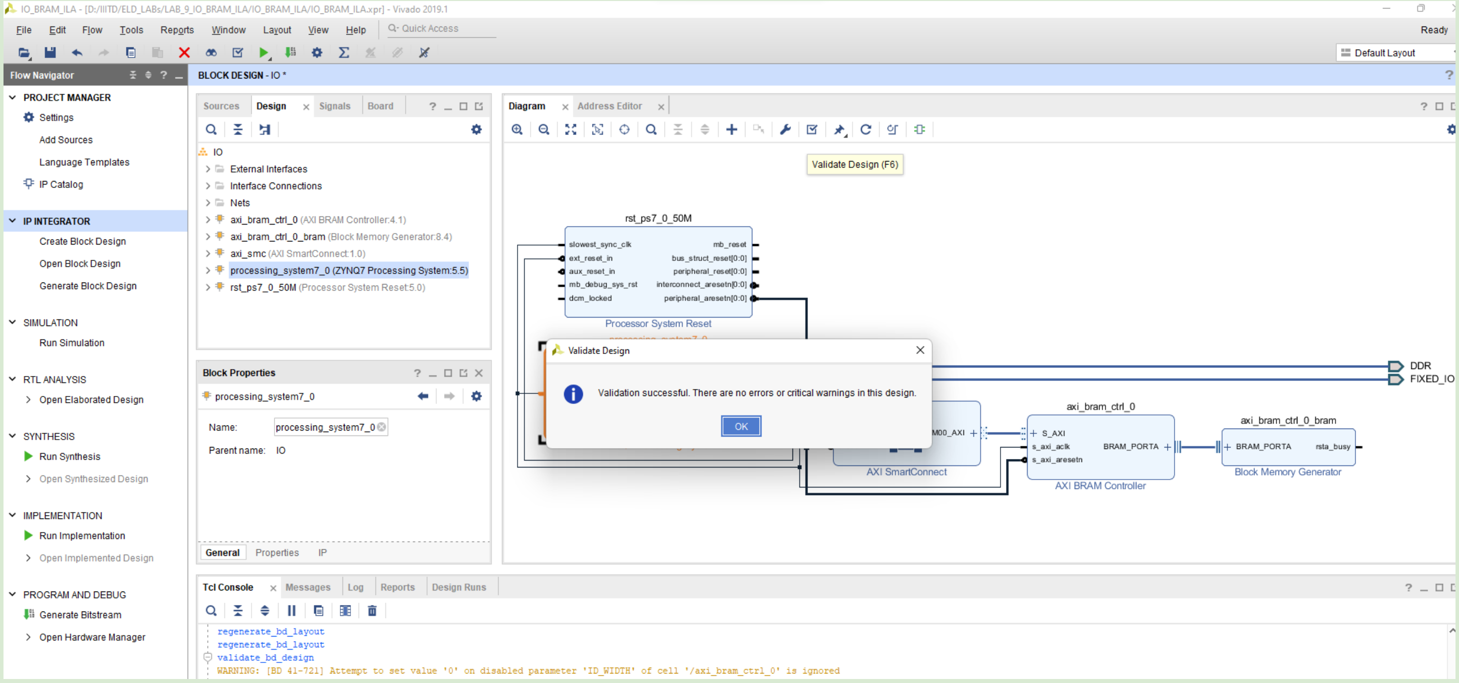
for part 2:


IO_BRAM_ILA - [D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.xpr] - Vivado 2019.1

Synthesis and Implementation Out-of-date details

BLOCK DESIGN - IO *

Validate the design, generate output product, and create HDL wrapper. DO NOT ever miss these steps.


IO_BRAM_ILA - [D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.xpr] - Vivado 2019.1

BLOCK DESIGN - IO *

Validate Design

Validation successful. There are no errors or critical warnings in this design.

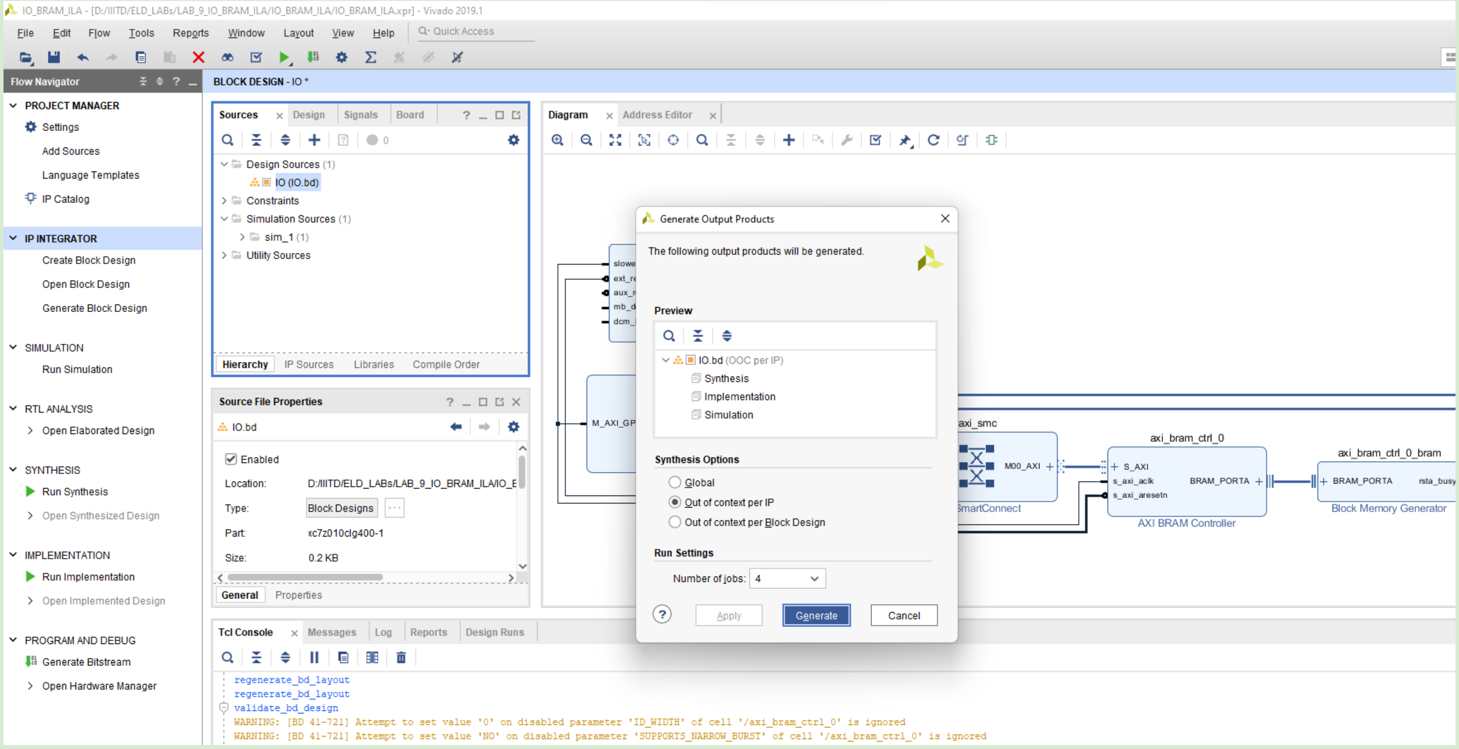
OK

Block Properties

Name: processing_system7_0

Parent name: IO

```
regenerate_bd_layout
regenerate_bd_layout
validate_bd_design
WARNING: [BD 41-721] Attempt to set value '0' on disabled parameter 'ID_WIDTH' of cell '/axi_bram_ctrl_0' is ignored
```



IO_BRAM_ILA - [D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.xpr] - Vivado 2019.1

BLOCK DESIGN - IO *

Generate Output Products

The following output products will be generated.

Preview

- IO.bd (OOC per IP)
  - Synthesis
  - Implementation
  - Simulation

Synthesis Options

○ Global
● Out of context per IP
○ Out of context per Block Design

Run Settings

Number of jobs: 4

Source File Properties

IO.bd

☑ Enabled

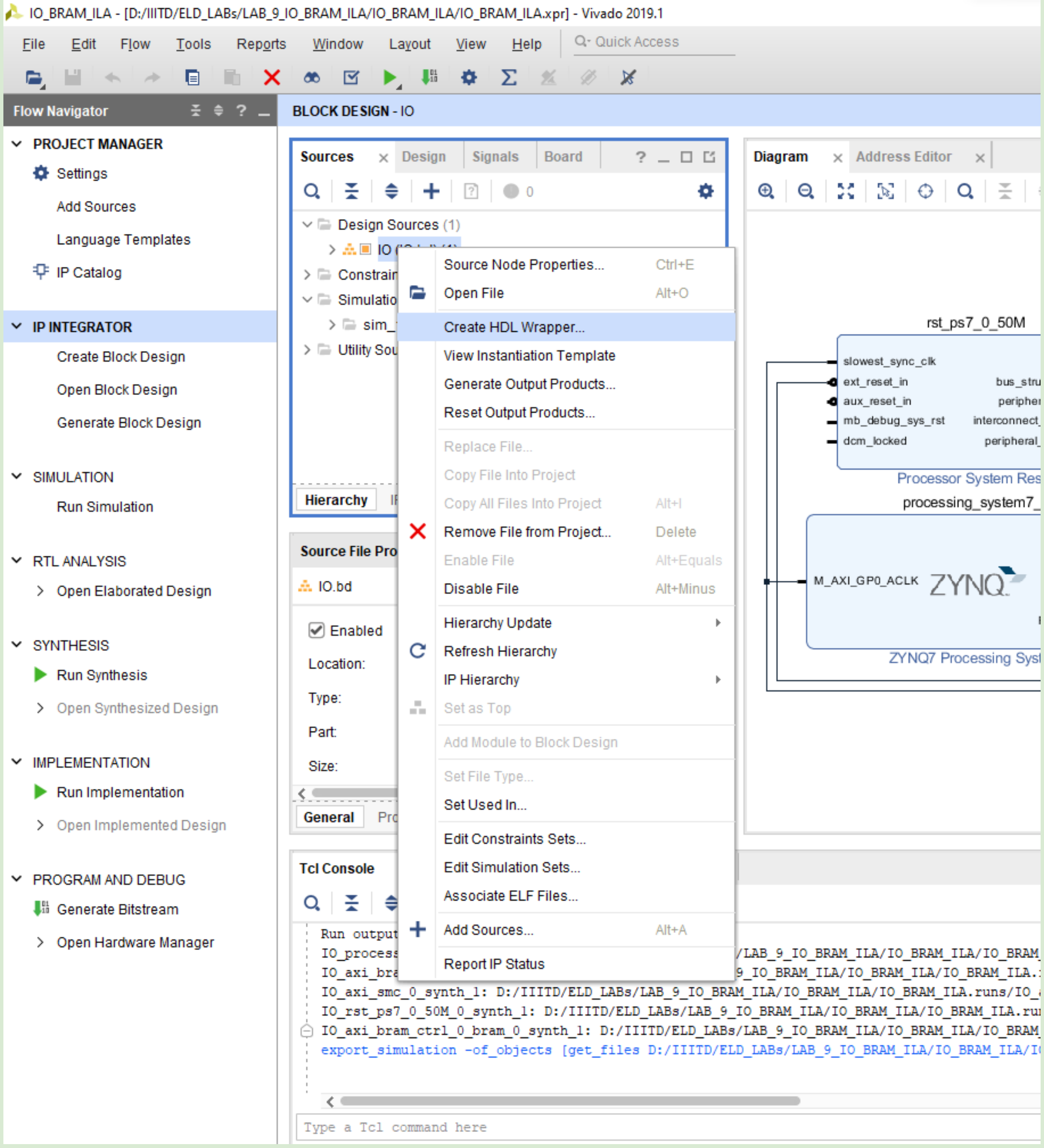
Location: D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_E

Type: Block Designs

Part: xc7z010clg400-1

Size: 0.2 KB

```
regenerate_bd_layout
regenerate_bd_layout
validate_bd_design
WARNING: [BD 41-721] Attempt to set value '0' on disabled parameter 'ID_WIDTH' of cell '/axi_bram_ctrl_0' is ignored
WARNING: [BD 41-721] Attempt to set value 'NO' on disabled parameter 'SUPPORTS_NARROW_BURST' of cell '/axi_bram_ctrl_0' is ignored
```

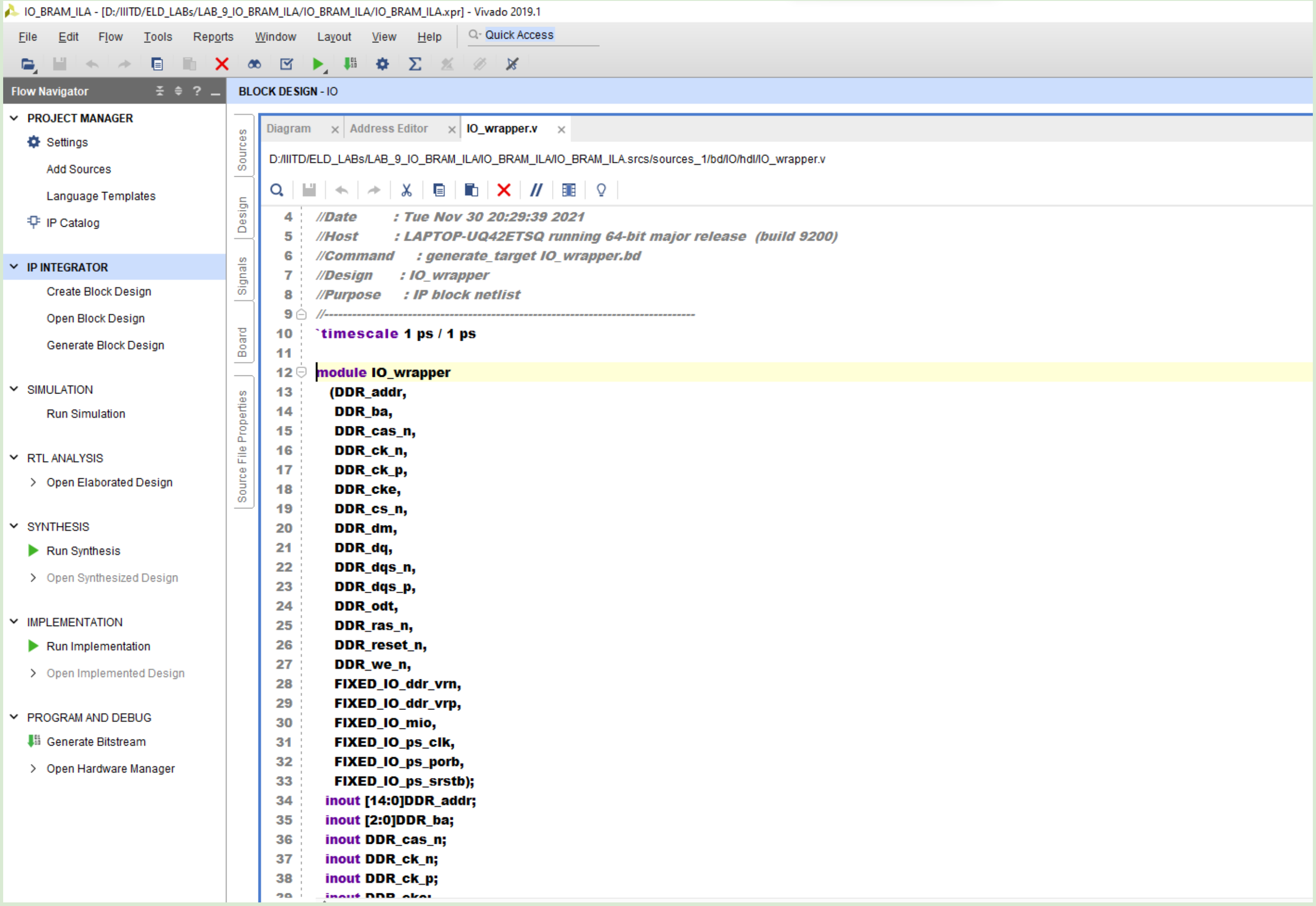


IO_BRAM_ILA - [D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.xpr] - Vivado 2019.1

BLOCK DESIGN - IO

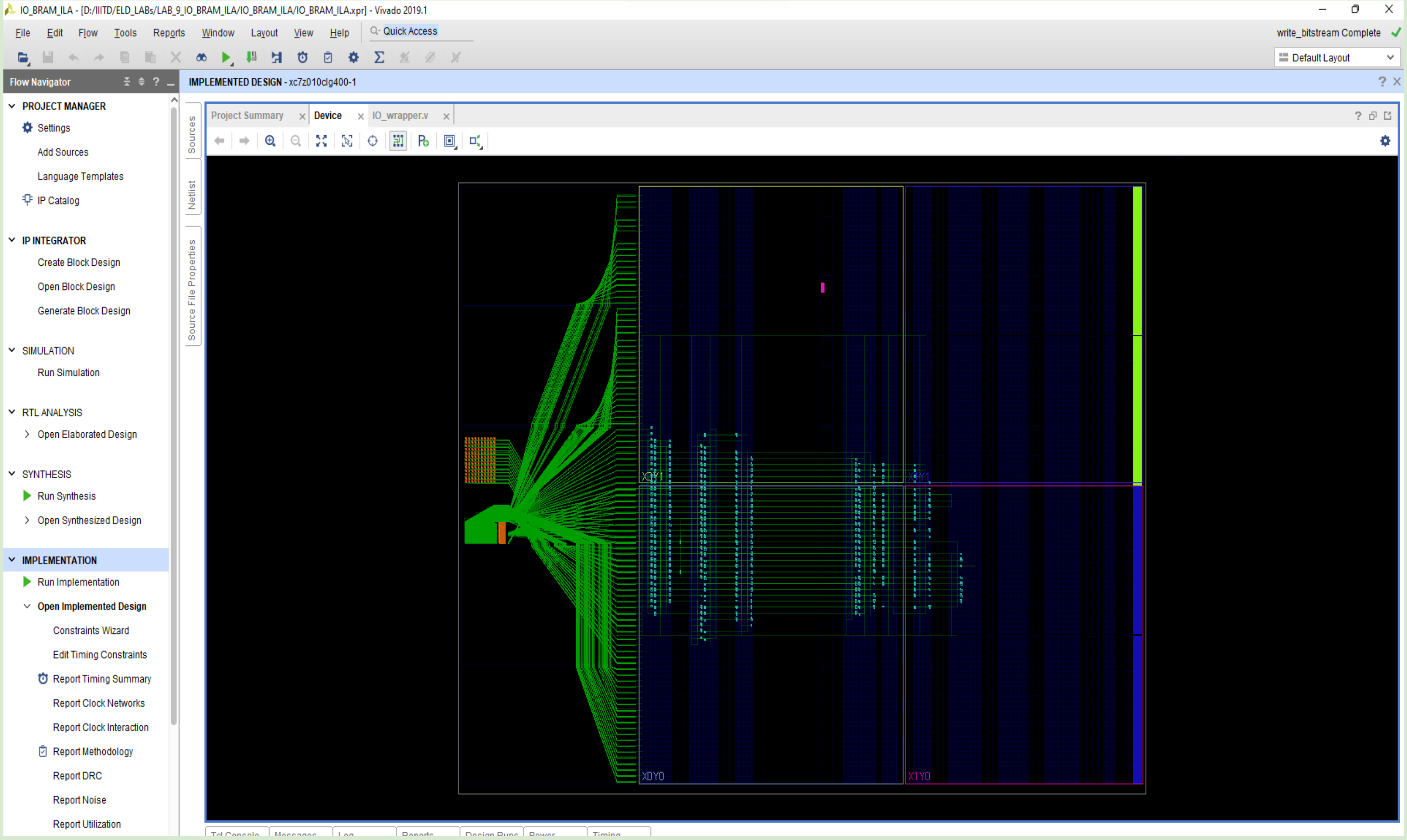
```
Run output
IO_process                                      /LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_
IO_axi_bra                                      9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.:
IO_axi_smc_0_synth_1: D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.runs/IO_
IO_rst_ps7_0_50M_0_synth_1: D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.ru
IO_axi_bram_ctrl_0_bram_0_synth_1: D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_
export_simulation -of_objects [get_files D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO
Type a Tcl command here
```

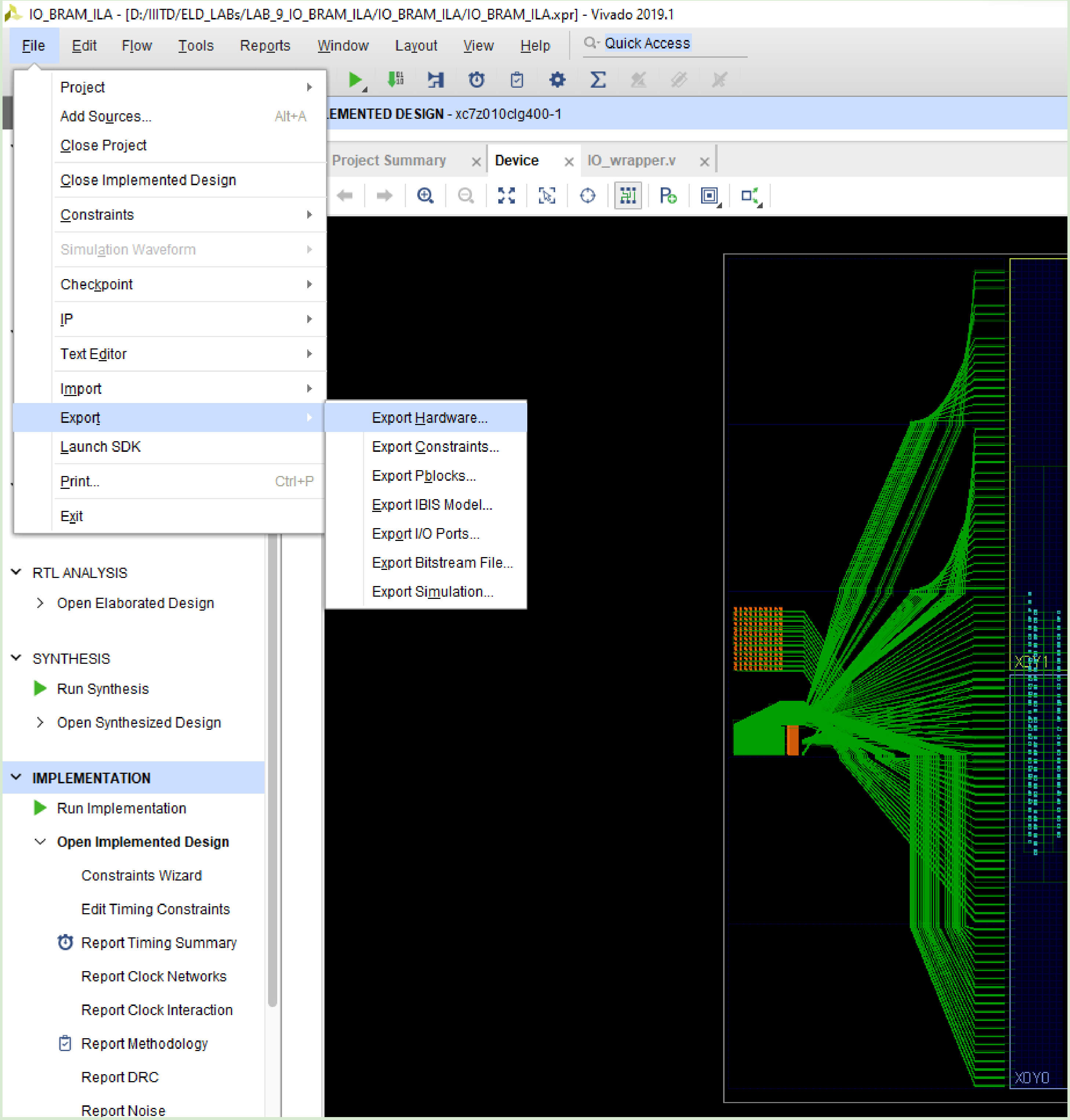
### Auto_Generated_HDL_Wrapper



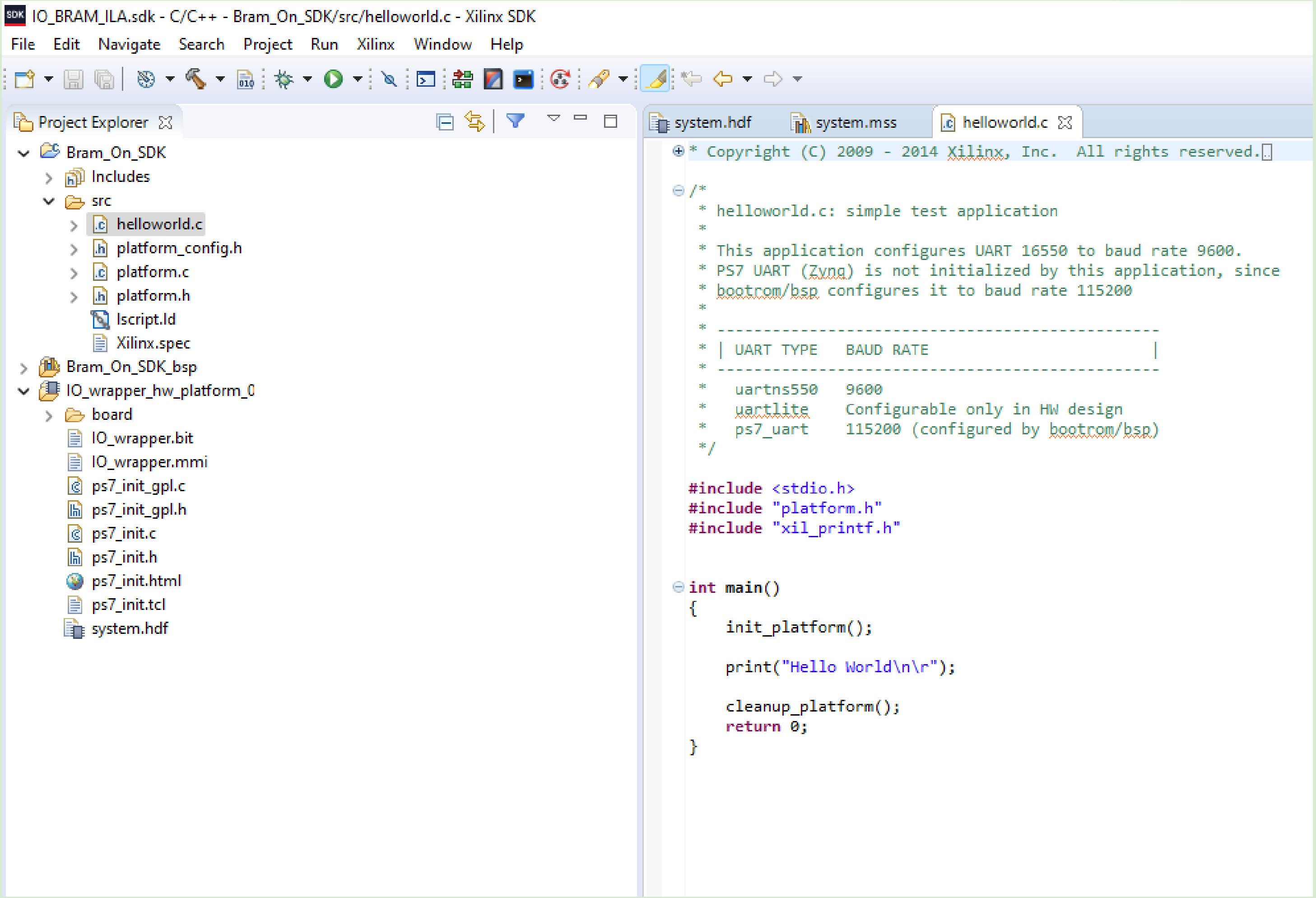
D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.srcs/sources_1/bd/IO/hdl/IO_wrapper.v

```
//Date        : Tue Nov 30 20:29:39 2021
//Host        : LAPTOP-UQ42ETSQ running 64-bit major release  (build 9200)
//Command     : generate_target IO_wrapper.bd
//Design      : IO_wrapper
//Purpose     : IP block netlist
//--------------------------------------------------------------------------------
`timescale 1 ps / 1 ps

module IO_wrapper
   (DDR_addr,
    DDR_ba,
    DDR_cas_n,
    DDR_ck_n,
    DDR_ck_p,
    DDR_cke,
    DDR_cs_n,
    DDR_dm,
    DDR_dq,
    DDR_dqs_n,
    DDR_dqs_p,
    DDR_odt,
    DDR_ras_n,
    DDR_reset_n,
    DDR_we_n,
    FIXED_IO_ddr_vrn,
    FIXED_IO_ddr_vrp,
    FIXED_IO_mio,
    FIXED_IO_ps_clk,
    FIXED_IO_ps_porb,
    FIXED_IO_ps_srstb);
  inout [14:0]DDR_addr;
  inout [2:0]DDR_ba;
  inout DDR_cas_n;
  inout DDR_ck_n;
  inout DDR_ck_p;
  inout DDR_cke;
```

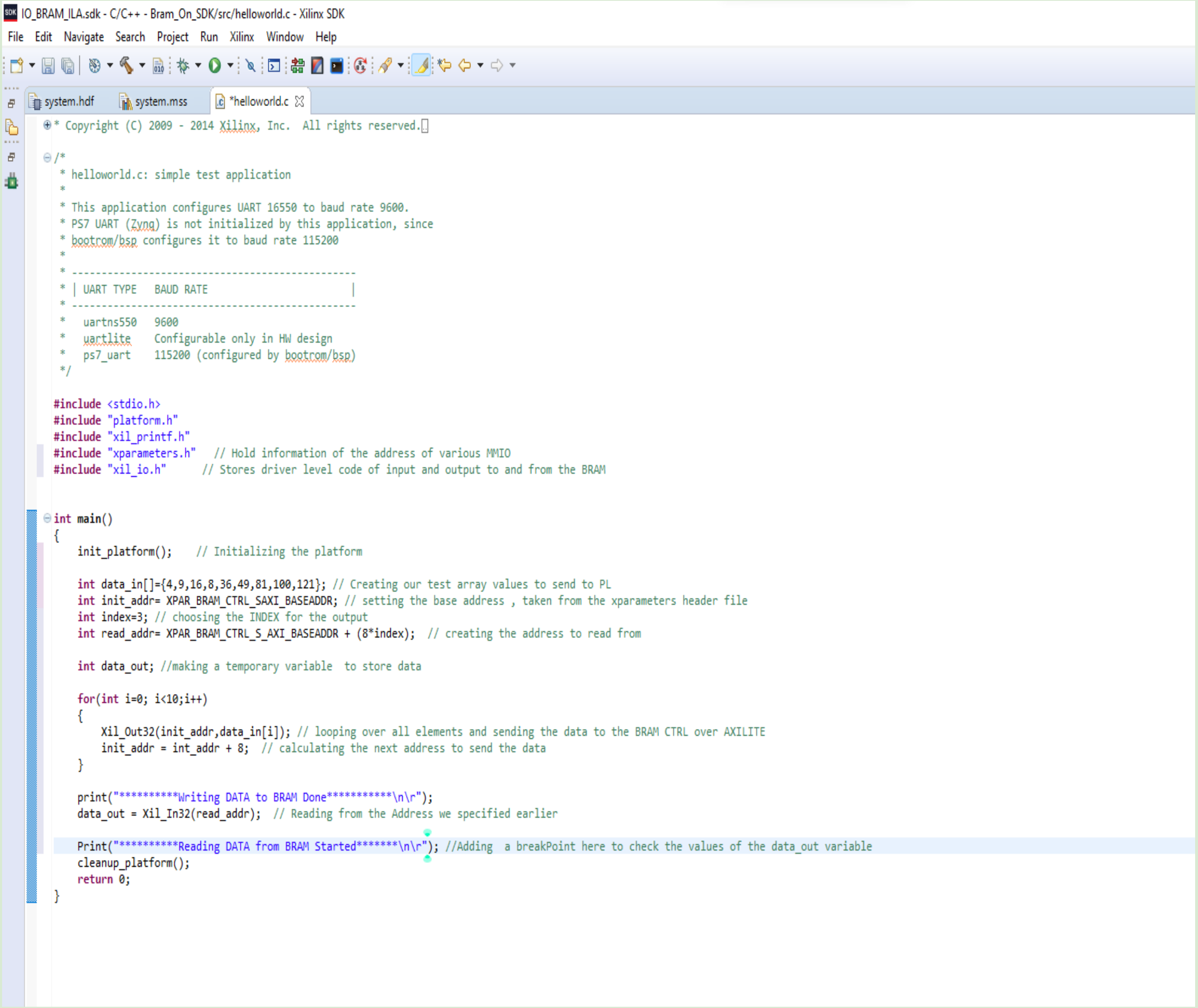



IO_BRAM_ILA - [D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.xpr] - Vivado 2019.1
File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Project
Add Sources... Alt+A
Close Project
Close Implemented Design
Constraints
Simulation Waveform
Checkpoint
IP
Text Editor
Import
Export
Launch SDK
Print... Ctrl+P
Exit
Export Hardware...
Export Constraints...
Export Pblocks...
Export IBIS Model...
Export I/O Ports...
Export Bitstream File...
Export Simulation...
EMENTED DESIGN - xc7z010clg400-1
Project Summary
Device
IO_wrapper.v
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
X0Y1
X0Y0

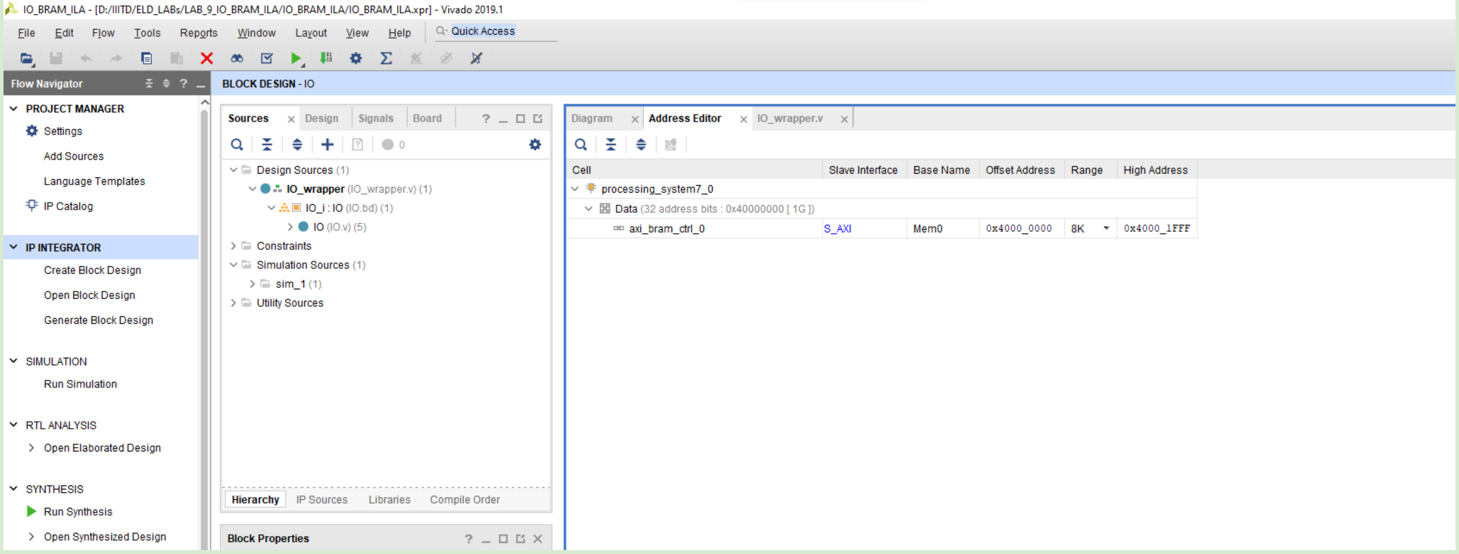
## Launching SDK and program in C and changing STD IN/OUT in BSP settings



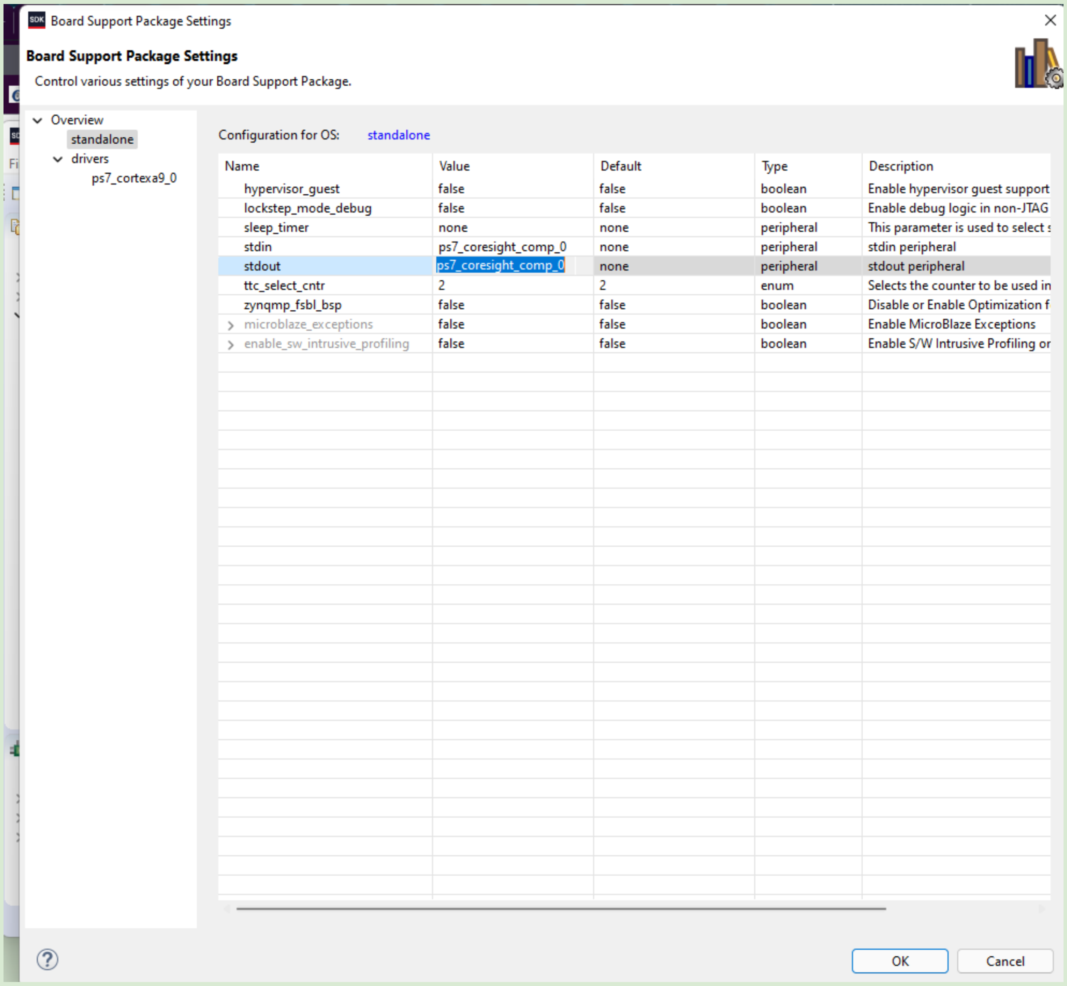
```c
* Copyright (C) 2009 - 2014 Xilinx, Inc.  All rights reserved.

/*
 * helloworld.c: simple test application
 *
 * This application configures UART 16550 to baud rate 9600.
 * PS7 UART (Zynq) is not initialized by this application, since
 * bootrom/bsp configures it to baud rate 115200
 *
 * ------------------------------------------------
 * | UART TYPE   BAUD RATE                        |
 * ------------------------------------------------
 *   uartns550   9600
 *   uartlite    Configurable only in HW design
 *   ps7_uart    115200 (configured by bootrom/bsp)
 */

#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"


int main()
{
    init_platform();

    print("Hello World\n\r");

    cleanup_platform();
    return 0;
}
```


IO_BRAM_ILA.sdk - C/C++ - Bram_On_SDK/src/helloworld.c - Xilinx SDK
File Edit Navigate Search Project Run Xilinx Window Help
system.hdf
system.mss
*helloworld.c

```
* Copyright (C) 2009 - 2014 Xilinx, Inc.  All rights reserved.

/*
 * helloworld.c: simple test application
 *
 * This application configures UART 16550 to baud rate 9600.
 * PS7 UART (Zynq) is not initialized by this application, since
 * bootrom/bsp configures it to baud rate 115200
 *
 * ------------------------------------------------
 * | UART TYPE   BAUD RATE                        |
 * ------------------------------------------------
 *   uartns550   9600
 *   uartlite    Configurable only in HW design
 *   ps7_uart    115200 (configured by bootrom/bsp)
 */

#include <stdio.h>
#include "platform.h"
#include "xil_printf.h"
#include "xparameters.h"   // Hold information of the address of various MMIO
#include "xil_io.h"      // Stores driver level code of input and output to and from the BRAM


int main()
{
    init_platform();    // Initializing the platform

    int data_in[]={4,9,16,8,36,49,81,100,121}; // Creating our test array values to send to PL
    int init_addr= XPAR_BRAM_CTRL_SAXI_BASEADDR; // setting the base address , taken from the xparameters header file
    int index=3; // choosing the INDEX for the output
    int read_addr= XPAR_BRAM_CTRL_S_AXI_BASEADDR + (8*index);  // creating the address to read from

    int data_out; //making a temporary variable  to store data

    for(int i=0; i<10;i++)
    {
        Xil_Out32(init_addr,data_in[i]); // looping over all elements and sending the data to the BRAM CTRL over AXILITE
        init_addr = int_addr + 8;  // calculating the next address to send the data
    }

    print("**********Writing DATA to BRAM Done***********\n\r");
    data_out = Xil_In32(read_addr);  // Reading from the Address we specified earlier

    Print("**********Reading DATA from BRAM Started*******\n\r"); //Adding  a breakPoint here to check the values of the data_out variable
    cleanup_platform();
    return 0;
}
```



Cell	Slave Interface	Base Name	Offset Address	Range	High Address
processing_system7_0					
Data (32 address bits : 0x40000000 [1G])					
axi_bram_ctrl_0	S_AXI	Mem0	0x4000_0000	8K	0x4000_1FFF



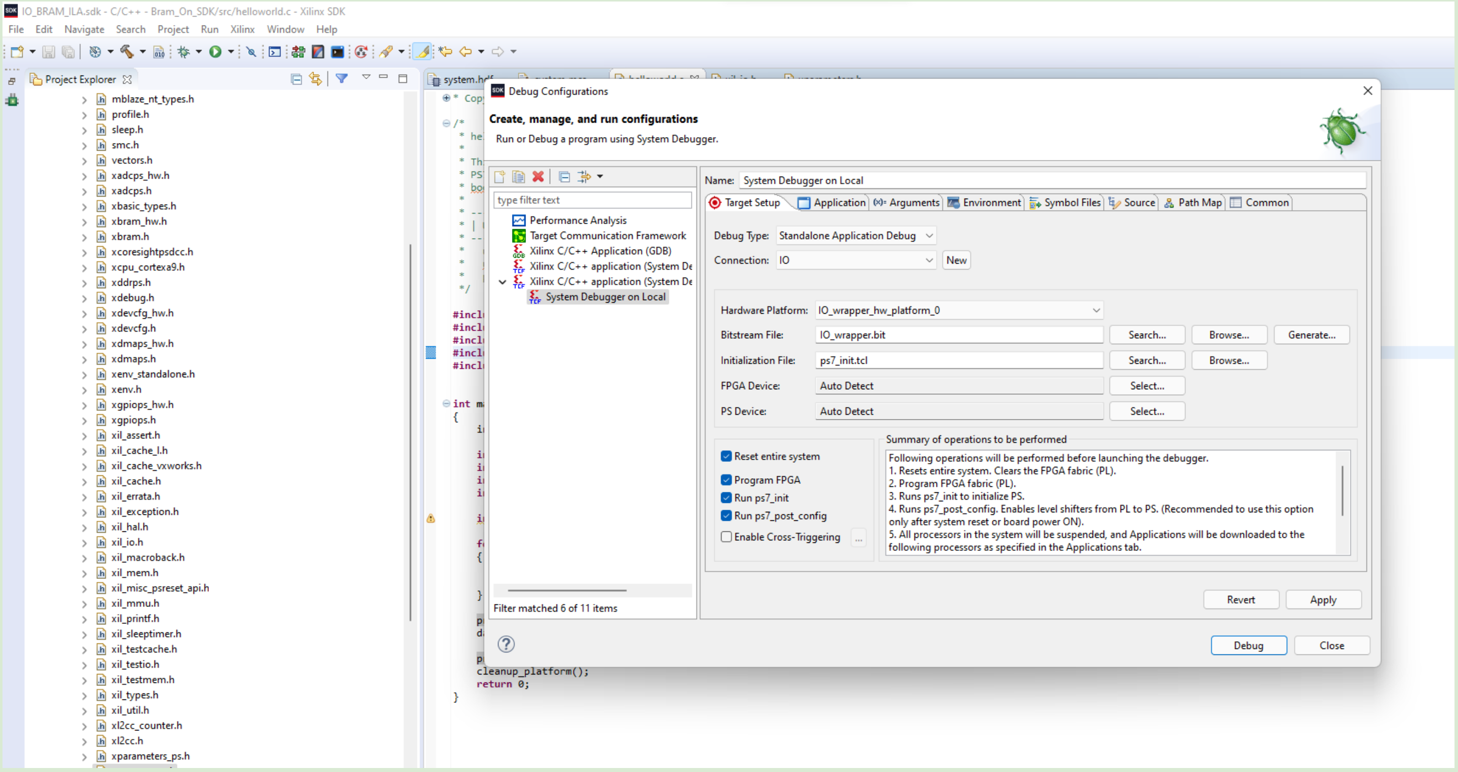
Board Support Package Settings

Control various settings of your Board Support Package.

Configuration for OS: standalone

Name	Value	Default	Type	Description
hypervisor_guest	false	false	boolean	Enable hypervisor guest support
lockstep_mode_debug	false	false	boolean	Enable debug logic in non-JTAG
sleep_timer	none	none	peripheral	This parameter is used to select s
stdin	ps7_coresight_comp_0	none	peripheral	stdin peripheral
stdout	ps7_coresight_comp_0	none	peripheral	stdout peripheral
ttc_select_cntr	2	2	enum	Selects the counter to be used in
zynqmp_fsbl_bsp	false	false	boolean	Disable or Enable Optimization f
› microblaze_exceptions	false	false	boolean	Enable MicroBlaze Exceptions
› enable_sw_intrusive_profiling	false	false	boolean	Enable S/W Intrusive Profiling or

## running program in debug mode



Create, manage, and run configurations

Run or Debug a program using System Debugger.

Name: System Debugger on Local

Debug Type: Standalone Application Debug

Connection: IO New

Hardware Platform: IO_wrapper_hw_platform_0

Bitstream File: IO_wrapper.bit

Initialization File: ps7_init.tcl

FPGA Device: Auto Detect

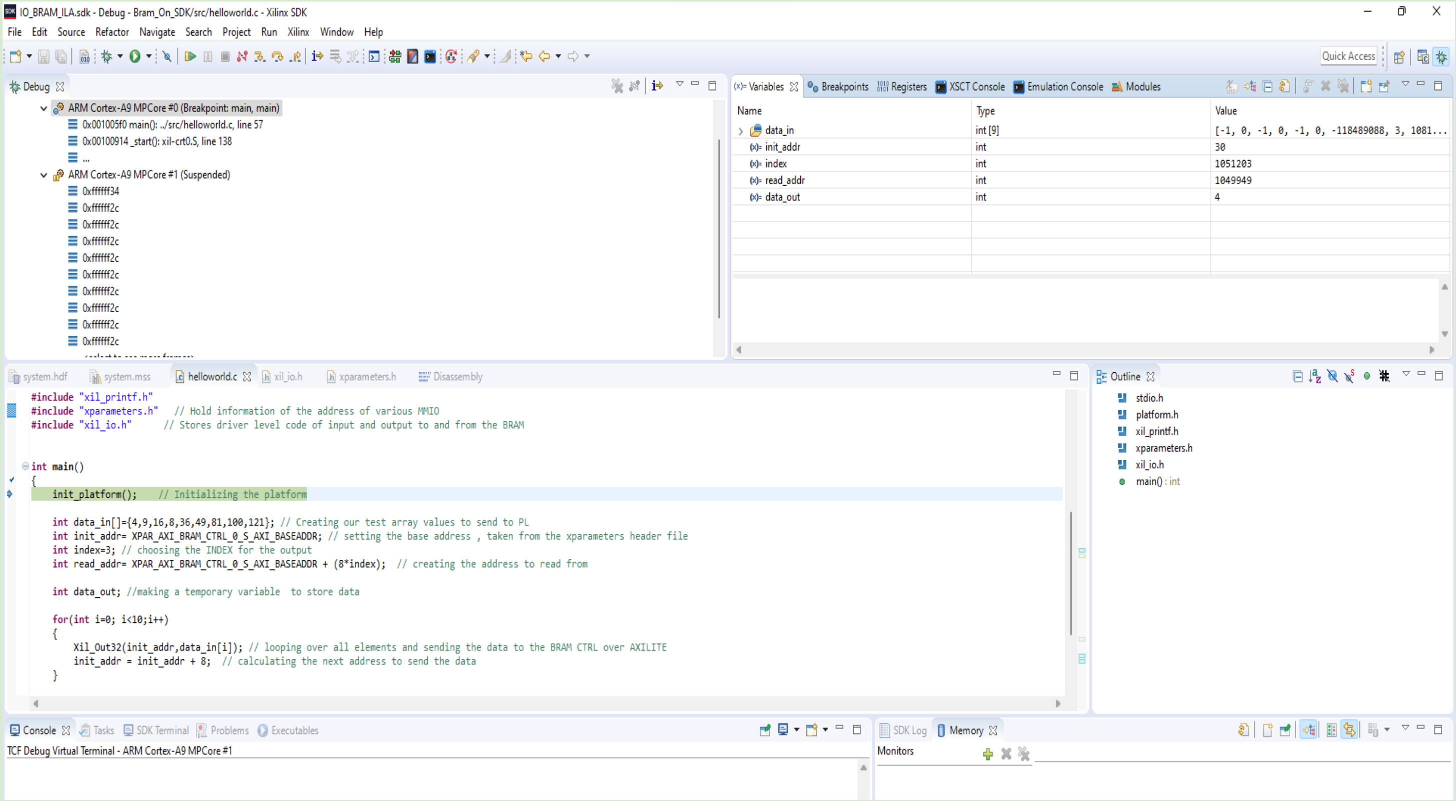
PS Device: Auto Detect

☑ Reset entire system
☑ Program FPGA
☑ Run ps7_init
☑ Run ps7_post_config
☐ Enable Cross-Triggering

Summary of operations to be performed

Following operations will be performed before launching the debugger.
1. Resets entire system. Clears the FPGA fabric (PL).
2. Program FPGA fabric (PL).
3. Runs ps7_init to initialize PS.
4. Runs ps7_post_config. Enables level shifters from PL to PS. (Recommended to use this option only after system reset or board power ON).
5. All processors in the system will be suspended, and Applications will be downloaded to the following processors as specified in the Applications tab.

```
cleanup_platform();
return 0;
}
```



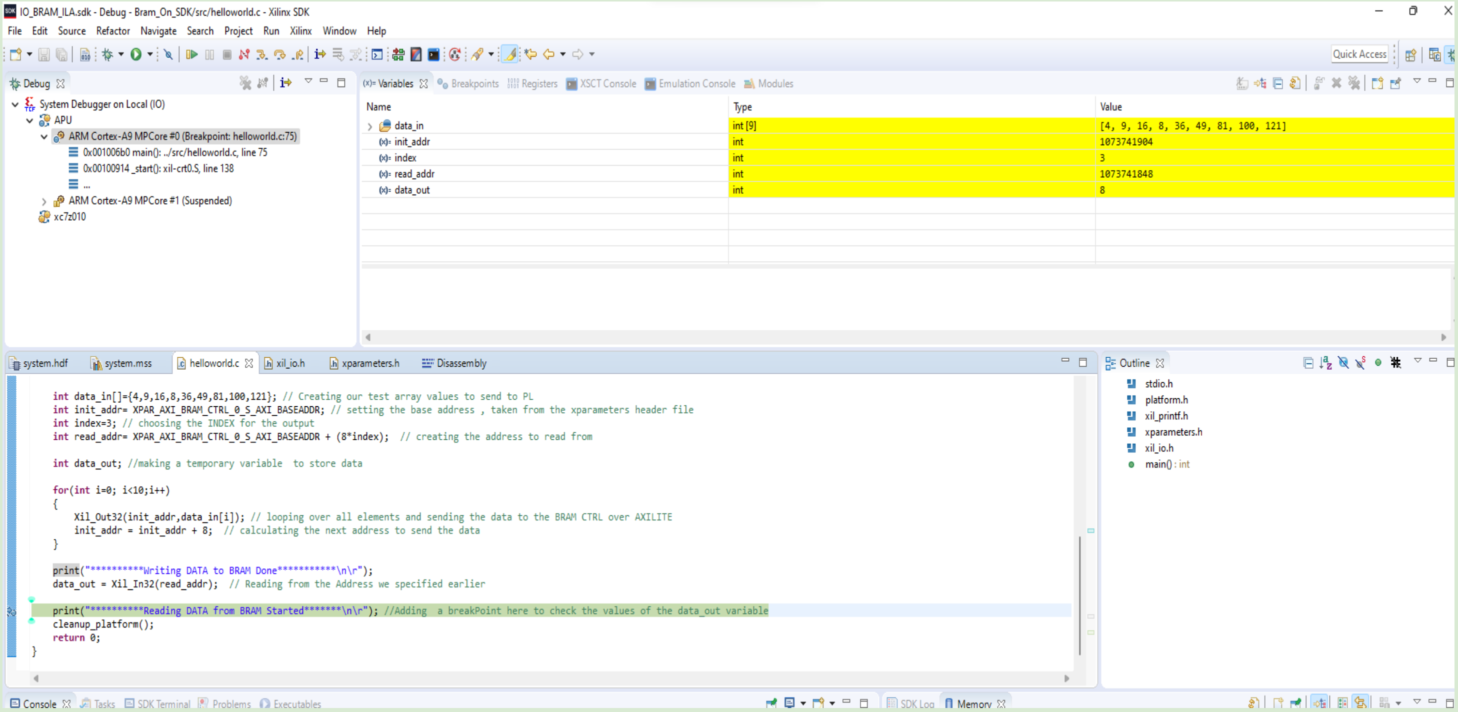
```
ARM Cortex-A9 MPCore #0 (Breakpoint: main, main)
    0x001005f0 main(): ../src/helloworld.c, line 57
    0x00100914 _start(): xil-crt0.S, line 138
    ...
ARM Cortex-A9 MPCore #1 (Suspended)
    0xfffff34
    0xffffff2c
    0xffffff2c
    0xffffff2c
    0xffffff2c
    0xffffff2c
    0xffffff2c
    0xffffff2c
    0xffffff2c
    0xffffff2c
```

Name	Type	Value
data_in	int [9]	[-1, 0, -1, 0, -1, 0, -118489088, 3, 1081...
init_addr	int	30
index	int	1051203
read_addr	int	1049949
data_out	int	4

```c
#include "xil_printf.h"
#include "xparameters.h"   // Hold information of the address of various MMIO
#include "xil_io.h"      // Stores driver level code of input and output to and from the BRAM


int main()
{
    init_platform();    // Initializing the platform

    int data_in[]={4,9,16,8,36,49,81,100,121}; // Creating our test array values to send to PL
    int init_addr= XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR; // setting the base address , taken from the xparameters header file
    int index=3; // choosing the INDEX for the output
    int read_addr= XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + (8*index);  // creating the address to read from

    int data_out; //making a temporary variable  to store data

    for(int i=0; i<10;i++)
    {
        Xil_Out32(init_addr,data_in[i]); // looping over all elements and sending the data to the BRAM CTRL over AXILITE
        init_addr = init_addr + 8;  // calculating the next address to send the data
    }
```

TCF Debug Virtual Terminal - ARM Cortex-A9 MPCore #1

Set the breakpoints properly and when we resume the program we will see the output.

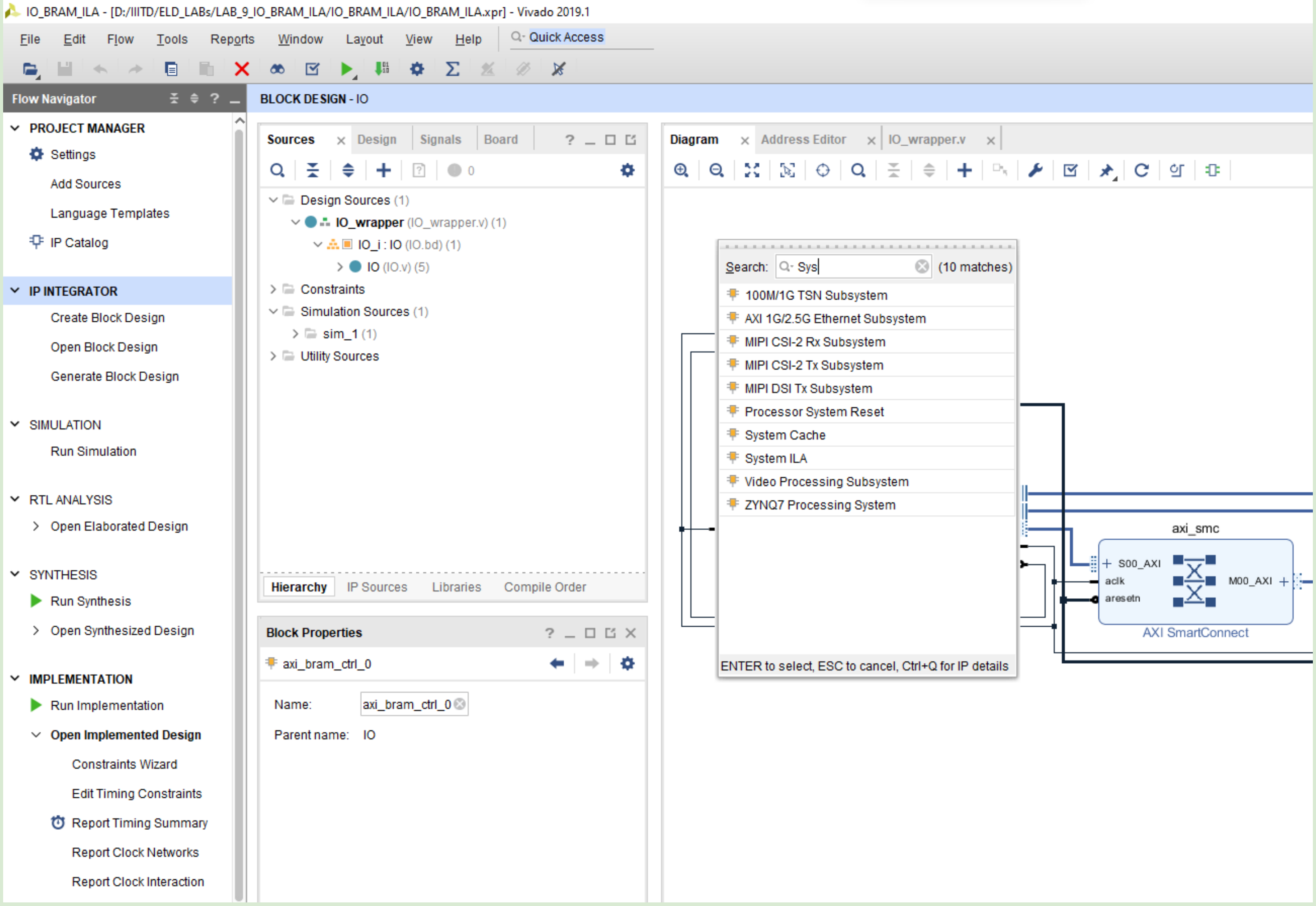


```
System Debugger on Local (IO)
  APU
    ARM Cortex-A9 MPCore #0 (Breakpoint: helloworld.c:75)
        0x001006b0 main(): ../src/helloworld.c, line 75
        0x00100914 _start(): xil-crt0.S, line 138
        ...
    ARM Cortex-A9 MPCore #1 (Suspended)
  xc7z010
```

Name	Type	Value
data_in	int [9]	[4, 9, 16, 8, 36, 49, 81, 100, 121]
init_addr	int	1073741904
index	int	3
read_addr	int	1073741848
data_out	int	8

```c
    int data_in[]={4,9,16,8,36,49,81,100,121}; // Creating our test array values to send to PL
    int init_addr= XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR; // setting the base address , taken from the xparameters header file
    int index=3; // choosing the INDEX for the output
    int read_addr= XPAR_AXI_BRAM_CTRL_0_S_AXI_BASEADDR + (8*index);  // creating the address to read from

    int data_out; //making a temporary variable  to store data

    for(int i=0; i<10;i++)
    {
        Xil_Out32(init_addr,data_in[i]); // looping over all elements and sending the data to the BRAM CTRL over AXILITE
        init_addr = init_addr + 8;  // calculating the next address to send the data
    }

    print("**********Writing DATA to BRAM Done***********\n\r");
    data_out = Xil_In32(read_addr);  // Reading from the Address we specified earlier

    print("**********Reading DATA from BRAM Started*******\n\r"); //Adding  a breakPoint here to check the values of the data_out variable
    cleanup_platform();
    return 0;
}
```

Now. Adding the.System ILA IP in the design block we created earlier And setting the port with.And number of probes.



IO_BRAM_ILA - [D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.xpr] - Vivado 2019.1

BLOCK DESIGN - IO

Search: Sys (10 matches)

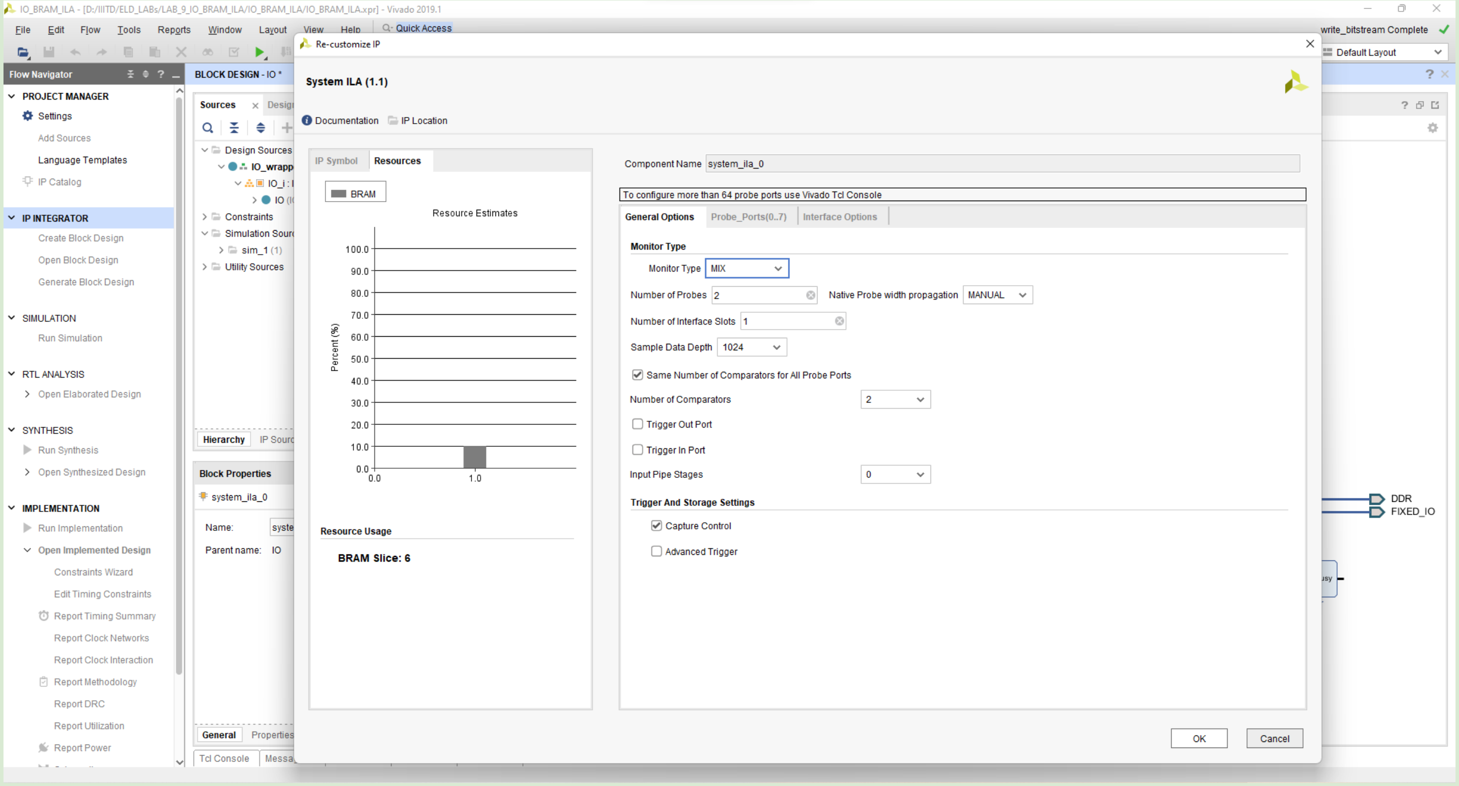
- 100M/1G TSN Subsystem
- AXI 1G/2.5G Ethernet Subsystem
- MIPI CSI-2 Rx Subsystem
- MIPI CSI-2 Tx Subsystem
- MIPI DSI Tx Subsystem
- Processor System Reset
- System Cache
- System ILA
- Video Processing Subsystem
- ZYNQ7 Processing System

ENTER to select, ESC to cancel, Ctrl+Q for IP details

Block Properties: axi_bram_ctrl_0

Name: axi_bram_ctrl_0

Parent name: IO



IO_BRAM_ILA - [D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.xpr] - Vivado 2019.1

Re-customize IP

System ILA (1.1)

Component Name: system_ila_0

To configure more than 64 probe ports use Vivado Tcl Console

General Options

Monitor Type

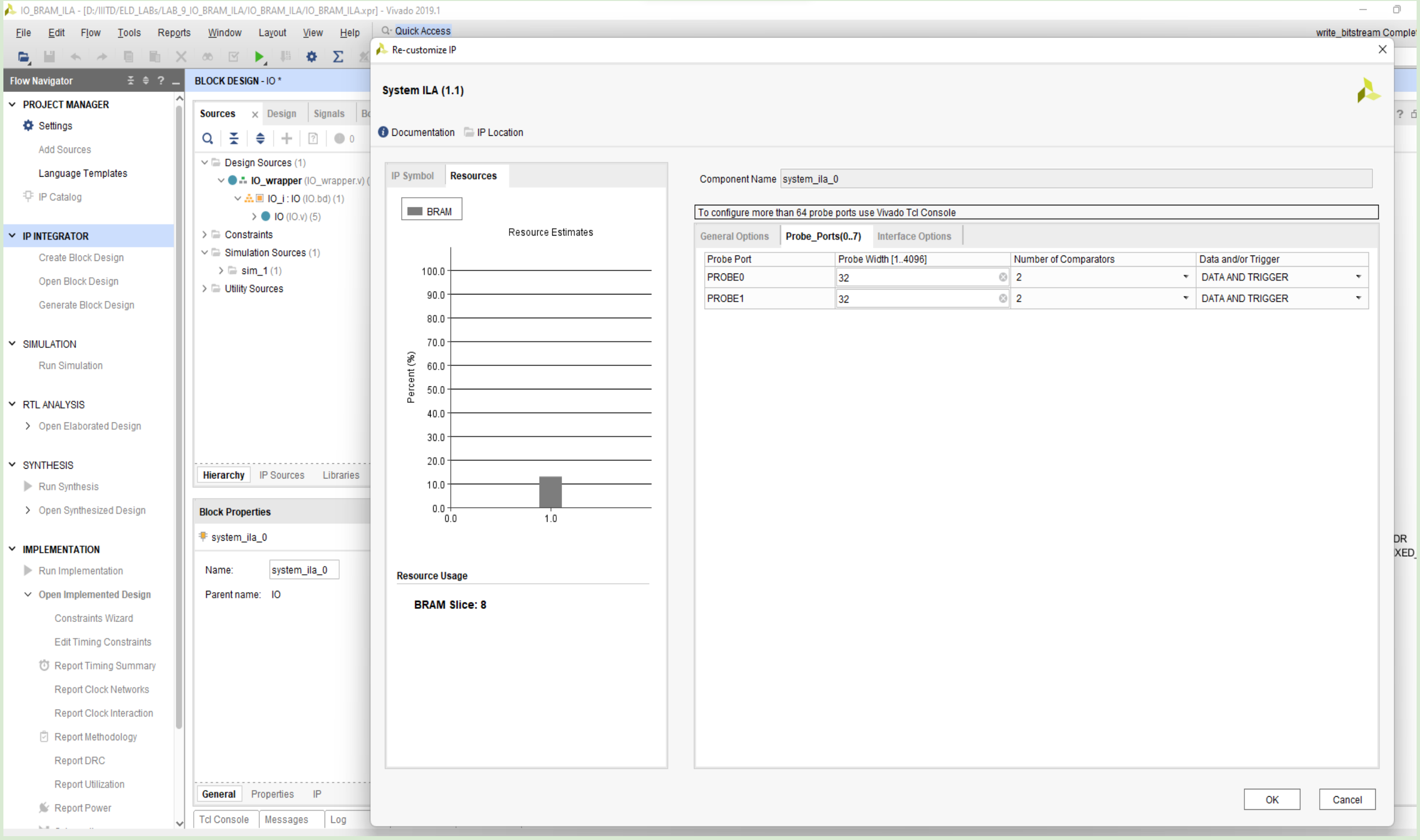
- Monitor Type: MIX
- Number of Probes: 2
- Native Probe width propagation: MANUAL
- Number of Interface Slots: 1
- Sample Data Depth: 1024
- ☑ Same Number of Comparators for All Probe Ports
- Number of Comparators: 2
- ☐ Trigger Out Port
- ☐ Trigger In Port
- Input Pipe Stages: 0

Trigger And Storage Settings

- ☑ Capture Control
- ☐ Advanced Trigger

Resource Usage

BRAM Slice: 6



IO_BRAM_ILA - [D:/IIITD/ELD_LABs/LAB_9_IO_BRAM_ILA/IO_BRAM_ILA/IO_BRAM_ILA.xpr] - Vivado 2019.1

Re-customize IP

System ILA (1.1)

Component Name: system_ila_0

To configure more than 64 probe ports use Vivado Tcl Console

General Options | Probe_Ports(0..7) | Interface Options

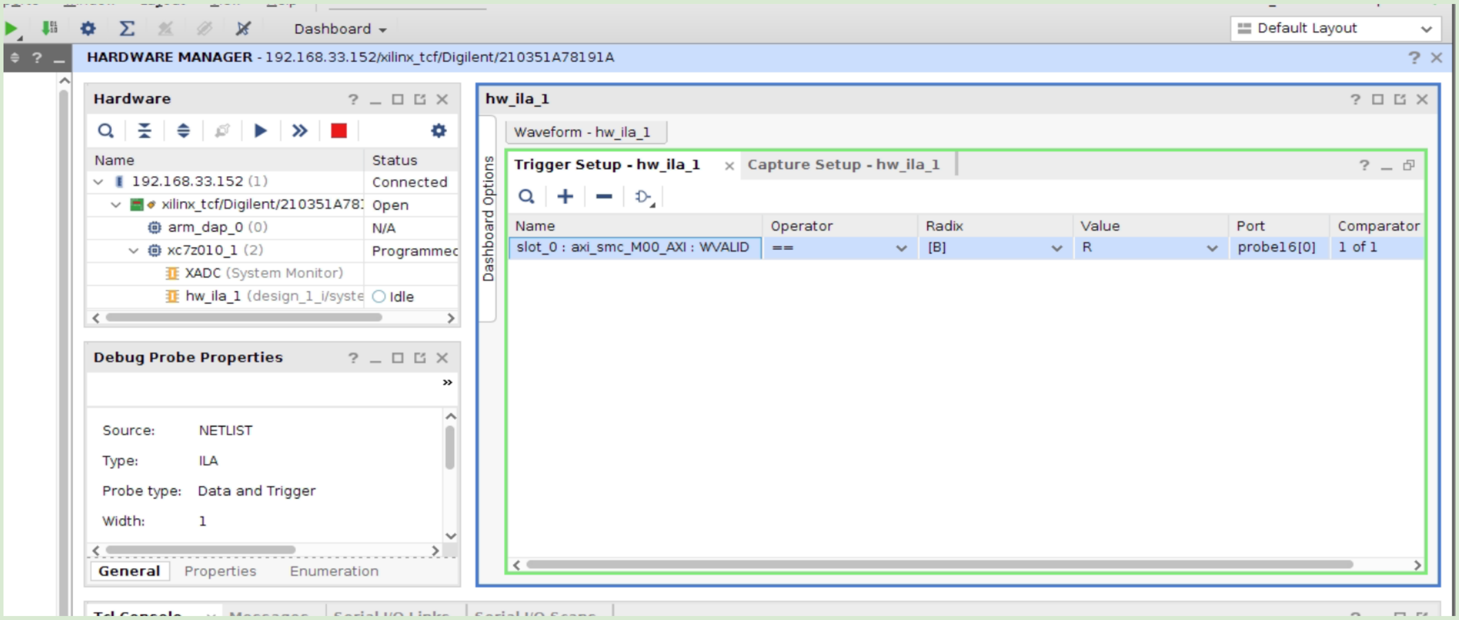
Probe Port	Probe Width [1..4096]	Number of Comparators	Data and/or Trigger
PROBE0	32	2	DATA AND TRIGGER
PROBE1	32	2	DATA AND TRIGGER

Resource Usage

BRAM Slice: 8

After validating, Automation, And creating the HDL wrapper.We will again follow the previous steps.And.Create a trigger in the ILA.Window in through hardware manager.And see the waveform.And the handshake of the.Transactions that were made in the.Program.

Output-put ILA:



HARDWARE MANAGER - 192.168.33.152/xilinx_tcf/Digilent/210351A78191A

Hardware

Name	Status
192.168.33.152 (1)	Connected
xilinx_tcf/Digilent/210351A781	Open
arm_dap_0 (0)	N/A
xc7z010_1 (2)	Programmed
XADC (System Monitor)	
hw_ila_1 (design_1_i/syste	Idle

Debug Probe Properties

Source: NETLIST

Type: ILA

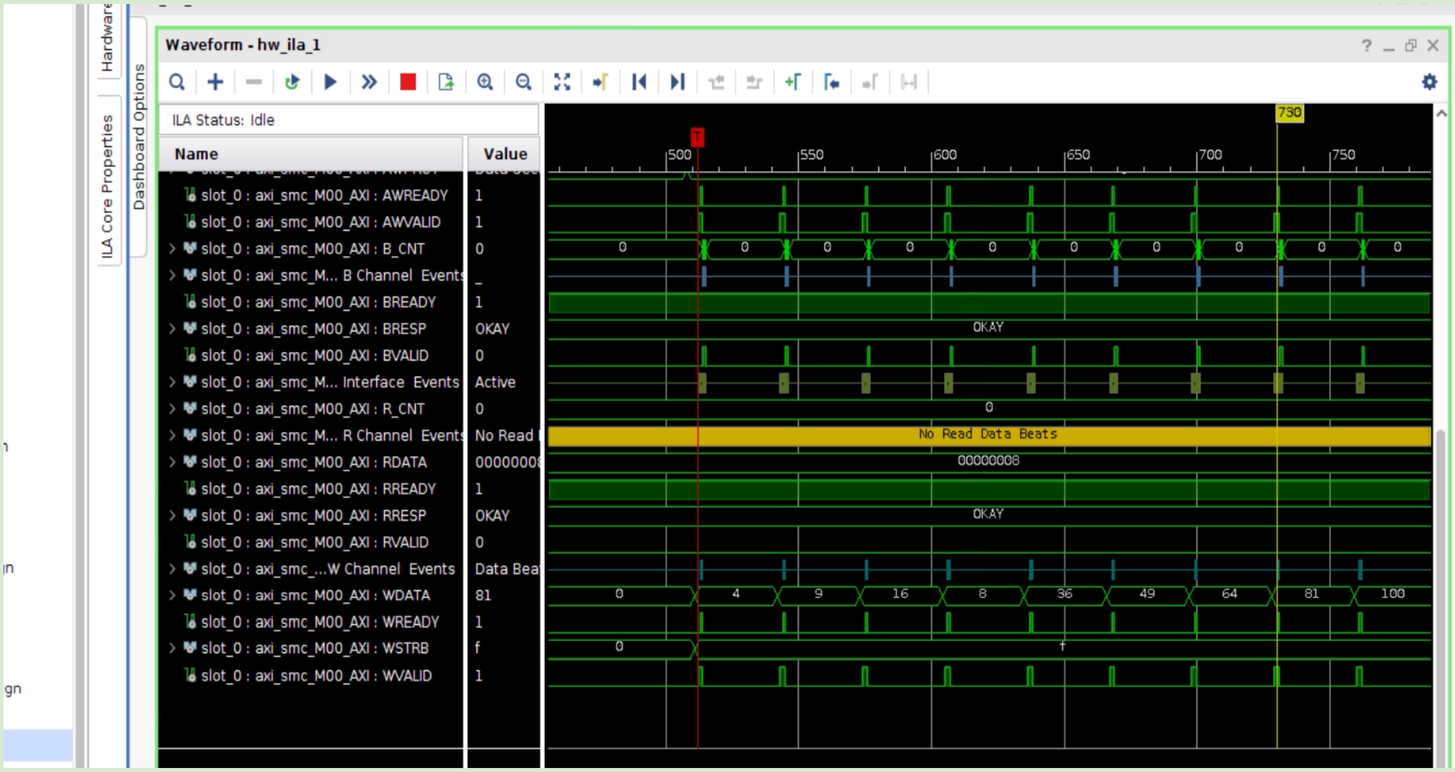
Probe type: Data and Trigger

Width: 1

hw_ila_1

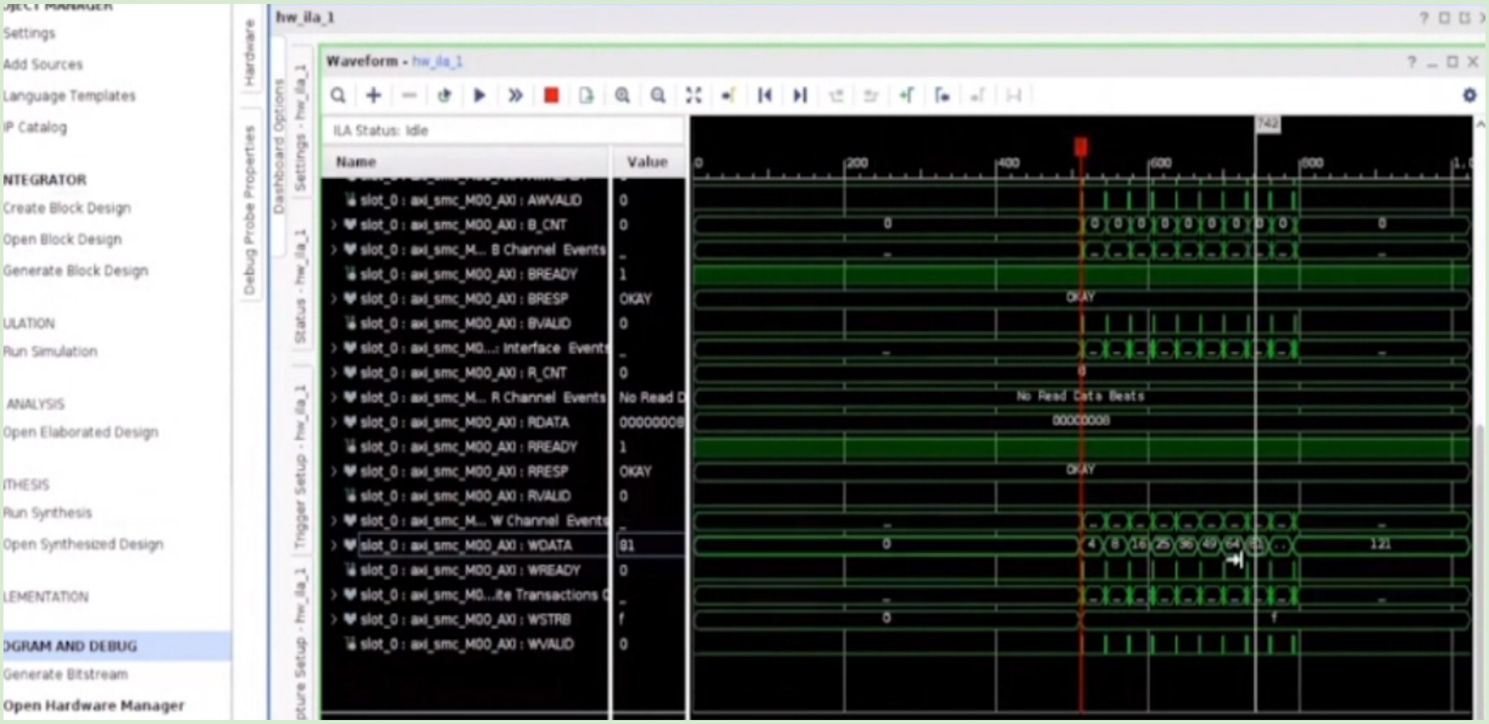
Trigger Setup - hw_ila_1

Name	Operator	Radix	Value	Port	Comparator
slot_0 : axi_smc_M00_AXI : WVALID	==	[B]	R	probe16[0]	1 of 1



ILA Status: Idle

Name	Value
slot_0 : axi_smc_M00_AXI : AWREADY	1
slot_0 : axi_smc_M00_AXI : AWVALID	1
slot_0 : axi_smc_M00_AXI : B_CNT	0
slot_0 : axi_smc_M... B Channel Events	_
slot_0 : axi_smc_M00_AXI : BREADY	1
slot_0 : axi_smc_M00_AXI : BRESP	OKAY
slot_0 : axi_smc_M00_AXI : BVALID	0
slot_0 : axi_smc_M... Interface Events	Active
slot_0 : axi_smc_M00_AXI : R_CNT	0
slot_0 : axi_smc_M... R Channel Events	No Read
slot_0 : axi_smc_M00_AXI : RDATA	00000008
slot_0 : axi_smc_M00_AXI : RREADY	1
slot_0 : axi_smc_M00_AXI : RRESP	OKAY
slot_0 : axi_smc_M00_AXI : RVALID	0
slot_0 : axi_smc_...W Channel Events	Data Bea
slot_0 : axi_smc_M00_AXI : WDATA	81
slot_0 : axi_smc_M00_AXI : WREADY	1
slot_0 : axi_smc_M00_AXI : WSTRB	f
slot_0 : axi_smc_M00_AXI : WVALID	1



ILA Status: Idle

Name	Value
slot_0 : axi_smc_M00_AXI : AWVALID	0
slot_0 : axi_smc_M00_AXI : B_CNT	0
slot_0 : axi_smc_M... B Channel Events	_
slot_0 : axi_smc_M00_AXI : BREADY	1
slot_0 : axi_smc_M00_AXI : BRESP	OKAY
slot_0 : axi_smc_M00_AXI : BVALID	0
slot_0 : axi_smc_M0...: Interface Events	_
slot_0 : axi_smc_M00_AXI : R_CNT	0
slot_0 : axi_smc_M... R Channel Events	No Read D
slot_0 : axi_smc_M00_AXI : RDATA	00000008
slot_0 : axi_smc_M00_AXI : RREADY	1
slot_0 : axi_smc_M00_AXI : RRESP	OKAY
slot_0 : axi_smc_M00_AXI : RVALID	0
slot_0 : axi_smc_M... W Channel Events	_
slot_0 : axi_smc_M00_AXI : WDATA	81
slot_0 : axi_smc_M00_AXI : WREADY	0
slot_0 : axi_smc_M0...ite Transactions C	_
slot_0 : axi_smc_M00_AXI : WSTRB	f
slot_0 : axi_smc_M00_AXI : WVALID	0

Conclusion:

Successfully created block design in Vivado using the BRAM AND ILA IP Integrator and configure the Zynq IP according to our needs and wrote C programs for Standalone system and seen the waveform output using ILA window