## CS 221 Logic Design

Fall 2021

By Wessam El-Behaidy & Salwa Osama

#### MIDTERM EXAM

Midterm Exam (based on announced schedule)

Day: Wed. 24 Nov.

Time: from 11 for Group1 (800 students)

from 12 for Group2 (395 students)

#### تنبيهات هامة

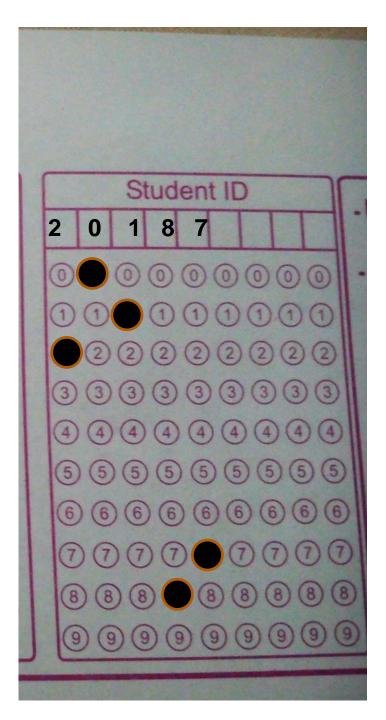
- الحضور للكلية قبل الموعد بنصف ساعة على الأقل
  - و يتواجد معك (قلم جاف- قلم رصاص استيكة)
- الاجابة في ورقة الاجابات الالكترونية بالقلم الرصاص وتحبر في النهاية
  - كتابة البيانات على ورقة الاسئلة وورقة الاجابة
  - تسليم كلا من ورقة الاسئلة وورقة الاجابة (عدم تسليم الورقتين يلغى امتحاثك)
    - و غير مسموح باستخدام الالة الحاسبة داخل الامتحان

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		00000	38 - ABCDE 4	8-ABCDE
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## الشكل العام لورقة التصحيح الألكتروني

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=	Date :		

## البيانات الأساسية



رقم الطالب

مثال:

رقم الجلوس: 20187

#### تعليمات هامة

- Use pencil or blue or black pen
- Fill the circle compeletly

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- Do not fill in more than one circle
- To change your answer use the eraser
- DO NOT USE THE CORRECTOR
- -For true & False questions, (mark (A) for true& (E) For false)

## مثال لإجابات مظللة بشكل صحيح

مثال: اجابة السؤال الأول B

T F	T F	T F	T F	T F
1.80000 - 2.08000	12.ABCDE	21.0000 22.0000	32-86000	42.88COC
3. A B C D	13 - A B C O E	23-ABCDE	33 - 8 8 0 0 8	43.88600
4-88600	14 - A B C O E	24 - A B C D E	34. A B C D E	44.0000
5.880DE	15-8800E	25 - A B C D E	35 - ABCDE	45-88CDE
6.88000	16-ABCOE	26-ABCOE	36 - A B C D E	46-88000
7-88CDD	17.8800E	27-8800E	37 - A B C D E	47.08COD
8.88000	18-8800E	28-ABCOE	38 - ABCDE	48 - A B C O E
9.08000	19-8800E	29-88000	39. ABCOE	49 - A B C D E
10.0000	20.88006	30-ABCDE	40 - A B C D E	50-88CDE
T F 51.88000	T F	T F	T F 81 - A B C D E	91 - ABCDE
52-ABCQE	62 - 8 8 6 0 6	72 - A B C D E	82 - A B C D E	92 - A B C D C

## مثال لإجابات مظللة بشكل خطأ

T F	T F	T F
2-0000	12 - A B C D E	22 - A B C D E
- 3- X ® © ® ©	13 - A B C O E	23 - A B C O E
- 4-8870B	14 - A B C O E	24 - A B C D E
5.00000	15 - 8 8 0 P E	25 - A B C D E
<b>-</b> 6.88000	16 - A B C O E	26 - A B C D E
7-88000	17 - A B C D E	27 - A B C D E
- 8. BBCCC	18 - (A) (B) (C) (D) (C)	28 - A B C D E
- 9.0000	19-88CDE	29 - A B C D E

#### INSTRUCTIONS OF THE EXAM

Faculty of Computers and Artificial Intelligence CS 221: Logic Design

Fall 2021- 2022 Time: 30 minutes Dr. Wessam El-Behaidy & Dr. Salwa Osama



جارمة حلوات Helwan University

(Group2\_Model A)

#### Please read the following instructions carefully:

- \* Remember to fill in your Name and Student ID. Only sheets with both a name and ID will be graded.
- Deliver both external answer sheet and the question paper. If not, your paper will not graded
- No Calculator is permitted
- This is a closed-book exam. You are forbidden from accessing any external material, notes, electronic material, or online resources.

Name:	ID:	

Attempt to answer ALL questions in this exam.

Multiple choice Questions (Circle only ONE answer per question on the external answer sheet. If more than one answer is selected, the question will NOT be graded.) [20 marks]

## COMBINATIONAL CIRCUITS

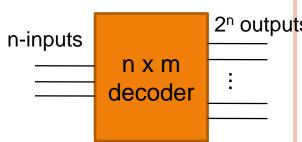
Lecture 6

11

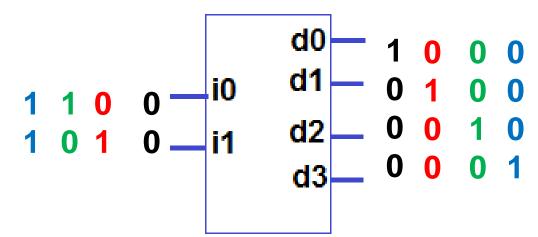
#### REMEMBER

- This chapter includes the <u>most important standard</u> combinational circuits:
  - Adders, Subtractors, Decoders, Encoders, Multiplexers and Demultiplexer.
- We will know their internal design and the functionality of each.
- But, remember our aim is to know how to think to design a circuit

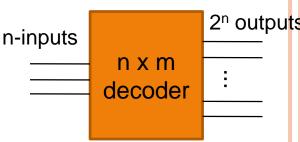
#### **DECODERS**



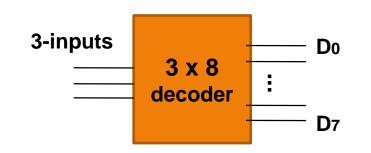
- A Decoder.
  - Is a popular combinational logic building block
  - It converts input binary number to one high output
- 2-input decoder
- → Has four possible input binary numbers
- → So, it has four outputs, one for each possible input binary number



#### **DECODERS**



- Decoders are called *n-to-m* line decoders, where m<=2<sup>n</sup>.
- A particular application of this decoder is:
   Binary-to-octal conversion;
  - inputs: binary representation and
  - outputs: its correspondence in octal representation.



#### 3-TO-8 LINE DECODER

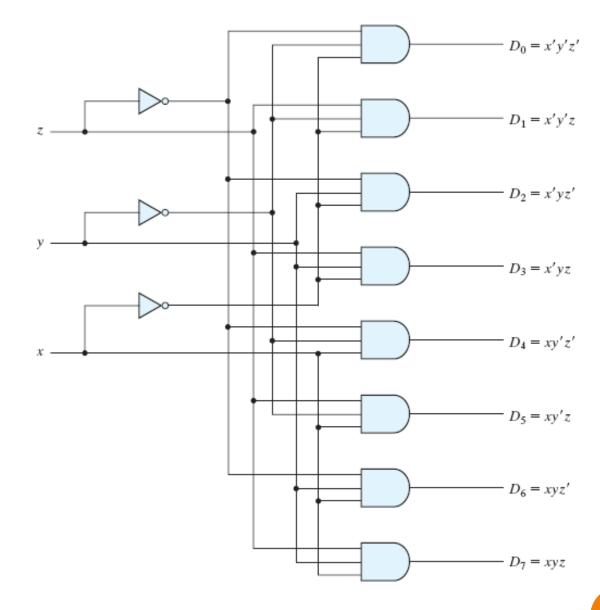
o 3 input variables =? outputs

$$\rightarrow$$
 2<sup>3</sup>=8 outputs

**Table 4.6** *Truth Table of a Three-to-Eight-Line Decoder* 

	Inputs	<u>.                                    </u>				Out	puts			
x	y	z	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	$D_3$	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	O	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

#### DECODERS

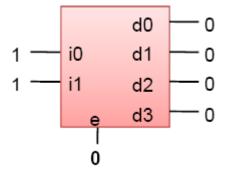


The output whose value is equal to 1 represents *the minterm* equivalent of the binary number currently available in the input lines

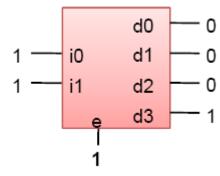
#### DECODER WITH ENABLE INPUT

#### Decoder with enable E

- if E=0, Outputs all 0



if E=1, Regular behavior



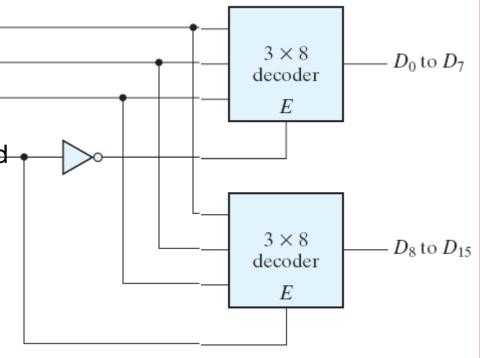
Е	i0	i1	d0	d1	d2	d3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1		1		
1	1	0			1	
1	1	1				1

How to use as a block

#### 4-TO-16 LINE DECODER

The 4-to-16 line decoder with x = 1 two 3-to-8 line decoder with x = 1 enable inputs

- When w=0,
  - the top decoder is enabled and the other is disabled
  - The bottom decoder outputs all 0's and the top eight outputs generate minterms 0000 to 0111
- When w=1,
  - the bottom decoder is enabled and the other is disabled
  - The top decoder outputs all 0's and the bottom eight outputs generate minterms 1000 to 1111

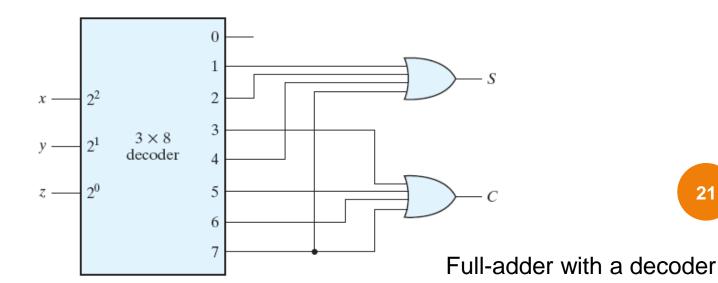


#### BOOLEAN FUNCTION IMPLEMENTATION

- Since any Boolean function can be expressed in sum of minterms form:
  - → A decoder with an external OR gate provides an implementation of the function
- Ex: Full-adder functions

$$S(x,y,z) = \Sigma(1,2,4,7)$$

$$C(x,y,z)=\Sigma(3,5,6,7)$$



#### **NOTES**

- A function with a long list of minterms requires an OR gate with large number of inputs
  - If the number of minterms >2<sup>n</sup>/2, then F 'can be expressed with fewer minterms
  - In this case, NOR gate is used. Since the sum is complemented and the normal output is generated

#### **ENCODERS**

- An encoder
  - It is a digital circuit that performs the inverse operation of a decoder
  - It has 2<sup>n</sup> inputs lines and n output lines
- An example of an encoder is:
  - Octal-to-binary conversion, it has:
    - o 8 inputs: the octal code and
    - 3 outputs: the corresponding binary number
- It is assumed that only one input has a value of 1 at any given time

y

X

Do

 $D_2$ 

 $D_3$ 

#### OCTAL TO BINARY ENCODER

**Table 4.7** *Truth Table of an Octal-to-Binary Encoder* 

Inpu	Inputs							Out	puts	
D <sub>0</sub>	<i>D</i> <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

It can be implemented with 3 OR gates

$$z = D_1 + D_3 + D_5 + D_7$$
  
 $y = D_2 + D_3 + D_6 + D_7$   
 $x = D_4 + D_5 + D_6 + D_7$ 

But, it has some limitations

#### OCTAL TO BINARY ENCODER:

#### LIMITATIONS

- This encoder has some limitations:
- It is assumed that only one input can be active at any given time,
  - If 2 inputs are active simultaneously, the output produces an undefined combination
  - To resolve this → higher priority with higher subscript
- A output with all 0's is generated when all the input are 0;
  - But this output is the same as when D0 is equal to 1
  - To resolve this → one more output is used to indicate whether at least one input is equal to 1.

How to design? Know internal?

#### PRIORITY ENCODER

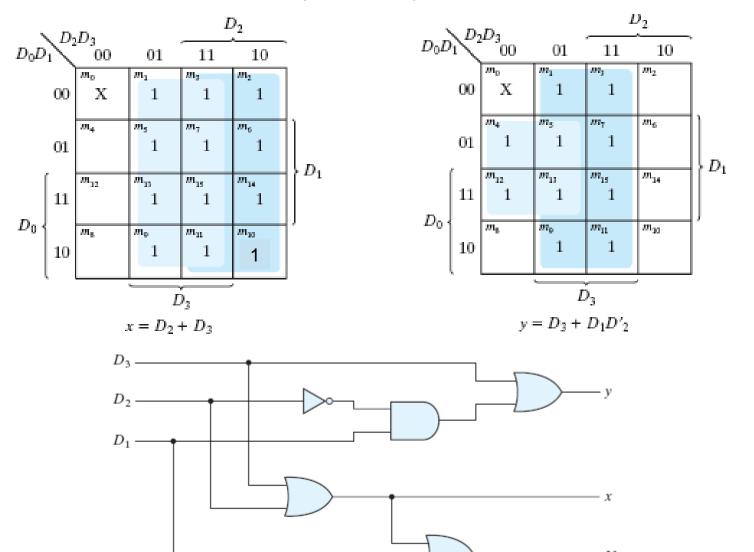
 A priority encoder is an encoder circuit that overcomes the limitations of octal-to-binary encoder previously implemented.

**Table 4.8** *Truth Table of a Priority Encoder* 

	Inputs				Output	s
D <sub>0</sub>	<b>D</b> <sub>1</sub>	D <sub>2</sub>	<b>D</b> <sub>3</sub>	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

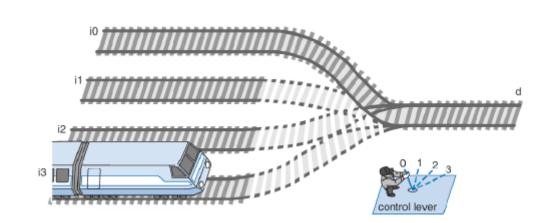
## PRIORITY ENCODER(CONT.)

 $D_0$ 



#### **M**ULTIPLEXERS

- A multiplexer (MUX) is a combinational circuit that
  - selects binary information from one of many input lines and
  - directs it to a single output line.
- It is also called a Data selector



- There are:
  - 2<sup>n</sup> input lines
  - n selection lines whose bit combinations determine which input is selected, and
  - Single output

#### TWO-TO-ONE MULTIPLEXER

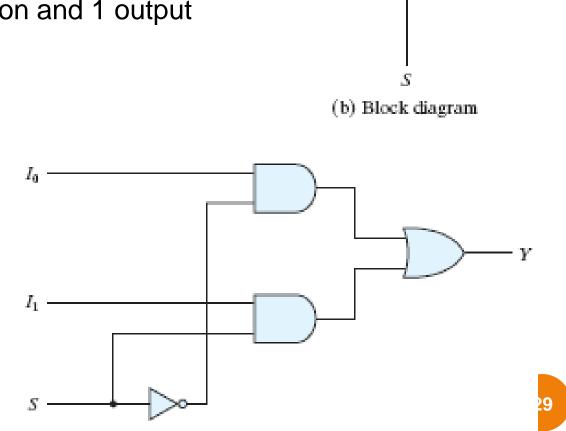
#### It has:

• 2 inputs, 1 selection and 1 output

S	Υ
0	I <sub>o</sub>
1	I <sub>1</sub>

$$Y = S'I_0 + SI_1$$

How to design? Know internal?



(a) Logic diagram

0

MUX

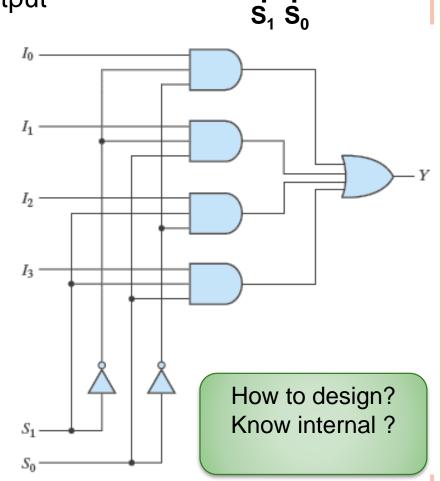
#### FOUR-TO-ONE MULTIPLEXER

#### It has:

• 4 inputs, 2 selection and 1 output

	$S_1$	$S_0$	Y
( ( 1 1	)	0 1 0 1	$I_0 \\ I_1 \\ I_2 \\ I_3$

$$Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$$



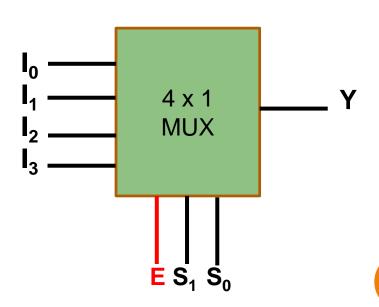
4 x 1

**MUX** 

#### MULTIPLEXER WITH ENABLE INPUT

- As decoder, multiplexer may have an enable input:
  - When E=0, the outputs are disabled
  - When E=1, normal multiplexer

Е	S1	S0	Υ
0	X	X	All 0's
1	0	0	$I_0$
1	0	1	I <sub>1</sub>
1	1	0	$I_2$
1	1	1	$I_3$



#### QUADRUPLE 2-TO-1 LINE MULTIPLEXER

- The circuit has 4 MUXs,
  - Each MUX:
    - select one of two input lines: A<sub>0</sub> or B<sub>0</sub>
    - Output Y<sub>0</sub>
    - Selection line S selects one MUX from the 4 MUXs.
- It can be seen as a circuit that selects one of two 4-bit numbers
- The enable input E must be active for normal operation.

Ε	S	Output Y			
1 0 0	X 0 1	all 0's select A select B			
Function table					

## QUADRUPLE 2-TO-1 LINE MULTIPLEXER

(CONT.)

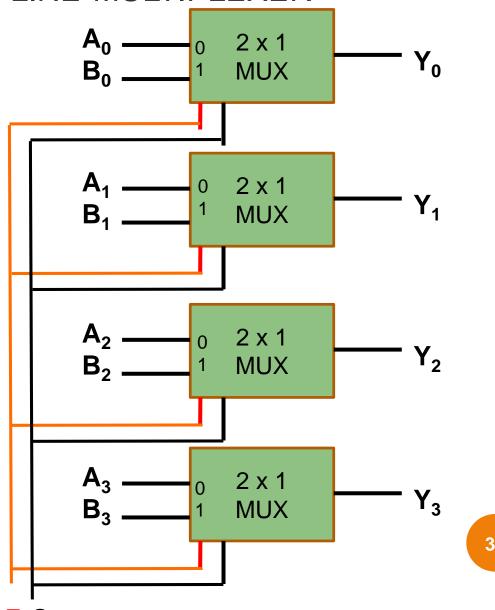
The unit is enabled when E=0

If S=0, the four A inputs have a path to the four outputs

If S=1, the four B inputs have a path to the four outputs

 When E=1, the outputs are all 0's regardless the value of S

Ε	S	Output $Y$
1	X	all 0's
0	0	select A
0	1	select B

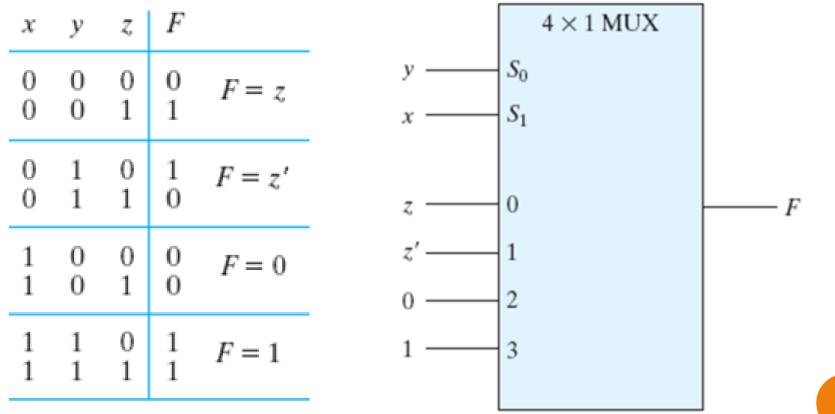


# ection 4.11

#### **BOOLEAN FUNCTION IMPLEMENTATION**

• Example 1:

$$F(x,y,z)=\Sigma(1,2,6,7)$$



The first n-1 variables are applied to selection inputs and we evaluate the output as a function of the last variable

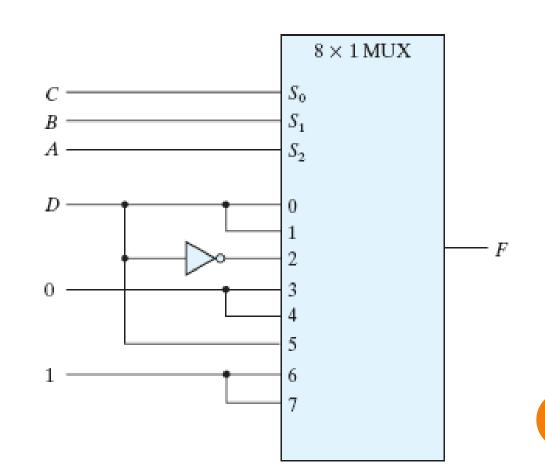
## BOOLEAN FUNCTION IMPLEMENTATION (CONT.)

How to use as a block

6

• Example2: F(A, B, C, D)=Σ(1,3,4,11,12,13,14,15)

A	B	C	D	F	
0	0	0	0	0	F = D
0	0	0	1	1	
0	0	1	0	0	F = D
0	0	1	1	1	
0	1	0	0	1	F = D'
0	1	0	1	0	
0 0	1 1	1 1	0 1	0	F = 0
1	0	0	0	0	F = 0
1	0	0	1	0	
1	0	1	0	0	F = D
1	0	1	1	1	
1 1	1 1	0 0	$0 \\ 1$	1 1	F = 1
1	1	1	0	1	F = 1
1	1	1	1	1	



#### MULTIPLEXER WITH A DECODER

- A 2<sup>n</sup>-to-1 line multiplexer is constructed from:
  - An n-to-2<sup>n</sup> decoder
  - AND gate for each 2<sup>n</sup> input lines
  - An OR gate

try to solve it?

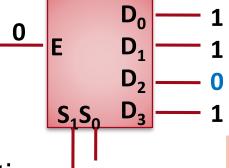
DEMULTIPLEXER
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E	A	B	$D_0$	$D_1$	$D_2$	$D_3$
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Demultiplixer is

A circuit that receives information from a single line and directs it to one of 2n output lines.

- Fig: 4.19
- The decoder with enable input can function as a demultiplexer.
- The decoder in fig. 4.9 can function as 1-to-4 line demultiplexer, when:
  - E is taken as data input
  - A and B as selection inputs
- Because decoder and demultiplexer operations to 10 obtained from the same circuit, a decoder with enable input is referred to as a decoder-demultiplexer



#### **THANKS**

We covered from:

Ch.4 (sec. 4.9→4.11)

Skip: three- state gates in sec. 4.11

Next lecture: Sequential circuits (latch & flip-flop)

