



CS 221 LOGIC DESIGN

Fall 2021

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SYNCHRONOUS SEQUENTIAL LOGIC ANALYSIS & DESIGN

Lecture 8

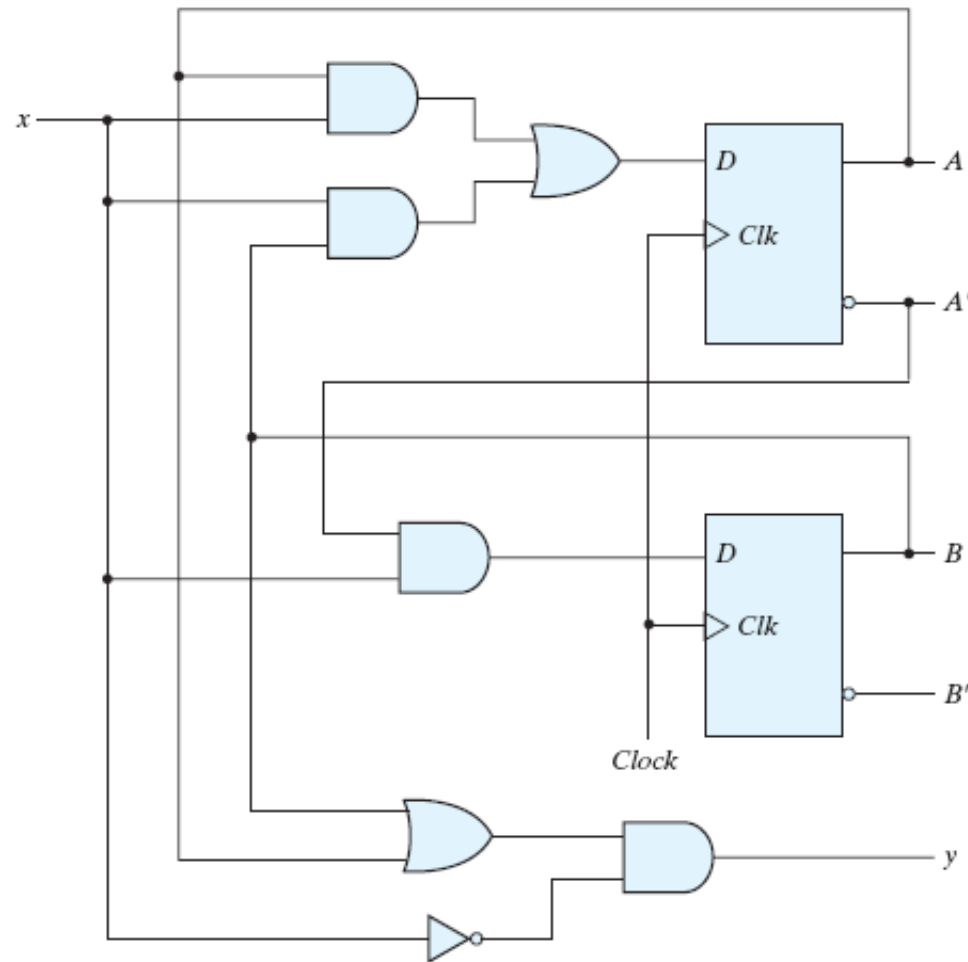
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ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS

- Analysis of clocked sequential circuits
 - ➔ describes what a given circuit will do under certain operating conditions
- Behavior of clocked sequential circuit
 - ➔ is determined from the inputs, the outputs, and the state of its flip-flops (present state)
- The analysis of a sequential circuits consists of obtaining:
 - **State table** (*transition table*) or
 - **State diagram**
- It is also possible to write Boolean expressions that describe the behavior of the sequential circuit ➔ **state equations**

STATE EQUATIONS

- The sequential circuit consists of:
 - Two D flip-flops (A and B)
 - An input x
 - An output y
- Determine next state of D flip-flops:
 - $A(t+1) = A(t)x(t) + B(t)x(t)$
 - $B(t+1) = A'(t)x(t)$
- The present state of the output y :
 - $y(t) = [A(t) + B(t)]x'(t)$



State equation

specifies the next state as a function of the present state and inputs

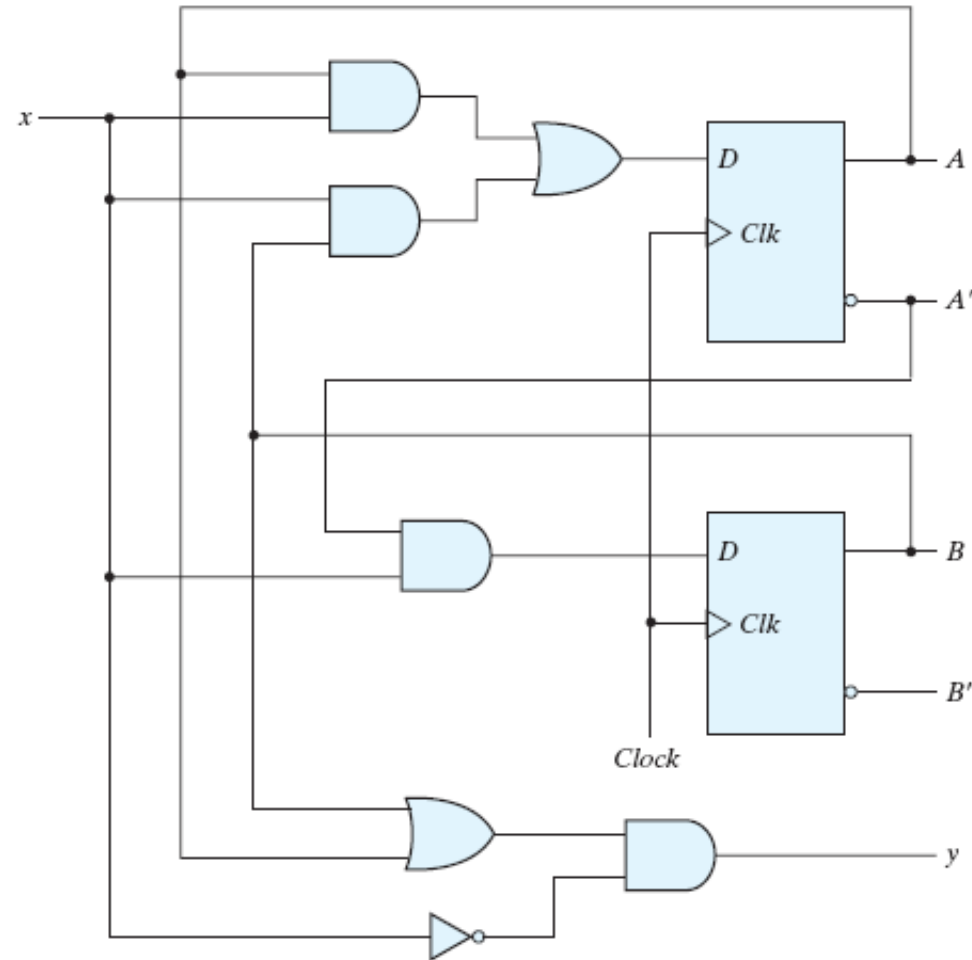
STATE TABLE

○ The state equations:

- $A(t+1) = Ax + Bx$
- $B(t+1) = A'x$
- $y = (A+B)x'$

Table 5.2
State Table for the Circuit of Fig. 5.15

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0



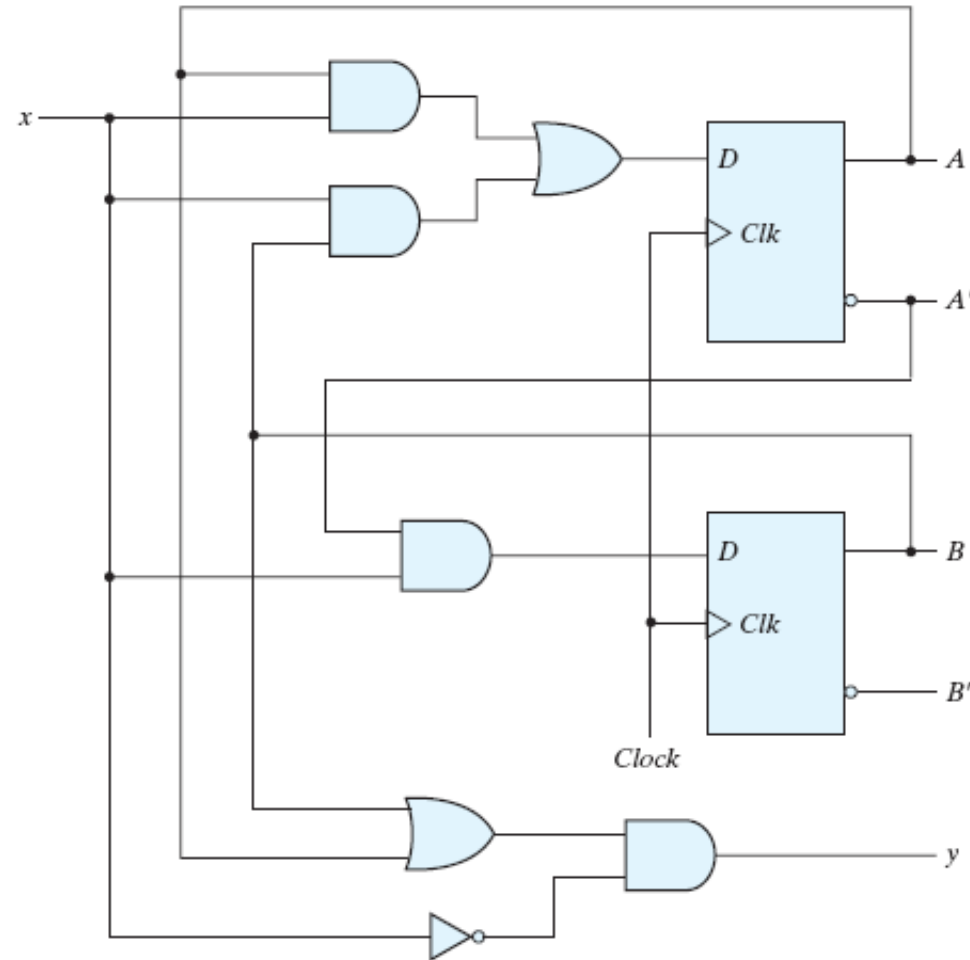
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Present State		Input x	Next State		Output y
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0



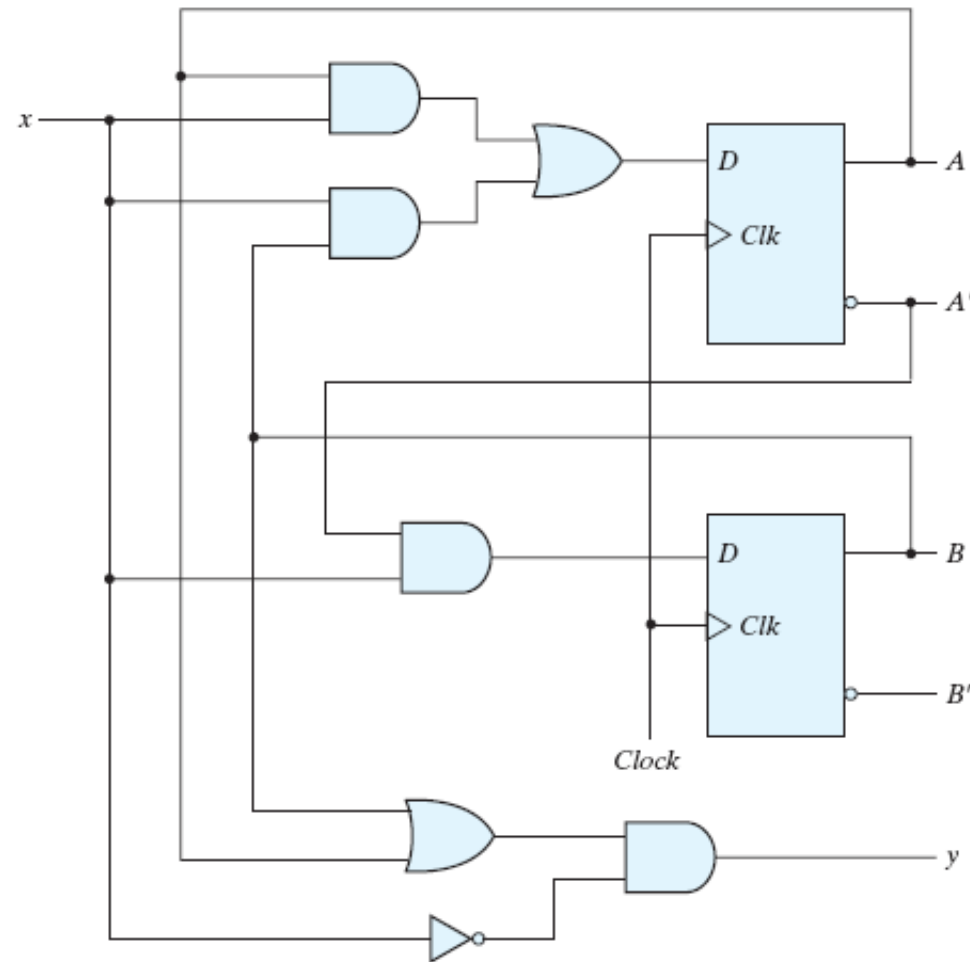
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0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0



TWO FORMS OF STATE TABLE

Table 5.2

State Table for the Circuit of Fig. 5.15

Present State		Input	Next State		Output
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Table 5.3

Second Form of the State Table

Present State		Next State				Output	
		x = 0		x = 1		x = 0	x = 1
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

○ The state equations:

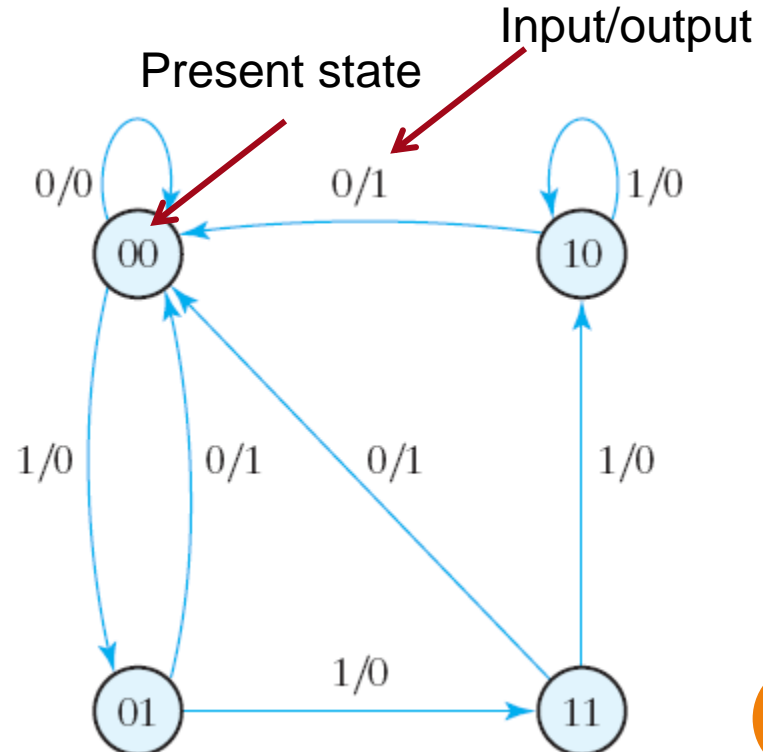
- $A(t+1) = Ax + Bx$
- $B(t+1) = A'x$
- $y = (A+B)x'$

STATE DIAGRAM

- The information available in a state table can be represented graphically in the form of a state diagram

Table 5.3
Second Form of the State Table

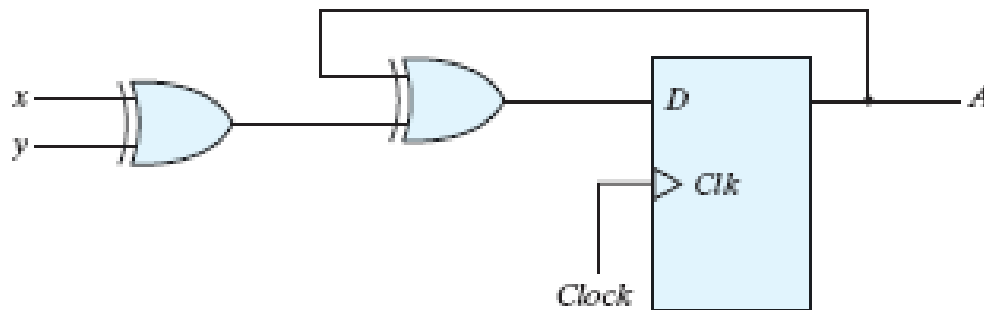
Present State		Next State				Output	
		$x = 0$		$x = 1$		$x = 0$	$x = 1$
A	B	A	B	A	B	y	y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0



ANALYSIS WITH D FLIP-FLOPS

- Input equation:

$$D_A = A \oplus x \oplus y$$

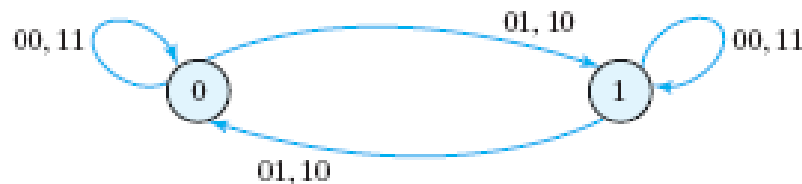


(a) Circuit diagram

XOR with 3 inputs
= **odd function**

Present state	Inputs		Next state
A	x	y	A
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table



(c) State diagram

FLIP-FLOP EQUATIONS

- **Output equations:**

- A set of Boolean functions describes the part of the combinational circuit that generates external outputs

- **Flip-flop Input equations (excitation equations):**

- A set of Boolean functions describes the part of the circuit that generates the inputs to the flip-flops

- Ex: $D_Q = x + y$

- The following input equation specifies an OR gate with inputs x and y connected to D input of a flip-flop whose output is labeled with the symbol Q

- Previous example (fig. 5.15)

- $D_A = Ax + Bx$
- $D_B = A'x$
- $y = (A+B)x'$



For D flip-flop, state equation = input equation

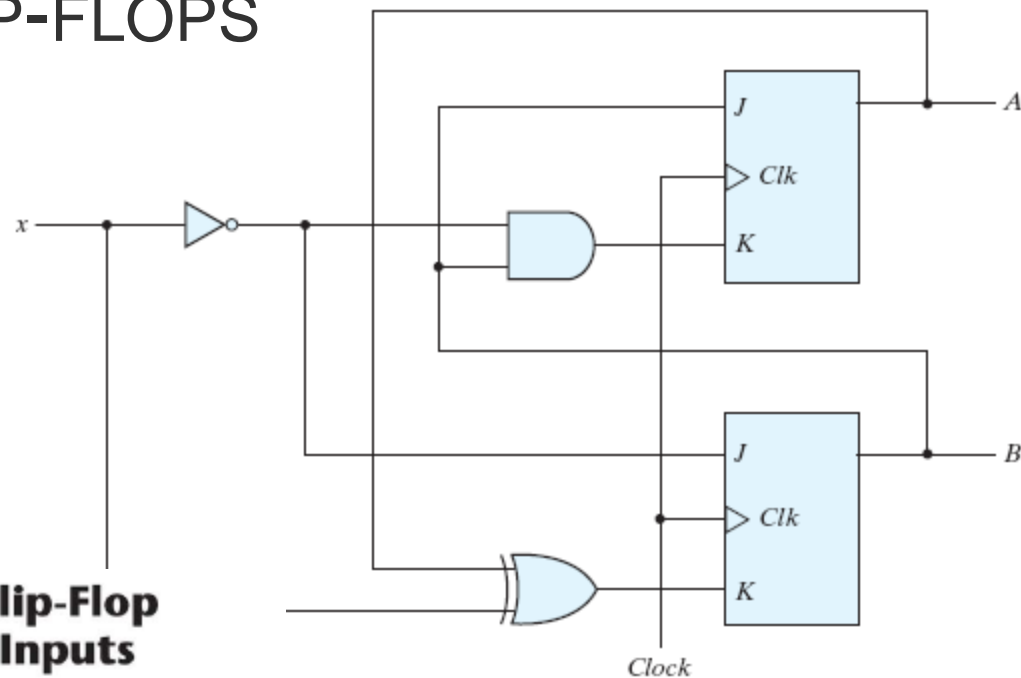
ANALYSIS WITH JK OR T FLIP-FLOPS

- When JK or T flip-flops are used, it is necessary to refer to the corresponding:
 - characteristic table or
 - characteristic equationto obtain the next-state values.

Method 1: Using Characteristic table

ANALYSIS WITH JK FLIP-FLOPS

- Determine input equations
 $J_A = B$, $K_A = Bx'$
 $J_B = x'$, $K_B = A'x + Ax' = A \oplus x$
- List binary values of each input equation
- Use characteristic table to determine the next state



Present State			Input		Next State		Flip-Flop Inputs			
A	B	x	A	B	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	1	0	0	1	0
0	0	1	0	0	0	0	0	0	0	1
0	1	0	1	1	1	1	1	1	1	0
0	1	1	1	0	1	0	1	0	0	1
1	0	0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0	0	0	0
1	1	0	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0

Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	$Q(t + 1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

Method 2: Using Characteristic eq.

ANALYSIS WITH JK FLIP-FLOPS

1. Determine input equations

$$J_A = B, K_A = Bx'$$

$$J_B = x', K_B = A'x + Ax' = A \oplus x$$

2. Substitute input equations into characteristic eq. to obtain state equations

$$A(t+1) = JA' + K'A$$

$$= BA' + (Bx')'A$$

$$= A'B + AB' + Ax$$

$$B(t+1) = JB' + K'B$$

$$= x'B' + (A \oplus x)'B$$

$$= B'x' + ABx + A'Bx'$$

3. Use characteristic state eq. to determine the next state values in state table

JK characteristic eq.

$$Q(t+1) = JQ' + K'Q$$

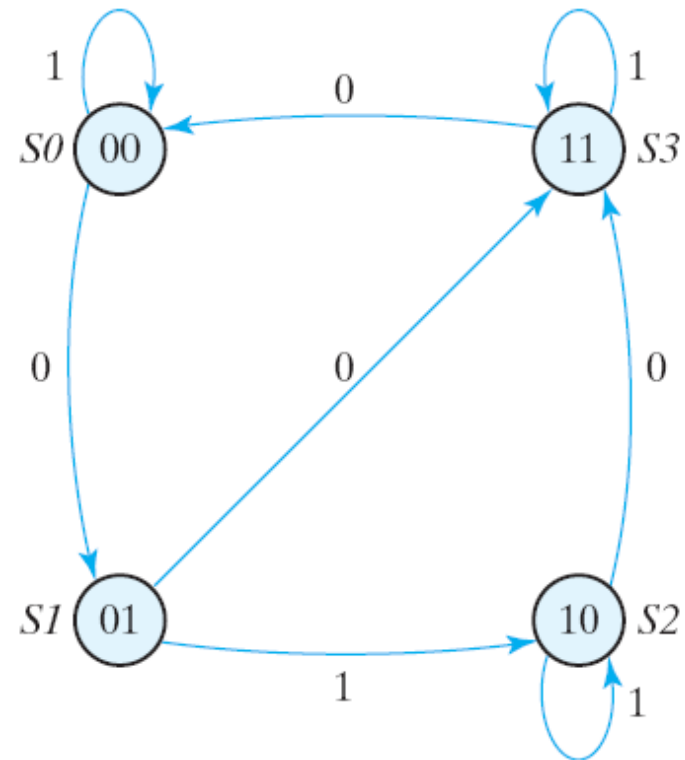
$$\rightarrow A(t+1) = JA' + K'A$$

$$\rightarrow B(t+1) = JB' + K'B$$

Present State		Input	Next State	
A	B		A	B
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

ANALYSIS WITH JK FLIP-FLOPS: STATE DIAGRAM

Present State		Input	Next State	
<i>A</i>	<i>B</i>		<i>A</i>	<i>B</i>
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1



T characteristic eq.
 $Q(t+1) = T \oplus Q = TQ' + T'Q$

ANALYSIS WITH T FLIP-FLOPS

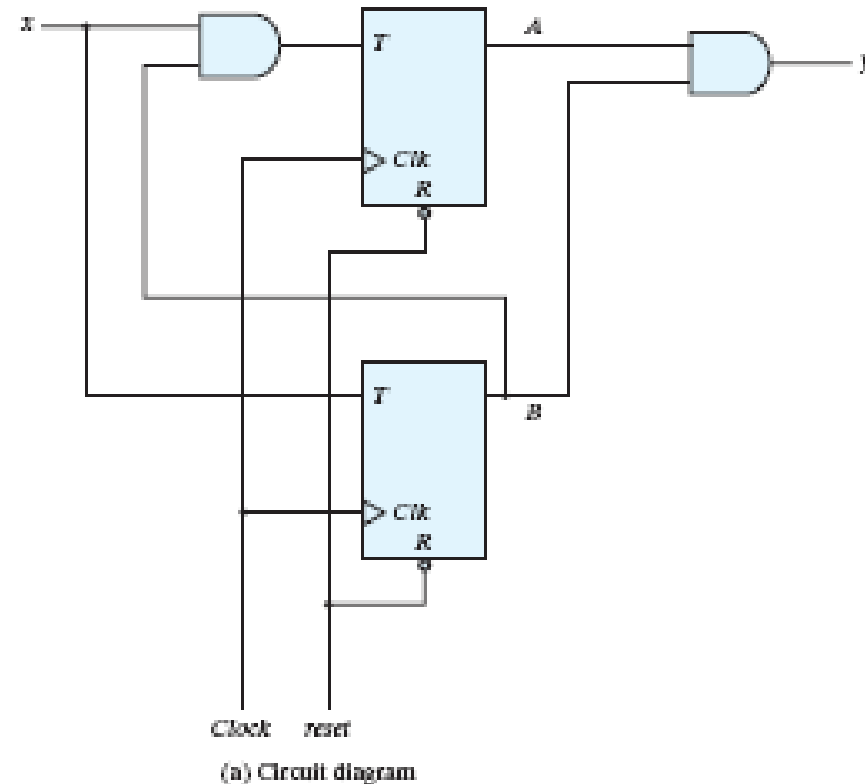
1. Determine input equations
 $T_A = Bx$, $T_B = x$, $y = AB$
2. Substitute input equations into characteristic eq. to obtain state equations

$$A(t+1) = T'A + TA'$$

$$= (Bx)'A + (Bx)A'$$

$$= AB' + Ax' + A'Bx$$

$$B(t+1) = x \oplus B$$
3. Use characteristic state eq. to determine the next state values in state table



ANALYSIS WITH T FLIP-FLOPS

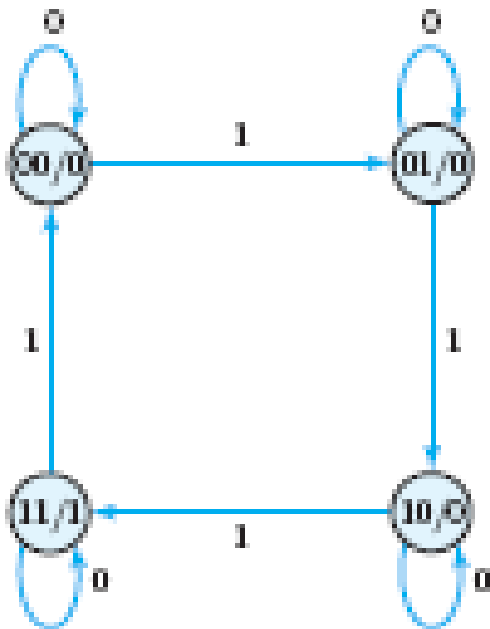
Next state equations:

$$A(t+1) = AB' + Ax' + A'Bx$$

$$B(t+1) = x \oplus B$$

State Table for Sequential Circuit with T Flip-Flops

Present State		Input x	Next State		Output y
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1



Notes:

- * As long as $x=1$, the circuit behaves as a *binary counter*
- * Here, the output depends on the present state only (**Moore model**) and independent of the input
 → inside each circle (present state/output)

THE DESIGN PROCEDURE

- ❑ Design procedure or methodologies specify hardware that will implement a desired behavior.
- ❑ Here, we will illustrate manual efforts for small circuits using D, JK and T flip-flops.

THE DESIGN PROCEDURE (CONT.)

- ❑ Procedure for designing synchronous sequential circuits:
 1. From word description and specifications, derive a state diagram for the circuit
 2. Reduce the number of states if necessary
 3. Assign binary values to the states
 4. Obtain the binary-coded state table
 5. Choose the type of flip-flops to be used
 6. Derive the simplified flip-flop input and output equations
 7. Draw the logic diagram

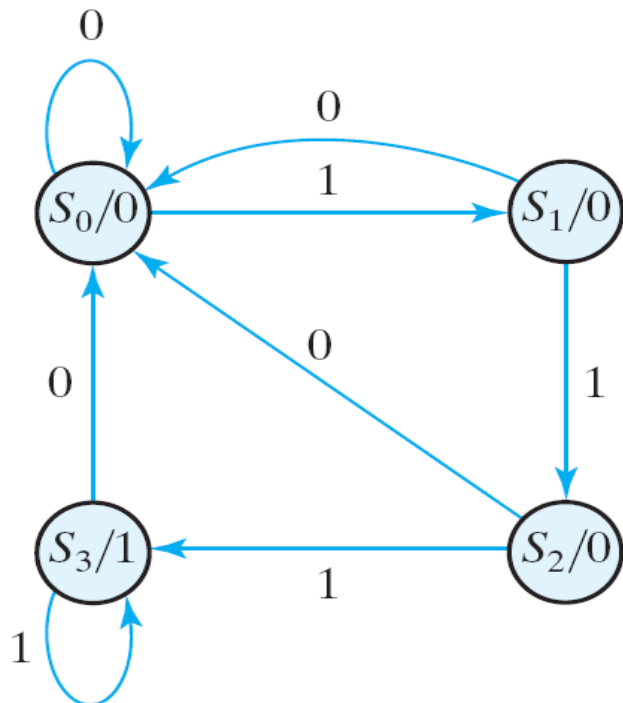
THE DESIGN PROCEDURE (CONT.)

- ❑ The part of the design that follows a well-defined procedure is referred to as *synthesis*
- ❑ Designers using logic synthesis tools (software) can follow a simplified process that develops an HDL description directly from state diagram
- ❑ The first step is a critical part of the process, because succeeding steps depend on it.

SEQUENCE DETECTOR EXAMPLE

□ Circuit's word description :

We wish to design a circuit that detects a sequence of 3 or more consecutive 1's in a string of bits coming through an input line



Input:

serial bit stream

Output:

$Y = 1$,

when 3 or more consecutive 1's are coming

$Y = 0$,

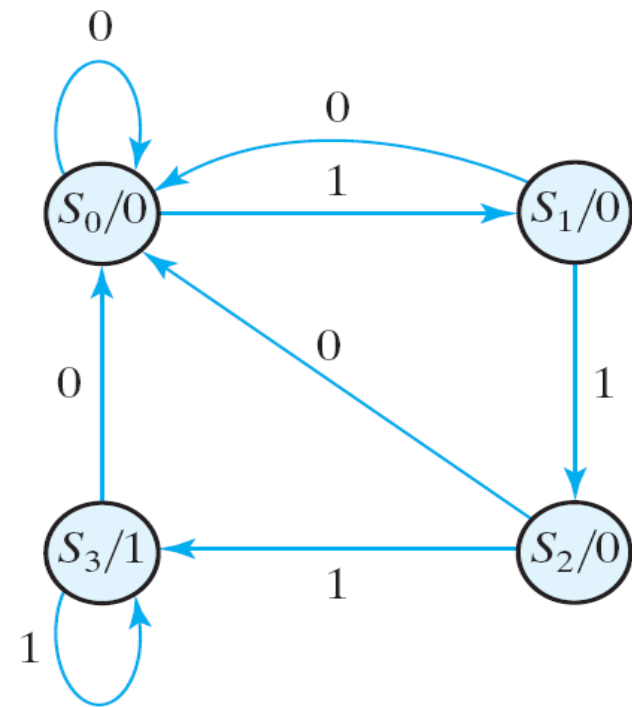
otherwise

→ No. of states=?

→ Moore Model

SEQUENCE DETECTOR EXAMPLE (CONT.)

- Synthesis using D flip-flop
- 3. Assign binary codes to the states
 $S_0=00$, $S_1=01$, $S_2=10$, $S_3=11$
- 4. Obtain the binary coded state table



Present State		Input x	Next State		Output y
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

- 5. Choose the type of flip-flops to be used
 - 2 D flip-flop
 - $Q(t+1) = D_Q$
 - Next state values specify the D input equations

SEQUENCE DETECTOR

EXAMPLE (CONT.)

- Synthesis using D flip-flop
- 6. Simplify the input and output eq.

$$A(t+1) = D_A(A, B, x) = \Sigma(3,5,7)$$

$$B(t+1) = D_B(A, B, x) = \Sigma(1,5,7)$$

$$y(A, B, x) = \Sigma(6,7)$$

Next State		Output
A	B	y
0	0	0
0	1	0
0	0	0
1	0	0
0	0	0
1	1	0
0	0	1
1	1	1

A	Bx		B	
	00	01	11	10
0	m ₀	m ₁	m ₃	m ₂
1	m ₄	m ₅	m ₇	m ₆

$$D_A = Ax + Bx$$

A	Bx		B	
	00	01	11	10
0	m ₀	m ₁	m ₃	m ₂
1	m ₄	m ₅	m ₇	m ₆

$$D_B = Ax + B'x$$

A	Bx		B	
	00	01	11	10
0	m ₀	m ₁	m ₃	m ₂
1	m ₄	m ₅	m ₇	m ₆

$$y = AB$$

SEQUENCE DETECTOR EXAMPLE (CONT.)

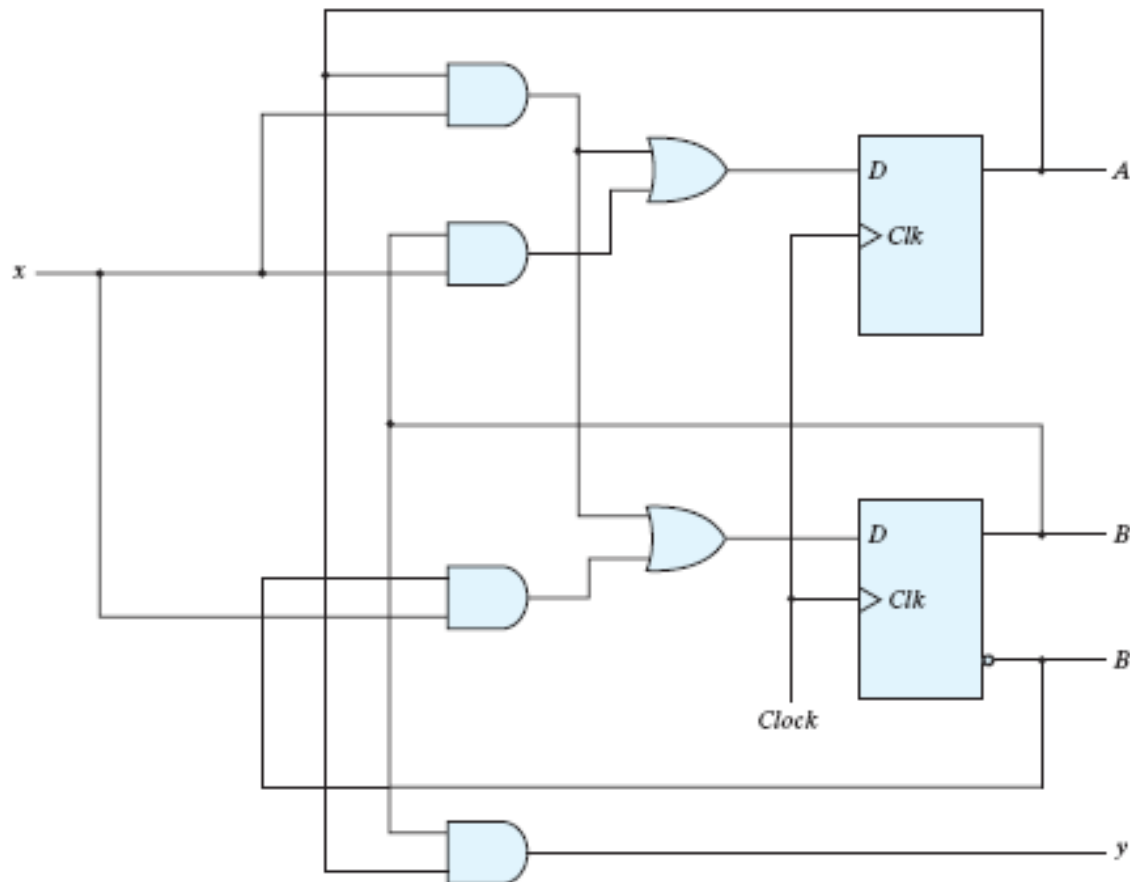
- Synthesis using D flip-flop
- 7. Draw the logic diagram

Input and output eq.:

$$D_A(A, B, x) = Ax + Bx$$

$$D_B(A, B, x) = Ax + B'x$$

$$y(A, B, x) = AB$$



الذين لم يمتحنوا امتحان الميترم

○ على الطلاب الاتى اسماءهم الحضور يوم الخميس 9 ديسمبر لمكتبى (فى الدور الثالث) الساعة 12 لاعادة امتحان الميترم:

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THANKS