CS 221
Logic Design

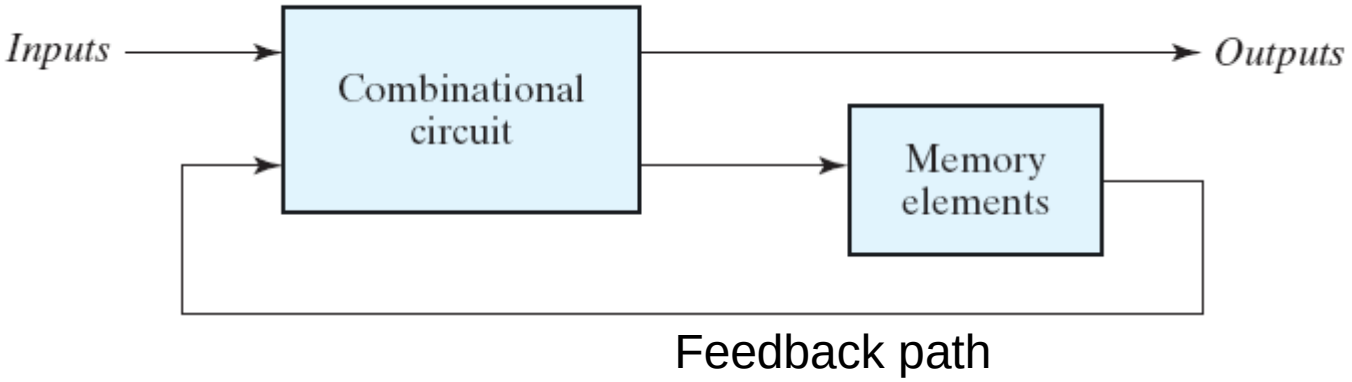
Fall 2021

By Wessam El-Behaidy & Salwa Osama

Synchronous sequential logic

Lecture 7

SEQUENTIAL CIRCUIT



- *The state* of sequential circuit defined by:
  - The binary information stored in memory elements at any given time
- The outputs in a sequential circuit is a function of:
  - Inputs
  - Present state

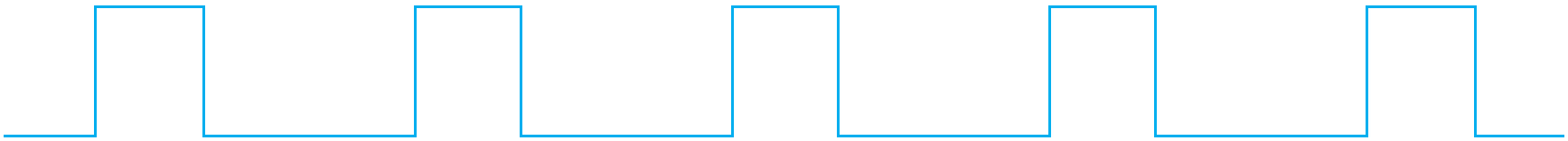
Main types of sequential circuits

- Synchronous sequential circuit
- Asynchronous sequential circuit

SYNCHRONOUS SEQUENTIAL CIRCUITS

- Synchronous circuit that use clock pulses to control storage elements

- ***Master clock generator***
  - It supplies a continuous train of clock pulses
  - The pulses are applied to all flip-flops and registers in the system

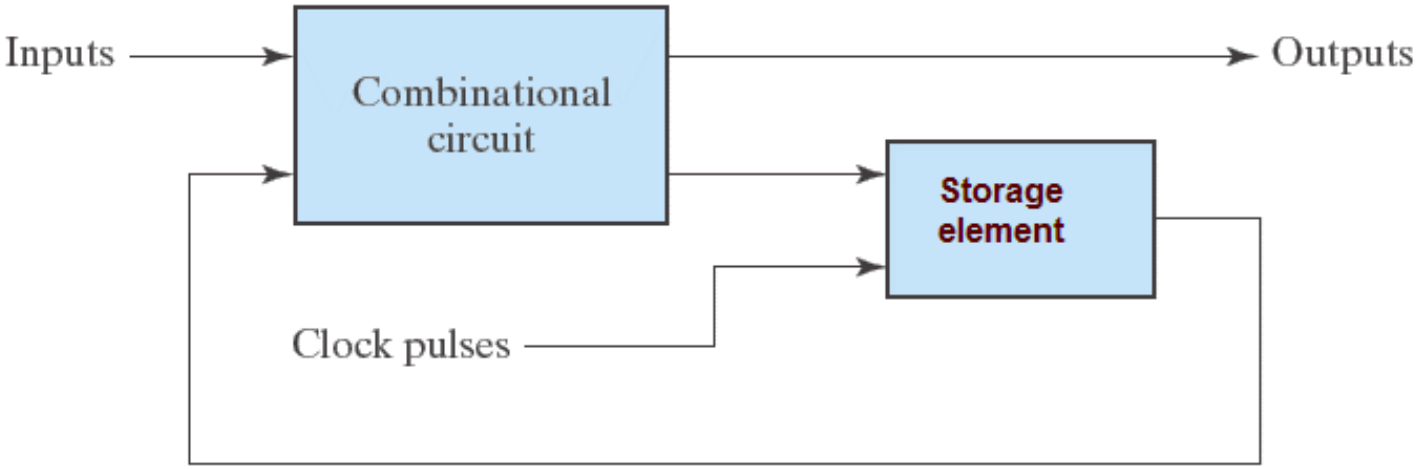


(b) Timing diagram of clock pulses

CLOCKED SEQUENTIAL CIRCUITS

- Synchronous sequential circuit that use clock pulses to control storage elements is called ***clocked sequential circuits***
- Also called ***Synchronous circuit***, because updating in storage element is synchronized to the occurrence of clock pulses

Synchronous clocked sequential circuit



(a) Block diagram

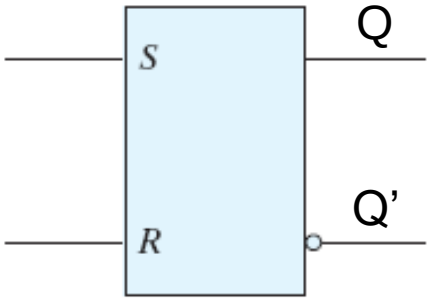
(b) Timing diagram of clock pulses

Storage elements

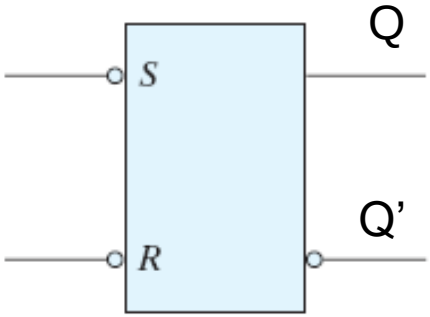
- Various types:
  - ***Latches:*** operate with signal level
  - ***Flip-flops:*** controlled by a clock transition
- They differ in :
  - the number of inputs they possess and
  - The manner in which the inputs affect the binary state
- Latches are the basic circuits from which the flip-flops are constructed

Q=1 ➔ set state Q=0 ➔Reset state

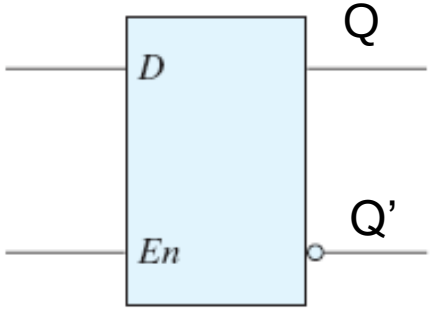
GRAPHIC SYMBOLS FOR LATCHES



SR



$\overline{S}\overline{R}$



D

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after S
0	1	0	1	
0	0	0	1	(after S
1	1	0	0	(forbidd

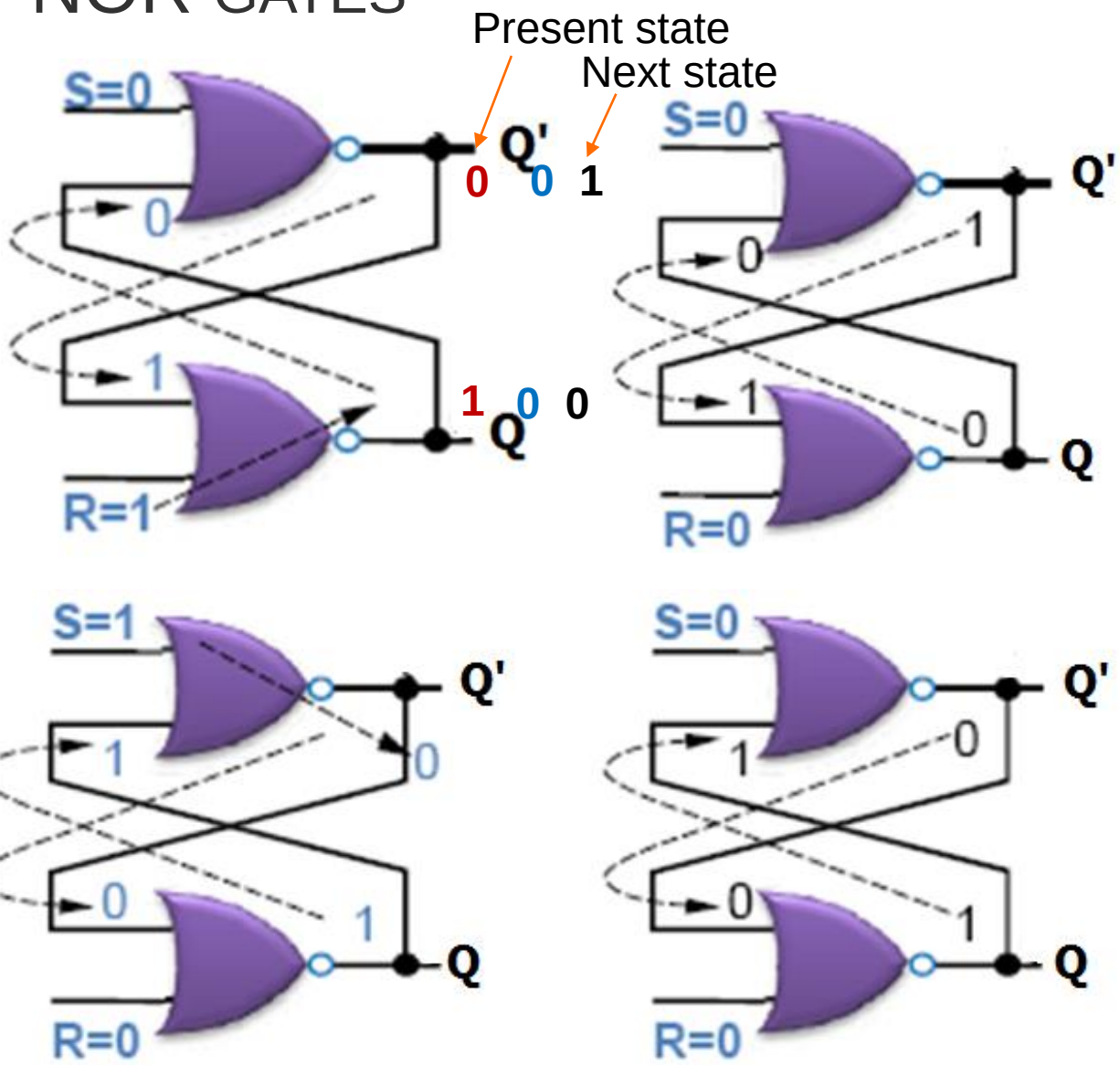
(b) Function table

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after S
0	1	1	0	
1	1	1	0	(after S
0	0	1	1	(forbidden)

(b) Function table

En	D	Next state of Q
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

SR LATCH WITH TWO CROSSED-COUPLED NOR GATES



S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table

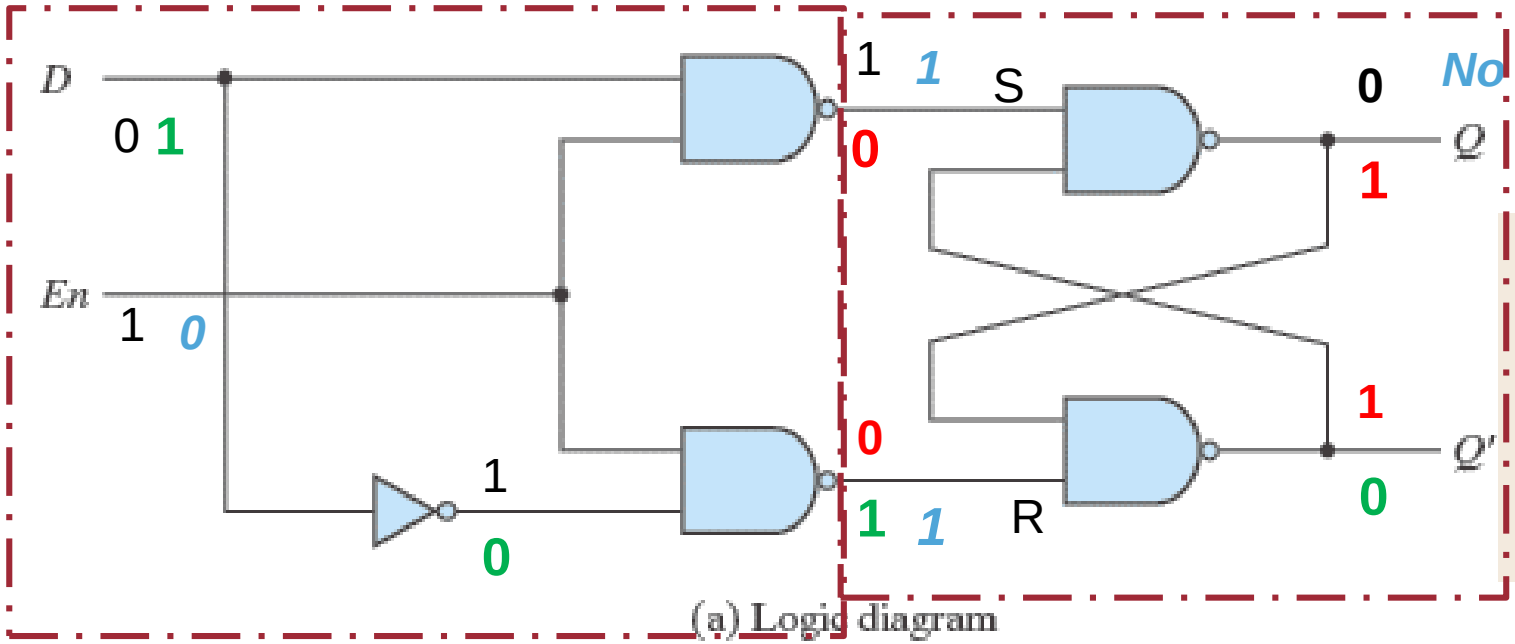
NOR: (x+1)'=0
(0+0)'=1

NAND: (x.0)'=1
(x.1)'=x'

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D LATCH (TRANSPARENT LATCH)

- To eliminate the undesirable condition in SR latch



(a) Logic diagram

S'R' latch
Cross-coupled
NAND gate
S=1,R=0,Q_{t+1}=0
S=0, R=1,Q_{t+1}=1
S=R=1,Q_{t+1}=Q

Control input

En	D	Next state of Q
0	X	No change
1	0	Q = 0; reset state
1	1	Q = 1; set state

TRIGGER

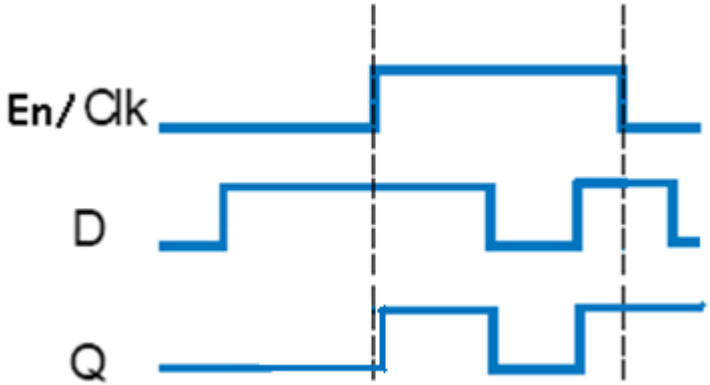
- The state of a latch or flip-flop is switched by a change in the control input, this momentary change is called a *trigger.*

D LATCH TRIGGER

- *The D latch* with pulses in the control input is triggered every time the pulse goes to the logic 1.

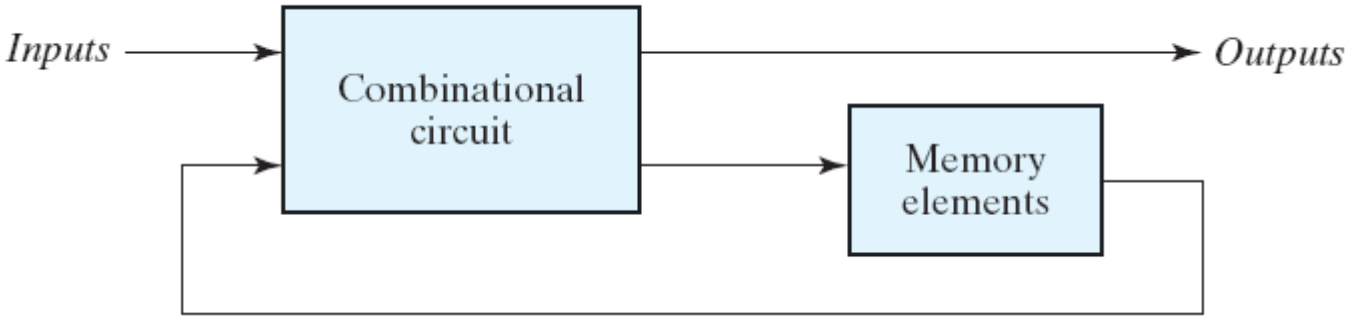
(a) Response to positive level

As long as the pulse input remains at this level, any changes in the data input will change the output and the state of the latch.



En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

LATCH PROBLEM



- When latches are used for storage element,
  - If the inputs applied to the latches change while the clock pulse is still at logic-1 level
  - The latches will respond to the new values and a new output state may occur
- The result is an unpredictable situation,

  ➔ the flip-flops are used

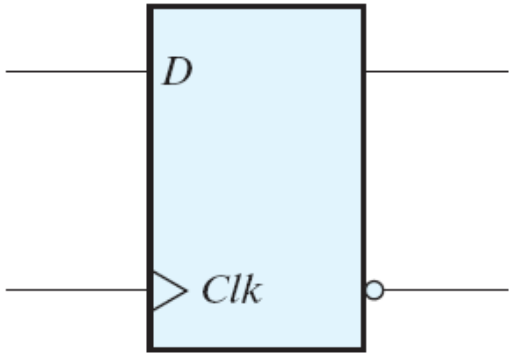
FLIP-FLOP TRIGGER

- The problem with the latch is that respond to a change in the *level* of a clock pulse
- The key to the proper operation of a flip-flop is to trigger it only during a signal *transition*

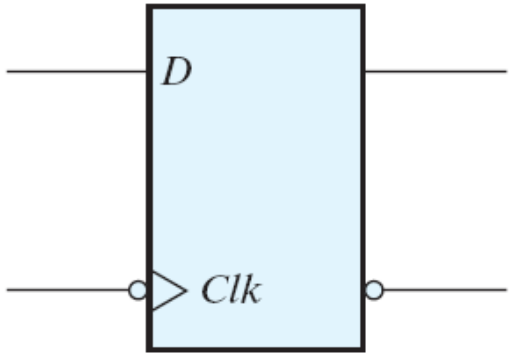
(b) Positive-edge response

(c) Negative-edge response

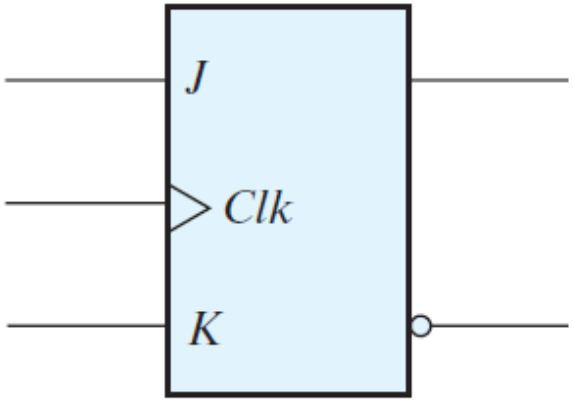
FLIP-FLOPS



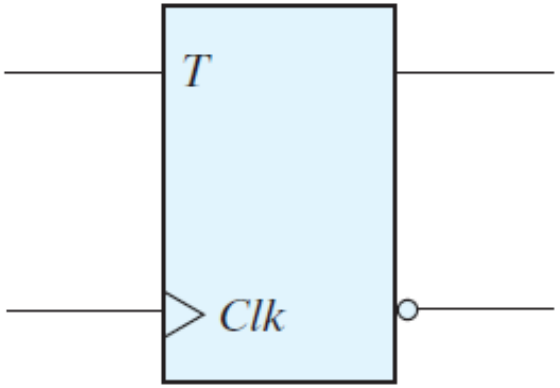
D flip-flop with positive edge



D flip-flop with negative edge



JK flip-flop



T flip-flop

A FLIP-FLOP FROM A LATCH

- *There are 2 ways:*

1. **Master/slave edge triggered D flip-flop**

Employ 2 latches in a special configuration that:

1. isolates the output of the flip-flop
2. Prevents it to be affected while the input is changing

2. **It uses 3 latches:**

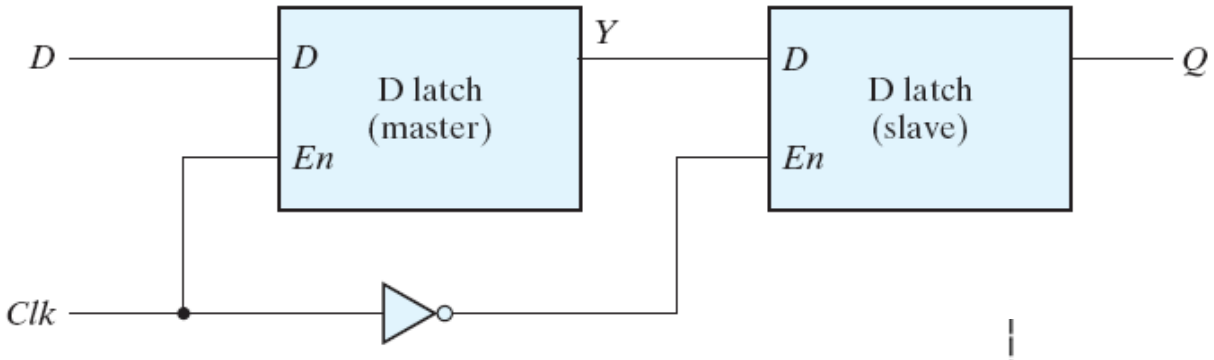
2 latches respond to the external D (data) and Clk (clock) and the 3rd provides the outputs for the flip-flop

1. triggers only during signal transition of synchronizing signal (clock)
2. Is disabled during the rest of the clock pulse

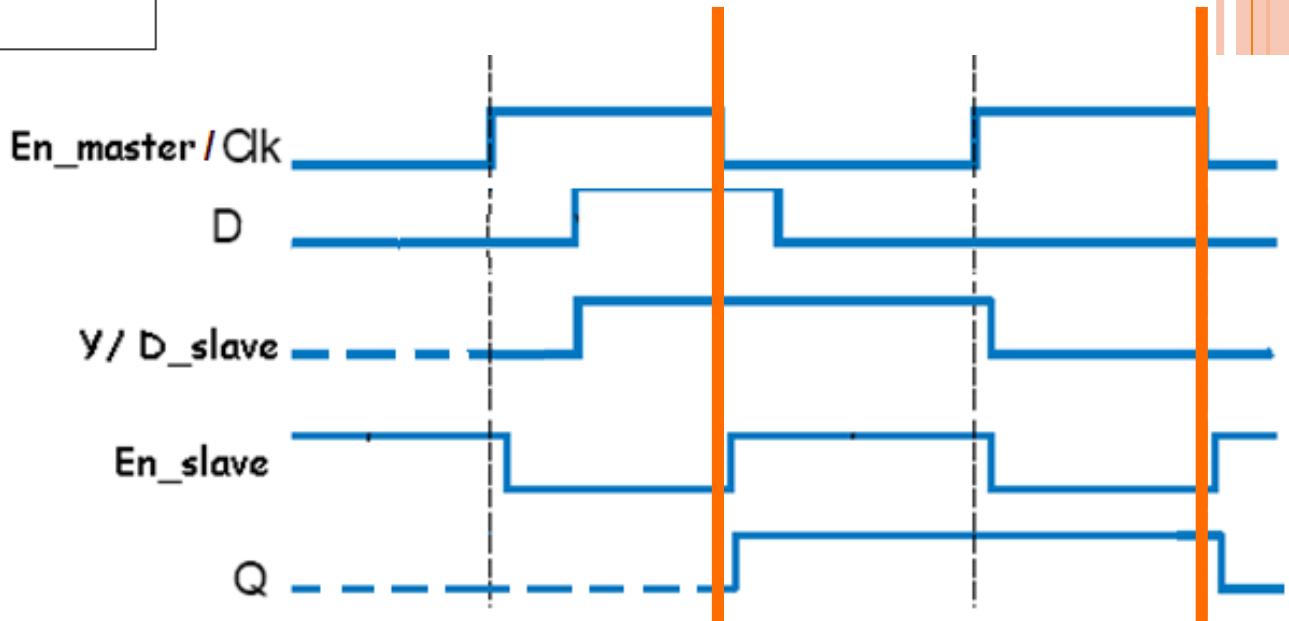
MASTER-SLAVE EDGE –TRIGGERED D FLIP-FLOP

- Constructed with 2 D latches and an inverter

  First latch: called ***master,*** Second latch: called ***slave***



En	*D*	Next state of Q
0	X	No change
1	0	$Q = 0$; reset stat
1	1	$Q = 1$; set state

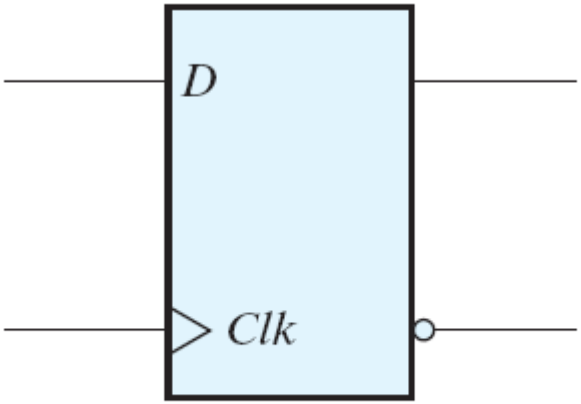


Behavior of master-slave flip-flop

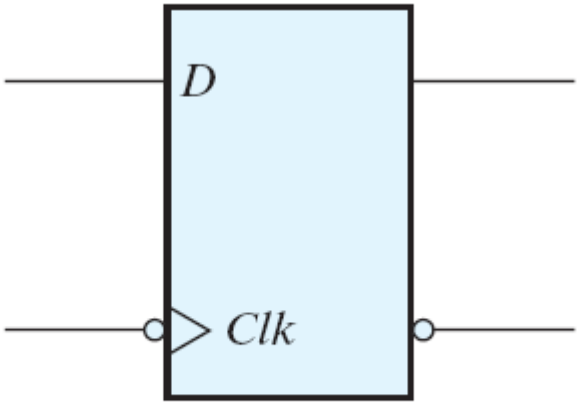
- Its behavior dictates that:
  - The output may change once
  - A change in the output is triggered by the **negative edge** of the clock
  - The change may occur only during the clock's negative level
- ***Note :***

  The value that is produced at the output is that value that as stored in the master stage immediately before the negative edge occurred
- Can we design the circuit to be triggered by positive edge?

Graphical symbol for edge-triggered D flip-flop



(a) Positive-edge



(a) Negative-edge

D Flop-flop characteristic table

D	Q(t + 1)	Next state
0	0	Reset
1	1	Set

JK FLIP-FLOP CHARACTERISTIC TABLE

J	K	Qt	Qt+1	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Table 5.1
Flip-Flop Characteristic Tables

JK Flip-Flop

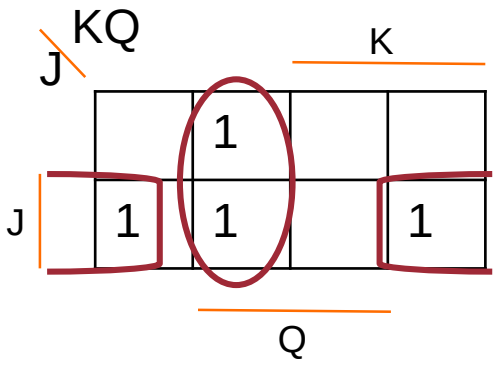
J	K	Q(t + 1)	
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q′(t)	Complement

Next state

Present state

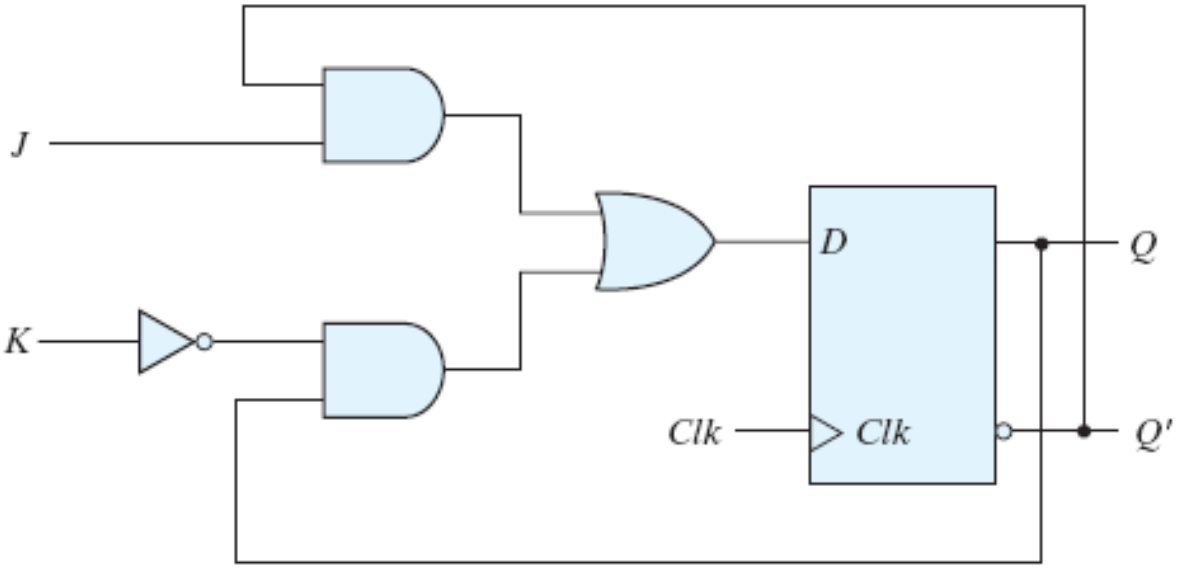
$D=Q(t+1)=JQ' + K'Q$

Design JK using D f/f

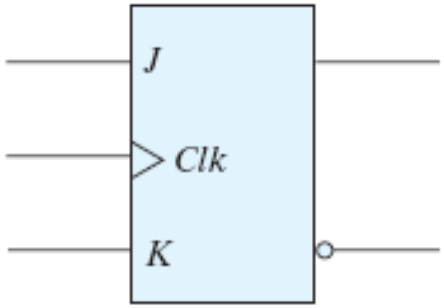


JK FLIP-FLOP FROM D FLIP-FLOP

- $Q(t+1)=JQ' + K'Q$



(a) Circuit diagram



(b) Graphic symbol

T FLIP-FLOP

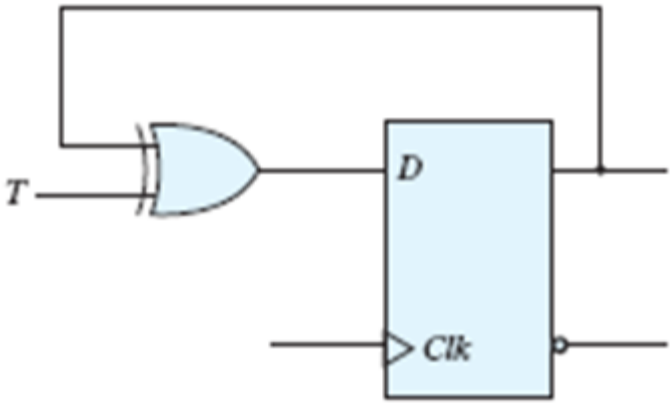
T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

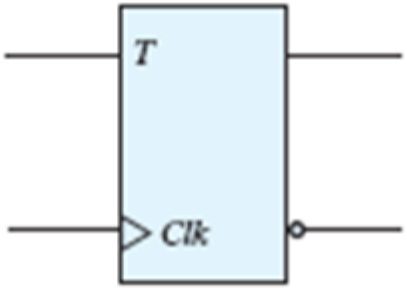
- *T* for *(toggle)* is a complementing flip-flop

$$D = T \oplus Q = TQ' + T'Q$$

- Used for designing binary counters



T flip-flop from D flip-flop



T flip-flop graphic symbol

T FLIP-FLOP FROM JK FLIP-FLOP

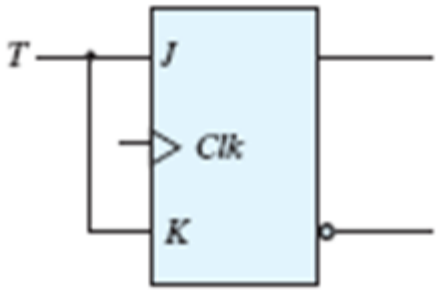
T	Qt	Qt+1	J	K
0	0	0	0	X
0	1	1	x	0
1	0	1	1	X
1	1	0	x	1

$J=T$

$K=T$

T Flip-Flop

T	Q(t + 1)	
0	Q(t)	No change
1	Q′(t)	Complement



(a) From *JK* flip-flop

Table 5.12
Flip-Flop Excitation Tables

Q(t)	Q(t = 1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(a) *JK*

Q(t)	Q(t = 1)	T
0	0	0
0	1	1
1	0	1
1	1	0

(b) *T*

CHARACTERISTIC EQUATIONS

The logical properties of a flip-flop, described in the characteristic table, can be expressed algebraically

- *D flip-flop*

  $Q(t+1)= D$

- *JK flip-flop*

  $Q(t+1)= JQ' + K'Q$

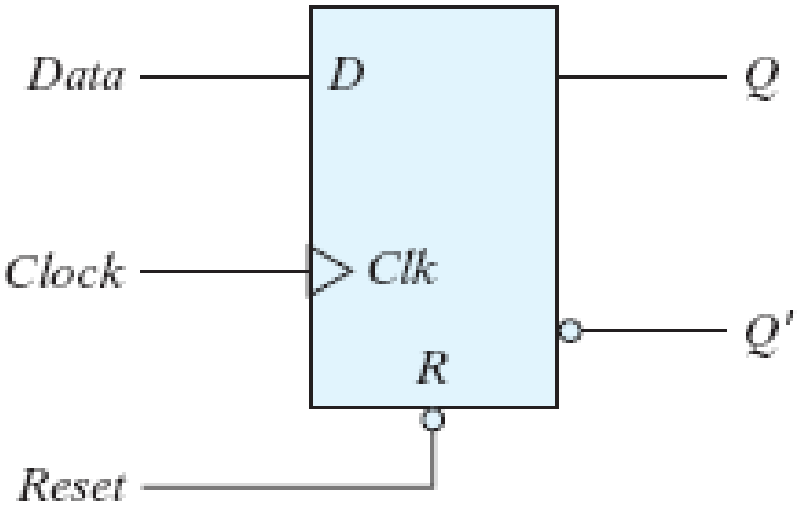
- *T flip-flop*

  $Q(t+1)= T \oplus Q = TQ' + T'Q$

Asynchronous Sequential circuit: Direct inputs

- Some flip-flops have asynchronous inputs that are used to force the flip-flop to a particular state **independently of the clock**
  - The input that set the flip flop to **1** is called ***preset*** or ***direct set***
  - The input that set the flip flop to **0** is called ***clear*** or ***direct reset***
- When power is turned on in a digital system, the state of the flip-flop is unknown
  - The direct inputs are useful for bringing all flip-flops to a known state prior the clocked operation

D-FLIP-FLOP WITH ASYNCHRONOUS RESET



(b) Graphic symbol

R	Clk	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table

Error in book

Quiz2

- Quiz2 on lect.5 to lect.6 will be next week.

Thanks

Next week: sequential circuits analysis and design