

VERDI Coverage Results

Hierarchy Modules Groups Asserts Statistics Tests																
Avg. Group Score:99.48% U+C:226 U:4 C:222 X:0 Avg. Group Inst. Score:99.48% U+C:226 U:4 C:222 X:0																
Group	Score	Instances	U+C	U	C	X	Goal	Weight	AtLeast	PerInst	Overlap	AutoBin	Missing	Comment		
Cg \$unit::alu_coverage:cg	99.48%		226	4	222	0	100%	1	1	0	1	64	64			
Cp clr	100.00%		2	0	2	0	100%	1	1		1	2				
Cp en_a	100.00%		2	0	2	0	100%	1	1		1	2				
Cp en_b	100.00%		2	0	2	0	100%	1	1		1	2				
Cp ina	100.00%		64	0	64	0	100%	1	1		1	64				
Cp inb	100.00%		64	0	64	0	100%	1	1		1	64				
Cp irq	100.00%		2	0	2	0	100%	1	1		1	2				
Cp opa	100.00%		4	0	4	0	100%	1	1		1	4				
Cp opb	100.00%		4	0	4	0	100%	1	1		1	4				
Cp out	93.75%		64	4	60	0	100%	1	1		1	64				
Cp rst	100.00%		2	0	2	0	100%	1	1		1	2				
Cn cg_cc	100.00%		8	0	8	0	100%	1	1				0			
Cn cg_cc_0	100.00%		8	0	8	0	100%	1	1				0			

Cover Groups					
Category	Total	Covered	Score	Uncovered	Excluded
Total Group Coverage Score			99.48%		
Total Group Coverage Instance S...			99.48%		
Cover Point	10	9	90.00%	1	0
Cover Point Bins	210	206	98.10%	4	0
Cover Cross	2	2	100.00%	0	0
Cover Cross Bins	16	16	100.00%	0	0
All Group Bins	226	222	98.23%	4	0
Group	1	0	0.00%	1	0
Group Instance Point					
Group Instance Point Bins					
Group Instance Cross					
Group Instance Cross Bins					
All Group Instance Bins					
Group Instance					

Name	Score	Line	Toggle	Branch
tb	96.24%	96.61%	98.57%	93.55%
dut	96.04%	96.00%	98.57%	93.55%
ifc	98.57%		98.57%	

Design Hierarchy

Metric	Total	Covered	Score	Uncovered	Excluded
Branch	31	29	93.55%	2	8
Toggle	140	138	98.57%	2	0
Line	59	57	96.61%	2	0
Total	230	224	97.39%	6	8
Average			96.24%		

Module List

Metric	Total	Covered	Score	Uncovered	Excluded
Bran...	31	29	93.55%	2	8
Toggle	140	138	98.57%	2	0
Line	59	57	96.61%	2	0
Total	230	224	97.39%	6	8
Aver...			96.24%		

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Modules

Groups

Asserts

Statistics

Tests

Name	Score	Line	Toggle	Branch
alu	96.04%	96.00%	98.57%	93.55%
tb_dut	96.04%	96.00%	98.57%	93.55%
alu_ifc	98.57%		98.57%	
tb	100.00%	100.00%		

CovSrc1: tb_dut

Uncovered

```

30  assert (alu_in_a != 8'hff ) else
31  $error("illegal input alu_in_a = 8'hff " );
32  assert (alu_in_b != 8'h03 ) else
33  $error("illegal input alu_in_b = 8'hff " );
34  alu_out<=(alu_in_a & alu_in_b);
35  if (alu_out==8'h00)
36  alu_irq<=1'b1;
37  if (alu_out==8'h00 && alu_irq_clr=
38  =1'b1)
39  alu_irq<=1'b1;
40  end
41  2'b10:begin
42  alu_out=alu_in_a | alu_in_b;
43  if (alu_out==8'hf8)
44  alu_irq<=1'b1;
45  if (alu_out==8'hf8 && alu_irq_clr=
46  =1'b1)
47  alu_irq<=1'b1;
48  end
49  2'b11:begin
50  alu_out=alu_in_a ^ alu_in_b;
51  if (alu_out==8'h83)
52  alu_irq<=1'b1;
53  if (alu_out==8'h83 && alu_irq_clr=
54  =1'b1)
55  alu_irq<=1'b1;
56  end
57  endcase
58  end
59  endmodule

```

CovDetail

Line

Toggle

FSM

Condition

Branch

Assert

Category	Coverage
Block	95.12%
Statement	96.00%

Status	Name	Line No.	Source
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Name	Score	Line	Toggle	Condition	Branch
tb	96.43%	98.28%	98.57%	88.89%	100.00%
dut	96.35%	97.96%	98.57%	88.89%	100.00%
ifc	98.57%		98.57%		