VHDL LAB2

Digital verification

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Table of Contents

DECODER

TEST CASES

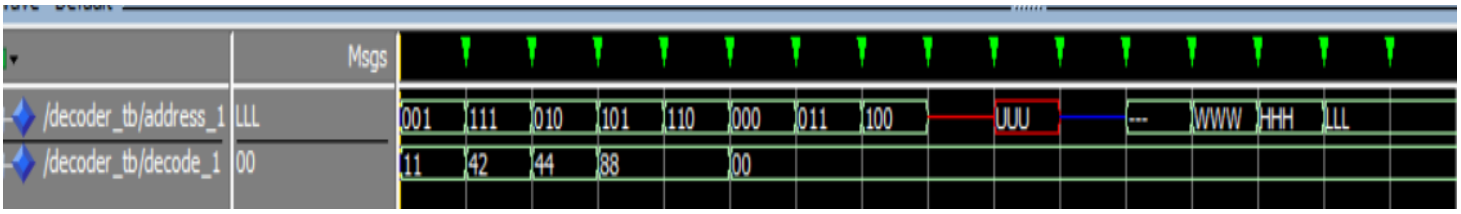
address	decode	
001	11	Normal case
111	42	Normal case
010	44	Normal case
101	88	Normal case
110	88	Normal case
000	00	Normal case
011	00	Normal case
100	00	Normal case
XXX	00	Corner case
ZZZ	00	Corner case
UUU	00	Corner case
---	00	Corner case
WWW	00	Corner case
HHH	00	Corner case
LLL	00	Corner case

SIMULATION RESULTS

```
VSIM 132> run
# ** Note:  PASSED: address=001,decode=11
#    Time: 20 ns  Iteration: 0  Instance: /decoder_tb
# ** Note:  PASSED: address=111,decode=42
#    Time: 40 ns  Iteration: 0  Instance: /decoder_tb
# ** Note:  PASSED: address=010,decode=44
#    Time: 60 ns  Iteration: 0  Instance: /decoder_tb
# ** Note:  PASSED: address=101,decode=88
#    Time: 80 ns  Iteration: 0  Instance: /decoder_tb
# ** Note:  PASSED: address=110,decode=88
#    Time: 100 ns  Iteration: 0  Instance: /decoder_tb

** Note:  PASSED: address=000,decode=00
   Time: 120 ns  Iteration: 0  Instance: /decoder_tb
** Note:  PASSED: address=011,decode=00
   Time: 140 ns  Iteration: 0  Instance: /decoder_tb
** Note:  PASSED: address=100,decode=00
   Time: 160 ns  Iteration: 0  Instance: /decoder_tb
** Note:  PASSED: address=XXX,decode=00
   Time: 180 ns  Iteration: 0  Instance: /decoder_tb
** Note:  PASSED: address=UUU,decode=00
   Time: 200 ns  Iteration: 0  Instance: /decoder_tb
```

```
** Note:  PASSED: address=ZZZ,decode=00
   Time: 220 ns  Iteration: 0  Instance: /decoder_tb
** Note:  PASSED: address=---,decode=00
   Time: 240 ns  Iteration: 0  Instance: /decoder_tb
** Note:  PASSED: address=www,decode=00
   Time: 260 ns  Iteration: 0  Instance: /decoder_tb
** Note:  PASSED: address=HHH,decode=00
   Time: 280 ns  Iteration: 0  Instance: /decoder_tb
** Note:  PASSED: address=LLL,decode=00
   Time: 300 ns  Iteration: 0  Instance: /decoder_tb
```

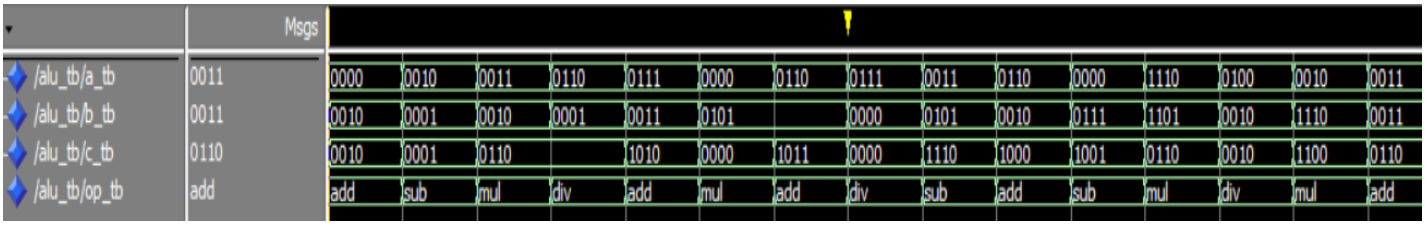


ALU

TEST CASES

operation	A (decimal)	B (decimal)	c (decimal)	
add	0000 (0)	0010 (2)	0010 (2)	Normal case
sub	0010 (2)	0001 (1)	0001 (1)	Normal case
mul	0011 (3)	0010 (2)	0001 error	Error injection
div	0110 (6)	0001 (1)	0110 (6)	Normal case
add	0111 (7)	0011 (3)	1010	Corner case
mul	0000	0101	0000	Corner case
add	0110	0101	1011	Normal case
div	0111	0000	Error	Error injection
sub	0011 (3)	0101(5)	1110 (-2)	Corner case
add	0110 (6)	0010 (2)	1000 (8)	Corner case
sub	0000 (0)	0111 (7)	1001 (-7)	Corner case
mul	1110 (-2)	1101 (-3)	0110 (6)	Corner case
div	0100 (4)	0010 (2)	0010 (2)	Normal case
div	0110(6)	1101(-3)	1110 (-2)	Corner case
mul	0010(2)	1110(-2)	1100(-4)	Corner case
add	0011(3)	0011(3)	0111 error	Error injection

SIMULATION RESULTS



alu_test_results - Notepad

File Edit Format View Help

```
. a = 0000, b = 0010, Expected c = 0010, Actual c = 0010. Test passed.
. a = 0010, b = 0001, Expected c = 0001, Actual c = 0001. Test passed.
. a = 0011, b = 0010, Expected c = 0001, Actual c = 0110. Test failed! Error message: failed in mul
. a = 0110, b = 0001, Expected c = 0110, Actual c = 0110. Test passed.
. a = 0111, b = 0011, Expected c = 1010, Actual c = 1010. Test passed.
. a = 0000, b = 0101, Expected c = 0000, Actual c = 0000. Test passed.
. a = 0110, b = 0101, Expected c = 1011, Actual c = 1011. Test passed.
. a = 0111, b = 0000, Expected c = 0111, Actual c = 0000. Test failed! Error message: failed in div
. a = 0011, b = 0101, Expected c = 1110, Actual c = 1110. Test passed.
. a = 0110, b = 0010, Expected c = 1000, Actual c = 1000. Test passed.
. a = 0000, b = 0111, Expected c = 1001, Actual c = 1001. Test passed.
. a = 1110, b = 1101, Expected c = 0110, Actual c = 0110. Test passed.
. a = 0100, b = 0010, Expected c = 0010, Actual c = 0010. Test passed.
. a = 0010, b = 1110, Expected c = 1100, Actual c = 1100. Test passed.
. a = 0011, b = 0011, Expected c = 0111, Actual c = 0110. Test failed! Error message: failed in add
```

Comparator

TEST CASES

a	b	equal_out	not_equal_out	
1111_0000	**1111_0000**	**1**	**0**	**corner_case**
0101_1011	0011_0101	0	1	normal_case
1111_1111	1111_0000	0	1	**corner_case**
0101_1011	0011_0101	0	1	normal_case
XXXX_XXXX	XXXX_XXXX	1	0	corner_case
UUUU_UUUU	UUUU_UUUU	1	0	corner_case
ZZZZ_ZZZZ	ZZZZ_ZZZZ	1	0	corner_case
HHHH_HHHH	HHHH_HHHH	1	0	corner_case
LLLL_LLLL	LLLL_LLLL	1	0	corner_case
WWWW_WWWW	WWWW_WWWW	1	0	corner_case
UUUU_XXXX	HHHH_UUUU	0	1	corner_case
----_----	----_----	1	0	corner_case
0111_0111	0011_1101	0	1	normal_case
1101_1011	1011_0101	0	1	normal_case
1100_0101	1100_0101	0	1	error_injection
0111_0111	0000_1101	1	0	error_injection
1101_1011	1011_0101	0	1	normal_case
1100_0101	1100_0101	1	0	normal_case
HHHH_HHHH	HHHH_HHHH	0	1	error_injection
LLLL_UUUU	WWWW_LLLL	1	0	error_injection

SIMULATION RESULTS

comparator_test_results - Notepad

File Edit Format View Help

```
. a = 11110000, b = 11110000, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 1, Actual not_equal_out = 0. Test passed.
. a = 01011011, b = 00110101, Expected equal_out = 0, Expected not_equal_out = 1, Actual equal_out = 0, Actual not_equal_out = 1. Test passed.
. a = 11111111, b = 11110000, Expected equal_out = 0, Expected not_equal_out = 1, Actual equal_out = 0, Actual not_equal_out = 1. Test passed.
. a = 01011011, b = 00110101, Expected equal_out = 0, Expected not_equal_out = 1, Actual equal_out = 0, Actual not_equal_out = 1. Test passed.
. a = XXXXXXXX, b = XXXXXXXX, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 1, Actual not_equal_out = 0. Test passed.
. a = UUUUUUUU, b = UUUUUUUU, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 1, Actual not_equal_out = 0. Test passed.
. a = ZZZZZZZZ, b = ZZZZZZZZ, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 1, Actual not_equal_out = 0. Test passed.
. a = HHHHHHHH, b = HHHHHHHH, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 1, Actual not_equal_out = 0. Test passed.
. a = LLLLLLLL, b = LLLLLLLL, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 1, Actual not_equal_out = 0. Test passed.
. a = WWWWWWWW, b = WWWWWWWW, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 1, Actual not_equal_out = 0. Test passed.
. a = UUUUXXXX, b = HHHHUUUU, Expected equal_out = 0, Expected not_equal_out = 1, Actual equal_out = 0, Actual not_equal_out = 1. Test passed.
. a = --------, b = --------, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 1, Actual not_equal_out = 0. Test passed.
. a = 01110111, b = 00111101, Expected equal_out = 0, Expected not_equal_out = 1, Actual equal_out = 0, Actual not_equal_out = 1. Test passed.
. a = 11011011, b = 10110101, Expected equal_out = 0, Expected not_equal_out = 1, Actual equal_out = 0, Actual not_equal_out = 1. Test passed.
. a = 11000101, b = 11000101, Expected equal_out = 0, Expected not_equal_out = 1, Actual equal_out = 1, Actual not_equal_out = 0. Test failed! Error message: failed in error_injec
. a = 01110111, b = 00001101, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 0, Actual not_equal_out = 1. Test failed! Error message: failed in error_injec
. a = 11011011, b = 10110101, Expected equal_out = 0, Expected not_equal_out = 1, Actual equal_out = 0, Actual not_equal_out = 1. Test passed.
. a = 11000101, b = 11000101, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 1, Actual not_equal_out = 0. Test passed.
. a = HHHHHHHH, b = HHHHHHHH, Expected equal_out = 0, Expected not_equal_out = 1, Actual equal_out = 1, Actual not_equal_out = 0. Test failed! Error message: failed in error_injec
. a = LLLLUUUU, b = WWWWLLLL, Expected equal_out = 1, Expected not_equal_out = 0, Actual equal_out = 0, Actual not_equal_out = 1. Test failed! Error message: failed in error_injec
```

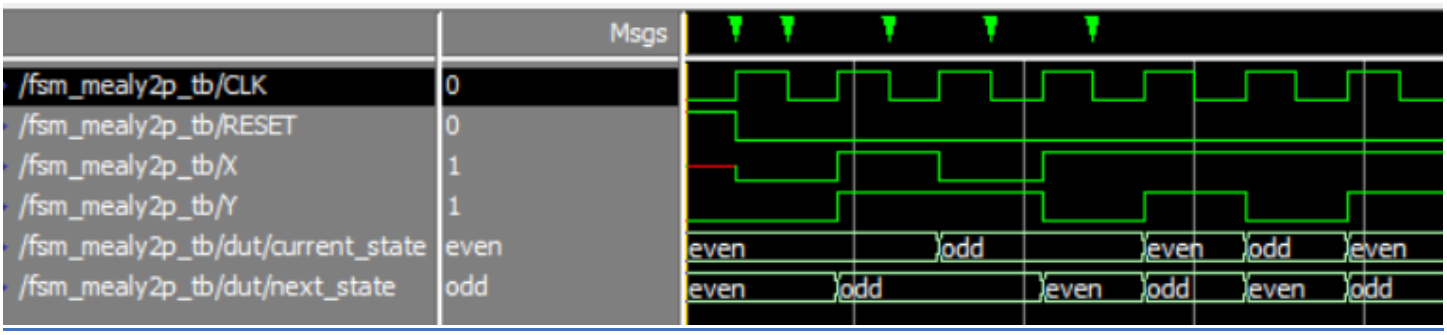
FSM MEALY 2P

TEST CASES

CLK	RESET	X (INPUT)	Y (OUTPUT)	
0	1	U	0	Check reset
1	0	0	0	Even state when x=0
0	0	0	0	Even state :output does not change without clk
1	0	1	1	Even state when x=1
1	0	0	1	Odd state when x=0
0	0	0	1	odd state :output does not change without clk
1	0	1	0	Odd state when x=1

SIMULATION RESULTS

```
* Note: PASSED:RESET
  Time: 15 ns  Iteration: 0  Instance: /fsm_mealy2p_tb
* Note: PASSED:even state , x=0
  Time: 30 ns  Iteration: 0  Instance: /fsm_mealy2p_tb
* Note: PASSED:even state :output doesnot change without clock
  Time: 30 ns  Iteration: 0  Instance: /fsm_mealy2p_tb
* Note: PASSED:even state , x=1
  Time: 60 ns  Iteration: 0  Instance: /fsm_mealy2p_tb
* Note: PASSED:odd state , x=0
  Time: 90 ns  Iteration: 0  Instance: /fsm_mealy2p_tb
* Note: PASSED:odd state :output doesnot change without clock
  Time: 90 ns  Iteration: 0  Instance: /fsm_mealy2p_tb
# 110> run
* Note: PASSED:odd state , x=1
  Time: 120 ns  Iteration: 0  Instance: /fsm_mealy2p_tb
```



FSM MOORE 2P

TEST CASES

CLK	RESET	X (INPUT)	Y (OUTPUT)	
0	1	U	0	Check reset
1	0	0	0	Even state when x=0
0	0	0	0	Even state :output does not change without clk
1	0	1	0	Even state when x=1
1	0	0	1	Odd state when x=0
0	0	0	1	odd state :output does not change without clk
1	0	1	1	Odd state when x=1

SIMULATION RESULTS

```
** Note: PASSED:RESET
   Time: 15 ns  Iteration: 0  Instance: /fsm_moore2p_tb
** Note: PASSED:even state , x=0
   Time: 30 ns  Iteration: 0  Instance: /fsm_moore2p_tb
** Note: PASSED:even state :output doesnot change without clock
   Time: 30 ns  Iteration: 0  Instance: /fsm_moore2p_tb
** Note: PASSED:even state , x=1
   Time: 60 ns  Iteration: 0  Instance: /fsm_moore2p_tb
** Note: PASSED:odd state , x=0
   Time: 90 ns  Iteration: 0  Instance: /fsm_moore2p_tb
** Note: PASSED:odd state :output doesnot change without clock
   Time: 90 ns  Iteration: 0  Instance: /fsm_moore2p_tb
M 128> run
** Note: PASSED:odd state , x=1
   Time: 120 ns  Iteration: 0  Instance: /fsm_moore2p_tb
```