Computer architecture project

single-cycle MIPS processor

The single-cycle microarchitecture executes an entire instruction in one cycle. The micro architecture will be simple, but cycle time is limited by the slowest instruction.

First to design a MIPS microarchitecture that executes instructions in a single cycle. We begin constructing the datapath by connecting the main elements (program counter, instruction memory, register file, data memory) with combinational logic that can execute the various instructions.

Then design the controller that provides Control signals to determine which specific instruction is carried out by the datapath at any given time. The controller contains combinational logic that generates the appropriate control signals based on the current instruction.

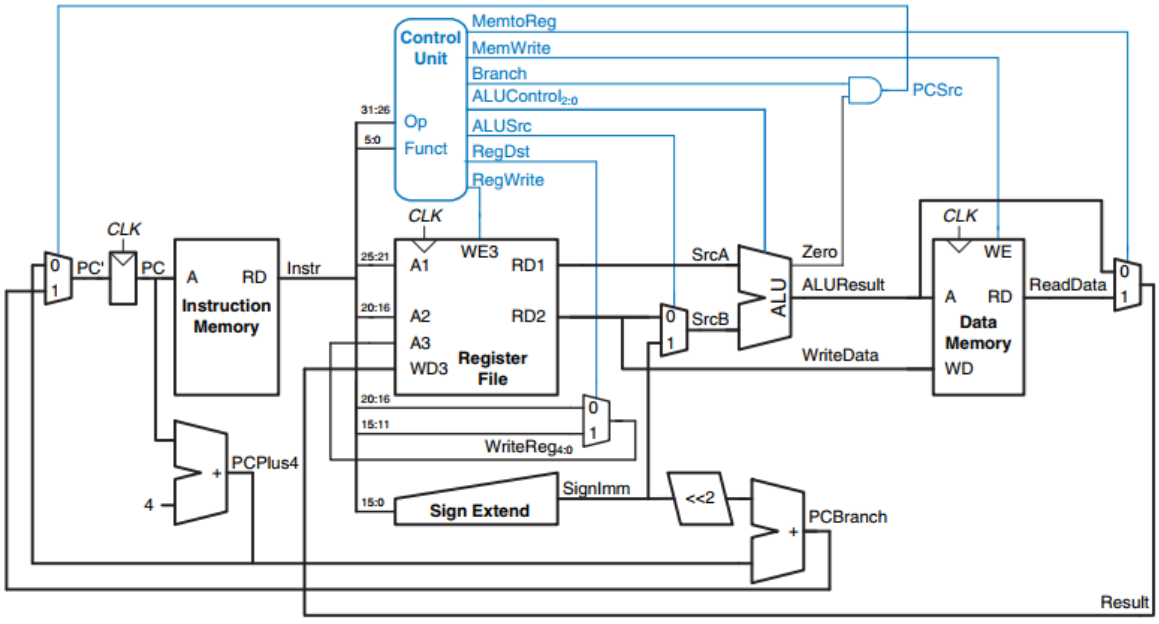

Figure 7.11 Complete single-cycle MIPS processor

The single cycle mips processor needs to handle only the following instructions:

1- R-type arithmetic/logic instructions: add, sub, and, or, slt, addi, ori
2- Memory instructions: lw, sw
3- Branches: beq, jal, j

Reference:

Digital Design and Computer Architecture second edition by David & Sarah Harris, chapter 7.