AN69061

Design, Manufacturing, and Handling Guidelines for Cypress Wafer Level Chip Scale Packages

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Software Version: None
Related Application Notes: None

AN69061 provides guidelines for the design, manufacture, and handling of Cypress wafer level chip scale packages on flexible printed circuits and rigid printed circuit boards.

Contents

1 Introduction

This application note is for engineers who design and develop surface mount technology (SMT), printed circuit boards (PCB), or flexible printed circuits (FPC) for wafer level chip scale package (WLCSP) devices.

These guidelines document the best practices for WLCSP assembly and PCB/FPC design to ensure good manufacturing yield and reliable performance. Many factors impact the manufacturing, performance, and reliability of final electronic products, including PCB and solder material selection, manufacturing equipment, and application specification requirements. Therefore, Cypress encourages you to validate these best practice guidelines through your own product development and qualification process.

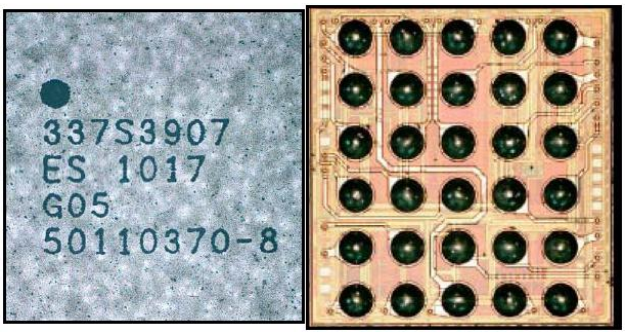
2 Why Use WLCSP Instead of Conventional Packages

WLCSP is a true die-scale package and offers the smallest footprint for each I/O count of any standard IC package such as QFN or Chip Array BGA. For example, the footprint of a 32-pin QFN package for one of Cypress's touchscreen products is 25 mm^2 (5.0 × 5.0 mm), while the equivalent WLCSP (Figure 1) with 30 balls is only 5.1 mm^2 (2.2 × 2.32 mm). The result is an 80 percent reduction in footprint area on the PCB.

WLCSP eliminates the first-level package (lead frame, die attach, wire bonds, and mold compound). It reduces the weight and three-dimensional space consumed by a lead frame-based package.

Similar to BGA, WLCSP has solder balls or bumps with available ball layouts in 0.5 mm or 0.4 mm pitch and can vary by specific product design and application requirement.

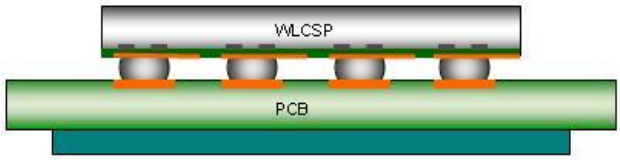
Figure 1. Construction of Cypress WLCSP (30 balls)



3 Cypress WLCSP Construction

Cypress builds its WLCSP devices using several wafer fabrication processes, including aluminum and copper metallization, low-K and non low-K dielectrics, and passivation. It does the laser marking on the reverse of the WLCSP die and attach the solder ball on the active circuitry side of the die, as shown in Figure 1. It then mounts a WLCSP device on a PCB that can be either rigid or flexible in form, as shown in Figure 2,

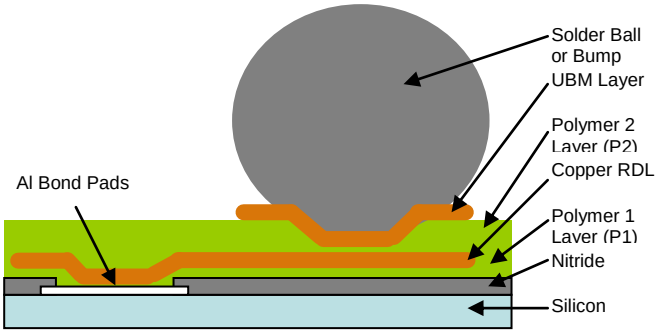
Figure 2. WLCSP Mounted on PCB



Without Underfill

The WLCSP process begins with the application of a polymer 1 layer (P1) over the silicon wafer. Cypress uses a photolithographic and etching process to pattern the P1 layer to create openings, which allow access to the aluminum pads on the die surface. For a die with perimeter-placed bond pads (supporting the traditional wire bond process), it plates and etches a copper redistribution layer (RDL) over the P1 layer. This creates electrical connections between the normal wire bond pads and an array of solder ball pads. Cypress applies a second polymer layer (P2) over the RDL. It patterns and etches the P2 layer with openings to metal pads to build under-bump metallization (UBM). It then permanently attaches plated solder bumps or dropped solder balls to the UBM pads by reflow, as shown in Figure 3.

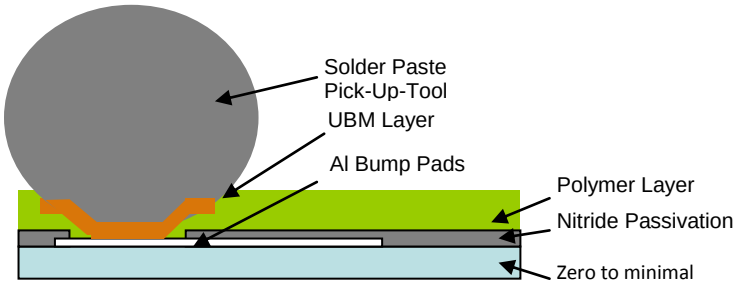
Figure 3. Solder Bump Structure with Copper RDL



3.1 Bump-On-Pad

Bump-on-Pad (BOP) is another type of WLCSP in which the bond pad to area array redistribution uses the final top metal layer (usually aluminum) instead of a copper RDL. In this case, Cypress applies a single polymer layer over the die surface and process to leave openings to the Al bump pads to build UBM. The polymer layer decreases stress in the WLCSP when it is subjected to shock and thermal cycling. Solder bumps are then plated or ball dropped directly to the UBM and then permanently reflowed, as shown in Figure 4.

Figure 4. Solder Bump Structure for BOP WLCSP



Cypress makes all WLCSP devices with SAC (Sn (tin), Ag (silver), and Cu (copper)) Pb-free solder alloys . Although compositional and manufacturing differences are minor, you should consider the end application when selecting the solder ball composition. Cypress recommends SAC396 for dropped solder balls and Sn2.3Ag for plated solder bumps (Table 1).

Table 1. Material Properties of Pb-free Solder Ball and Bump

Properties	SAC396	Sn2.3Ag
Sn (%)	95.5	97.7
Ag (%)	3.9	2.3
Cu (%)	0.6	0.0
Liquidous point (°C)	220.0	221.0
Elastic modules (Gpa)	52.0	52.7
Ultimate tensile strength	43.7	58.0
Yield stress (Mpa)	31.3	24.8
CTE @ 20°C (PPM/°C)	21.4	30.0

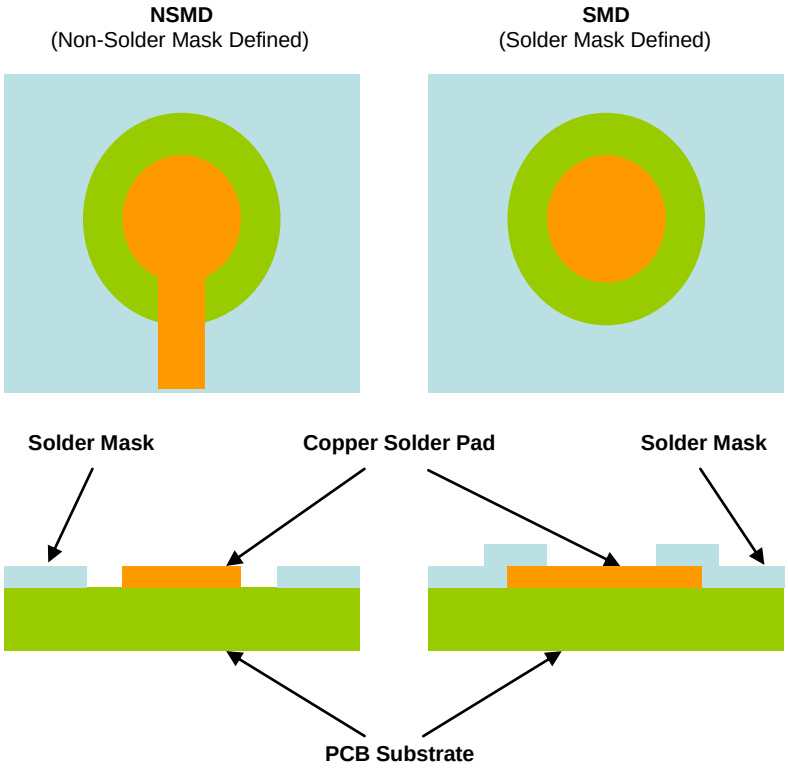
4 WLCSP PCB Layout Guidelines

4.1 Land Pattern Recommendations

PCB fabrication uses two types of land pad patterns during surface mount assembly (Figure 5).

- Non-solder mask defined (NSMD) – The metal pad on the PCB to which a package ball, pad, or pin attaches is smaller than the solder mask opening.
- Solder mask defined (SMD) – The solder mask opening is smaller than the copper pads.

Figure 5. NSMD and SMD Land Patterns



Underfill is an epoxy used to fill out the gaps created by the WLCSP when it is mounted on the PCB for improved reliability. For FPC board applications that require underfill, Cypress recommends SMD pads to minimize underfill issues. NSMD pads are not recommended when the PCB applications require potential rework, because NSMD pads are prone to peel off after multiple thermal exposures. However, NSMD produces a more reliable solder joint during thermal cycle stress because of the additional adhesion strength provided by the copper pad sidewall to which the solder will also wet.

Cypress strongly suggests that you carry out a complete design of experiment (DOE) and reliability test to determine the most suitable pattern for the given PCB application. Table 2 compares the pros and cons of both patterns. Each Cypress WLCSP datasheet contains detailed package outlines for the device.

Table 2. NSMD Versus SMD

NSMD		SMD	
Pros	**Cons**	**Pros**	**Cons**
Solder ball wets on the sidewall of the exposed copper pads, thus improving solder joint reliability.	Solder mask opening creates moats that allow underfill deposits. This irregular distribution of underfill may introduce stress on the solder mask and the copper trace.	Copper pads are stronger, since the solder mask overlaps the copper. This improves bond adhesion between the pad and the laminate.	Less space forms in between pads when routing signal traces.
Wider space forms when routing signal traces due to small copper pad area.	Potential underfill voiding as the solder mask opening provides challenges on the capillary action of the underfill.	Copper pads have a bigger area, thus improving PCB to pad chemistry during flexing and excessive thermal exposure.	Absence of copper side wall reduces the reliability of the solder joint to which it adhere

4.2 Board Material Selection and Thickness

Standard glass or epoxy substrates are compatible with several Cypress WLCSP devices. High-temperature FR4 laminate is preferable to standard FR4 as it enhances package reliability; the coefficient of thermal expansion (CTE) of high-temperature FR4 laminate (12–16 ppm/°C) is lower than that of standard FR4 (14–18 ppm/°C) and is closer to that of silicon (~2.5 ppm/°C).

The actual CTE of a board is design dependent. Numerous factors—such as the number of metal layers in the PCB, trace density, laminate material, mounted component's population density, and operating environment affect the thermal expansion. For the greatest reliability, the PCB laminate glass transition temperature should be above the operating range of the intended application (Tg > 170 °C recommended).

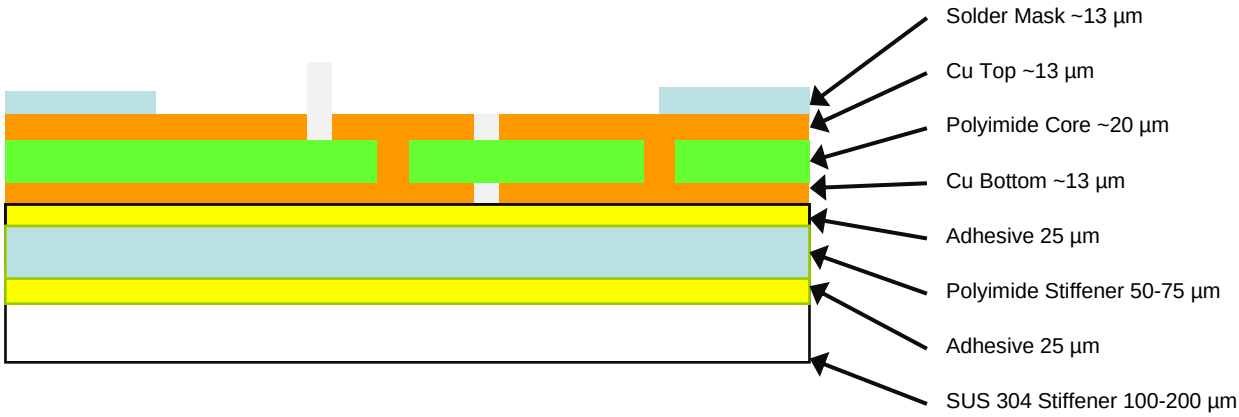
Board thickness values currently used in the industry range from 0.016 to 0.093 inch (0.4 to 2.3 mm). Thinner boards are more flexible, resulting in greater reliability during thermal cycling and improved thermal fatigue life in comparison to thicker boards.

The FPC, as shown in Figure 6 is another PCB application for WLCSP assembly, especially for Cypress's touchscreen products on handheld devices. There are multiple factors in FPC material selection and design; for example, flex polymer material and thickness, copper thickness, and stiffener material and thickness. Cypress recommends the SUS304 (JIS identifier for 18/8 Stainless Steel) stiffener to enhance the thermal and mechanical strength of WLCSP devices. When using a metallic stiffener in CapSense® applications, the additional parasitic capacitance of the stiffener must be taken into account.

Depending on the application, Cypress WLCSP devices can be board mounted on different board-pad surface finishes with matching solder paste to form a complete joint. Nickel-based finishes have been a popular choice due to the higher substrate shelf life, improved corrosion resistance, better thermal stability of solder joints, and good reworkability. Among these finishes, Electroless Ni Immersion Gold (ENIG) has become popular.

Other surface finish alternatives used by manufacturers include immersion Au, immersion Ag, organic solder preserves (OSP), solder-on-pad (SOP), and electrolytic Ni-Au. Among these alternative surface finishes, the most promising technologies are the SOP and electrolytic Ni-Au. SOP is the easier solution and has very good solder wetting compared to electrolytic Ni-Au. Available options are SAC SOP, SnPb SOP, and Cu SOP, with the latter being the most popular because degradation on the substrate's pad finish takes longer compared to the others. Cu SOP degrades 50 times slower than the ENIG pad surface.

Figure 6. Typical FPC Structures



For optimal board reliability with Cypress WLCSP devices, the recommended ratio between the solder ball and substrate pad size is 1:1. Cypress recommends that you contact Cypress Support (www.cypress.com/support) for FPC layout design rules and review.

5 WLCSP SMT Guidelines

The following SMT guidelines must be evaluated for WLCSP applications:

- Stencil design
- Electromagnetic shielding
- Solder paste
- Package placement
- Reflow
- Underfill
- SMT rework

5.1 Stencil Design

It is important to follow the stencil design guidelines in IPC-7525 for all assemblies. It is essential to use good-quality stencils to achieve good-quality solder paste printing. You can achieve better solder stencil performance by using laser-cut or electroformed stencils rather than chemically etched stencils. For tight pitch components, Cypress recommends electroformed stencils, because they give better paste release action and consequently consistent solder paste volume. The solder stencil opening should be identical for all solder pads in the WLCSP array to prevent unbalanced solder-ball height.

Laser-defined apertures or electroformed stencils provide the crispest printing results. The aperture area ratio is the ratio of the stencil aperture cross section to the aperture wall area. The aspect ratio is the ratio of the stencil aperture diameter to the aperture height. To get the best solder paste transfer, Cypress recommends an area ratio of ≥0.66 or an aspect ratio of ≥1.5. Square stencil apertures provide the most consistent paste transfer. For a 400-µm pitch, the recommended stencil alignment accuracy is ±50 µm at 3-sigma.

One of the most critical aspects of SMT is to achieve a robust and consistent solder paste printing process. This requires several process monitors, such as paste volume control and stencil inspection, to ensure equal amounts of solder paste are deposited on the PCB pads. Overprinting results in solder bridging, while nonuniform printing often results in opens after reflow due to poor coplanarity. On the other hand, marginally insufficient solder paste can create a narrow solder joint after reflow, which can trigger reliability failures in the field.

Cypress recommends the use of X-ray inspection after reflow to ensure proper placement and solder wetting. The process also requires periodic stencil cleaning by solvent during the inline process for consistent paste printing and after every use prior to storage.

5.2 Electromagnetic Shielding

Shielding of the WLCSP for electromagnetic, thermal and mechanical protection can present issues during the SMT process. There are four considerations with respect to electronic magnetic shielding: dimensions between the WLCSP, PCB, pads, and components; type of shielding; shield design; and shield placement.

The critical dimensions between the WLCSP, PCB pads, and components are shown in Figure 7 and Table 3. The type of shielding is also critical for the WLCSP with underfill applications.

Figure 8 shows a 3-foot shield that is not ideal for underfill applications due to a potential voiding issue. A 3-foot shield is not a good design, because it creates a potential vacuum source during underfill dispense. This vacuum, compounded by the shield's wall surface, disturbs the capillary action of the underfill. Such a phenomenon triggers underfill voids. The voids can accumulate pressure during thermally stressed conditions and release unwanted energy that can cause die crack, topside delamination, UBM cracking, and solder bridging as shown in Figure 9. Also, solder bridging can be induced during the onset of paste printing and placement when the critical dimensions for the shield are not fully reviewed per the application.

Table 3. Electromagnetic Shielding Dimensions

Description		Specs Minimum (mm)
A	WLCSP edge to PCB edge	2.00
B	WLCSP edge to WLCSP edge	4.00
C	WLCSP edge to component pad edge	2.50
D	Shield edge to component pad edge	2.00
E	Shield edge to PCB edge	2.00
G	WLCSP Pad edge to shield pad	3.50
H	WLCSP edge to shield wall	3.00
I	Shield height to PCB	155×(package thickness)

Figure 7. Electromagnetic Shielding Dimensions

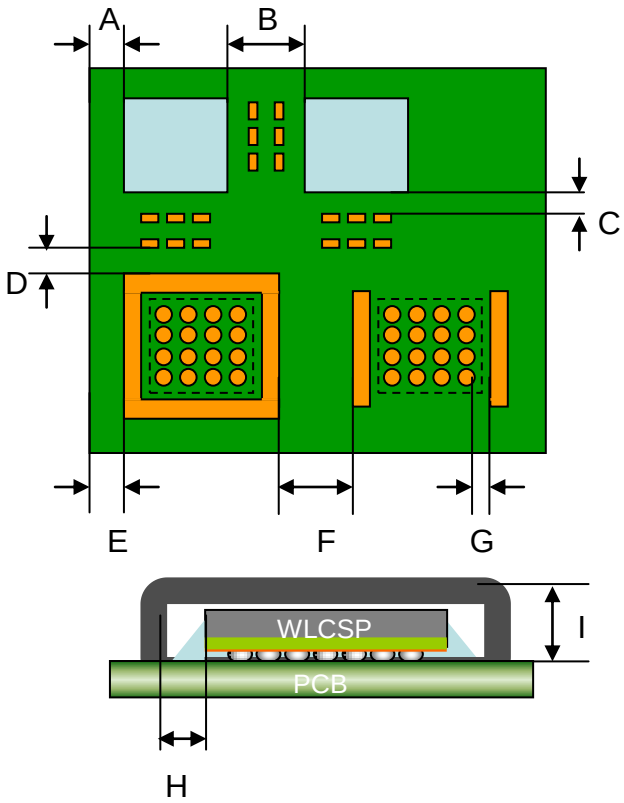


Figure 8. Examples of Shields

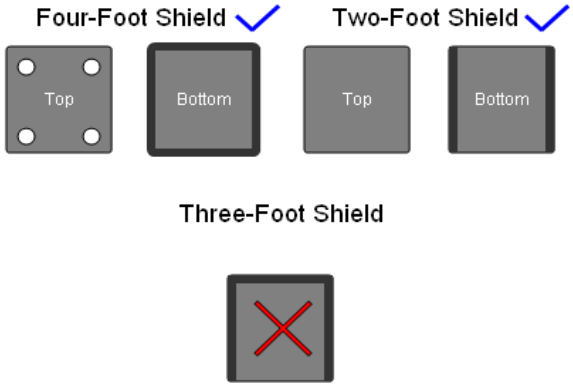
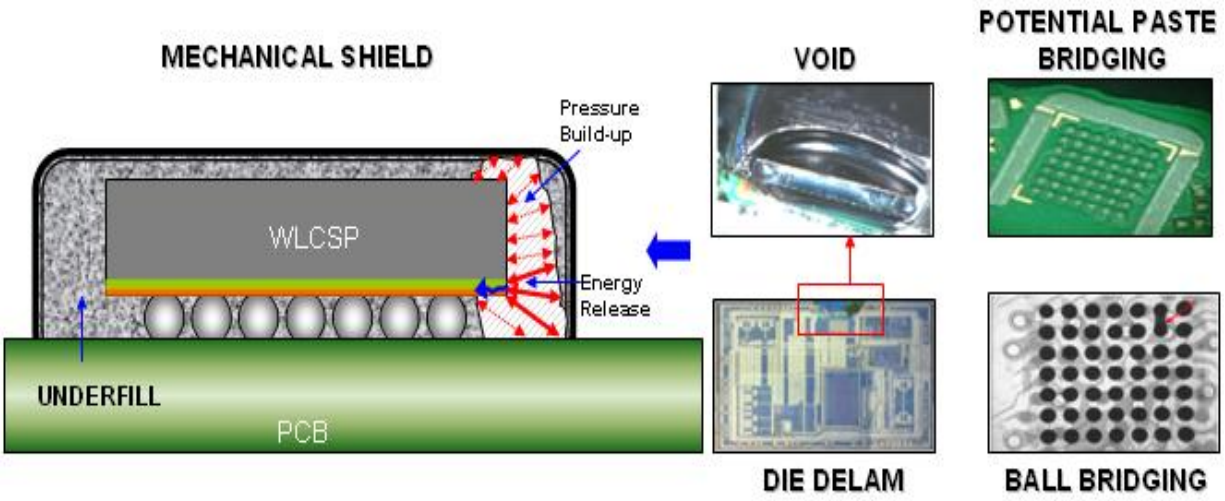


Figure 9. Potential Failures Due to Improper Shield Design and Placement



5.3 Solder Paste

The solder paste printing process transfers solder paste (typically an industry-standard, Pb-free solder paste containing Sn-Ag-Cu) by squeezing the paste over the predefined stencil mask. Cypress recommends that you automate the periodic cleaning of the stencil underside to improve solder paste volume uniformity and promote better paste release. Avoid manual cleaning, because it will dent and damage the stencil and degrade its paste printing quality.

The best board-level reliability performance occurs when maximum device standoffs exist under the WLCSP. To obtain this, the following practices are recommended:

- Maximum allowable solder paste volume without encountering paste bridging
- Automated optical inspection to monitor solder paste volume uniformity
- No-clean solder paste with a particle size no larger than 40 µm (Type 3)
- No use of solder paste with active or acid-based flux to avoid potential corrosion issues

5.4 Package Placement

Typical surface mount pick and place equipment can assemble WLCSP devices to a PCB or FPC when the equipment is properly optimized for WLCSP parts.

WLCSP technology provides robust self-alignment with screen-printed solder paste when the solder ball height is greater than 0.15 mm. When the solder ball standoff is less than 0.15 mm, more caution is required for self-alignment. The proper ratio between the pick and place tool and the package size must be observed at a minimum of 80 percent to provide a uniform distribution of stress on the package during placement.

Additional recommendations concerning placement force for the best success with component placement processes are as follows:

- Placement Z-height on the board should be set to zero or to a critical distance between the PCB and WLCSP before it is dropped or placed. Avoid setting a bond force, which can overdrive the package to the surface of the board. This is a common setup mistake, which eventually leads to mechanical overstress (MOS) when the resultant force drives back the solder ball toward the topside of the die, which damages it.
- Maximum component placement force depends on the WLCSP structures as well as the mounting board materials. Although each solder ball is manufactured to withstand a load force of 35 grams, Cypress recommends avoiding any force applied on the WLCSP by setting the Z position to zero as minimum. Exceeding this force may reduce reliability because of excessive mechanical stress on the device that causes topside damage on the surface of the WLCSP.

- During component transfer via conveyor, there is a possibility of component displacement or skewing prior to reflow. Optimize conveyor speed and transfer to avoid jerking and fast motion. If the process requires realignment of the package on the board prior to reflow, do not use metal tweezers to correct the component placement. Instead, use a soft tool such as a vacuum pen or equivalent.

5.4.1 Pick and Place Process

During component pickup from carrier tape, Cypress recommends a Z-height distance between the WLCSP and the pickup tool. Define the vacuum pressure at approximately 60 to 70 kpa to lift the WLCSP from the pocket of the carrier tape. This practice prevents direct contact and MOS on the WLCSP during pickup.

Set the Z-height distance between the WLCSP and the pickup tool to zero or with a minimal gap, as shown in Figure 10. The vacuum lifts out the package from the pocket of the carrier tape.

Similarly, set the Z-height during placement to zero or with a minimum gap height to avoid overdrive during board placement, as shown in Figure 11.

Figure 10. WLCSP – Pickup on Carrier Pocket

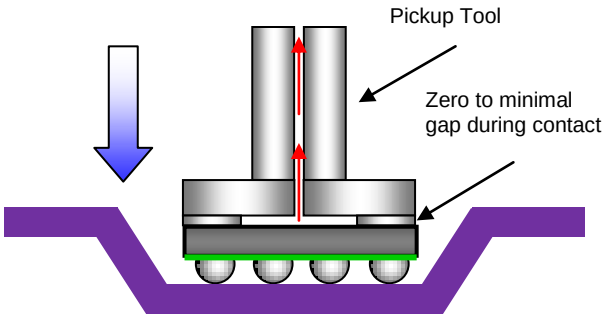
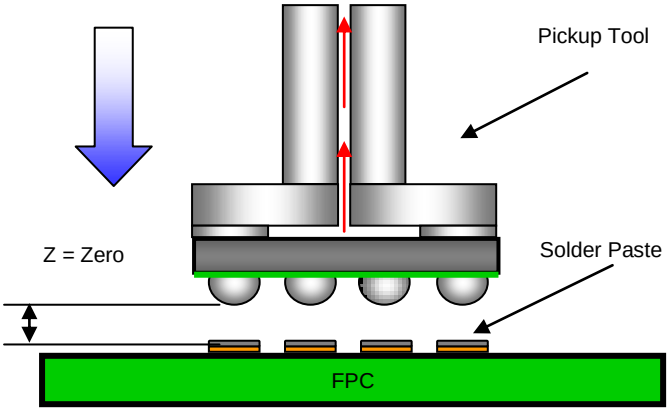


Figure 11. WLCSP Placement on FPC Board



5.5 Reflow

All Cypress WLCSP devices are 100 percent Pb free (Sn-Ag-Cu or Sn-Ag). Therefore, Pb-free solder paste with a Pb-free reflow profile is recommended. If any application requires a solder paste with lead, contact Cypress Support (www.cypress.com/support) for a technical consultation. For the standard application, Cypress recommends the following:

- For an improved soldering response, use a reflow furnace with a nitrogen purge that has an oxygen content below 50 ppm.
- Determine the actual reflow temperatures based on thermal loading effect measurements within the furnace, including the complexity of the components on the board and the board size and thickness. Well-constructed profiling tools must be available to achieve accurate temperature settings.
- For Pb-free (Sn-Ag-Cu or Sn-Ag) solder, the reflow profile is critical. The Sn-Ag-Cu solder alloy melts at ~220 °C. The reflow temperature peak at joint level should be from 15 to 20 °C higher than the melting temperature. See Table 4 for more details about maximum reflow temperature.

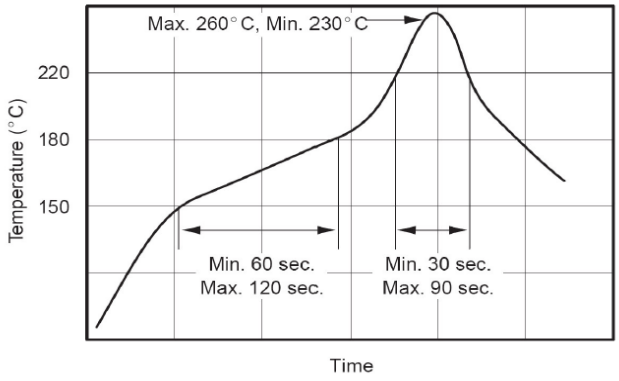
Table 4. Recommended Reflow Parameters for Sn-Ag-Cu Paste

Process Step	Lead-Free Solder
Ramp rate	3 °C/second
Preheat	150 to 180 °C 60 to 180 seconds
Time above liquidus (220 °C)	30 to 90 seconds

Process Step	Lead-Free Solder
Peak temperature	255 °C ±5 °C
Time within 5 °C of peak temperature	10 to 20 seconds
Ramp-down rate	Maximum 6 °C/second

- Higher reflow temperatures than the qualified temperature can cause delamination and solder joint issues within the package.
- Dwell time in the soldering zone (with temperatures higher than 220 °C) must be kept as short as possible to prevent component and substrate damage. The peak temperature must not exceed 260 °C. Use a controlled atmosphere (N_2 or N_2H_2) during the reflow, especially above 150 °C.
- To avoid any cleaning operation, use a no-clean flux.
- All of Cypress's WLCSPs are qualified at 260 °C reflow with MSL1. Typical temperature profiles for the Pb-free (Sn-Ag-Cu or Sn-Ag) solder and the corresponding critical reflow parameters are shown in Figure 12 and Table 4.

Figure 12. Recommended Reflow Profile for Sn-Ag-Cu Paste



- Ramp-down must not be abrupt and should not exceed the recommended rate to avoid potential UBM cracking due to thermal shock as the parts get out of the reflow outside ambient temperature. Similarly, avoid the installation of high-speed air ionizers at the exit of the reflow, because they introduce thermal shock to the package. Figure 28 shows a UBM crack due to thermal fatigue.
- A good quality solder joint occurs when the solder wets the entire solder land from the WLCSP solder ball. Make the surface of the joint smooth and the shape symmetrical. Ensure that all the soldered joints on a chip are uniform. Voids in the solder joint after reflow can occur during the reflow process when the reflow profile is not properly tuned based on the recommended profile. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits, and voids. A common failure associated with a poor reflow process and oxidation is a head-in-pillow effect. Proper storage and handling of the WLCSP solder ball and reflow profile optimization can eliminate this source of failure.

5.6 Underfill Process

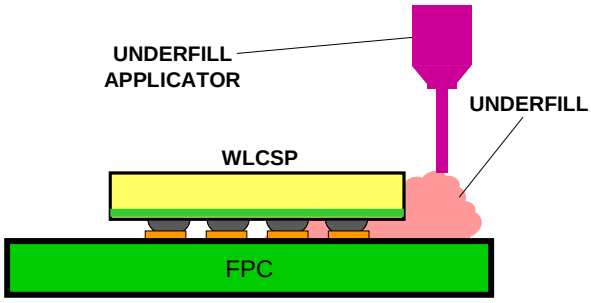
Cypress originally designed the WLCSP without an underfill application. However, a thermal cycle test exceeding the standard reliability conditions yielded mechanical failures on solder joints. These failures often relate to a CTE mismatch between the package and board.

In most cases, a reliable underfill is deployed to make both the package and board compliant with each other. The underfill bridges the gap in CTE between the package and the board through encapsulation of the solder joint, as shown in Figure 13.

This behavior of the underfill protects the small bumped solder joint from excessive solder fatigue, unwanted package moisture, ionic contaminants, radiation, solder bump extrusion, thermal shock, mechanical shock, and vibration, which are all common aspects of the SMT application.

Underfill application is advisable if the solder ball diameter is <200 µm and the succeeding process operating temperature requirement is greater than the melting point of the solder joint. Some manufacturers consider underfill undesirable because of the additional process and cost it introduces during board mount. However, the reliability margin it provides offsets these negative factors. Figure 14 illustrates a surface mount with and without underfill.

Figure 13. Underfill Process

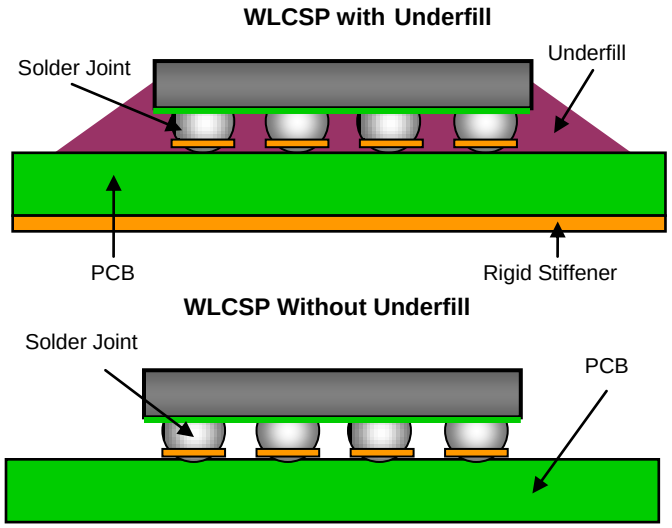


Underfill selection depends on several factors such as the combination of WLCSP size, WLCSP construction material and dimensions, circuit board structure and materials, and reliability requirements. Contact Cypress Support for further details on underfill (www.cypress.com/support).

The following is a list of recommendations for selecting the type of PCB and underfill:

- Rigid multilayered FR4 PCB does not require underfill for Cypress WLCSP devices with a solder ball diameter of >200 µm.
- Flex PCB requires the use of underfill for all WLCSPs regardless of die size to achieve maximum reliability.
- Rigid metal (or other) stiffeners such as SUS304 (Stainless Steel) enhance board-level reliability with respect to thermal and mechanical stress.
- High CTE epoxy is not acceptable as an underfill material, because CTE mismatch causes higher stress on WLCSP products. Likewise, silicone cannot be used, because it does not provide the enhanced mechanical support needed for an underfill material. Underfill CTE must be close to the CTE of the solder joint.
- Cypress has observed significant differences in performance from different underfill types and suppliers. The use of optimized underfill material derived from an actual DOE is strongly recommended. If requested, Cypress will review your underfill material selection; contact Cypress Support (www.cypress.com/support).

Figure 14. Surface Mount with Underfill Versus Without Underfill



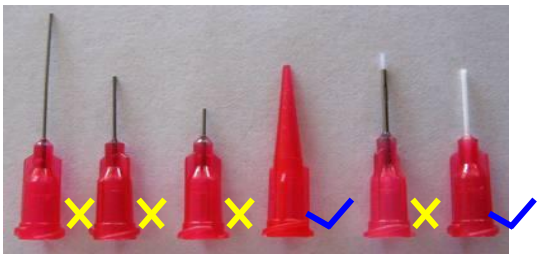
5.7 WLSCP Underfill Process Requirements

5.7.1 Needles

Needles are very important in the manipulation of underfill flow. Many types and sizes of needles are available on the market, as shown in Figure 15:

- **Conventional metal shafts**: Provider additional heat application on needle for improved dispensing
- **Plastic tips and shafts**: Prevent die chipping and scratch on the PCB
- **Tapered plastic tips**: Reduce back pressure in the pump—ideal for fine pitch dispensing

Figure 15. Needles for Underfill Dispense



Cypress recommends soft plastic needles without metal to reduce the impact force of the needle when it collides with the WLCSP die edge due to manual underfill dispensing. A 0.25-inch needle keeps back pressure on the pump low. The needle diameter controls the line width during dispensing. Cypress recommends the use of 22 gauge needles, with a 410-µm inner diameter, to dispense underfills at a rate of 10 to 20 mg/s. Use lower gauge needles when dispensing minimal underfill on very small packages. Twenty gauge needles with a 610-µm inner diameter enable good control at larger flow rates. For manually dispensed underfill, use a plastic conical tip to reduce contact on the edge of the die and reduce mechanical damage.

5.7.2 Prebake

Substrates must be free from moisture for a good and reliable underfill. Prebake is necessary to prevent voiding and delamination during curing. Plasma cleaning improves the flow rate, improves the fillet height and uniformity, and promotes effective interface adhesion. As a result, plasma treatment prevents the delamination and void formation that can result in a shortened lifetime for microelectronic devices.

5.7.3 Dispensing

Cypress recommends the use of an auto-dispensing machine for underfill dispensing to reduce the mechanical damage caused by manually dispensing the underfill on the edge of the die. Underfill volume is controlled to optimize reliability and appearance. The ideal underfill should be dispensed to completely fill the solder ball area of the die and provide a good fillet that covers greater than 50 percent of the edges of the die but not more than 75 percent. Dispense volume variations lead to undesired fillet size variations. An estimation of the volume is possible with simple calculations. Determine the final volume by trial and error by processing a number of assemblies, each with a different volume of underfill, and reliability testing. A change in substrate supplier or substrate manufacturing process or solder ball type requires another volume evaluation.

Because the total bond area of the solder ball is always much smaller than the respective areas of the die and the substrate, the stress on an individual solder ball is relatively large. By absorbing energy during thermal cycling, the underfill reduces this stress by a factor of about 10. When no underfill is present, the solder ball absorbs the stress created by the mismatch in CTE between the package and the PCB, which is typically large.

Underfill also prevents solder extrusion during thermal cycling. Successfully applied underfill functions as an isotropic compression container around each solder ball and prevents them from extruding to form shorts within each other. At the same time, underfill prevents the initiation of cracks in solder balls by eliminating free surfaces at grain boundaries, where cracks can propagate.

To some degree, underfill also serves as a heat sink to dissipate heat from the die. However, for this to occur, all regions of the cured underfill must have the same thermal characteristics; variations can cause overheating in the die.

The space occupied by the fluid underfill consists of the under-die volume and the fillet surrounding the die. Calculate the entire volume of fluid to dispense with the following equation:

$$VTOTAL = VGAP - VBALLS + VFILLET$$

Where:

V_{GAP} = Volume under the die (die length × die width × underfill gap)

V_{BALLS} = Volume of the interconnect solder balls (area of cross section of solder ball × underfill gap × number of solder balls)

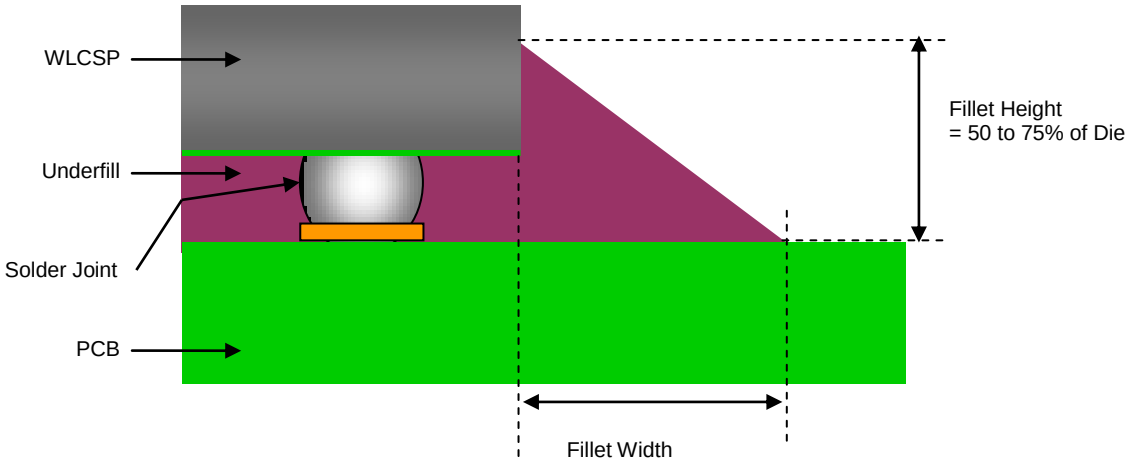
V_{FILLET} = Volume in the fillet

The volume under the die (V_{GAP}) must take into account the anticipated variation in the underfill gap. The underfill gap varies if the size of the solder balls varies. The goal is to accurately dispense a volume that is an average of the solder balls' size.

Accurate calculation of the volume of the fillet (V_{FILLET}) is critical because the fillet acts as a reservoir that compensates for normal variations in the under-die volume. Calculate V_{FILLET} by multiplying the desired area of the fillet by four. Underfill fillets typically have a low contact angle, which in turn speeds the underfill process and lowers the viscosity of the underfill material. Speed increases if the distance or vertical height of the gap under the die is large. Similarly, smaller and rounder filler particles increase the speed of underfill.

Making the fillet wider increases the volume of the reservoir and is one method to increase the dispensing tolerances. However, widening the fillet increases the X-Y dimensions of the underfill as well. Since stresses resulting from thermal mismatch are most severe at the corners (because they are farthest from the center), an increase in the height and width of the fillet by more than 50 percent of the die thickness generally increases the opportunities for corner cracking, side chipping, and delamination (Figure 16).

Figure 16. Underfill Fillet Layout

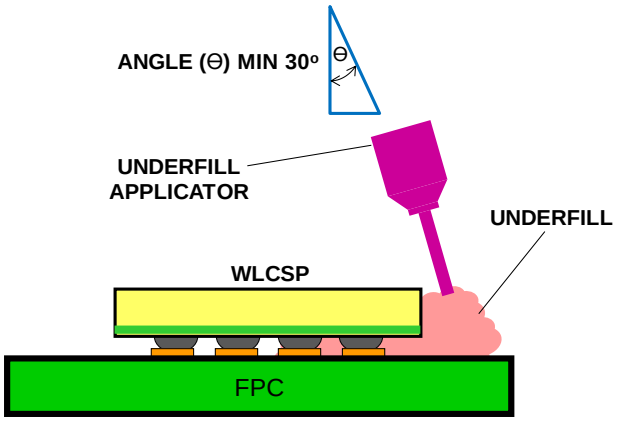


Use the following equation to calculate the volume of fillet (V_{FILLET}):

$$V_{FILLET} \approx 4 \times (1/2 \times L \times W \times H)$$

Figure 17 shows the recommended manual dispensing of underfill with a minimum slanting angle of 30°. The angle reduces contact between the needle and the edge of the die and thus minimizes damage to the WLCSP die edge. The recommended fillet height is about 50 to 75 percent of the die thickness to reduce flexural stress on the corner and edge of the die. The needle for manual dispensing should be made of soft plastic material.

Figure 17. Manual Underfill Process



5.7.4 Dispense Pattern

The dispense pattern is the two-dimensional step made by a needle as underfill is dispensed onto a WLCSP assembly. While there are several possible dispense patterns, the goal is to achieve a void-free, underfilled assembly with a small fillet that requires a minimum of flow time and time in the dispenser. Optimizing the dispense pattern maximizes reliability, conserves assembly real estate, and controls time expenditures. Developing a pattern for a properly designed flip chip assembly requires a tradeoff between dispenser time and the area covered by the fillets. Flow time is high for a larger die. A straight line (I-shaped) along one edge of the die is simple to implement for a die that requires a relatively small dispense fillet and control of air entrapment. Dispense along the longer side to minimize flow time. The pattern length generally varies from 50 to 125 percent of the die edge length. The greater lengths minimize the dispense fillet but increase the probability of trapped air at the far edge of the die. A bent line (L-shaped) dispense pattern along two adjacent die edges produces the smallest dispense edge fillets and shortest flow times.

Figure 18 shows 100 percent and 60 percent straight I-shaped dispense patterns on the length of the die edge. Faster flow along the die edges may necessitate a shorter dispense length to prevent void formation at the midpoint of the opposite side.

Figure 18. I-Shaped Dispense Patterns

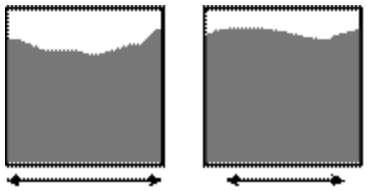
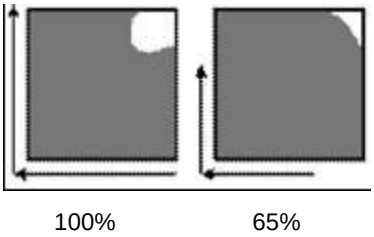


Figure 19 shows 100 percent and 65 percent L-shaped dispense patterns on the length of the die. Faster flow along the die edges may necessitate a shorter dispense length to prevent void formation in the opposite corner.

Figure 19. L-Shaped Dispense Patterns



If self-filleting is not acceptable or if you want symmetric fillets, then complete the initial pattern with a “seal pass.” Start with an I-shaped dispense pattern and complete with a U-shaped pattern. Alternatively, start with an L-shaped dispense pattern and complete with a second L-shaped pattern to dispense underfill along the remaining die edges to complete the gap. You can manipulate dispense parameters to control the quality of dispensing. To dispense an even line of underfill typically requires that the dispensing pump start before pattern motion begins. This gives the viscous underfill time to touch the substrate before the needle starts to move.

The distance from the die should be sufficiently great that the needle never strikes the die and that no underfill spills onto the die during dispensing (a reliability issue). This generally requires a spacing of at least 250 µm. Control the needle height to provide a uniform line of underfill along the die. A 250-µm height between the board and needle tip is optimal, especially if the underfill tends to string.

5.7.5 Post-Dispense Staging

Limit staging or exposure of uncured underfill to the ambient atmosphere to one hour to avoid moisture absorption. A timer preset to sound an alarm before the one-hour lapse period gives the operator time to put the underfilled parts into the oven for curing.

Properly cured, bulk underfill is unlikely to be affected by the absorption of moisture at atmospheric pressure. However, absorption of moisture by the liquid underfill prior to cure can be very damaging. The moisture chemically reacts with the underfill to degrade cured properties. Moisture can come from a moist assembly or from the atmosphere. Moisture affects surface appearance and surface physical properties the most since moisture enters the liquid mass by diffusion and convection. Underfill contaminated by moisture prior to cure often exhibits a spotted white or milky appearance after cure. Underfill cured while it contains moisture may exhibit very poor solvent resistance or depressed thermal stability.

5.7.6 Curing

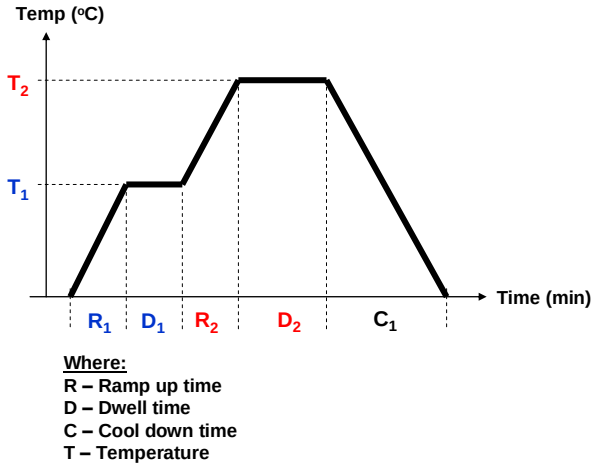
Curing is the process by which the liquid underfill—composed of fillers, resins, cross-linking agents, catalysts, and so on—is deliberately converted to a solid form that is chemically and physically stable. Usually, curing involves heating the underfill for a predetermined time at one or more temperatures.

The underfill must remain at the specified temperature for the required time. Control of the heating rate to cure underfill or of the cooling rate after curing is not necessary. Cypress recommends curing rates of greater than 10 °C per minute to reduce the loss of anhydride curing agents.

A variety of oven types are acceptable for curing underfills, including box and belt-style convection ovens, IR ovens, and conduction (non-convection) ovens. Cypress does not recommend the use of ovens under vacuum because of the possibility of inducing voids from minute quantities of dissolved gases or trapped air. Ensure that the oven provides a uniform, consistent temperature at all times. IR ovens may require extra attention to ensure uniform temperatures. Slow heating in non-convection ovens may require extra attention to assure the required dwell time at temperature.

If the application results in voids under the die or excessive stress or warp, it may be preferable to use a cure with two or more steps (Figure 20). With multistage cures, underfilled units partially cure, or gel, at a lower temperature. They are then heated a second time to a higher temperature to achieve full cure. This produces a final solid with less overall shrinkage than that produced at the higher temperature alone and enables initial hardening (gelling) of the underfill at a temperature less likely to evolve gases that cause voids.

Figure 20. Two-Step Cure Process



Any equipment discussed previously is acceptable for performing multistage curing. Belt-style ovens are probably the most convenient, because you can program the stages into succeeding zones of the oven. Physically moving the underfilled units from one oven to another is also acceptable provided that no more than a few minutes elapse. Protecting heat-sensitive underfilled units, curing faster, or finding compatibility with inline assembly processes are common reasons for considering nonstandard cure schedules.

Generally speaking, increasing the cure temperature by 10 °C from the required temperature reduces the cure time by 50 percent. Reducing the cure temperature by 10 °C doubles the time required to cure the underfill. The chemistry of the underfill in question limits the applicability of these guidelines.

Note: Exercise caution when modifying a cure schedule from the recommended time at temperature.

5.7.7 Pot Life

The pot life is the period during which the underfill can be processed excluding the thaw time. You must discard underfill whose pot life is exceeded to avoid viscosity and capillary issues. Since the demands on the flow properties of underfills vary considerably from one application to another, the pot life also varies. The real pot life in a given application is determined experimentally.

Underfill datasheets commonly set the pot life to the time required for a doubling of the viscosity. This number is valid for a comparison of similar underfills and as a starting point for real pot life determinations. Higher temperatures greatly impair pot life, because temperature accelerates the chemical cross-linking reactions. Advancement, the term used for the undesirable chemical cross-linking of underfills, accelerates after thawing and more quickly in a warm environment.

Eventually, the viscosity exceeds that which provides acceptable processing (flow speed or distance), rendering the underfill useless. Shielding a syringe from the substrate heaters or a warm dispensing environment may extend pot life significantly. Every 10 °C increase in underfill temperature roughly doubles the pot life. Aging of the underfill in its original cartridge or syringe does not significantly affect its properties after a proper cure; it only affects flow and viscosity. If the underfill processes properly, then final, cured properties are unaffected.

5.8 Jet Underfill Machine Process

The key element of a jet dispensing system is a valve that meters and ejects fluid droplets. Air pressure retracts an internal spring-driven plunger, allowing a precise amount of fluid from the reservoir to enter the chamber under pressure. The spring-driven plunger then returns to its seat, ejecting the fluid as a droplet though the nozzle.

5.8.1 Jetting Advantages

- **Component density:** Placing a needle safely between components requires more space than jetting a small drop between them. For a small PCB board with a high component density, jet underfill is the best dispensing system.
- **Fillets:** Because of the narrower fluid edge, the 100-micron droplet stream creates smaller fillets than needle dispensing. This allows closer placement of the die to a board edge or to bond pads.
- **Speed:** Jet dispensing is faster than needle dispensing, because the needle must be lifted vertically away from the substrate between dispensed dots or lines, while the non-contact jet travels in the x-y plane without being lifted between dots or a line. It can dispense “on the fly” without stopping.
- **Contact-free:** The jet nozzle is positioned well above any die. Needles may strike an adjacent chip, causing damage to the needle and possibly to the die. Die clipping creates a yield loss for needle dispensing. Jet dispensing eliminates that risk.
- **Lower cost:** Jet dispensing of flip chip underfills allows denser component spacing, greater throughput, contact-free dispensing, and higher yields than needle dispensing, resulting in 50 to 66 percent lower operating costs than for needle dispensing.
- **Die stacking:** 3D packaging with stacked, wire-bonded die requires a minimum wetted area to bring bond pads close to the die. Jetting stacked die underfill also eliminates the risk of needle contact with the wire bond.

5.9 WLCSP Rework

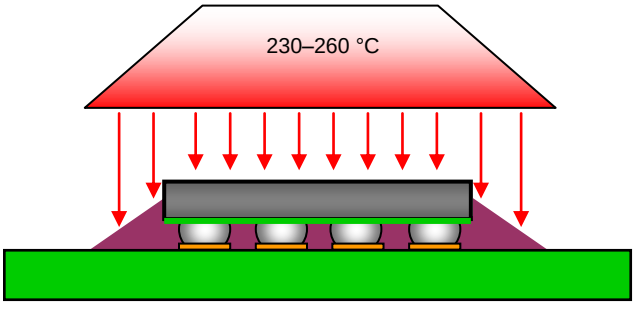
The rework of WLCSP devices is similar to that of ball grid array packages, but more difficult because of the exposed silicon substrate and possible presence of underfill. It is important to use a controlled and qualified process to carry out rework. A qualified process prevents mechanical and ESD damage to the device. The ability to rework components with underfill depends on the characteristics of the underfill. There are underfills on the market that can be reworked by the application of heat and proper cleaning.

Prior to attempting any rework, ensure that the assembly is moisture free. This prevents moisture damage to the board or other components during rework. Eutectic solder requires underboard preheating at 100 to 125 °C. Pb-free solder requires underboard preheating at 150 to 170 °C.

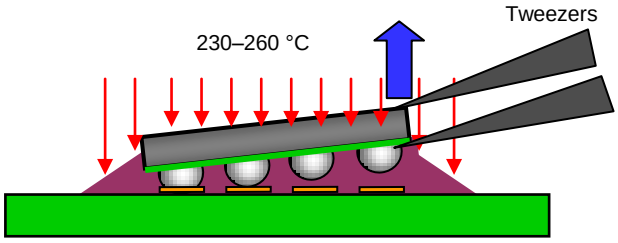
For cured underfill, it is not practical or recommended to remove conventional underfill for the repair of a flawed assembly. Conventional underfill encapsulants are practically impervious to everything except concentrated acids. Removable underfills are available for chip mount and CSP assemblies. The application of concentrated acids plus heat to underfilled units removes the underfill. Another method is the use of heat and light abrasion. After this, the die or CSP is then pulled off during heating.

The following procedure is a recommended rework flow for an example reworkable underfill SUF1577-15:

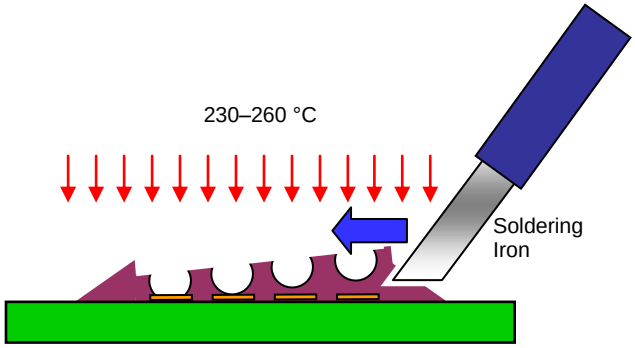
1. Heat the WLCSP at 230–260 °C with a focused IR, hot air blow gun, or plate, depending on the accessibility of the unit on the PCB.



2. Using plastic tweezers, lightly scrape off the fillet of the underfill. At this point, the solder is also melted, and you can lift the WLCSP away from the board.

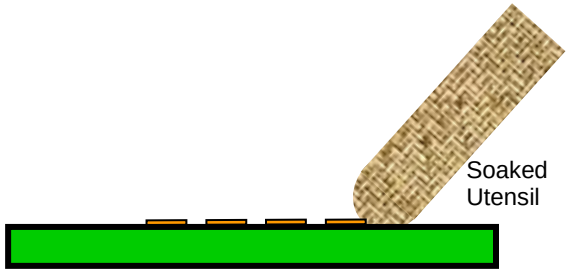


3. Using a soldering iron with a flat tip (paper knife type), lightly scrape off the remaining solder and underfill material. Use a solder wick in tandem to surgically extract any excess solder.



4. Wipe the board with a lint-free cloth utensil soaked in a cleaning solvent such as alcohol and inspect for pad lift or damaged copper pads.

   Cypress recommends the SMD pad type for applications that may require frequent rework.



Focused infrared technology is preferable to traditional hot-gas rework for removal of the solder balls from WLCSP devices. Focused IR allows more accurate removal and replacement of WLCSP devices without heating the adjacent components on a PCB/FPC.

Cypress recommends component replacement for parts removed from the board. It is also recommended that you avoid reuse, as the reused part may reduce reliability. If the component must be reused, component removal requires a three-stage (ramp-up, hold, ramp-down) reflow profile. Otherwise, you can use a direct ramp-up for faster device removal.

For optimal rework results, follow this checklist:

- Restrict the peak temperature to 240 to 250 °C for up to 90 seconds with Pb-free solder balls.
- Maintain the temperature delta across the solder joints at ≤10 °C.
- Maintain the temperature around the component undergoing rework at ≤150 °C.
- Maintain the component top temperature at ≤260 °C for Pb-free devices.
- Do not use flux, because it adds a process step and additional cost.

- Maintain air velocity as low as possible to avoid component skew (for example, 500 FCH for top heater, 100 FCH for bottom heater).
- Use a nitrogen atmosphere to achieve better heat distribution and removal as well as limit oxidation of conductor surfaces.
- Use a zero-force vacuum pick-up during the transition to cool down to avoid the bridging of reflowed solder balls.
- After reflow, complete an X-ray inspection for verification of alignment, bridging, voids, die shear, and/or die pulling.

Note: You must clean the surface of the substrate carefully and remove all solder and flux residues and/or underfill.

5.9.1 Component Replacement

It is critical to clean the rework site with solvent prior to component replacement to remove any surface contamination and oxides. For solder paste/flux application, use a mini-stencil with a squeegee of the same width as the stencil. Cypress recommends the alignment of the apertures with the solder pads under 50 to 100x magnification. The device placement machine should allow fine adjustment in X, Y, and rotation axes. Do not use tweezers when manually mounting the WLCSP on the rework area. Instead, use a vacuum pen to place a new WLCSP unit on the board.

Follow the paste manufacturer's recommendation for the reflow profile, with the maximum temperature not to exceed the package qualification level. Reflow profiles developed for initial placement or rework can also be used. A three-stage (ramp-up, hold, ramp-down) profile may result in a smaller temperature distribution across the site.

6 Cypress WLCSP Reliability Test Data

6.1 Component-Level Reliability Test

Cypress performs all component-level reliability tests according to internal specification 25-00112. Its qualification procedures and requirements comply with various industry standards including JEDEC/IPC and MIL-STD-883. Table 5 lists the major stress tests for component-level reliability.

Table 5. WLCSP Qualification Stress Tests

Test Method	Test Conditions	MSL	Duration
Temp cycles Cond B	–55 to +125 °C	MSL 1	1,000 cycles
HAST	180 °C/85% RH	MSL 1	96 hours
Pressure cook test	121 °C/100% RH	MSL 1	96 hours
High-temperature storage	150 °C	NA	1,000 hours

Detailed qualification reports for specific Cypress WLCSP products are available upon request through Cypress Sales or on the website (www.cypress.com).

6.2 Board-Level Reliability Test (Temp Cycles)

6.2.1 Board Assembly Information

- Daisy chains are built on the circuit board and device for the worst-case Cypress WLCSP product (typically the largest die size by technology family) and are surface mounted on the test PCB.
- FR4 printed circuit board of 1.0-mm nominal thickness with 8-layer metal stackup, according to the IPC-9701 standard.
- Pad diameter of 0.2 to 0.21 mm with NSMD pads, no via-in-pad, with organic surface protectant (OSP) for metal land finish are used for board mount.
- 15 units per board with single side mount, Sn-Ag 3 percent-Cu 0.5 percent solder paste (no clean type).
- 0.20-mm square aperture, 0.08-mm thickness metal stencil.
- Reflow profile for Pb-free Sn-Ag-Cu at peak is 238 °C.

6.2.2 Test Condition (JESD 22-A104D/IPC-9701)

- Temperature: –40 to +85 °C or –40 to +125 °C with 15 minutes of dwell time for a typical frequency of two cycles per hour or less
- Monitoring: Dynamic electrical monitoring is done during the temperature cycle test.

6.2.3 Failure Criteria

- Threshold resistance of electrical open according to JEDEC criteria
- Minimum cycles with no failure: 1,000 cycles at –40 to +85 °C, 500 cycles at –40 to +125 °C

6.3 Board-Level Test (Drop Test) According to JESD22-B111 (for Handheld Products)

6.3.1 Board Assembly Information

- Same as Board-Level Reliability Test (Temp Cycles)

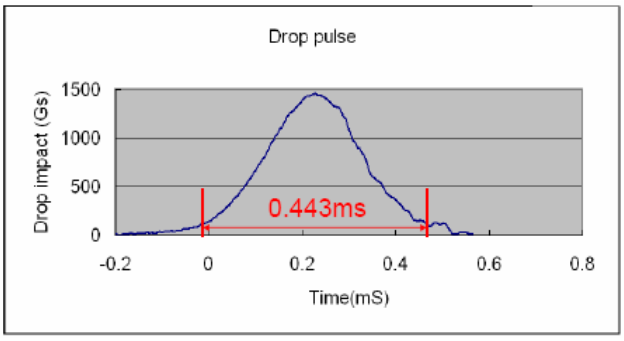
6.3.2 Test Condition

- Drop test specification and procedure according to JEDEC criteria (JESD22-B111)
- 200 drop tests are conducted.

6.3.3 Failure Criteria

- Any intermittent discontinuity or resistance greater than 1 kΩ lasting for 1 µs or longer is a failure event. The first event of intermittent discontinuity followed by three additional such events during five subsequent drops is a registered failure
- Minimum drop test cycles with no failure: 100 drops

Figure 21. Drop Test Impact Force Profile



6.4 Board-Level Cyclic Bend Test

6.4.1 Board Assembly Information

- Same as Board-Level Reliability Test (Temp Cycles) except nine units per board

6.4.2 Test Condition JESD22-B113

- Four-point cyclic bend at 3 Hz
- Support span: 110 mm
- Load span: 75 mm
- 2.0-mm anvil deflection

- 1E6 bend cycles

6.4.3 Failure Criteria

- Threshold: Greater than 1 kΩ
- Minimum bend test cycles with no failure: 1E6 bend cycles

7 Package Thermal Resistance

The thermal resistance of each WLCSP product is in the device datasheet. The typical simulation condition is either a 2- or 4-layer PCB, depending on the application of the product.

Θ_{JA} (Theta Ja, thermal resistance of junction-to-ambient) in accordance with JEDEC EIA/JESD51-2 is a value that measures the conduction of heat from the hottest junction temperature on the die to the ambient near the component. Typically, the heat generated on the die surface passes through the silicon to the exposed package surfaces and through solder balls to the board.

Θ_{JC} (Theta Jc, thermal resistance from junction-to-case) represents the thermal performance of the package when the board is adhered to a metal housing or heat sink.

8 WLCSP Handling During Packing, Shipping, and SMT

8.1 WLCSP Off-Board Reprogramming

To prevent mechanical handling damage in programmer sockets, either order WLCSP devices for programmable products that are custom programmed by Cypress or use onboard programming. Cypress is not responsible for damage incurred from off-board programming due to improper device handling. The manufacturer must carefully design the socket to prevent MOS on the WLCSP. The plunger tool must not present extreme mechanical overdrive while testing spring loads. The contact area of the plunger must be optimized.

8.2 Susceptibility to MOS

Because of the properties of silicon and other materials used in IC circuitry, WLCSPs are brittle and subject to MOS damage when not handled and assembled properly. Unlike conventionally packaged parts, even moderate MOS damage can render a WLCSP nonfunctional or unreliable. The three primary detrimental mechanical stresses are compressive, flexural, and impact. Take care when designing, handling, and manufacturing to adequately protect WLCSPs against impact and mechanical stress. For an overview of MOS, refer to Table 6.

8.3 WLCSP Packing and Shipping on Carrier Tapes

WLCSPs are vulnerable to oxidation, contamination, and mechanical damage. Open and handle boxes, moisture barrier bags, and reels only at approved workstations. Loose units that are outside their original carrier tape packing are compromised. They cannot be recovered by picking them up with tweezers and loading them on the carrier tape.

Cypress selected the original packing materials to provide adequate protection to the WLCSP units through a normal distribution and manufacturing process. WLCSPs are delivered in tape and reel to be fully compatible with standard high-volume packing. The features of tape and reel materials are in accordance with product packaging.

Verify that the reel has all the following, as shown in Figure 22:

- Manufacturing label for device lot identification
- ESD warning label (It is not necessary to place an ESD sticker in the lock reel with an embossed ESD label.)
- Humidity indicator card (HIC)
- Desiccant pack: Use one 60-g desiccant pack for each bag. For 30-g packs, place two packs for each moisture barrier bag (MBB).

Figure 22. Packing Requirements for Cypress WLCSP

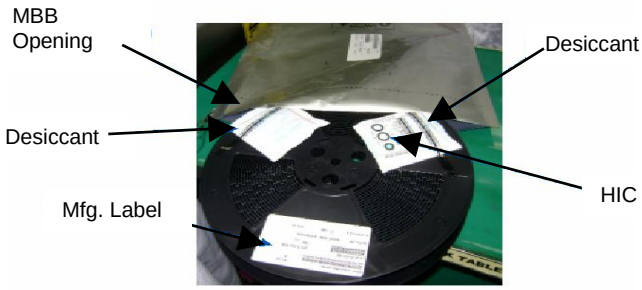
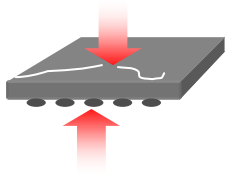
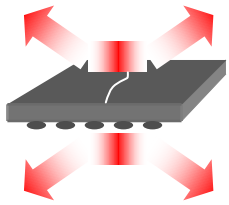
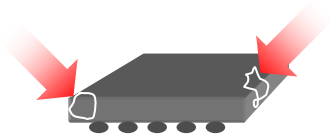


Table 6. WLCSP MOS Summary

Moment of Force	Probable Causes	Recommendations
 COMPRESSIVE/OVERDRIVE	▪ Mishandling on carrier tapes ▪ In-transit shipment handling issues ▪ Board mount pick and place process ▪ Pick and place on sockets and carrier tapes during off-board programming ▪ Mishandling after SMT	▪ Proper CAD fit analysis on carrier tapes ▪ Corner stress release tape design ▪ Thicker backside laminate ▪ Optimized pick and place parameter for carrier tape handling and SMT ▪ Observe proper handling protocols in all subprocesses at SMT
 BENDING/FLEXURAL	▪ Unoptimized underfill fillet height due to manual dispensing ▪ Unoptimized fillet width due to manual dispensing ▪ CTE mismatch due to wrong underfill ▪ Drop and vibration forces during handling	▪ Optimize manual dispensing process needle-to-die edge distance. ▪ Optimize underfill volume so fillet height and width follow. ▪ Make sure that underfill matches or is close to the CTE of the solder joints. ▪ Observe proper handling protocols on all subprocesses at SMT.
 BLUNT FORCE/IMPACT	▪ Mishandling on carrier tapes ▪ In-transit shipment handling issues ▪ Needle-to-die edge collision during manual underfill process ▪ Board mount pick and place process ▪ Pick and place on sockets and carrier tapes during off-board programming ▪ Mishandling after SMT ▪ Other subprocess handling at SMT	▪ CAD fit analysis on carrier tapes ▪ Corner stress release tape design ▪ Thicker backside laminate ▪ Optimized dispense position and needle design suitable for manual underfill dispensing ▪ Optimized pick and place parameter for carrier tape handling and SMT ▪ Proper handling protocols on all subprocesses at SMT

The moisture sensitivity level (MSL) of a component indicates its floor life and storage conditions after the original container has been opened. All Cypress WLCSP products are moisture sensitivity level 1 (MSL1) at 260 °C reflow peak temperature, in accordance with JEDEC standard J-STD-020.

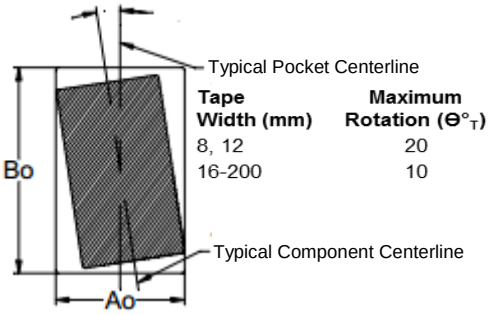
CAD fit simulation between unit and tray pockets is done during carrier tape selection to test proper fit and prevent MOS of the WLCSP parts during shipment.

Standard carrier tape and reel selection is in accordance with EIA-481-D-2008. All conditions stated in this standard must be met to ensure proper handling of the WLCSP. Figure 23 shows the EIA-481-D-2008 standard for maximum component rotation and lateral movement on the tape pocket.

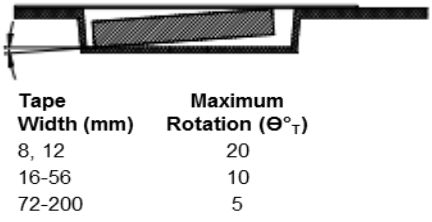
An example of a standard carrier tape drawing for a WLCSP device with the dimensions 3.215 × 3.215 × 0.51 mm (±0.5 mm) is shown in Figure 24.

Figure 23. EIA-481-D-2008 Standard

Maximum Component Rotation for Punched and Embossed Carrier

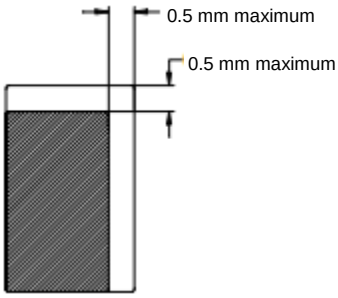


Top View

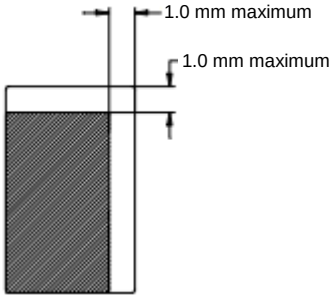


Side View

Maximum Lateral Movement for Punched and Embossed Carrier

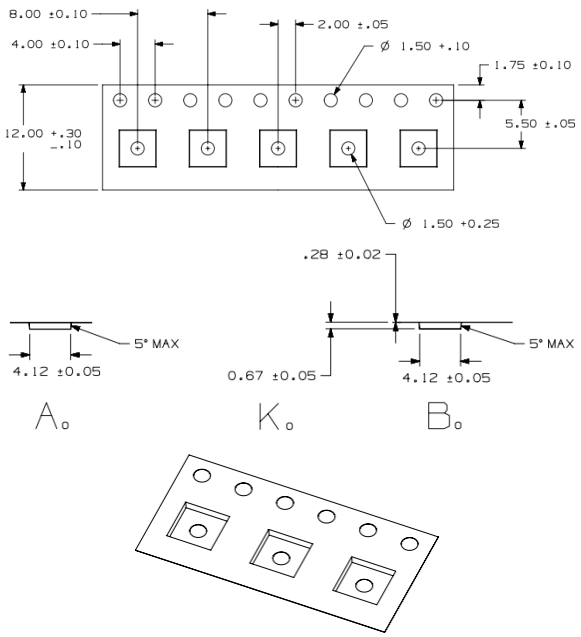


8 mm and 12 mm Tape



16-200 mm Tape

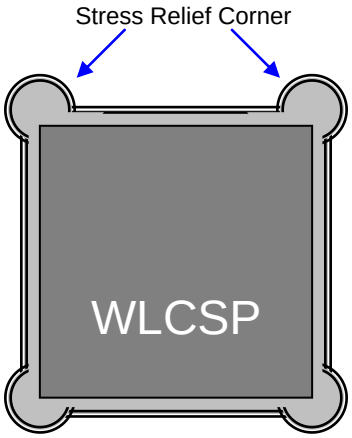
Figure 24. Standard Carrier Tape Drawing for WLCSP



A hole on the pocket of the carrier is available to prevent air buildup during WLCSP placement on the pocket. This prevents misplacement from backflush and mechanical damage from stress during the placement of units. For other WLCSP package sizes, contact Cypress Support (www.cypress.com/support) to obtain the appropriate carrier tape configurations.

Carrier tape designs may also incorporate corner stress relief areas such as the dog bone carrier tape shown in Figure 25.

Figure 25. Dog Bone Carrier Tape Design



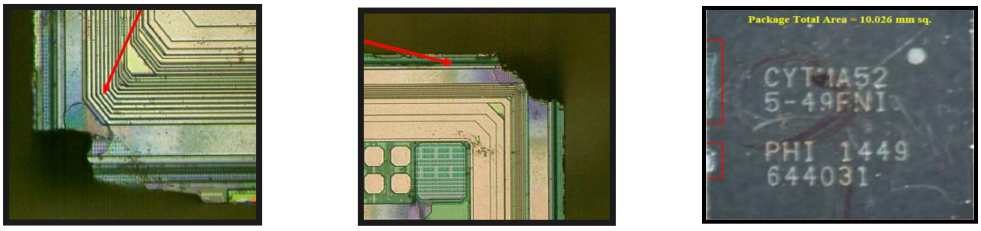
9 Primary Failure Modes at SMT

9.1 Die Chipping

Because it is composed of polymers, crystalline lattice silicon, and ultrathin active metal circuitry, the package of the WLCSP is fragile. Cracks of any form can propagate when the package is subjected to sustained MOS. Damage to circuitry may result in complete or partial functional loss, while backside lamination peel off does not affect the functionality of the package, as shown in Figure 26.

Backside lamination peeling on the marking side is acceptable if it does not exceed 10% of the die area.

Figure 26. Gross Chip-out and Backside Lamination Peel Off

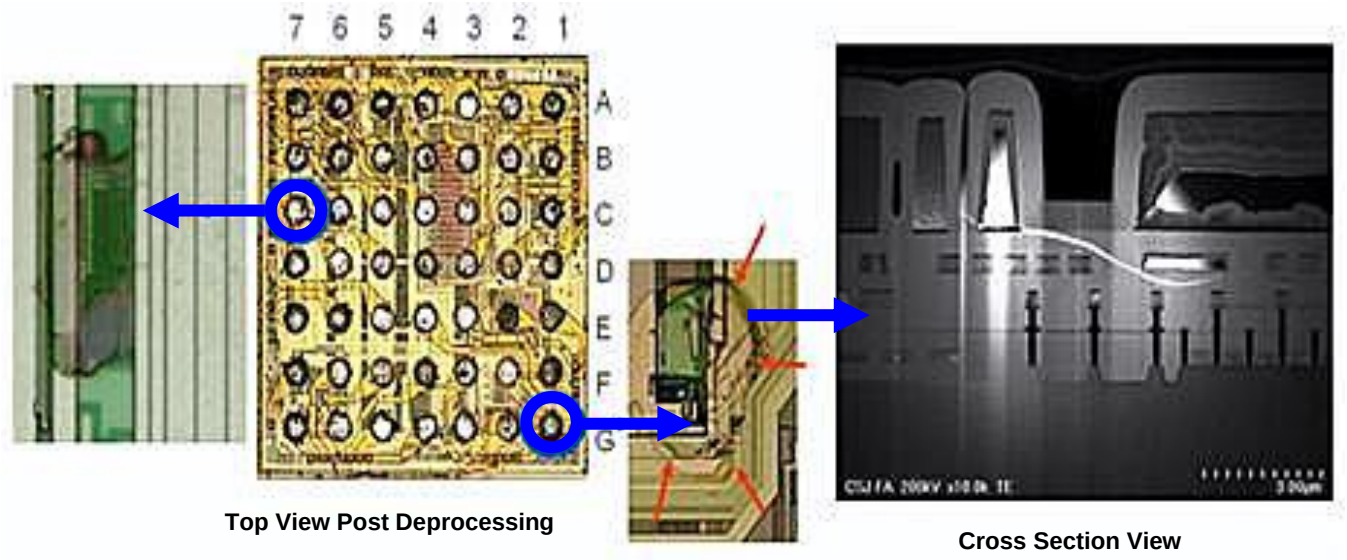


9.2 Passivation to Metal Layer Damages

The solder ball of the WLCSP directly attaches to the active side of the die. This allows compressive stress dissipation from the solder ball to underlying layers of passivation, UBM, and active metal circuitry. This stack of layers is a few tenths of a micron thick and is prone to MOS. Although the repassivation layers (such as P1, P2, UBM, and RDL) provide some level of physical protection, these areas are prone to compressive force during pick and place. When not optimized, this can change the critical dimensions of the inner circuitry, which allows cut metal traces and shorted interconnects.

Exposure to bending and tensile mechanical overstresses can inflict similar damage within the circuit layer, as shown in Table 4. Unlike obvious blunt force impact and cracks, these failure mechanisms may not be readily visible without time-consuming and costly WLCSP deprocessing, cross section and SEM/TEM, or high magnification examination (Figure 27).

Figure 27. WLCSP Deprocessed, Showing Massive Passivation to Metal Layer Damage



9.3 UBM-Solder Ball-PCB Pad Interconnect Failure

The most common field failure mechanism of WLCSP occurs on the UBM to PCB pad interconnect system. The following are a partial list of failure locations and scenarios:

- **UBM to solder joint crack:** This interconnect failure typically exhibits itself as an intermittent continuity failure during electrical testing (Figure 28). For the WLCSP with underfill, it appears as a white spot during CSAM. The cross section shows a crack propagating between the solder to UBM interface. Typical causes are thermal shock post reflow due to a sudden change in temperature from reflow to cold ambient temperature and rapid cooldown. Blunt force impact can also trigger this failure when applied in a shearing direction.
- **Solder to PCB pad crack:** This type of failure exhibits intermittent to direct open circuit failures during electrical testing. The crack can extend from partial to full disconnect of the solder ball to the PCB pad. A solder to copper pad crack can be caused by a shearing force impact while the WLCSP is mounted on the PCB. In some cases, flexural stress attributed to CTE mismatches can also trigger this failure.
- **PCB pad lift:** This is another form of solder to PCB pad crack. It is common to NSMD copper PCB pad patterns, because there is no solder mask overlapping to hold the copper pad. As the solder joint dissipates MOS, this type of failure occurs because of multiple thermal exposures during rework or component replacement.
- **Intermetallic (IMC) formation:** Intermetallic growth between UBM to solder and solder to copper PCB pad is normal between alloys of two metals when exposed to multiple temperatures during SMT (Figure 29). When initiated, intermetallic growth propagates until all of the available metals are consumed. In most cases, multiple reflow and rework during SMT causes premature intermetallic growth, which shortens the life of the solder joint. These failures are often exhibited by brittleness in the solder joint, which results in continuity or structural failures.

Figure 28. UBM – Solder Joint Crack

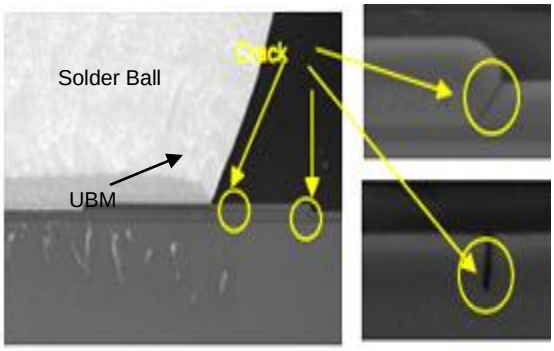
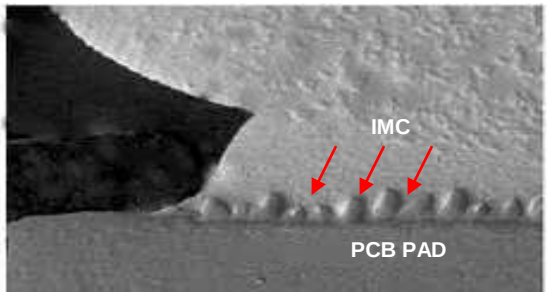


Figure 29. IMC Formation



- **Drop test failures:** The Cypress WLCSP is commonly used in handheld multimedia applications. This application exposes the WLCSP to mishandling such as dropping the PCB board. This event exposes the interconnect system to mechanical shock that is more than the allowable load that the materials can bear. The absorbed impact from this MOS dissipates quickly to the solder joint interconnect and can cause solder joint fracture, which can yield intermittent continuity failure during electrical testing. The Cypress WLCSP has undergone Board Level Reliability Testing and has passed all Drop Test requirements in accordance with JESD22-B111 (for Hand-Held Products).
- **Failures related to fatigue:** When mounted on the PCB, the WLCSP is exposed to repetitive differential expansion and contraction of various interacting elements. This phenomenon is known as a mismatch in CTE between the different materials on the board, which results in a cyclic fatigue force. This form of MOS can weaken the interconnect and result in electrical failures. Time domain reflectrometry (TDR) is a nondestructive analytical tool that you can use to verify interconnect failure locations between the WLCSP and the PCB. TDR employs a short rise time pulse transmitted along the interconnect, where each conductive trace has its own electrical signature. These electrical signatures are in the form of wave signals. A failing unit generates a signal that tells whether the discontinuity occurs at the die level, bump level, or PCB level.

10 Reference Documents

1. Amkor Technology, “Application Note for Surface Mount Assembly of Amkor’s Eutectic and Lead-Free CSPnl™ Wafer Level Chip Scale Packages.”
2. AN73071, “Design and Manufacturing with Summit Microelectronic’s WLCSP Products,” Summit Microelectronics Corp., Pages 2–3, April 2, 2010.

Document History

Document Title: AN69061 - Design, Manufacturing, and Handling Guidelines for Cypress Wafer Level Chip Scale Packages

Document Number: 001-69061

Revision	ECN	Origin of Change	Submission Date	Description of Change
**	3228586	BSC	04/15/2011	New application note.
*A	3381728	WYSI	10/10/2011	Complete update and rewrite to include changes in WLCSP Handling, SMT Guidelines, SMT Rework. Updated template.
*B	3649974	WYSI	08/30/2012	Added Electromagnetic Shielding Guidelines for SMT Updated template according to current Cypress standards Text and grammar edits Replaced most images, tables, and graphics
*C	4345117	KSH	04/14/2014	ECN Sunset due, no change on the content.
*D	4930956	WYSI	09/23/2015	Updated underfill process section and recommendations Text and grammar edits

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