# Design and Simulation of a FPGA-based Demodulator for Low-bit Remote Subcarrier Signal

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***Abstract*— This paper mainly introduced a FPGA-based design model for low-bit Remote Subcarrier. This demodulation method is designed to accomplish carrier synchronization and bit synchronization quickly and effectively. It can achieve synchronization in FPGA which refer to the theory of software wireless. We should validate the arithmetic whether can satisfy the need for feasibility and reliability. The Simulation results of the design model show the model can meet the demodulation request.**

***Keywords : Low-bit rate; Remote Sub-carrier; FPGA; Carrier synchronization***

## I. INTRODUCTION

With the further investigator of deep space exploration, demands for the quality of deep space control communications is increasing including precision, speed, bit error rate (BER), etc.Because of the long distance, the received signal power is very small, so it can not have a high code rate in the process of data transmission. A certain code rate corresponds to a ratio between the input bit energy and the noise power spectral density ( $E_b/N_0$ ). In the process of transmission, it needs a narrow bandwidth of phase-lock loop when the data transfer rate is low, but it may reduce the dynamic capability of the phase-lock cloop. The technology of low-bit rate data transfer is a key issue. The improving on the credibility of remote cell in satellites establishes the safety and credibility running of satellite[1].

## II. THE DESIGN OF DEMODULATOR

### A. The Structure of the Demodulator

With the development of wireless, software-defined radio idea has been applied in remote communications, not only can reduce the hardware size and cut costs, but also can improve accuracy, versatility and portability of the system. Versatility and portability are all better if the ideas of software wireless used. According to the characteristic of remote control sub-carrier input signal and the requirements of the demodulation performance, a reasonable all-digital demodulator for remote control sub-carrier signal should be designed to satisfy these conditions. The demodulator shown in Fig.1 is designed to meet the requirements of the low-bit rate. It can also be used to the demodulation of high-bit rate data.

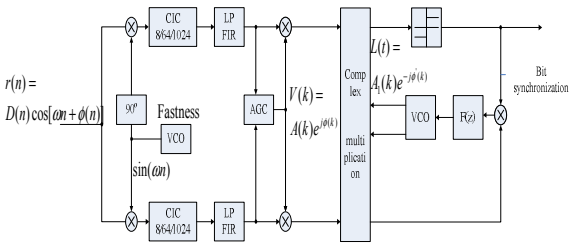


Fig.1. The structure of the demodulator

The Carrier recovery loop in this demodulator is costas loops with hard-limited in-phase channel I[2]. It is different from the traditional costas loops. The signal after hard-limiting in the channel I multiplied by singal in channel Q to obtain the phase error signal. The Gardner arithmetic

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can be used for bit-Synchronization [3]. Digital Automatic Gain Control accommodates the amplitude of base-band signal to mediate. It remains the signal output from carrier synchronization loop basically constant power.

The main features of demodulator shown in Fig.1 are that both of digital down converter (DDC) and automatic gain control (AGC) are one-way operation. In this demodulator, the branch of feedback is short, time delay is small, the system will be more stable. The carrier tracking loop and bit synchronization loop which are very important to the stability of the system keep independent of each other. Another feature of demodulator shown in Figure 1 is that the sampling rate and code rade remain relatively constant for the carrier recovery loop and bit synchronization loop, the system parameters can be the same for different code rates, just only need to change the extraction parameter of decimation filter. The loop filter chose is the ideal loop points.

### *B. Loop Parameter Design*

#### *1) SNR in Loop*

Periodic hopping is the noise under the action of the loop phase error happened cycle skipping phenomenon, loop jump is a loss of lock once a cycle. The loop needs certain $SNR_L$ to make the loop maintain the longer period of time locking (non-occurrence of periodic hopping). As a command frame needs to transmit for a certain period of time before it stops, it should ensure that a data frame in the transmission occurred during the jump probability is less than a circle of design specifications.

The average time of periodic hopping is as follows:

$$T_{AV} = \frac{\pi^2 \rho I_0^2(\rho)}{2B_L} \tag{1}$$

Where

$$\rho = SNR_L = \frac{1}{\sigma^2_{\theta no}} \tag{2}$$

$\sigma^2_{\theta no}$ is the carrier phase noise variance which output from phase-locked loop VCO[4]. $I_o$ is zero-order modified Bessel function of first kind. In process of design, the time of periodic hopping has great impact on $SNR_L$.

The relation of $SNR_L$ and $E_b/N_0$ is:

$$SNR_L = \frac{E_b}{N_o}\frac{R_b}{B_L} = K\frac{E_b}{N_o} \tag{3}$$

Where $K$ is the ratio of code rate and the loop noise equivalent bandwidth.

#### *2) Loop Capture and Tracking Speed*

According to the PLL parameters, we can analyze the PLL loop capture and tracking speed.

Where rapid capture bandwidth is:

$$\Delta\omega_L = 2\xi\omega_n \tag{4}$$

The time of phase capture is:

$$T_L = \frac{5}{\xi\omega_n} \tag{5}$$

The condition of the achieved for time of phase capture is that the admission of deviation is far smaller than the frequency of rapid capture frequency. The time of rapid capture phase is not applied when the code rate is low, in this condition, the frequency capture can be used to settle this problem.

The time of the capture frequency is:

$$T_p = \frac{\Delta\omega_o^2}{2\xi\omega_n^3} \tag{6}$$

In this demodulator model, the extraction parameters of decimation filter can be changed to meet the requests of different code rates. For example, the parameters are set for low code rate which is 7.8125bps, and then magnify the extraction parameters according to the ratio between the code rate and 7.8125bps. In the abstract, the contradiction between the frequence offset of carrier and the time of capture is not serious when the code rate is higher than 7.8125bps, such as 125bps, 1000bps, 2000bps, etc. In this condition, the loop bandwidth can be designed much smaller to improve the value of $SNR$ in loop ($SNR_L$). It can make the system locked in much lower value of $E_b/N_0$.

## III. PREPARE YOUR PAPER BEFORE STYLING

The model of demodulator is constructed based on

Matlab/Simulink. The major used tool boxes and module libraries are Simulink sources, communication blockset and DSP blockset. Those module libraries offered the familiar communication modules, and it provides effective help to the FPGA design of signals simulation.

### C. *The Simulation of Carrier Loop*

The capture and tracking of carrier synchronization loop are relatively complex when meet the burst signal. Fig.2 is the results of simulation for carrier tracking loop.

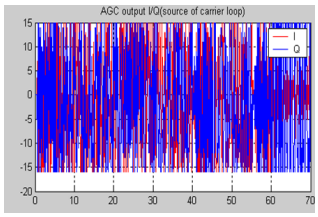


Fig.2(a) The result of AGC

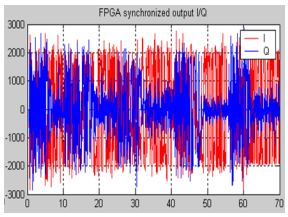


Fig.2(b) baseband signal

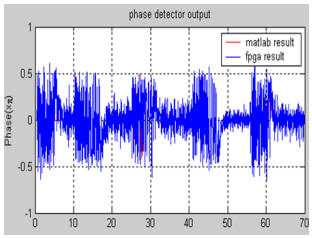


Fig.2(c) phase detector output

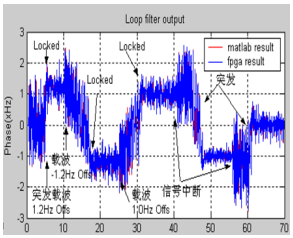


Fig.2(d)Loop filter output(burst signal)

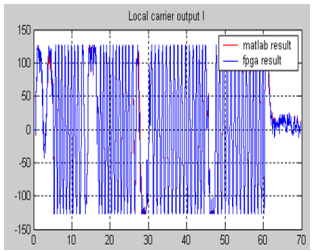


Fig.2(e) Local carrier output I

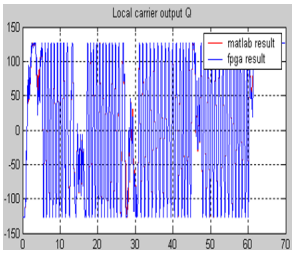


Fig.2(f) Local carrier output Q

Fig.2. the Comparison of carrier tracking loop between matlab & FPGA

Fig. 2 is easily to understand except Fig.2 (d). It will be explained as follows. First, there is only noise, then input burst carrier (frequency offset: 1.2 $H_z$) about at 5 seconds. After captured the signals about at 10 seconds, setting carrier frequency offset to -1.2 $H_z$. After captured, at about 26 seconds, changing carrier frequency offset to 1 $H_z$. After locked, interrupt signals at 40 seconds and 57 seconds (end of burst input), after finished these 2 burst signals. After a period of loss of lock, the signals are both captured after input burst different frequence offset.

### D. *The Simulation of* $SNR_L$ *and* $BER$

The simulink model can be used to simulate the $SNR_L$ and $BER$. In the process of the simulation, the theoretical $SNR_L$ results are based on the liner model in the analysis[4].

$$SNR_L = \frac{1}{\sigma_{\theta no}^2} \tag{7}$$

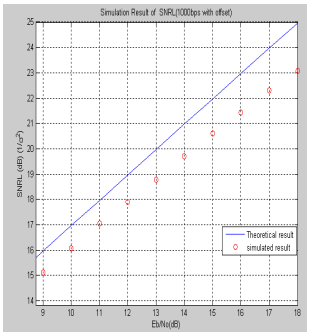


Fig.3(a)1000bps $SNR_L$

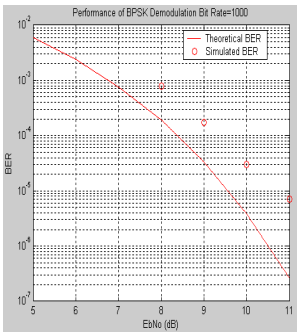


Fig.3(b) 1000bps BER

Fig.3 The comparison of SNRL and BER in 1000bps

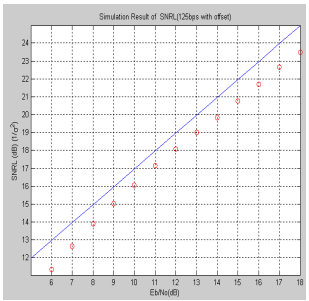


Fig.4(a)125bps $SNR_L$

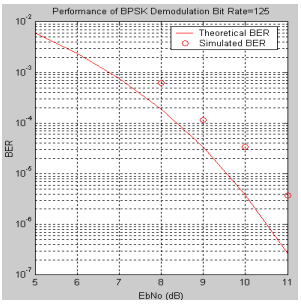


Fig.4(b) 125bps BER

Fig.4. The comparison of SNRL and BER in 125bps

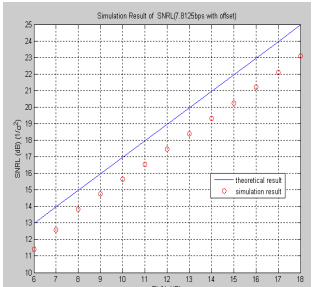


Fig.5(a)7.8125bps $SNR_L$

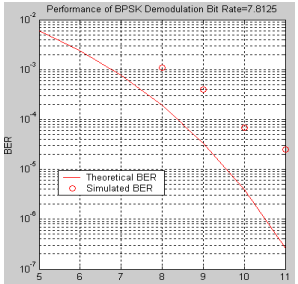


Fig.5(b) 7.8125bps BER

Fig.5. The comparison of SNRL and BER in 7.8125bps

Fig.3, Fig.4 and Fig.5 show the results of $SNR_L$ and $BER$ compared between theory value and simulation value in

different code rates. It can easily find that $SNR_L$ is bigger than 15dB when $E_b/N_0$ is bigger than 10dB, the bit error rate of the demodulator is lower than$1 0^{-4}$. These can satisfy the requests of the conditions of capture and bit error rate.

## IV. CONCLUSIONS

In this paper, a demodulator for remote control sub-carrier signal is designed to meet the conditions in low bit-rate. The simulation results show the feasibility of this demodulator. The results refered in this paper are the preliminary investigation of the demodulation system. Next, the demodulation arithmetic will be downloading to FPGA to validate whether this demodulation can meet our requests.

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