Multi-channel data acquisition and wireless communication FPGA-based system, to real-time remote monitoring

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***Abstract*—In this paper, a low cost, stand-alone and configurable data acquisition system with wireless communication to remote host is presented. The system allows recording up to eight multiplexed analog signals, with 12-bits resolution in variable ranges and a maximum sampling rate 11,500 S/s for each channel. The realization of the systems was done using FPGA as the main chip, and control multi-channel ADC chip to collect data. The data are transmitted to the host using wireless connectivity technologies Bluetooth or XBee, these data can be displayed and analyzed by computer application. The channels, sampling frequency and transmission rate can be configured by the user.**

Keywords: Multi-channel data adquisition; FPGA based Digital System; Wireless data adquisition.

I. INTRODUCTION

Data acquisition (DAQ) systems are widely used in industrial and laboratory applications such as control, monitoring, test and measurements, automation, and so on. The main purpose of DAQ systems is to measure physical phenomena, converting the analog signal into a digital signal and then sent the data collected for further analysis [1]. Commercial DAQ cards are differentiated by their viabilities such as sampling frequency, scale of acquired signal, power and requirements, but are generally high in cost and they need a PC at the collection site. Embedded systems to data acquisition are often require the participation of the embedded operating system [2], thus the attention must be given to co-design techniques that can accelerate software execution. The software execution time can be reduced by implementing critical loops in hardware. The Field Programmable Gate Arrays (FPGA) technology has blurred the distinction between hardware and software, because it can be configured to implement specific software function to reduce cycle time for execution.

In the high speed multi-channel data acquisition system where the signals require be detected at the same time and sometimes includes multiple sampling frequencies, it is necessary interacting with the control system unit to configure o establishing the corresponding parameters, such that the signals can be processed either on board or outside. The modern onboard FPGA can not only overcome the deficiency of the MCU or the DSP and meet the requirements of system for real-time and synchronization, but also for embedded applications using System-On-Chip (SoC) FPGA platforms with the high level coordination, versatility and full-stacked operative system.

By the other hand, the widespread adoption of wireless technologies such as Bluetooth (IEEE 802.15.1) [3] and XBee (IEEE 802.15.4) [4] in the last years for industrial, scientific and domestic applications, have emerged in mobile applications. The Digi XBee series OEM modules implement the IEEE 802.15.4 radio and ZigBee networking protocol and have become very popular in application system development.

In this paper, our researching is on the design and implementation of multi-channel real-time data acquisition and wireless transmission system developed using FPGA platforms, with Bluetooth and XBee technologies. Such a design has the advantages of low cost, flexibility, scalability, interoperability, as compared with other commercial systems.

The rest of the paper is organized as follows. In Section 2, related works are presented. In Section 3, the overall system architecture and hardware components are described. In Section 4, the design hardware architectures are presented in details. Experimental results are presented in Section 5 to demonstrate the usefulness of the design. Finally, the conclusions are presented in Section 6.

II. RELATED WORK

In the literature, different designs to DAQ FPGA-based systems have been reported. The main characteristics are high-speed [5, 6] and portable data acquisition system based on FPGA and USB connection [7, 8, 9, 10], or networking [11, 12], with multi-channel [13, 14, 15] and

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oriented to specific applications: radio astronomy [16], positron emission tomography (PET) scanners [17, 18], detection of methane drainage in coal mine safety field [19], special devices [20].

So in this paper, a reconfigurable data acquisition system and user configuration is designed and implemented with methods of static reconfiguration.

III. System Architecture

A. General system diagram

Multi-channel data acquisition system is development on DE0-Nano-SoC board of Terasic [21], and is composed of Linear Technology A/D converter multi-channel, Altera Cyclone V FPGA chip, and wireless interface (Bluetooth and Xbee) off-chip. The system is synchronized through master clock board. Hardware architectures provide clock signal for ADC and for wireless interface device. The block diagram of the general system is shown in Figure 2.

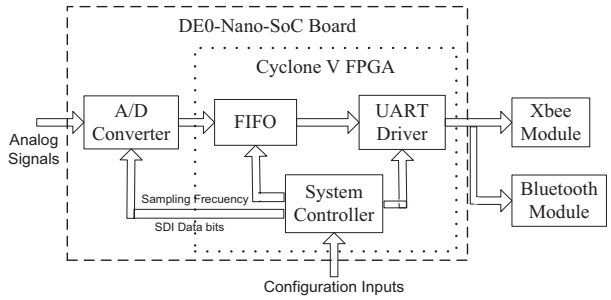


Figure 1. Block diagram of the DAQ system. Architectures to storage (FIFO) and interface drivers are implemented on FPGA chip.

B. Hardware components

Linear Technology LTC2308. The A/D converter chip used is the LTC2308 which has is a low noise and power consumption, 500Kbps, 8-channel, 12-bit and SPI/MICROWIRE compatible serial interface. The internal conversion clock allows the external serial output data clock (SCK) to operate at any frequency up to 40MHz [22].

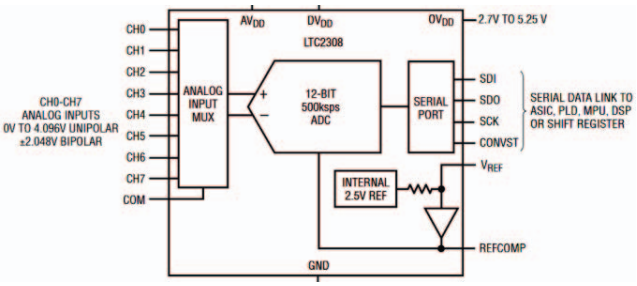


Figure 2. Block diagram ADC LTC2308. The analog input MUX and operation modes can be programmed by a 6-bit D_{IN} word through SDI terminal.

Altera Cyclone V FPGA. The Altera Cyclone V SE 5CSEMA4U23C6N device, has Dual ARM Cortex-A9 MPCore with CoreSight System On Chip (SOC), integrated circuit Cyclone V SE FPGA, with 40K Logic Elements, maximum CPU clock frequency 925MHz, 224 18x19 Multipliers and 5,761 kb embedded memory.

XBee Pro S1. The Digi XBee series modules implement the IEEE 802.15.4 radio and ZigBee networking protocol for its physical layer and MAC. Zigbee is a high-level communication protocols used to create Wireless Personal Area Networking (WPAN). Transmission distances to 10–100 meters depending on power output and environmental characteristics. ZigBee devices work in 868 MHz, 915 MHz and 2.4 GHz frequency bands having a maximum data rate 250Kbps.

HC-06 Bluetooth Module. This module is a serial interface converter to Bluetooth adapter. The module can be set by AT commands, and have two modes: master and slave, but the mode cannot be switched during the process of communication. The IEEE 802.15.1 standard defined the Bluetooth specification to create WPAN.

IV. Hardware Architectures of the System

A. A/D Converter Control.

SPI controller was developed to control the conversion process. A long CONVST pulse is used. The Figure 3 shows time diagram to programming ADC. According to the diagram, "the conversions are initiated by a rising edge on the CONVST input. Once a conversion cycle has begun, it cannot be restarted. Between conversions, a 6-bit input word (D_{IN}) at the SDI input configures the MUX and programs various modes of operation. As the D_{IN} bits are shifted in, data from the previous conversion is shifted out on SDO After the 6 bits of the DIN word have been shifted in, the ADC begins acquiring the analog input in preparation for the next conversion as the rest of the data is shifted out" [22]. The Figure 4 shows the Register Transfer Level (RTL) architecture corresponding to SPI controller.

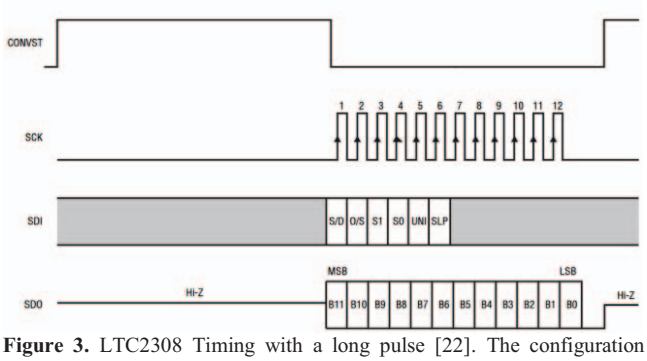


Figure 3. LTC2308 Timing with a long pulse [22]. The configuration signals are: S/D can be Single-Ended/Differential-bit; O/S can be Odd/Sing-bit; S1 and S0 addressing select bit; UNI can be Unipolar/Bipolar, and SLP active Sleep Mode.

B. FIFO architecture.

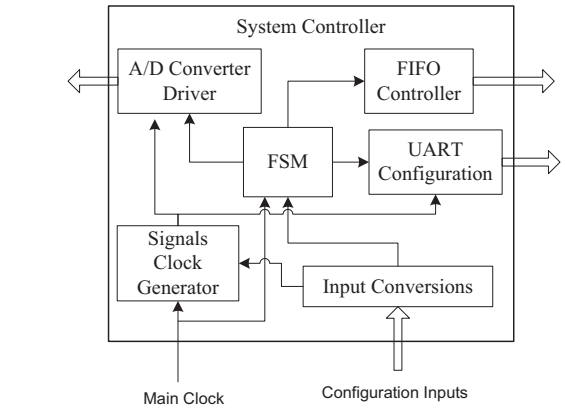
A dual clock First-In First-Out (FIFO) buffer was used to cross data between the two different clock domains: sampling frequency A/D converter (from 1 to 25 MHz) and transmission rate (from 9600 bps to 921600 bps). In the systems clock frequency domain, the serialized outputs are continuously stored in twelve bits shift register, before they will send to FIFO buffer. The Finite State Machine (FSM) FIFO, in the system controller, wait until collected data of the last active channel will be sent through wireless module, before start a new acquisition.

C. UART Driver.

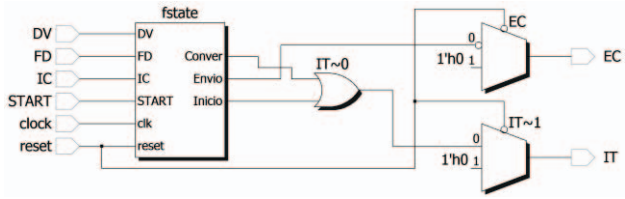
A general port input/output (GPIO), is used to send serial data. Subsystem architecture (Fig. 6) is used to set the baud rate in the output. UART interface will read out the data when it is filled in the FIFO, and send to the host through the wireless link, and finally the data can be display in the host with software application.

D. System controller.

The architecture of the control system includes FSM to coordinate the synchronization of signal acquisition (SPI module), and serial transmission to the Dual port FIFO. The Figure 7 b) and Figure 8 show the corresponding architectures.



a)



b)

Figure 7. a) General system controller blocks and theirs interconnections between modules. b) The FSM to synchronize the acquisition and sending of the data to the FIFO memory.

This architecture was complete multi-channel data acquisition system and wireless transmission using EDA tools (Quartus II, of Intel FPGA) and languages (VHDL) to design FPGA, and the system simulation and verification in the EDA software (ModelSim). Matlab is used to receive data through serial port in PC.

E. Bluetooth and Xbee modules.

The wireless modules are configured through AT commands. The mode for both is slave to receive data from UART driver architecture. With both can be set baud rate from 9600 to 921600 b/s. Terminal software like Putty [23] was used configure the devices.

V. Experimental Results

To test the system, we use analog signal produced by the function generator and observe the final data stored in the PC memory. Then we compared data with the original analog signal. The Figure 9 and Figure 10 shows the practical wave and storage wave corresponding.

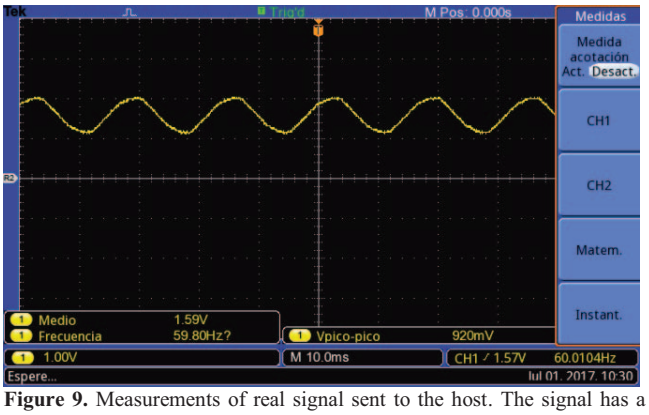


Figure 9. Measurements of real signal sent to the host. The signal has a 1.59Vdc and 920mVpp, frequency of 60Hz. This signal is obtained from digital oscilloscope.

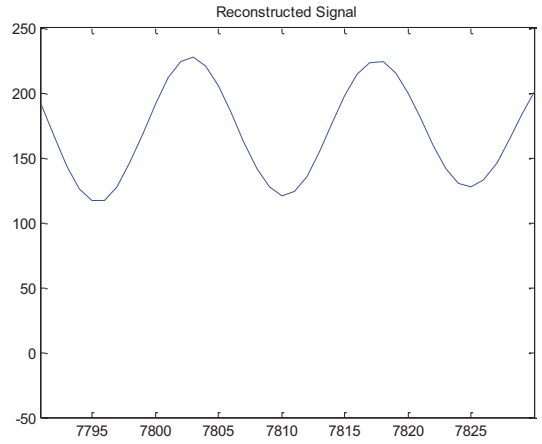


Figure 10. Signal reconstructed with Matlab, from data received from the remote DAQ system. Each cycle is represented by 16 samples. The resolution for this case is established in 10mV/bit.

VI. CONCLUSIONS

This work described a multi-channel data acquisition system based on FPGA. Several architectures were made to development the system. Experiments show that the system can convert the analog signals to digital signal and send to host computer. The data acquired by using custom sampling frequency and baud rate. The entire system is designed to be simple, stable and low cost.

The future work, the system will be expanded to use with embedded ARM processor included in the board.

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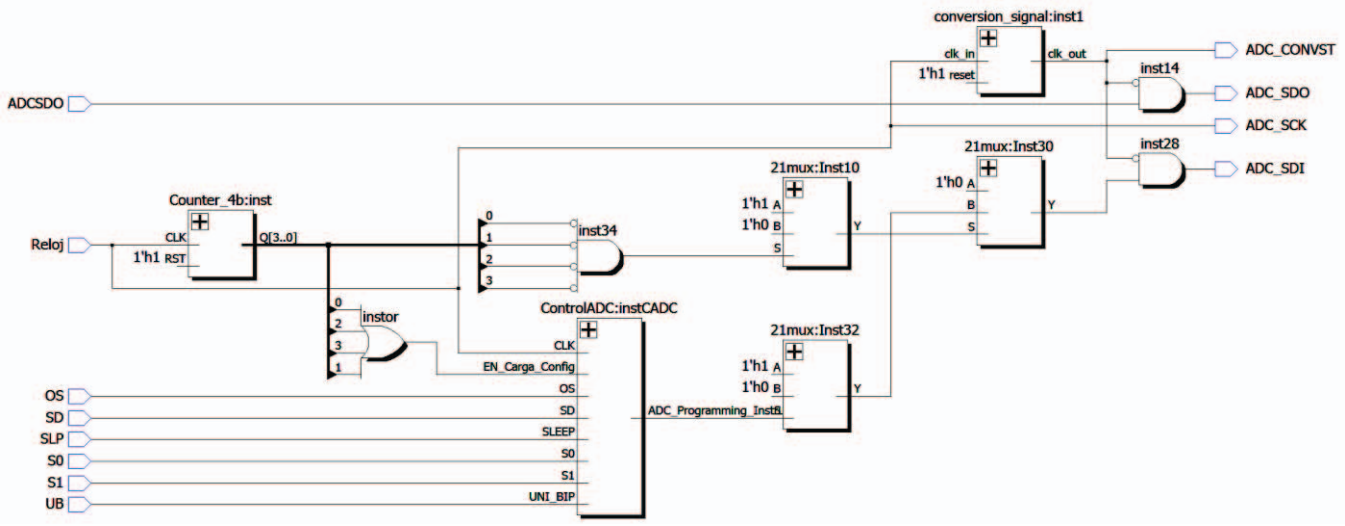


Figure 4. SPI controller architecture. The 4-bit counter counts 16 cycles in high for the acquisition of the signal and 16 cycles in low for the sending of the 12 output bits parallel to the configuration instruction for the next sample.

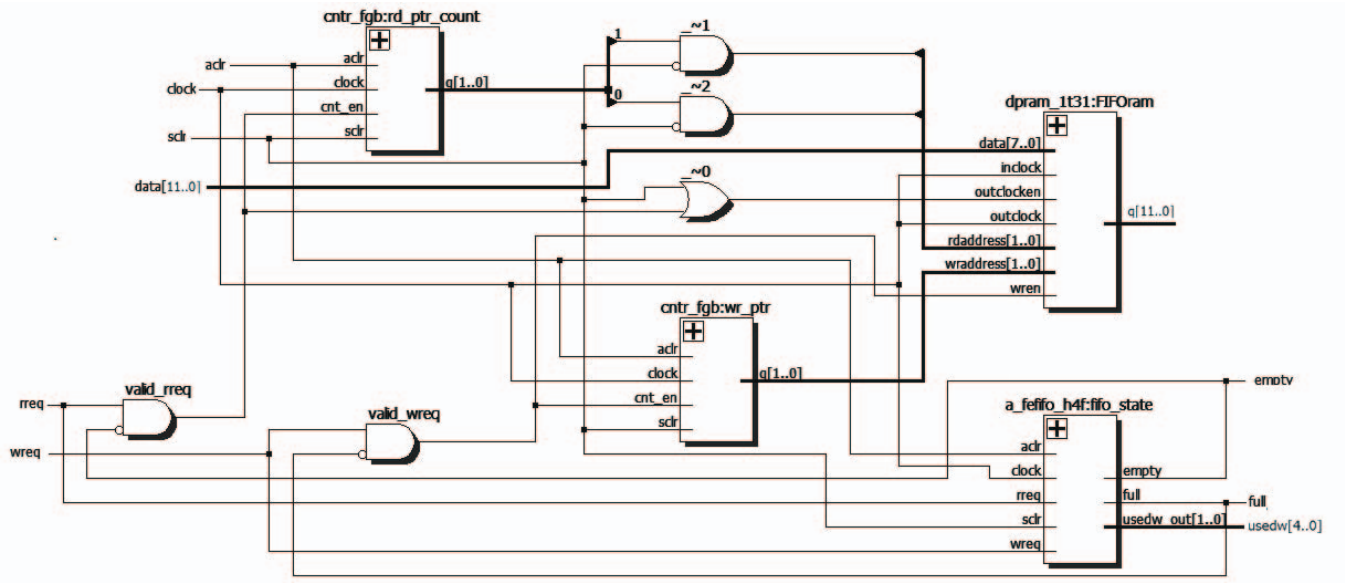


Figure 5. Dual-port FIFO architecture. Two counters are used to addressing the data to read and write operations. Dual ported RAM of 12-bit and 32 words is used to storage data.

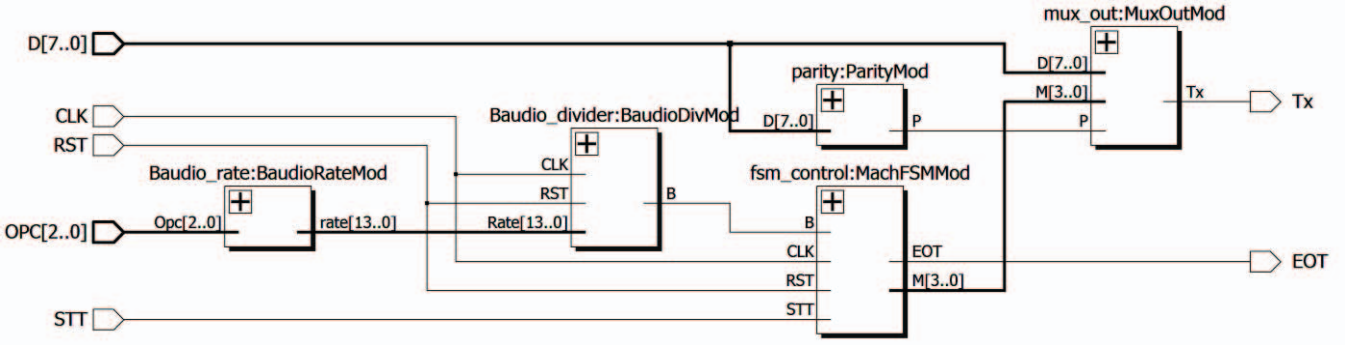
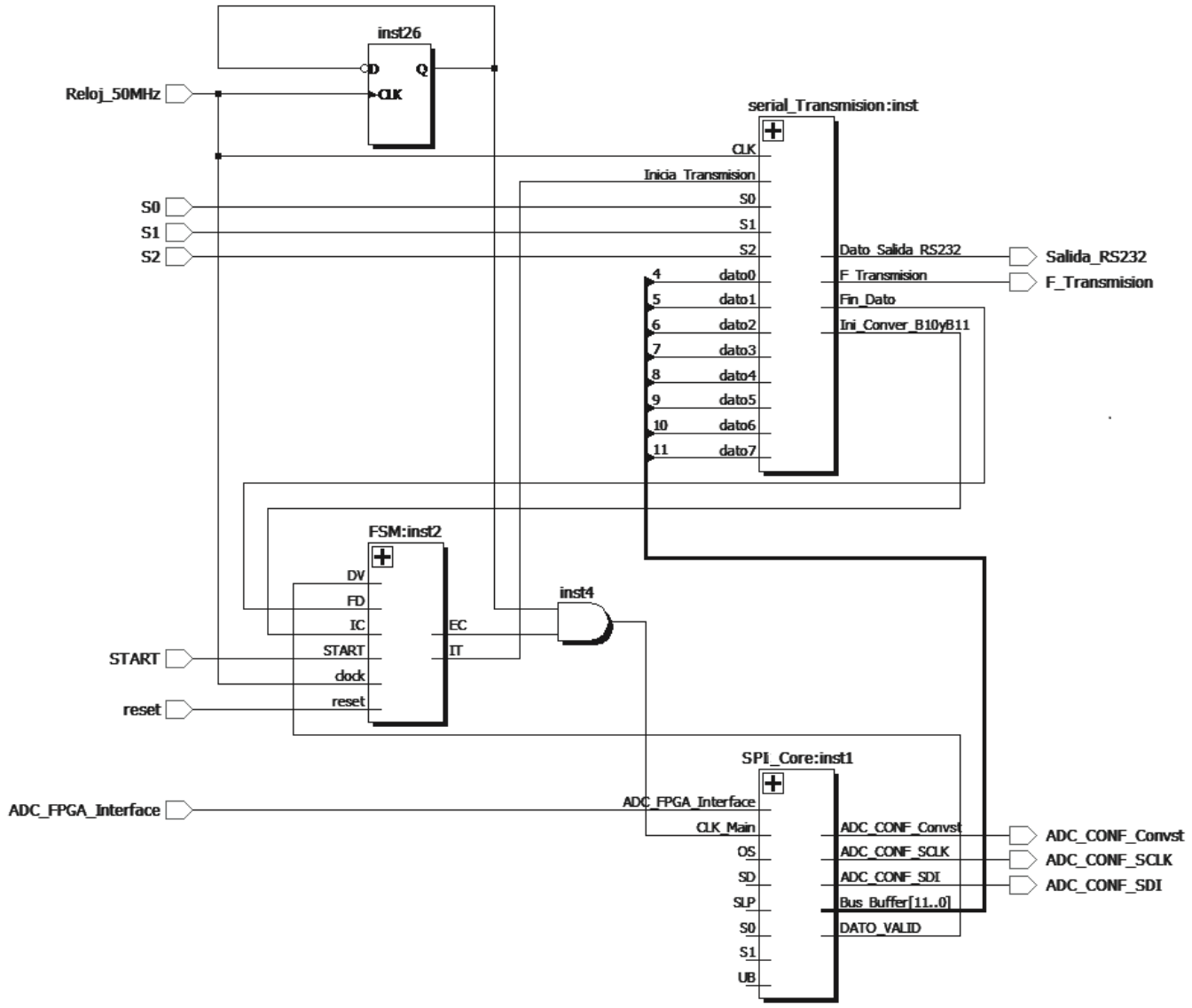


Figure 6. UART driver architecture. Serial transmission use baud rate module. ParityMod verify odd parity. MachFSMMod together MuxOutMod send data from FIFO to serial data in the transmission format.



c)

Figure 7. a) General system controller blocks and theirs interconnections between modules. b) The FSM to synchronize the acquisition and sending of the data to the FIFO memory, c) RTL architecture of the subsystem, it show the interconnections between SPI core and serial transmission register.