AVR077: Opto Isolated Emulation for the DebugWIRE

8-bit AVR® Microcontrollers

Application Note

1. Features

- **DebugWIRE emulation**
- **Opto isolation**
- **Works with AVR Dragon™ and JTAGICE mkII**

2. Introduction

This application note describes how to implement an optoisolated interface for the DebugWIRE.

This device could help the debug of applications with non isolated power supply like ballast, motors, vacuum cleaners, refridgerators, etc.

Design engineers should use debugging tools on applications with high current and/or voltage with great care; indeed, these applications can only be interruped at specific points of the sofware. A break point at a wrong location can easily damage the application.

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3. Theory of Operation

On several applications, the MCU is powered from a low cost power supply that is connected directly to the AC line voltage. In this case, the MCU V_{DD} and V_{SS} pins can reach hundreds of volts above ground. If a debugging tool were connected directly to the MCU with such an application, two possibilities could occur depending on the construction of the tool's power supply:

- If the tools power supply is isolated from ground, debugger will rise to AC line potential in relation to ground. So the debugging tool will be at a voltage potentially lethal for the end user.
- If the tools power supply is referenced to ground, a short between mains and ground will occur, resulting in a blown fuse or a damage to either the application or the development tool.

Fortunately, using the debug facilities of AVR microcontrollers with an optoisolated interface, designers can safely and quickly develop these applications

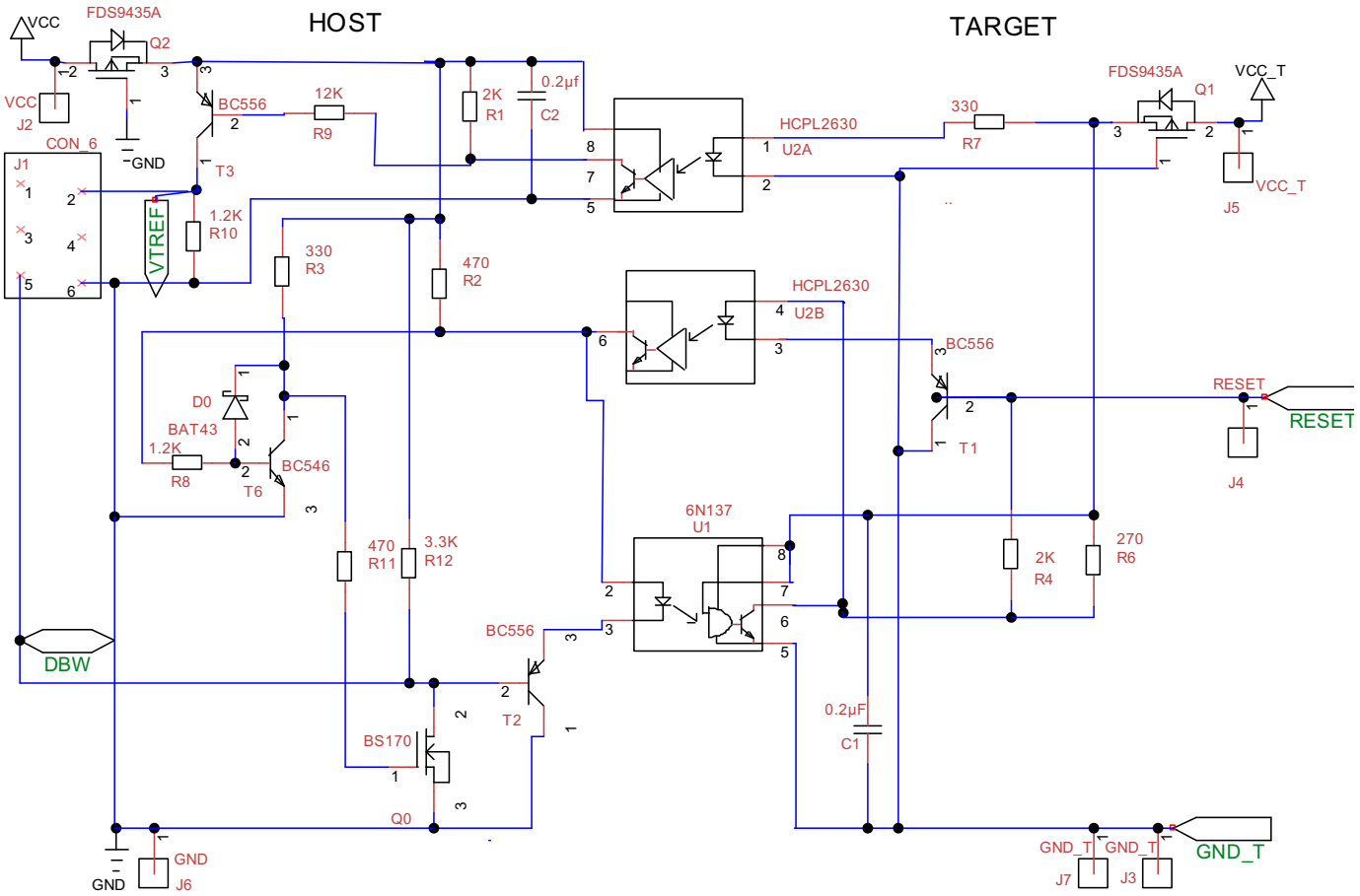
This application note shows the debug interfaces for the AVR DebugWIRE. Similar principles could be used to isolate SPI programming interface or JTAG debug interface.

4. DebugWIRE opto-isolation

The opto isolation circuit for the debugWIRE is shown on Figure 4-1. Two signals are optoisolated, the target voltage indication (Vtref) and the Reset/DebugWIRE signal.

The interface circuit is protected against reverse polarity by the PMosfet Q1 and Q2.

Figure 4-1. opto isolation circuit



4.1 Target voltage indication

The circuit uses the upper opto isolator and works as follows:

• If the target is powered, the LED in U2A is lit. This is detected by the photodiode and the optoisolated transistor is switched ON pulling the base of transistor T3 low. The output VTREF is then at high level.

• If the target is not powered, the LED in U2A is not lit. The optoisolated transistor is switched OFF, so the base of transistor T3 is pulled high. The output VTREF is then pulled down at low level by the R10 resistor.

4.2 DebugWIRE interface

The circuit uses the two lower opto isolators to allow opto-isolated bidirectional communications on a bidirectional digital pin.

The communication from Host to Target works as follows:

• When DBW is at low level, transistor T2 is ON and the LED in U1 is lit. This is received by the photo detector and switches on the transistor in U1. This causes RESET to be pulled to ground thru resistor R4 and also ensures that the LED in U2B is OFF. This means the transistor in U2B is also OFF.

• When DBW is at logic ‘1’, transistor T2 is OFF, The output transistor in U1 is OFF. RESET is pulled high by resistors R4. The LED in U2B is OFF. Thus there is no feedback to DBW.

• If DBW is not driven, for example if it is connected to a tristated I/O pin, it is pulled high by R12. From the description above, it can be seen that the output will then be high also.

• If both DBW and RESET are not driven, both pins will be pulled high.

On the Target side, this simple circuit havs enough strength to drive the reset pin of an AVR.

The communication from Target to Host is similar, but the circuit must be improved to drive the DBW pin of the JTAGICE mkII or the AVRDragon.

• When RESET is at logic ‘0’, transistor T1 is ON and the LED in U2B is lit. This is received by the photo detector and switches on the transistor in U2B so transistor T6 is off. This causes DBW to be pulled to ground by Mosfet Q0 and also ensures that the LED in U1 is OFF. This means the transistor in U1 is also OFF.

• When RESET is at logic ‘1’, transistor T1 is OFF, The output transistor in U2B is OFF. T6 saturates and Q0 is OFF so DBW is pulled high by resistors R12. The LED in U1 is OFF. Thus there is no feedback to RESET.

The circuit is bidirectional. However, the user should not drive both terminals at the same time. This will not cause any damage to the circuit, but it will increase the current consumption

The connector target interface on the JTAGMK2 is shown below:

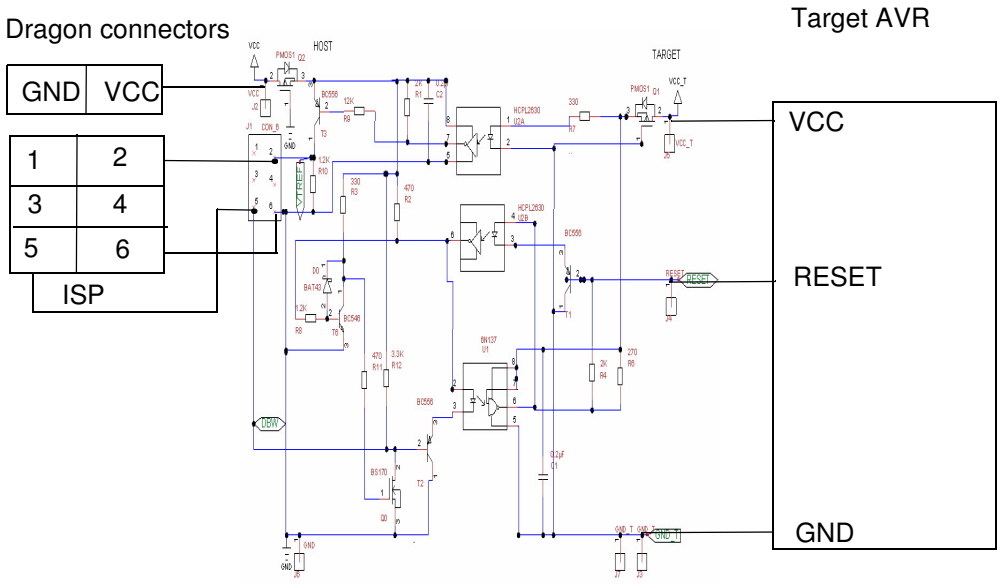
Table 4-1. JTAGMK2 connector

JTAGICE mkII probe	Target pins	Squid Cable Colors	Dragon or STK500 ISP pinout
Pin 1 (TCK)	SCK	Black	3
Pin 2 (GND)	GND	White	6
Pin 3 (TDO)	MISO	Grey	1
Pin 4 (VTref)	VTref	Purple	2
Pin 5 (TMS)	Not present	Blue	Not present
Pin 6 (nSRST)	RESET	Green	5
Pin 7 (Not connected)	Not present	Yellow	Not present
Pin 8 (nTRST)	Not present	Orange	Not present
Pin 9 (TDI)	MOSI	Red	4
Pin 10 (GND)	GND	Brown	Not present

4.3 AVR Dragon interface

Since the AVR Dragon provides the Vcc connector, it is easy to supply the Target side of the opto isolated interface. Figure 4-2 shows the basic principle for this application.

Figure 4-2. DebugWIRE isolated interface with AVR Dragon emulator

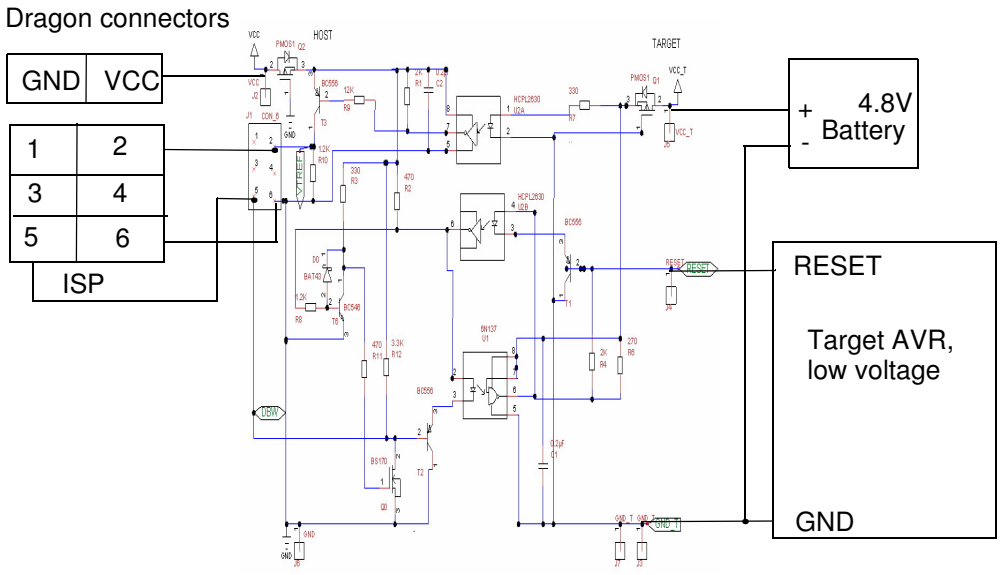


4.4 AVR Dragon interface, low voltage target

When the target works at low voltage, a dedicated battery must supply the interface. Figure 4-2 shows the basic principle for this application.

With this schematic, a permanent current will be drawn on the AVR reset pin protection diode and the VTREF indicates the battery voltage rather than the target voltage. This situation could be improved with few schematic changes: two Shottky diodes to protect the RESET line, one NPN transistor to control the current in U2A when the target voltage in on.

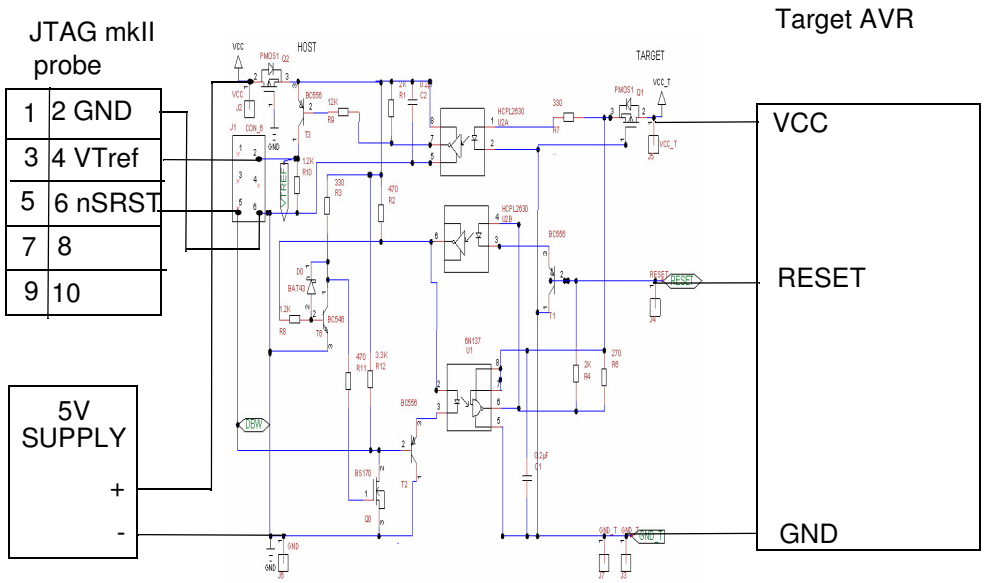
Figure 4-3. DebugWIRE isolated interface with AVR Dragon emulator



4.5 JTAG mkII interface

Using the same interface circuit is also possible with the JTAGICE mkII. As the JTAGICE mkII do not provides a Vcc pin it is mandatory to use an isolated power supply for the target side of the interface. Figure 4-4 shows the basic principle for this application.

Figure 4-4. DebugWIRE isolated interface with JTAG mkII emulator



5. Conclusion

This application note provides a way to use the JTAGICE mkII or the AVR Dragon emulators on non-isolated AC line powered applications.

The components easy fit on a VeroBoard prototype board.

This interface has been tested on a simple application up to 16 MHz at 5V Vcc. Although the optocouplers are not specified for low voltage, the interface works fine at full speed down to 3.6V.

The low voltage target solution has been tested at 8MHz down to 2.2V.

6. BOM

The table below gives the circuit BOM.

Reference	Quantity	Name	Description
C1,C2	1	0.2µF	
D0	1	BAT43	Schottky diode
J1	1	CON_6	6 pins ISP connector
Q0	1	BS170	N Channel FET
Q1,Q2	2	FDS9435A	P Mosfet for reverse battery protection
R1,R4	2	2K	
R10,R8	2	1.2K	
R11,R2	2	470	
R12	1	3.3K	
R3,R7	2	330	
R6	1	270	
R9	1	12K	
T1,T2,T3	3	BC556	PNP general purpose
T6	1	BC546	NPN general purpose
U1	1	6N137	Single channel High Speed Optocouplers
U2	1	HCPL2630	Dual channel High Speed Optocouplers

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