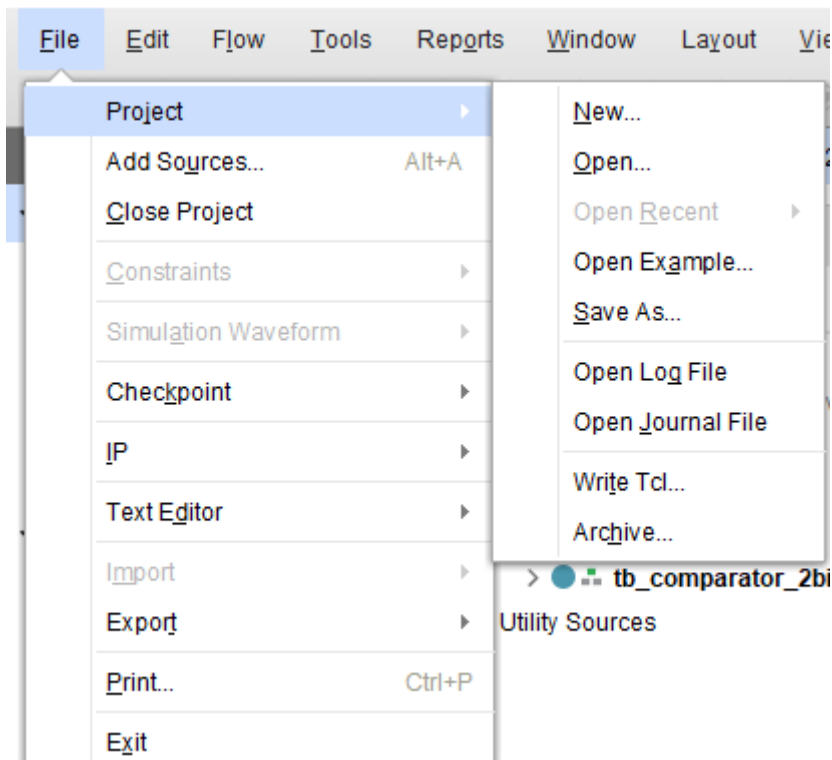
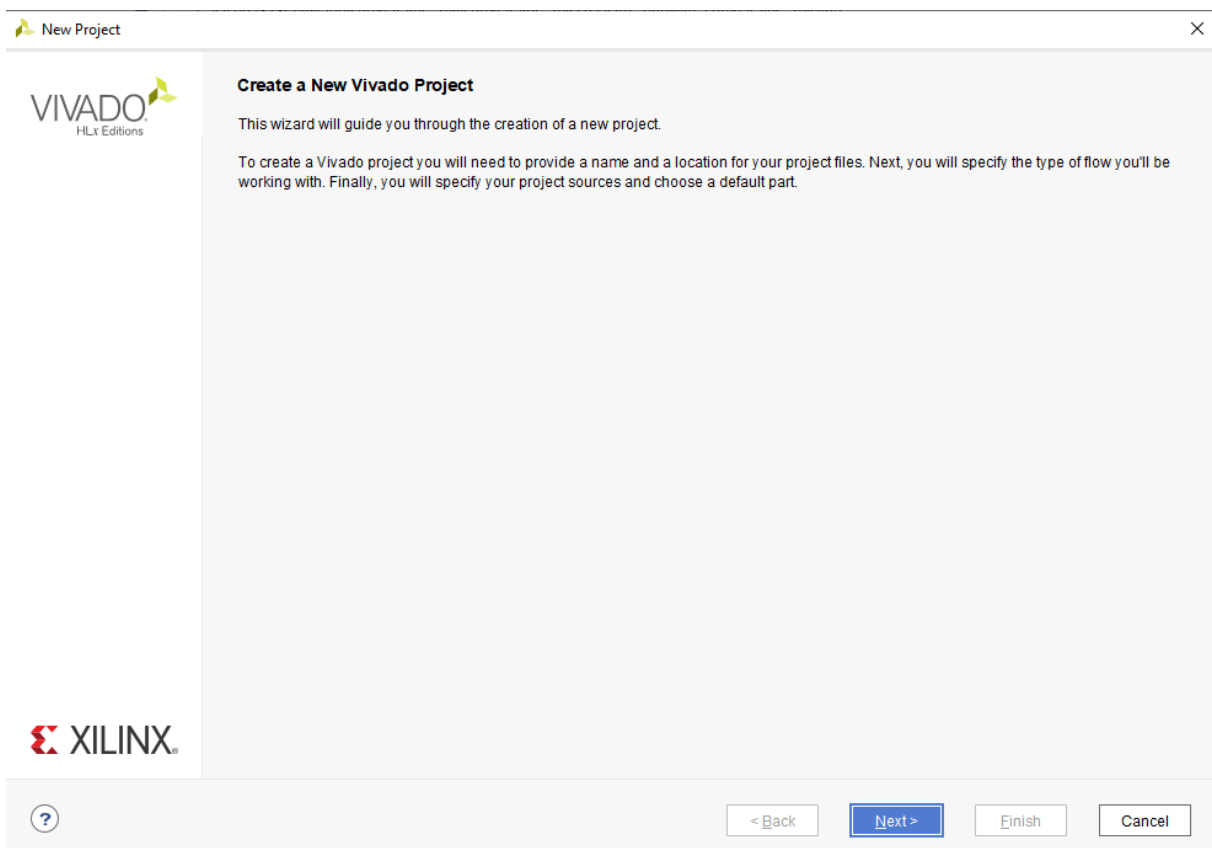


# Založení projektu ve Vivadu

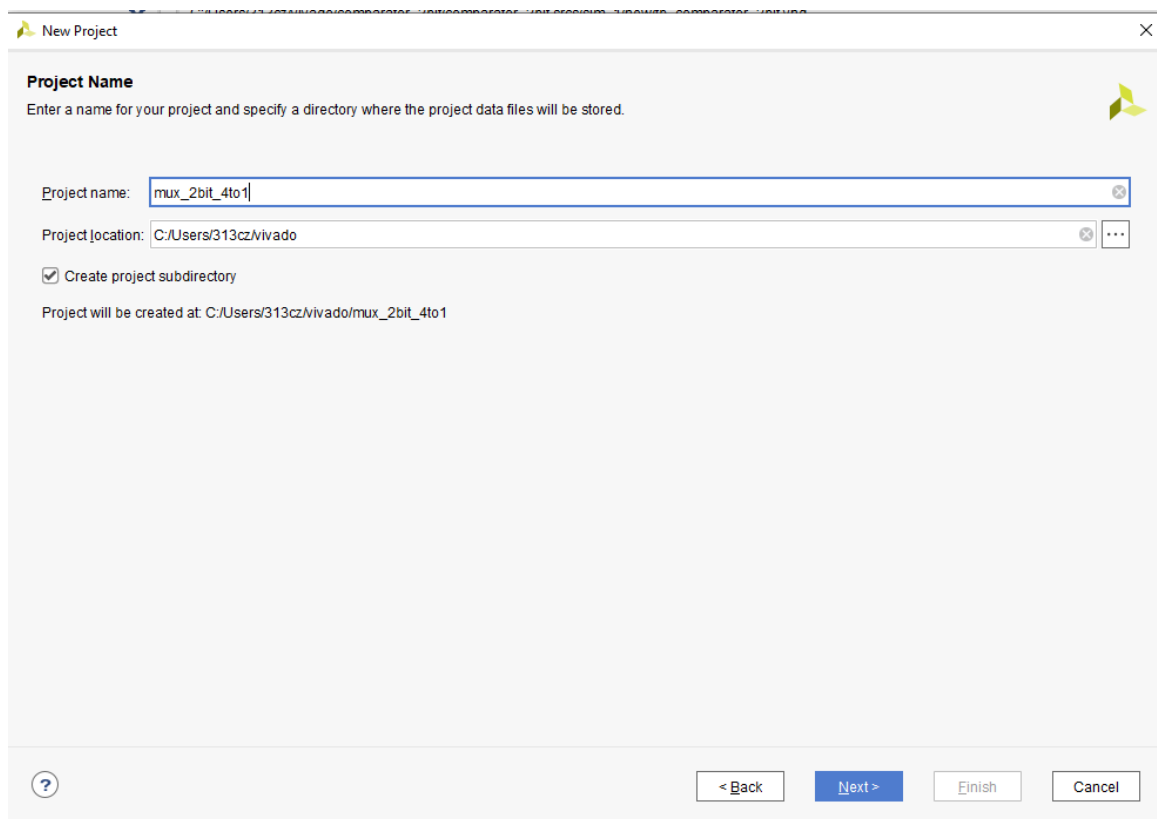
1)Klineme na záložku File/Project/New...



2)Otevře se nám okno s vytvořením nového projektu, klikneme na Next



### 3) Zde zvolíme jméno projektu a jeho umístění



**New Project**

**Project Name**  
Enter a name for your project and specify a directory where the project data files will be stored.

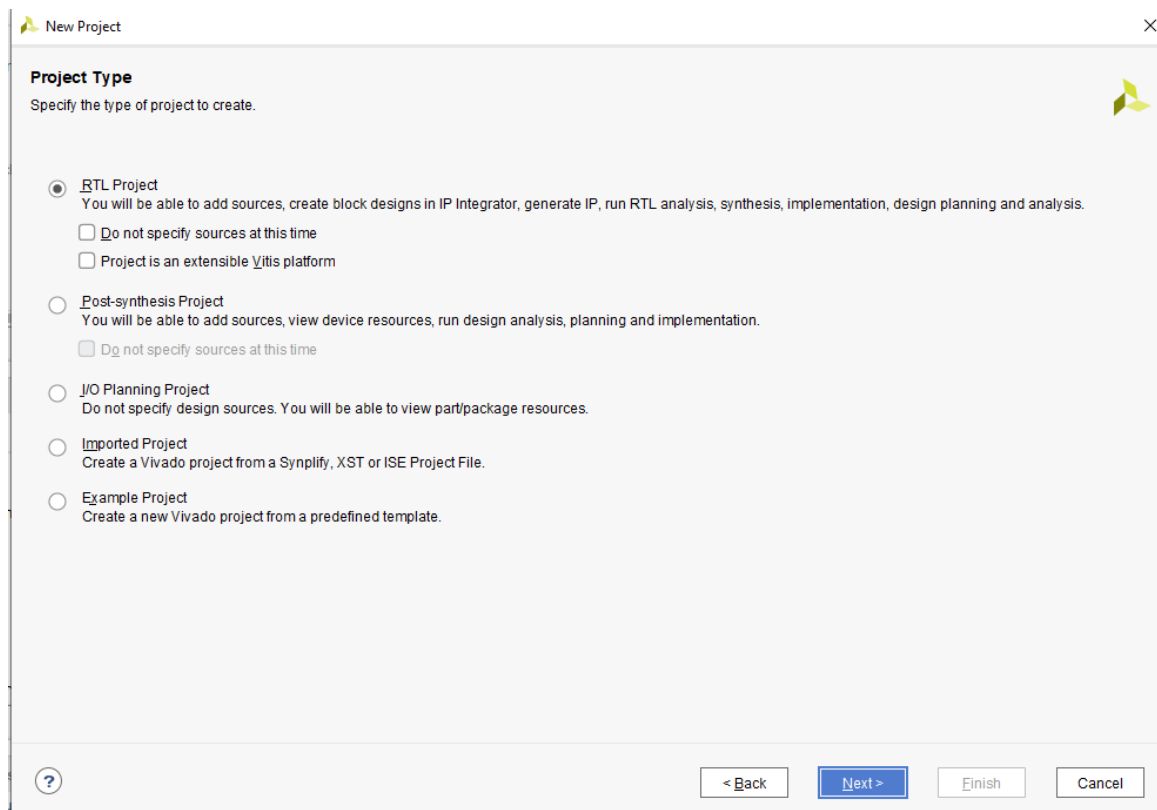
Project name:

Project location:

☒ Create project subdirectory

Project will be created at: C:/Users/313cz/vivado/mux\_2bit\_4to1

### 4) Typ projektu zvolíme RTL



**New Project**

**Project Type**  
Specify the type of project to create.

☒ **RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
☐ Do not specify sources at this time  
☐ Project is an extensible Vitis platform

☐ **Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.  
☐ Do not specify sources at this time

☐ **I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**  
Create a new Vivado project from a predefined template.

5)Vytvoříme VHDL source file se stejným názvem jako projekt

New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

+ | - | ↑ | ↓

Use Add Files, Add Directories or Create File buttons below

Create Source File

Create a new source file and add it to your project.

File type:

VHDL

File name:

mux\_2bit\_4to1

File location:

<Local to Project>

?

OK

Cancel

Add Files

Add Directories

Create File

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

Target language:

Verilog

Simulator language:

VHDL

?

< Back

Next >

Finish

Cancel

+ | - | ↑ | ↓

	Index	Name	Library	HDL Source For	Location
	1	mux_2bit_4to1.vhd	xil_defaultlib	Synthesis & Simulation	<Local to Project>

## 6) Constrain soubory nevytváříme

New Project

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.

+ - ↑ ↓

Use Add Files or Create File buttons below


Add Files

Create File

☐ Copy constraints files into project

? < Back Next > Finish Cancel

7)Nahoře vybereme záložku Boards

 New Project

### Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All

Package: All

Temperature: All

Family: All

Speed: All

Static power: All

Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE
xc7vx415tffv1158-2L	1158	350	257600	515200	880	0	2160	48	0
xc7vx415tffv1158-1	1158	350	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-3	1927	600	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-2	1927	600	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-2L	1927	600	257600	515200	880	0	2160	48	0
xc7vx415tffv1927-1	1927	600	257600	515200	880	0	2160	48	0
xc7vx485tffg1157-3	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-2	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-2L	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1157-1	1157	600	303600	607200	1030	0	2800	20	0
xc7vx485tffg1158-3	1158	350	303600	607200	1030	0	2800	48	0

?

< Back

Next >

Finish

Cancel

## 8) Zvolíme desku Nexys A7-50

New Project





**Default Part**  
Choose a default Xilinx part or board for your project.

Parts | **Boards**

[Reset All Filters](#)

Vendor: All Name: All Board Rev: Latest

Search: Q:

Display Name	Preview	Vendor	File Version	Part
<a href="#">Alpha-Data ADM-PCIE-7V3</a>		alpha-data.com	1.1	xc7vx690tffg1157-2
<a href="#">Kintex-Ultrascale Alphadata board</a>		alpha-data.com	1.0	xcku060-ftva1156-2-e
<b>Nexys A7-50T</b>		digilentinc.com	1.0	xc7a50tiscg324-1L
<a href="#">ZedBoard Zynq Evaluation and Development Kit</a> Add Companion Card <a href="#">Connections</a>		em.avnet.com	1.4	xc7z020clg484-1
<a href="#">Artix-7 AC701 Evaluation Platform</a>				

[?](#) < Back Next > Finish Cancel

## 9) A potvrdíme vytvoření objektu

New Project

**VIVADO**  
HLS Editions

**New Project Summary**

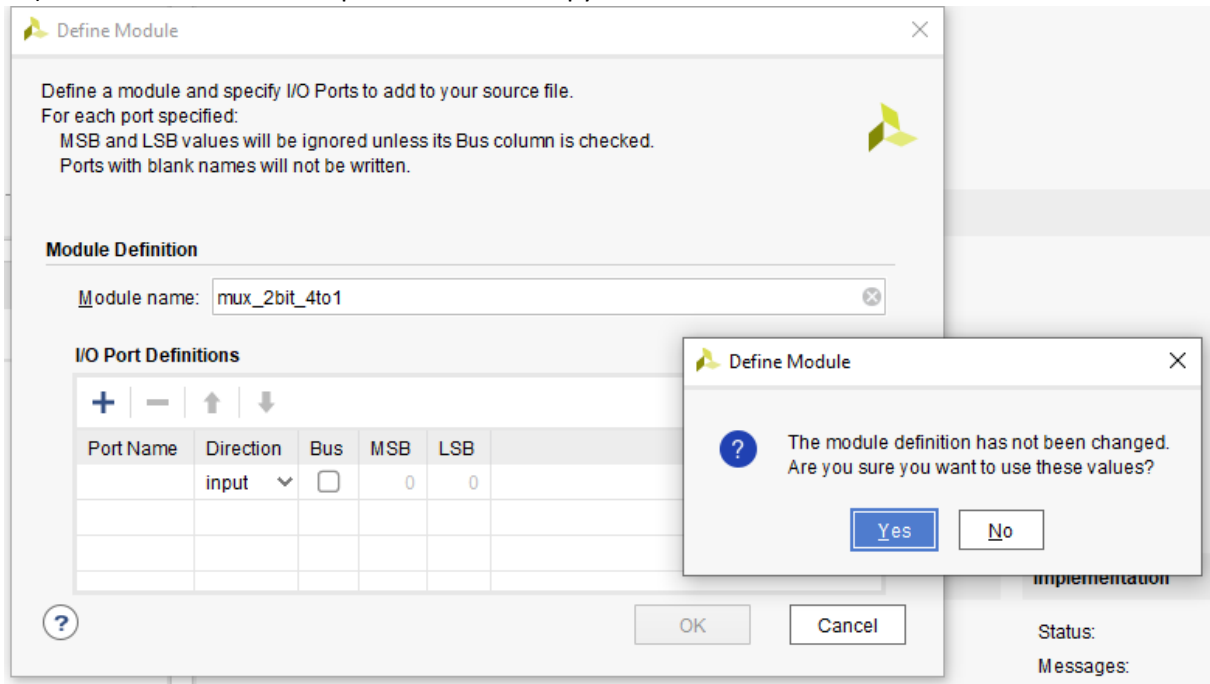
- i** A new RTL project named 'mux\_2bit\_4to1' will be created.
- i** 1 source file will be added.
- w** No constraints files will be added. Use Add Sources to add them later.
- i** The default part and product family for the new project:  
Default Board: Nexys A7-50T  
Default Part: xc7a50tiscg324-1L  
Product: Artix-7  
Family: Artix-7  
Package: csg324  
Speed Grade: -1L

**XILINX**

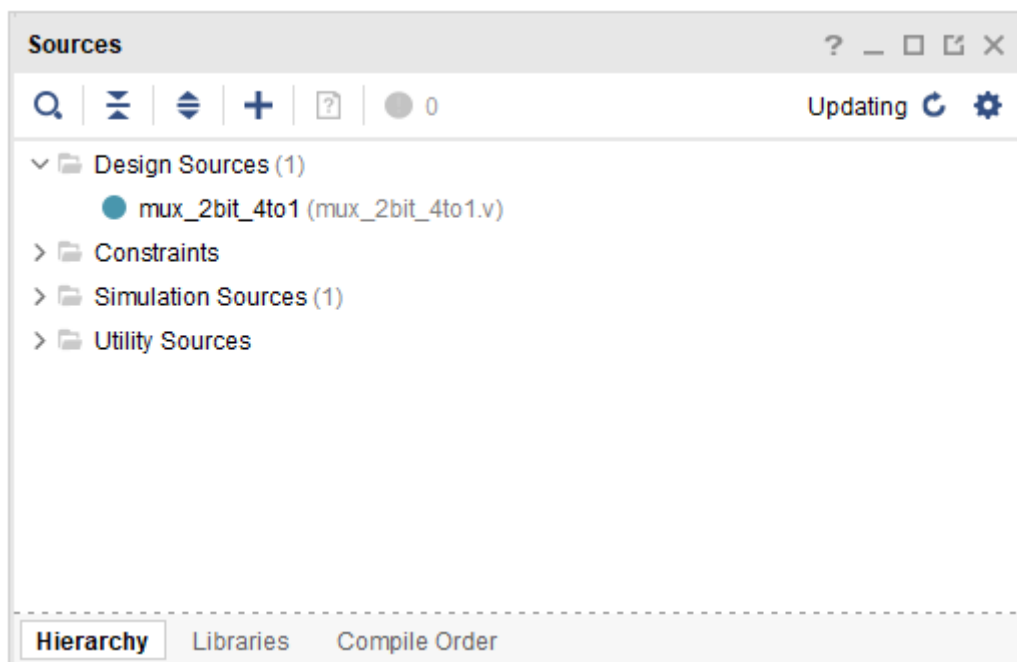
To create the project, click Finish

[?](#) < Back Next > **Finish** Cancel

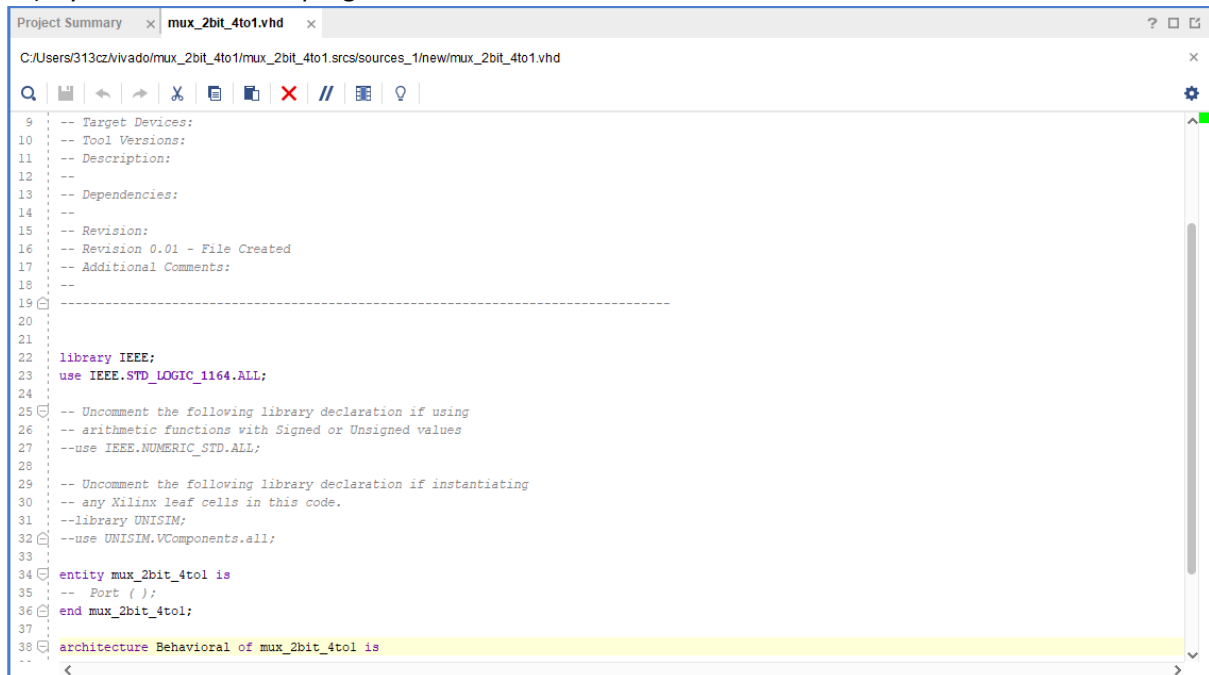
10) Pokud chceme můžeme předdefinovat vstupy



11) Nyní máme vytvořený projekt a v části sources otevřeme náš zdrojový soubor



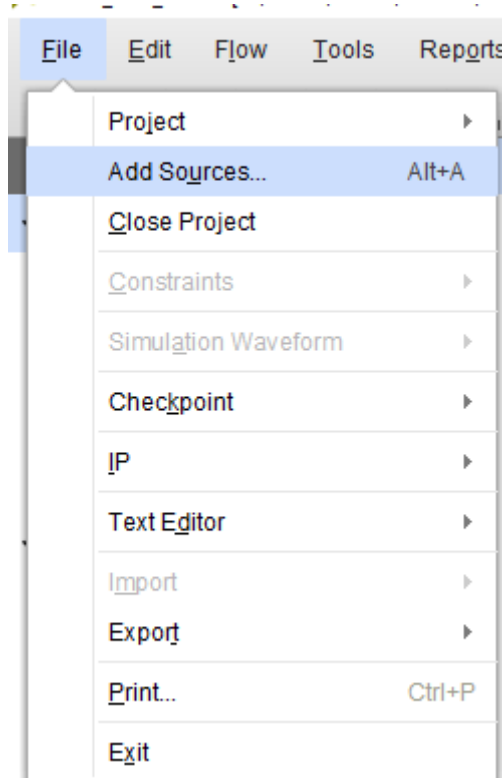
## 12) Nyní můžeme už náš program editovat



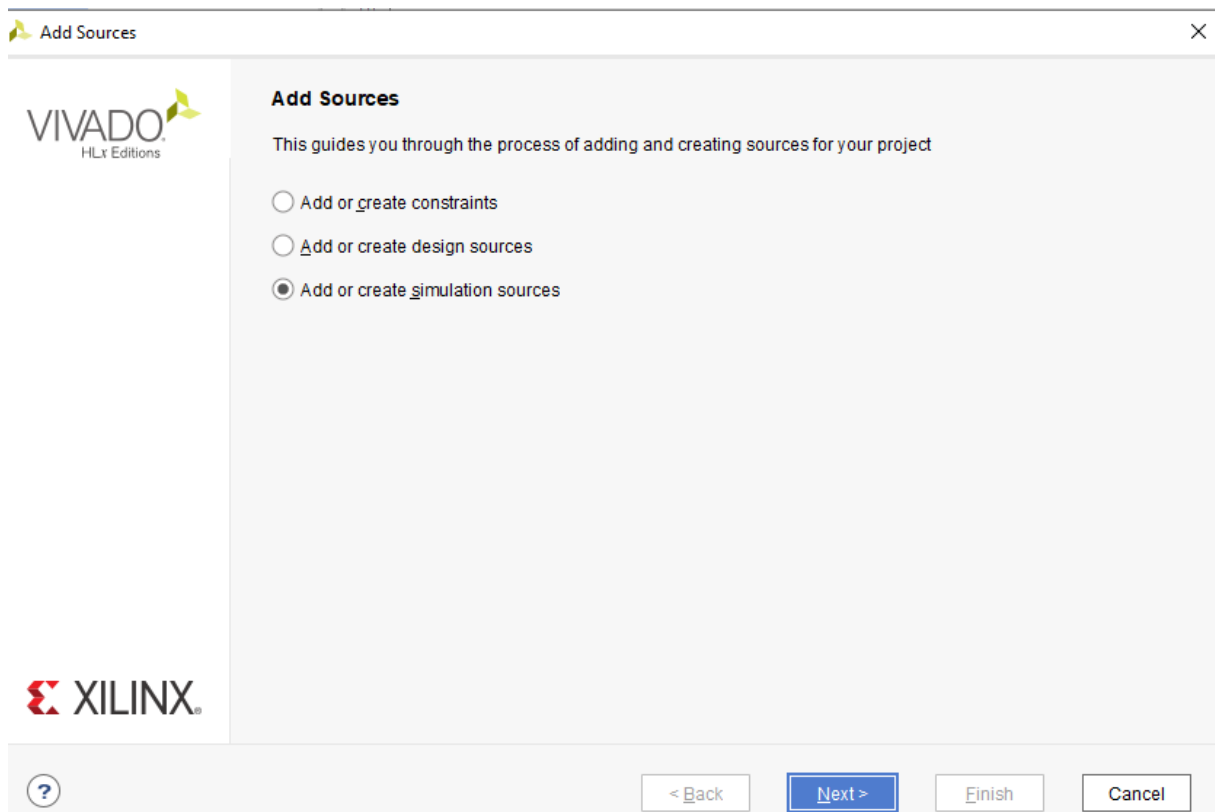
```
9  -- Target Devices:
10 -- Tool Versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity mux_2bit_4to1 is
35 -- Port ( );
36 end mux_2bit_4to1;
37
38 architecture Behavioral of mux_2bit_4to1 is
39 --
```

# Vytvoření Test benche

1)Klikneme na záložku File/Add Sources...

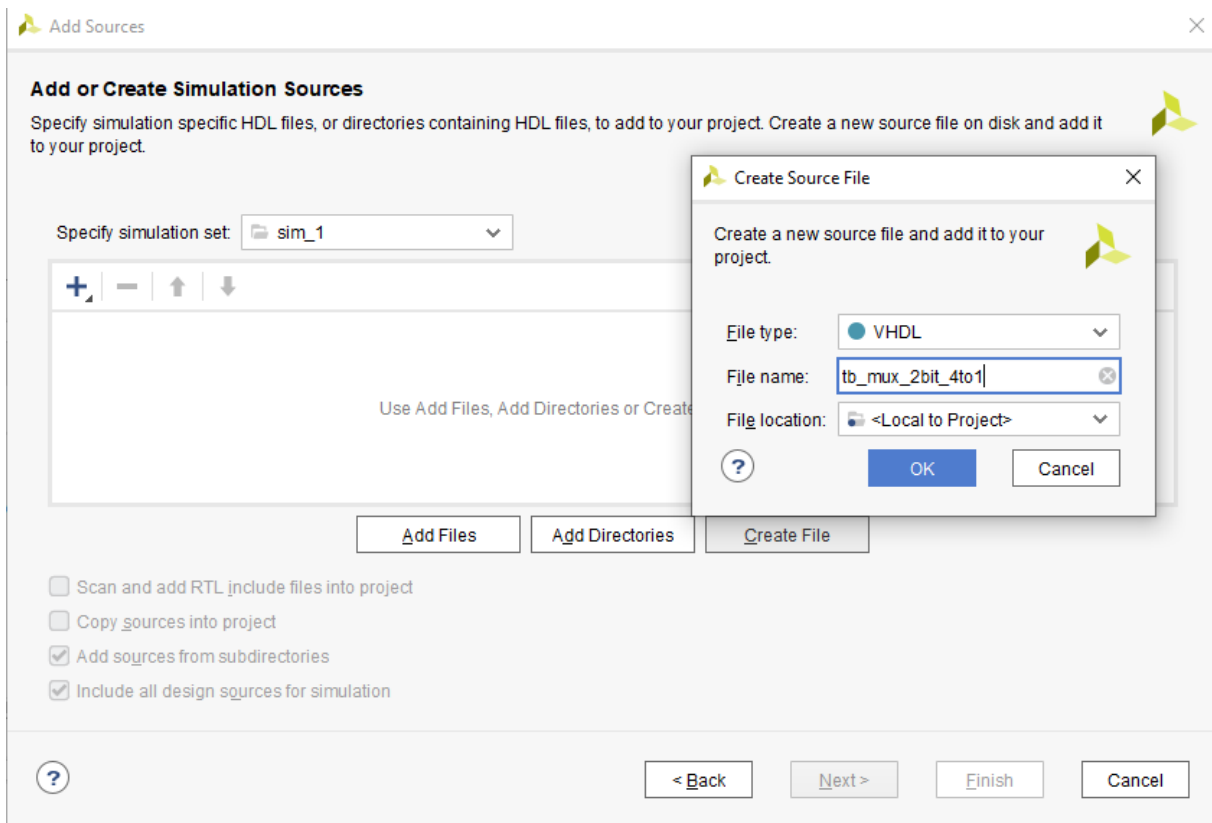


2)Vybereme Add or create simulation sources








3) Vytvoříme VHDL source file tb\_název/ a dokončíme

 Add Sources

**Add or Create Simulation Sources**

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim\_1


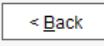
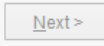

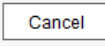
Use Add Files, Add Directories or Create File

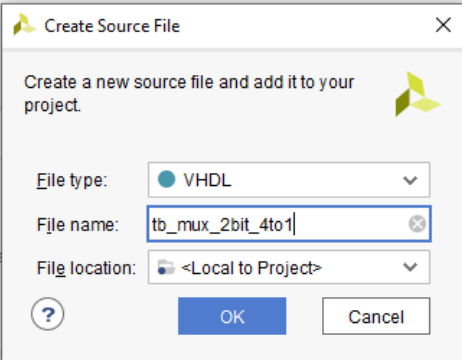
☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

☒ Include all design sources for simulation




 Create Source File

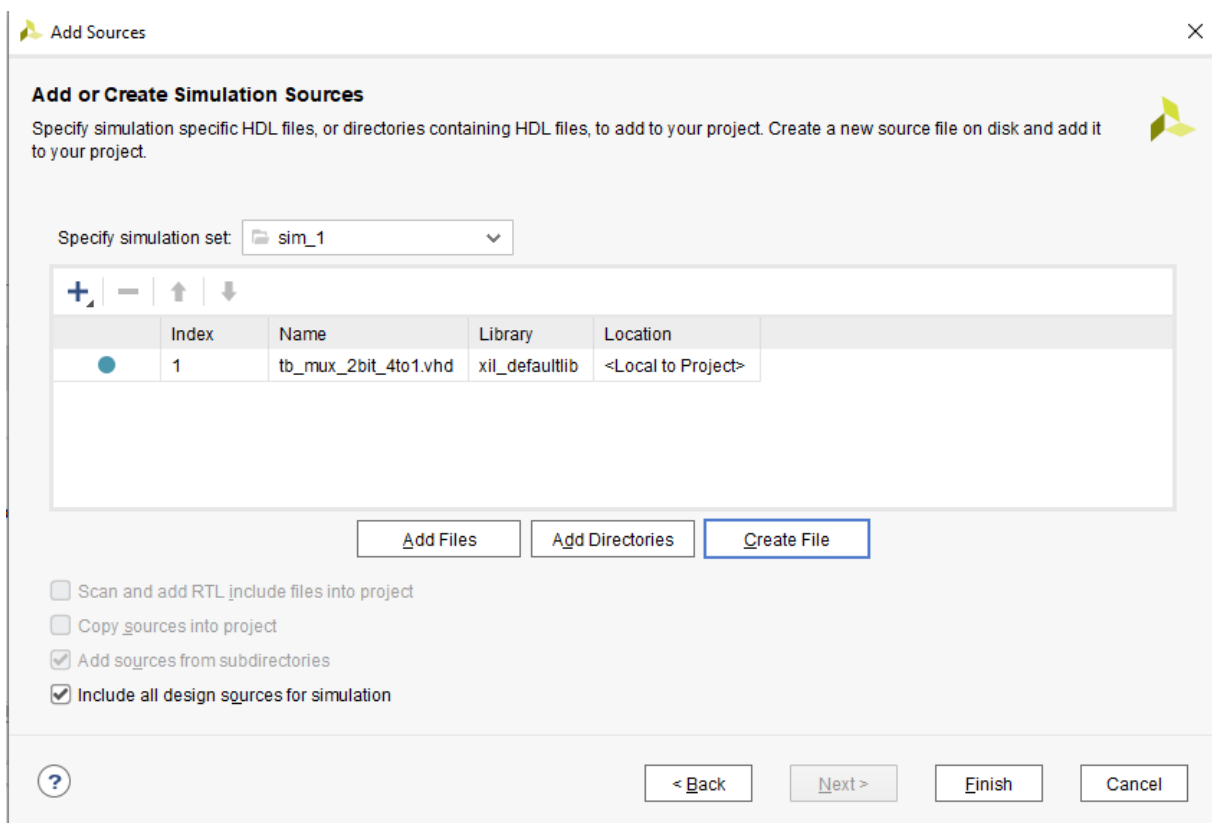
Create a new source file and add it to your project.

File type: VHDL

File name: tb\_mux\_2bit\_4to1

File location: <Local to Project>




  


 Add Sources



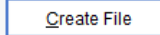
**Add or Create Simulation Sources**

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim\_1

	Index	Name	Library	Location
	1	tb_mux_2bit_4to1.vhd	xil_defaultlib	<Local to Project>


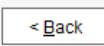
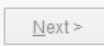
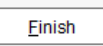
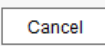
  

☐ Scan and add RTL include files into project

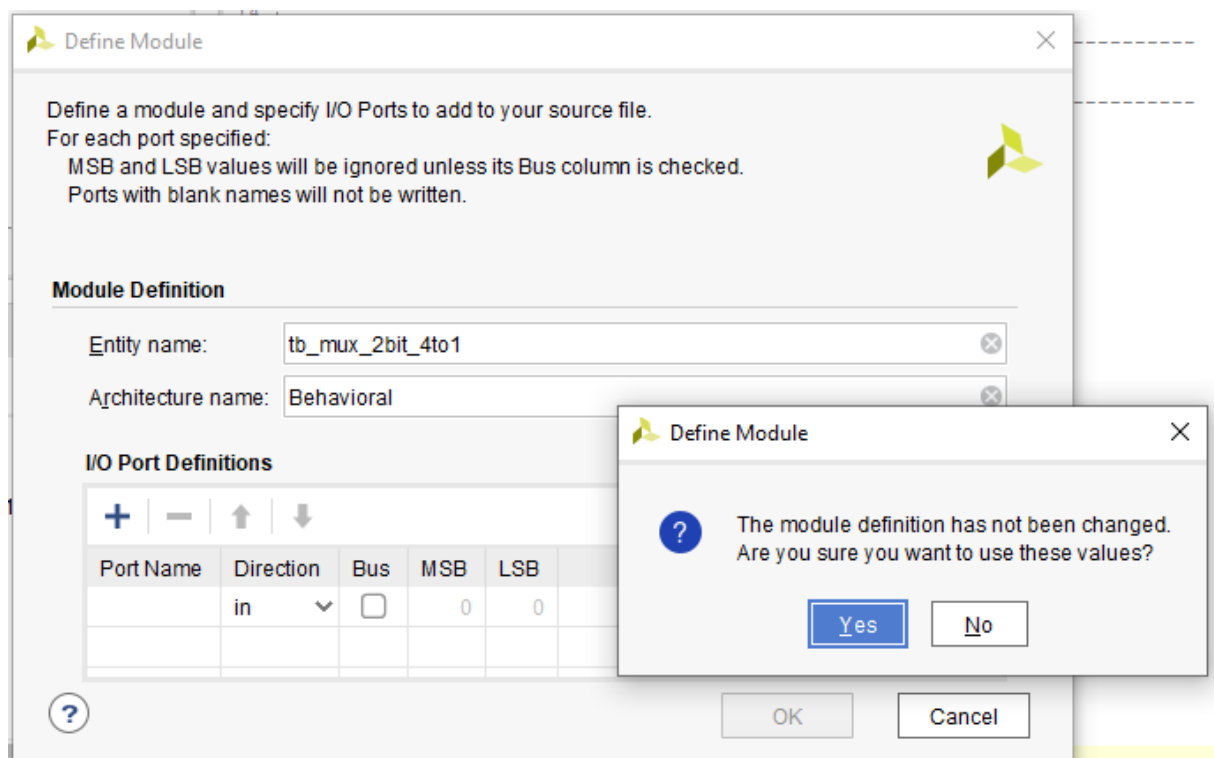
☐ Copy sources into project

☒ Add sources from subdirectories

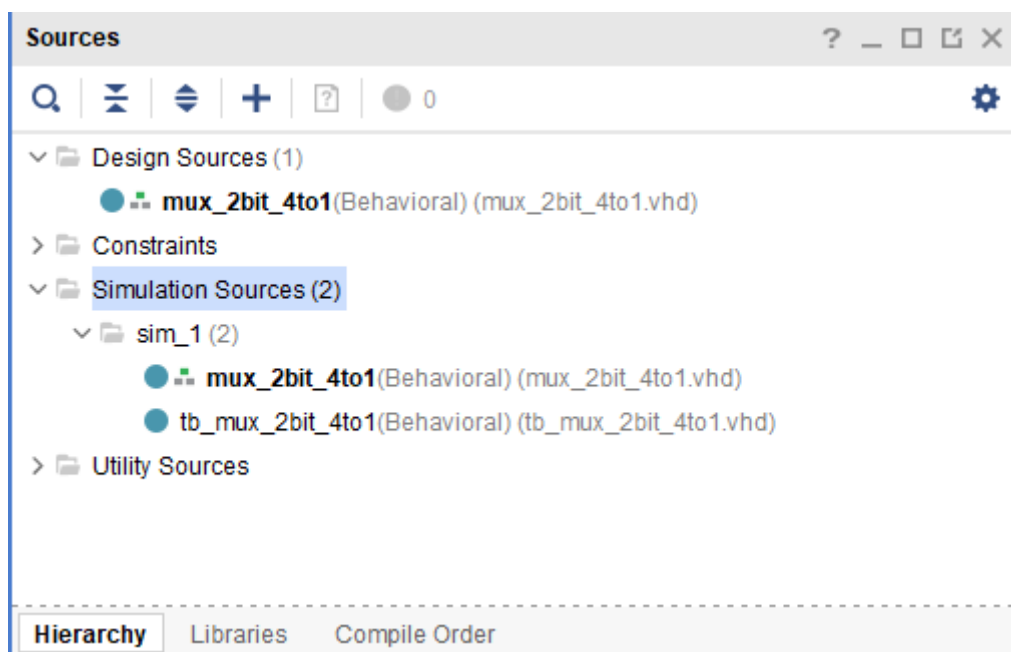
☒ Include all design sources for simulation

4) Pokud chceme můžeme předdefinovat vstupy

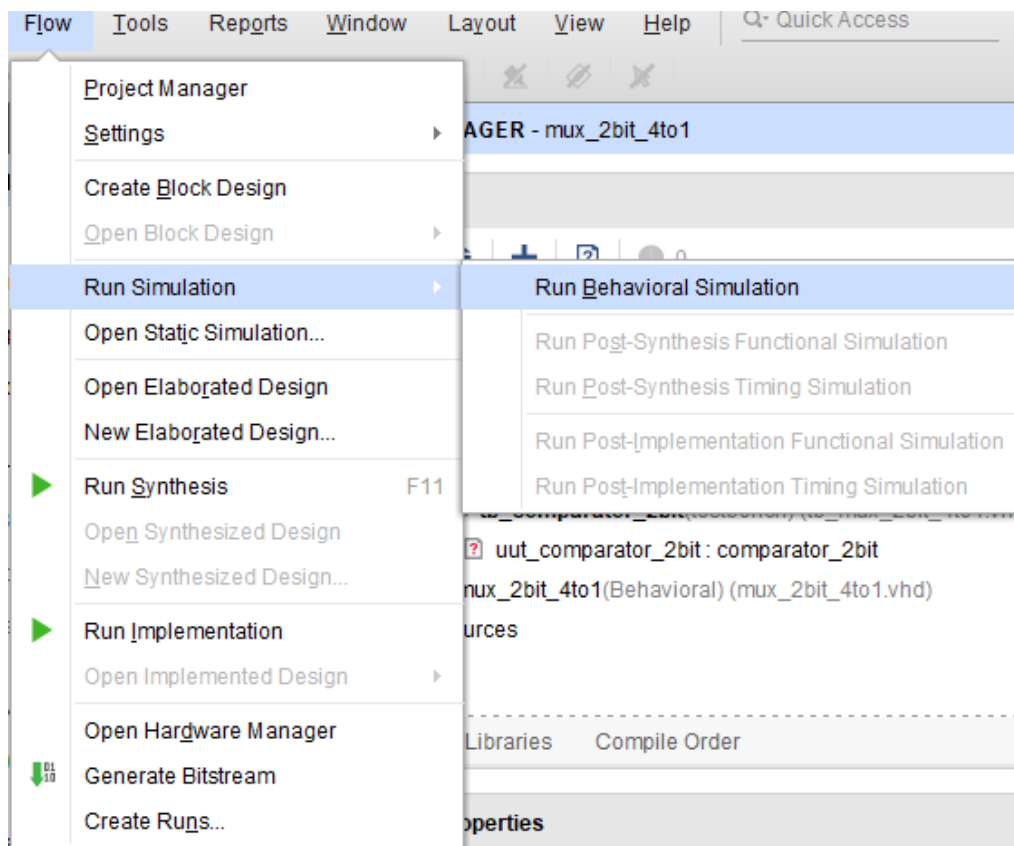


5) Test bench opět nalezneme v záložce sources

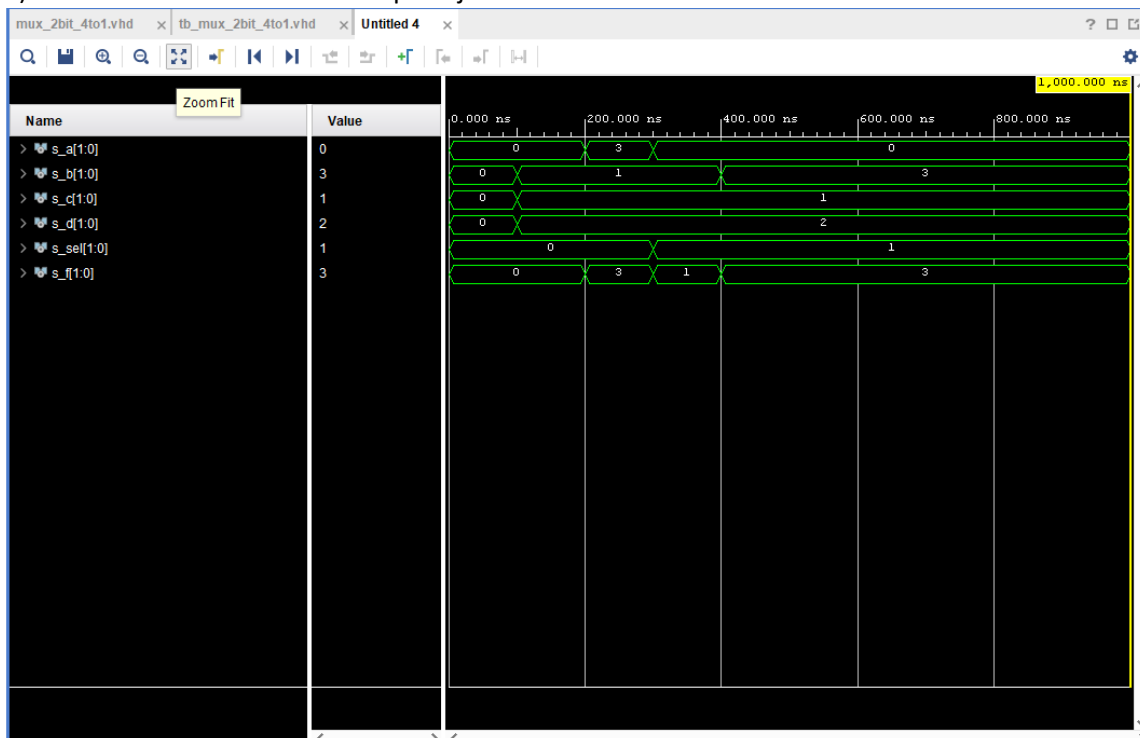


# Spuštění simulace

1)Klineme na Flow/Run Simulation/ Run Behavioral simulation

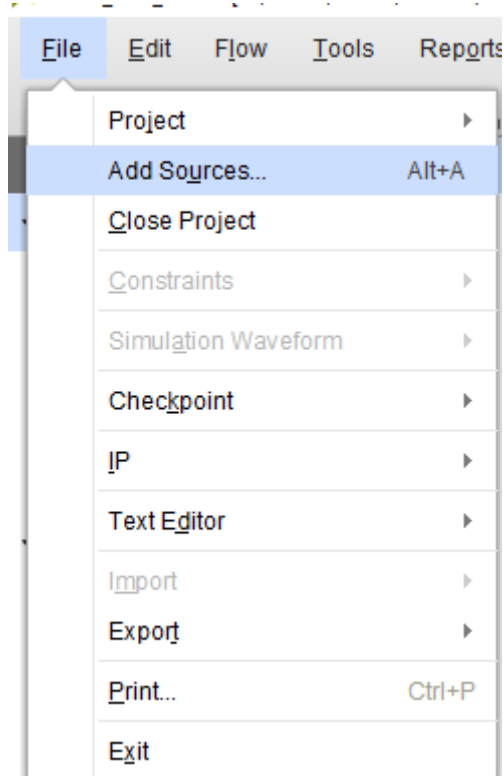


2) Pro dobré zobrazení simulace použijeme funkci Zoom fit

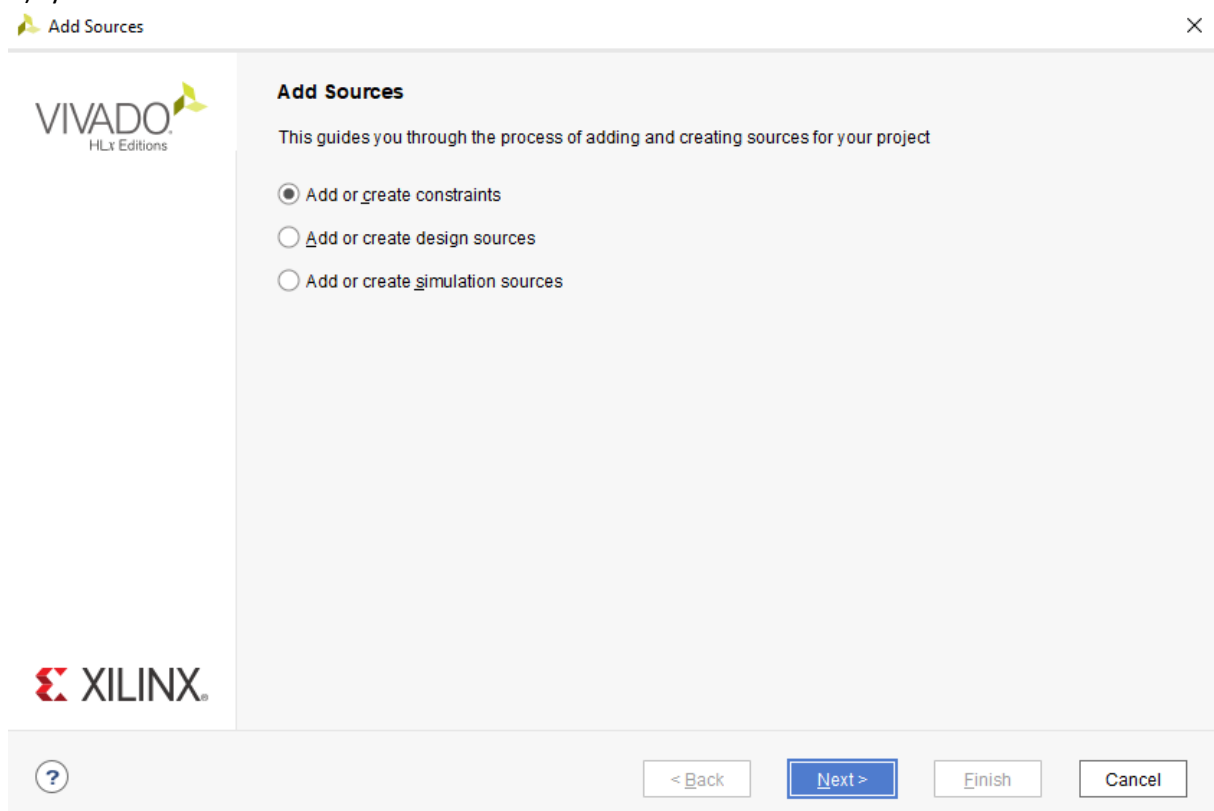


# Vytvoření constraints souboru

1) Klikneme na záložku File/Add Sources...



2) Vybereme Add or create constraints



### 3) Vytvoříme nový XDC source file a potvrdíme

**Add Sources**

**Add or Create Constraints**

Specify or create constraint files for physical and timing constraint to add to your project.

Specify constraint set: constrs\_1 (active)

Use Add Files or Create File

☐ Copy constraints files into project

**Create Constraints File**

Create a new constraints file and add it to your project

File type: XDC

File name: nexys-a7-50t.xdc

File location: <Local to Project>

**Add Sources**

**Add or Create Constraints**

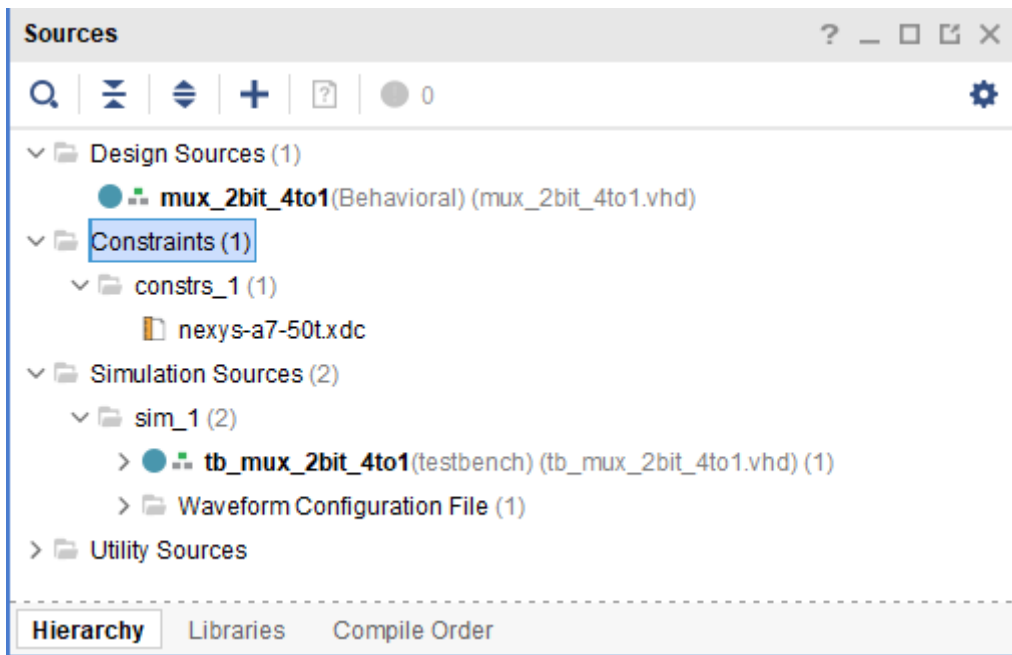
Specify or create constraint files for physical and timing constraint to add to your project.

Specify constraint set: constrs\_1 (active)

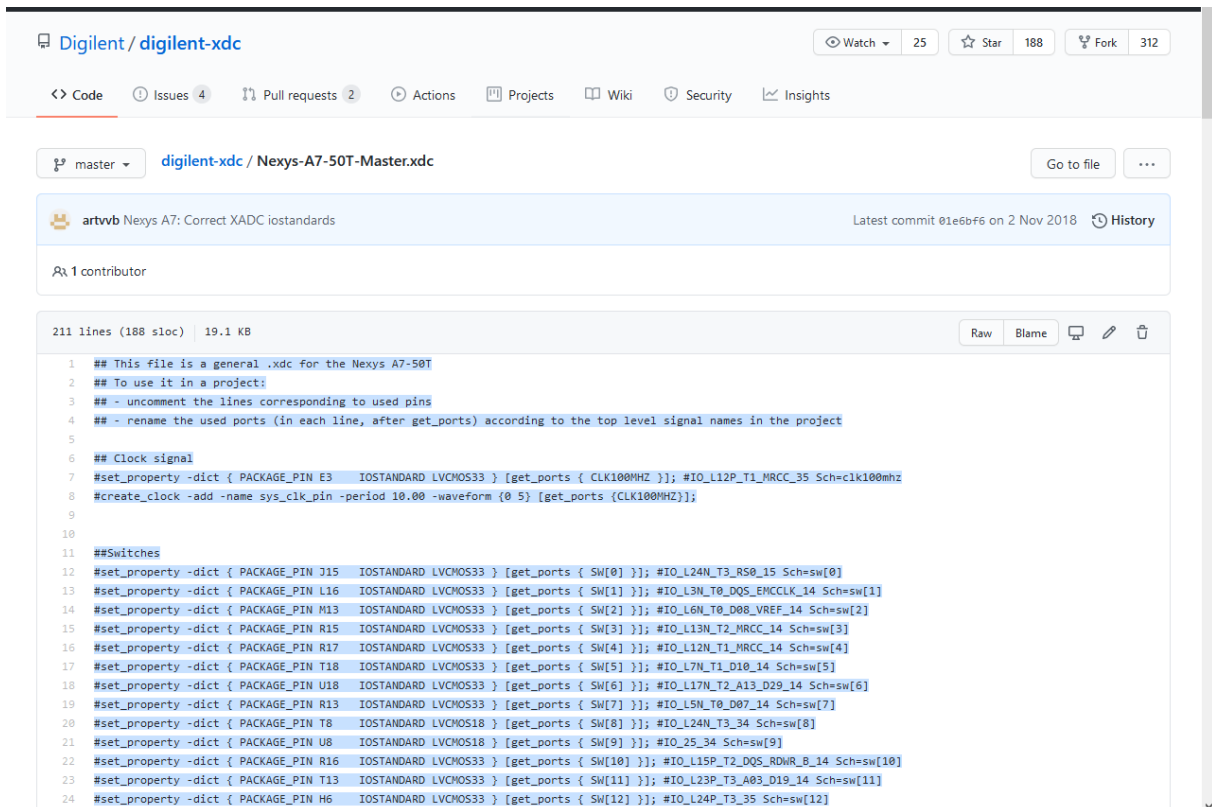
Constraint File	Location
nexys-a7-50t.xdc	<Local to Project>

☐ Copy constraints files into project

#### 4) Opět otevřeme přes sources



#### 5) Vložíme data z Githubu výrobce



## 6) Změníme požadované vstupy a výstupy

```
4 ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6 ## Clock signal
7 #set_property -dict { PACKAGE_PIN E3      IOSTANDARD LVCMOS33 } [get_ports { CLK100MHZ }]; #IO_L12P_T1_MRCC_35 Sch=clk100mhz
8 #create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports {CLK100MHZ}];
9
10
11 ##Switches
12 set_property -dict { PACKAGE_PIN J15      IOSTANDARD LVCMOS33 } [get_ports { a_i[0] }]; #IO_L24N_T3_R50_15 Sch=sw[0]
13 set_property -dict { PACKAGE_PIN L16      IOSTANDARD LVCMOS33 } [get_ports { a_i[1] }]; #IO_L3N_T0_D05_EMCCLK_14 Sch=sw[1]
14 set_property -dict { PACKAGE_PIN M13      IOSTANDARD LVCMOS33 } [get_ports { b_i[0] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
15 set_property -dict { PACKAGE_PIN R15      IOSTANDARD LVCMOS33 } [get_ports { b_i[1] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
16 set_property -dict { PACKAGE_PIN R17      IOSTANDARD LVCMOS33 } [get_ports { c_i[0] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
17 set_property -dict { PACKAGE_PIN T18      IOSTANDARD LVCMOS33 } [get_ports { c_i[1] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
18 set_property -dict { PACKAGE_PIN U18      IOSTANDARD LVCMOS33 } [get_ports { d_i[0] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
19 set_property -dict { PACKAGE_PIN R13      IOSTANDARD LVCMOS33 } [get_ports { d_i[1] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
20 #set_property -dict { PACKAGE_PIN T8       IOSTANDARD LVCMOS18 } [get_ports { SW[8] }]; #IO_L24N_T3_34 Sch=sw[8]
21 #set_property -dict { PACKAGE_PIN U8       IOSTANDARD LVCMOS18 } [get_ports { SW[9] }]; #IO_25_34 Sch=sw[9]
22 #set_property -dict { PACKAGE_PIN R16      IOSTANDARD LVCMOS33 } [get_ports { SW[10] }]; #IO_L15P_T2_D05_RDWR_B_14 Sch=sw[10]
23 #set_property -dict { PACKAGE_PIN T13      IOSTANDARD LVCMOS33 } [get_ports { SW[11] }]; #IO_L23P_T3_A03_D19_14 Sch=sw[11]
24 #set_property -dict { PACKAGE_PIN H6       IOSTANDARD LVCMOS33 } [get_ports { SW[12] }]; #IO_L24P_T3_35 Sch=sw[12]
25 #set_property -dict { PACKAGE_PIN U12      IOSTANDARD LVCMOS33 } [get_ports { SW[13] }]; #IO_L20P_T3_A08_D24_14 Sch=sw[13]
26 set_property -dict { PACKAGE_PIN U11      IOSTANDARD LVCMOS33 } [get_ports { sel_i[0] }]; #IO_L19N_T3_A09_D25_VREF_14 Sch=sw[14]
27 set_property -dict { PACKAGE_PIN V10      IOSTANDARD LVCMOS33 } [get_ports { sel_i[1] }]; #IO_L21P_T3_D05_14 Sch=sw[15]
28
29 ## LEDs
30 set_property -dict { PACKAGE_PIN H17      IOSTANDARD LVCMOS33 } [get_ports { f_o[0] }]; #IO_L18P_T2_A24_15 Sch=led[0]
31 set_property -dict { PACKAGE_PIN K15      IOSTANDARD LVCMOS33 } [get_ports { f_o[1] }]; #IO_L24P_T3_R51_15 Sch=led[1]
32 #set_property -dict { PACKAGE_PIN J13      IOSTANDARD LVCMOS33 } [get_ports { LED[2] }]; #IO_L17N_T2_A25_15 Sch=led[2]
33 #set_property -dict { PACKAGE_PIN N14      IOSTANDARD LVCMOS33 } [get_ports { LED[3] }]; #IO_L8P_T1_D11_14 Sch=led[3]
```