
STM32
CubeMX

1. Description

1.1. Project

Project Name	SSS_CIS
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	03/16/2024

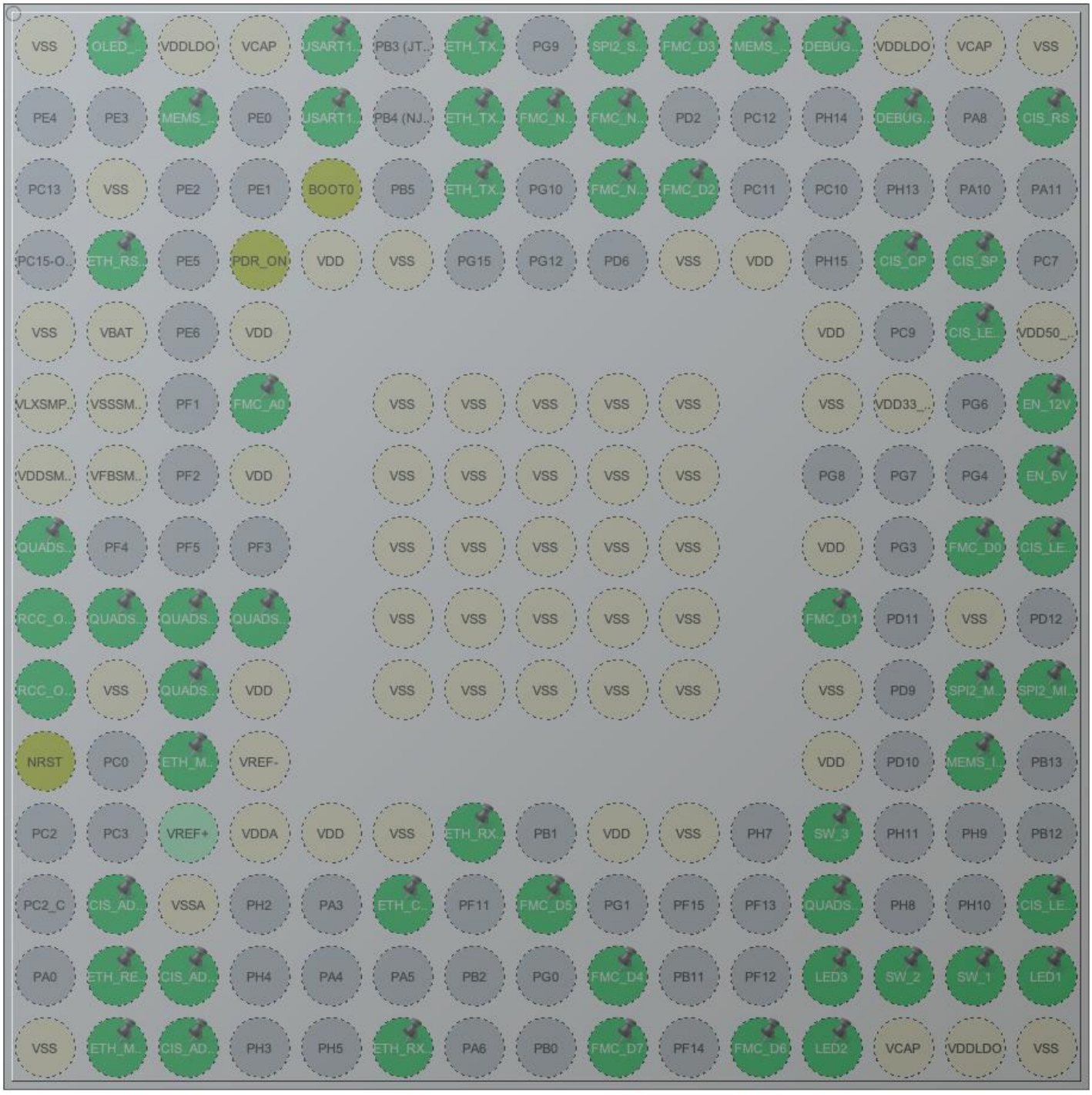
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H745/755
MCU name	STM32H745IIKx
MCU Package	UFBGA176
MCU Pin number	201

1.3. Core(s) information

Core(s)	ARM Cortex-M7 ARM Cortex-M4

2. Pinout Configuration



UFBGA176 +25 (Top view)

3. Pins Configuration

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PB8 *	I/O	GPIO_Output	OLED_RESET
A3	VDDLDO	Power		
A4	VCAP	Power		
A5	PB6	I/O	USART1_TX	
A7	PG11	I/O	ETH_TX_EN	
A9	PD3	I/O	SPI2_SCK	
A10	PD1	I/O	FMC_D3	
A11	PA15 (JTDI) *	I/O	GPIO_Input	MEMS_FSYNC
A12	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
A13	VDDLDO	Power		
A14	VCAP	Power		
A15	VSS	Power		
B3	PB9	I/O	SPI2_NSS	MEMS_CS
B5	PB7	I/O	USART1_RX	
B7	PG13	I/O	ETH_TXD0	
B8	PD7	I/O	FMC_NE1	
B9	PD5	I/O	FMC_NWE	
B13	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
B15	PA12 *	I/O	GPIO_Output	CIS_RS
C2	VSS	Power		
C5	BOOT0	Boot		
C7	PG14	I/O	ETH_TXD1	
C9	PD4	I/O	FMC_NOE	
C10	PD0	I/O	FMC_D2	
D2	PC14-OSC32_IN (OSC32_IN) *	I/O	GPIO_Output	ETH_RST
D4	PDR_ON	Reset		
D5	VDD	Power		
D6	VSS	Power		
D10	VSS	Power		
D11	VDD	Power		
D13	PA9	I/O	TIM1_CH2	CIS_CP
D14	PC8	I/O	TIM8_CH3	CIS_SP
E1	VSS	Power		
E2	VBAT	Power		

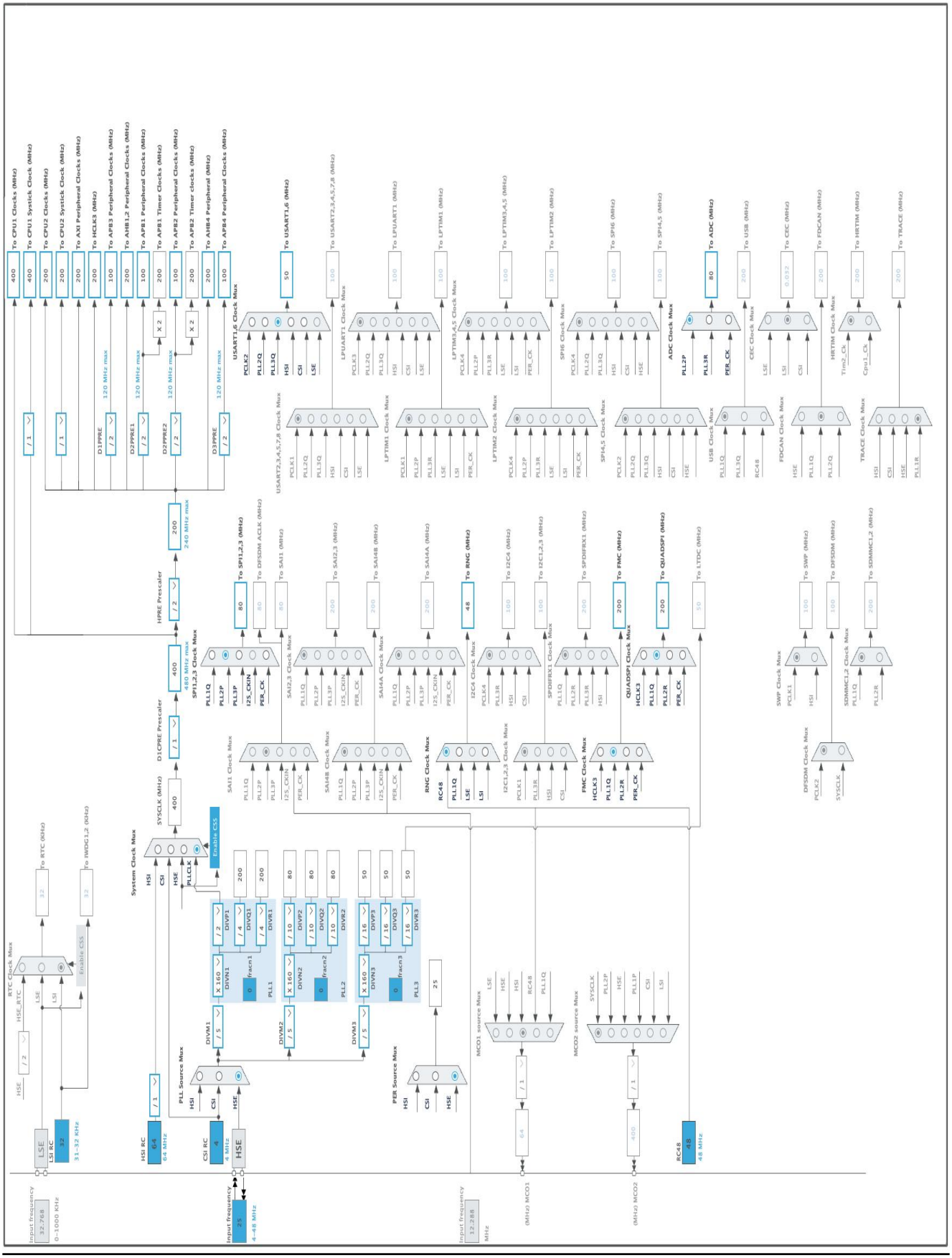
Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
E4	VDD	Power		
E12	VDD	Power		
E14	PC6	I/O	TIM3_CH1	CIS_LED_B
E15	VDD50_USB	Power		
F1	VLXSMPS	Power		
F2	VSSSMPS	Power		
F4	PF0	I/O	FMC_A0	
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F12	VSS	Power		
F13	VDD33_USB	Power		
F15	PG5 *	I/O	GPIO_Output	EN_12V
G1	VDDSMPS	Power		
G2	VFBSMPS	Power		
G4	VDD	Power		
G6	VSS	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G15	PG2 *	I/O	GPIO_Output	EN_5V
H1	PF6	I/O	QUADSPI_BK1_IO3	
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H12	VDD	Power		
H14	PD14	I/O	FMC_D0	
H15	PD13	I/O	TIM4_CH2	CIS_LED_R
J1	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
J2	PF8	I/O	QUADSPI_BK1_IO0	
J3	PF7	I/O	QUADSPI_BK1_IO2	
J4	PF9	I/O	QUADSPI_BK1_IO1	
J6	VSS	Power		
J7	VSS	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		
J12	PD15	I/O	FMC_D1	
J14	VSS	Power		
K1	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
K2	VSS	Power		
K3	PF10	I/O	QUADSPI_CLK	
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K12	VSS	Power		
K14	PB15	I/O	SPI2_MOSI	
K15	PB14	I/O	SPI2_MISO	
L1	NRST	Reset		
L3	PC1	I/O	ETH_MDC	
L4	VREF-	Power		
L12	VDD	Power		
L14	PD8	I/O	GPIO_EXTI8	MEMS_INT
M4	VDDA	Power		
M5	VDD	Power		
M6	VSS	Power		
M7	PC5	I/O	ETH_RXD1	
M9	VDD	Power		
M10	VSS	Power		
M12	PE14	I/O	GPIO_EXTI14	SW_3
N2	PC3_C	I/O	ADC3_INP1	CIS_ADC_3
N3	VSSA	Power		
N6	PA7	I/O	ETH_CRS_DV	
N8	PE8	I/O	FMC_D5	
N12	PB10	I/O	QUADSPI_BK1_NCS	
N15	PH12	I/O	TIM5_CH3	CIS_LED_G
P2	PA1	I/O	ETH_REF_CLK	
P3	PA1_C	I/O	ADC2_INP1	CIS_ADC_2
P9	PE7	I/O	FMC_D4	
P12	PE12 *	I/O	GPIO_Output	LED3

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
P13	PE13	I/O	GPIO_EXTI13	SW_2
P14	PE15	I/O	GPIO_EXTI15	SW_1
P15	PH6 *	I/O	GPIO_Output	LED1
R1	VSS	Power		
R2	PA2	I/O	ETH_MDIO	
R3	PA0_C	I/O	ADC1_INP0	CIS_ADC_1
R6	PC4	I/O	ETH_RXD0	
R9	PE10	I/O	FMC_D7	
R11	PE9	I/O	FMC_D6	
R12	PE11 *	I/O	GPIO_Output	LED2
R13	VCAP	Power		
R14	VDDLDO	Power		
R15	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	SSS_CIS
Project Folder	/Users/zhonx/Documents/Workspaces/Workspace_SSS/SSS_CIS
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x400
Minimum Stack Size	0x800

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_ADC2_Init	ADC2
6	MX_ADC3_Init	ADC3
7	MX_FMC_Init	FMC
8	MX_USART1_UART_Init	USART1
9	MX_TIM1_Init	TIM1
10	MX_TIM3_Init	TIM3
11	MX_TIM4_Init	TIM4

Rank	Function Name	Peripheral Instance Name
12	MX_TIM5_Init	TIM5
13	MX_TIM8_Init	TIM8
14	MX_RNG_Init	RNG
15	MX_CRC_Init	CRC
16	MX_LWIP_Init	LWIP
17	MX_TIM6_Init	TIM6
18	MX_QUADSPI_Init	QUADSPI
19	MX_SPI2_Init	SPI2
20	MX_FREERTOS_Init	FREERTOS_M7

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name
1	MX_DMA_Init	DMA
2	MX_GPIO_Init	GPIO
3	MX_FMC_Init	FMC
4	MX_USART1_UART_Init	USART1

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H745/755
MCU	STM32H745IIKx
Datasheet	DS12923_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

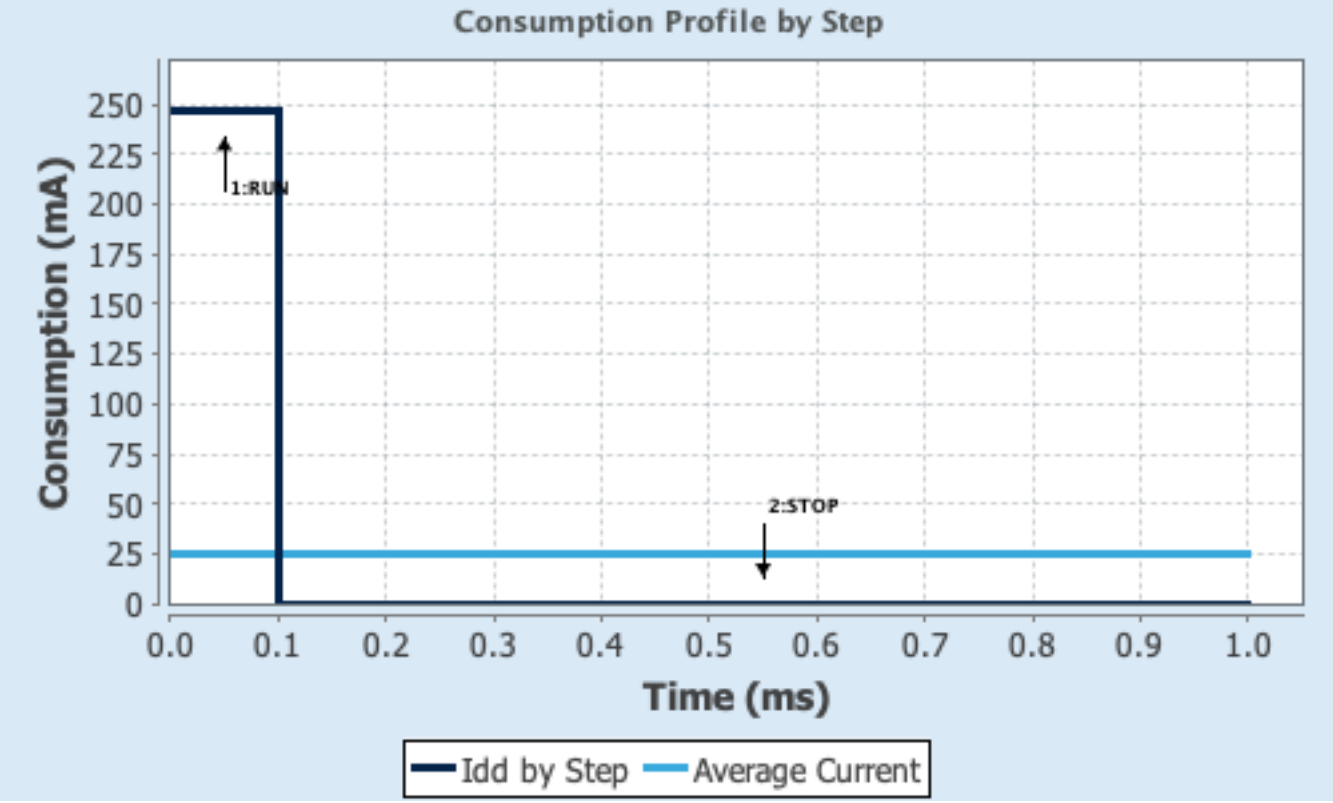
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN/CRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	CM7: ITCM/Cache / CM4: FLASH_B/ART	CM7: NA / CM4: NA
CM7 Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL_IPs_ON	LSE Flash-ON
CM4 Frequency	240 MHz	0 Hz
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	247 mA	145 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days, 21 hours	Average DMIPS	1027.2001 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
250
225
200
175
150
125
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Peripherals and Middlewares Configuration

2.1. ADC1

mode: IN0

2.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 1 Capture Compare 1 event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 0
Sampling Time	**2.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.2. ADC2

IN1: IN1 Single-ended

2.2.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 1 Capture Compare 1 event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 1
Sampling Time	**2.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.3. ADC3

IN1: IN1 Single-ended

2.3.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D3

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	**ADC 12-bit resolution ***
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 1 Capture Compare 1 event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 1
Sampling Time	**2.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

2.4. CORTEX_M7

2.4.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Speculation default mode Settings:

Speculation default mode	Disabled

Cortex Interface Settings:

CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	**Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers ***

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x30044000 ***
MPU Region Size	**32KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	**level 1 ***
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x30040000 ***

MPU Region Size	**1KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	**ENABLE ***
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x24000000 ***
MPU Region Size	**64B ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled

2.5. CRC

mode: Activated

2.5.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D3

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

2.6. DEBUG

Debug: Serial Wire

2.6.1. Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	

2.7. ETH

Mode: RMII

2.7.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30040200 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Length	**1524 ***

2.8. FMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: LCD Interface

LCD Register Select: A0

Data: 8 bits

2.8.1. NOR/PSRAM 1:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D1

NOR/PSRAM control:

Memory type	LCD Interface
Bank	Bank 1 NOR/PSRAM 1
Write operation	Enabled

Write FIFO	Enabled
Extended mode	**Enabled ***

NOR/PSRAM timing:

Address setup time in HCLK clock cycles	**8 ***
Data setup time in HCLK clock cycles	**10 ***
Bus turn around time in HCLK clock cycles	**5 ***
Access mode	A

NOR/PSRAM timing for write accesses:

Extended address setup time	**8 ***
Extended data setup time	**10 ***
Extended bus turn around time	**5 ***
Extended access mode	A

2.8.2. Bank Mapping:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D1

Mapping parameters:

FMC bank mapping	Default mapping

2.9. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

2.9.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting

Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

2.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

2.10.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D3

Power Parameters:

SupplySource	PWR_DIRECT_SMPS_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Product revision	rev.V

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 4 and 8 MHz
PLL3 input frequency range	Between 4 and 8 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range
PLL3 clock Output range	Wide VCO range

2.11. RNG

mode: Activated

2.11.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2
Clock Error Detection	Enable

2.12. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

2.12.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**20.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low

Master Ss Idleness	**10 Cycle ***
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	**Enable ***
Master Keep Io State	**Master Keep Io State Enable ***
IO Swap	Disabled

2.13. SYS

Timebase Source: TIM2

2.13.1. Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	

2.14. SYS_M4

Timebase Source: SysTick

2.14.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

2.15. TIM1

Channel1: PWM Generation No Output

Channel2: PWM Generation CH2

2.15.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**prescalerValue ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**counterPeriod ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	**Enable (Trigger delayed for master/slaves simultaneous start) ***
Trigger Event Selection TRGO	**Output Compare (OC1REF) ***
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	**PWM mode 2 ***
Pulse (16 bits value)	**pulseValueCH1 ***
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**pulseValueCH2 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.16. TIM3

Slave Mode: External Clock Mode 1

Trigger Source: ITR0

Channel1: PWM Generation CH1

2.16.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**prescalerValue ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**counterPeriod ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**pulseValue ***
Output compare preload	Enable

Fast Mode	Disable
CH Polarity	High

2.17. TIM4

Slave Mode: External Clock Mode 1

Trigger Source: ITR0

Channel2: PWM Generation CH2

2.17.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**prescalerValue ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**counterPeriod ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**pulseValue ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.18. TIM5

Slave Mode: External Clock Mode 1

Trigger Source: ITR0
Channel3: PWM Generation CH3
2.18.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**prescalerValue ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**counterPeriod ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	**pulseValue ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

2.19. TIM6
mode: Activated
2.19.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**prescalerValue ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**counterPeriod ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

2.20. TIM8

Slave Mode: External Clock Mode 1

Trigger Source: ITR0

Channel3: PWM Generation CH3

2.20.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**prescalerValue ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**counterPeriod ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***
Slave Mode Controller	ETR mode 1

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable

- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	**pulseValue ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

2.21. USART1

Mode: Asynchronous

2.21.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Baud Rate	**2000000 ***
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

2.22. FREERTOS_M7

Interface: CMSIS_V1

2.22.1. Config parameters:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled

CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

2.22.2. Include parameters:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

2.22.3. Advanced settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	**Enabled ***

Project settings (see parameter description first):

Use FW pack heap file	Enabled

2.23. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

2.23.1. General Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.1.2

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	**Disabled ***

IP Address Settings:

IP_ADDRESS (IP Address)	**192.168.000.010 ***
NETMASK_ADDRESS (Netmask Address)	**255.255.255.000 ***
GATEWAY_ADDRESS (Gateway Address)	**192.168.000.001 ***

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Enabled
CMSIS_VERSION (CMSIS API Version used)	CMSIS v1
RTOS_USE_NEWLIB_REENTRANT (RTOS used - 1)	Enabled

Platform Settings:

PHY Driver	Choose/LAN8742

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

2.23.2. Key Options:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	**10*1024 ***
LWIP_RAM_HEAP_POINTER (RAM Heap Pointer)	**0x30044000 ***

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	3
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0
LWIP_SOCKET_SELECT (Select for Socket)	Enabled
LWIP_SOCKET_POLL (Poll for Socket)	Enabled

2.23.3. PPP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

2.23.4. IPv6:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

2.23.5. HTTPD:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	**Enabled ***

2.23.6. SNMP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

2.23.7. SNTP/SMTP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **)	Disabled

2.23.8. MDNS/TFTP:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	

	Cortex-M7
Power Domain:	D1

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

2.23.9. Perf/Checks:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

2.23.10. Statistics:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

2.23.11. Checksum:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Enabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Enabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Enabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

2.23.12. Debug:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

2.23.13. Platform Settings:

Driver_PHY	LAN8742

*** User modified value**

3. System Configuration

3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
ADC1	PA0_C	ADC1_INP0	Analog mode	No pull-up and no pull-down	n/a	CIS_ADC_1	Cortex-M7	D2
ADC2	PA1_C	ADC2_INP1	Analog mode	No pull-up and no pull-down	n/a	CIS_ADC_2	Cortex-M7	D2
ADC3	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	CIS_ADC_3	Cortex-M7	D3
DEBUG	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a		Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
ETH	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
FMC	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PD7	FMC_NE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PD5	FMC_NWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PD4	FMC_NOE	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High		Cortex-M7 Cortex-M4*	D1
QUADSPI	PF6	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PF8	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PF7	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PF9	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PF10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
	PB10	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7	D1
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a		Cortex-M7* Cortex-M4	D3
SPI2	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PB9	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MEMS_CS	Cortex-M7	D2
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very**		Cortex-M7	D2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
					High *			
TIM1	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	CIS_CP	Cortex-M7	D2
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	CIS_LED_B	Cortex-M7	D2
TIM4	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	CIS_LED_R	Cortex-M7	D2
TIM5	PH12	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	CIS_LED_G	Cortex-M7	D2
TIM8	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***	CIS_SP	Cortex-M7	D2
USART1	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-M7* Cortex-M4	D2
GPIO	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_RESET	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA15 (JTDI)	GPIO_Input	Input mode	**Pull-up ***	n/a	MEMS_FSYNC	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	CIS_RS	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ETH_RST	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EN_12V	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EN_5V	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD8	GPIO_EXTI8	**External Interrupt Mode with Falling edge**	**Pull-up ***	n/a	MEMS_INT	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE14	GPIO_EXTI14	**External Interrupt Mode with Falling edge**	No pull-up and no pull-down	n/a	SW_3	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE13	GPIO_EXTI13	**External Interrupt Mode with Falling edge**	No pull-up and no pull-down	n/a	SW_2	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE15	GPIO_EXTI1	**External Interrupt**	No pull-up and no pull-	n/a	SW_1	Cortex-M7*	Cortex-M7*

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
		5	**Mode with Falling edge**	down			Cortex-M4	Cortex-M4
	PH6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4

* Initialized context

3.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Stream0	Peripheral To Memory	**Very High ***
ADC2	DMA1_Stream1	Peripheral To Memory	**Very High ***
ADC3	DMA2_Stream0	Peripheral To Memory	**Very High ***
SPI2_RX	DMA2_Stream7	Peripheral To Memory	**High ***
SPI2_TX	DMA2_Stream6	Memory To Peripheral	**High ***

ADC1: DMA1_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

ADC2: DMA1_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

ADC3: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full

Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

SPI2_RX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI2_TX: DMA2_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

3.3. BDMA configuration

nothing configured in DMA service

3.4. MDMA configuration

nothing configured in DMA service

3.5. NVIC configuration

3.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream1 global interrupt	true	5	0
TIM2 global interrupt	true	15	0
SPI2 global interrupt	true	5	0
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	5	0
DMA2 stream0 global interrupt	true	5	0
Ethernet global interrupt	true	5	0
DMA2 stream6 global interrupt	true	5	0
DMA2 stream7 global interrupt	true	5	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
USART1 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM5 global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
CM4 send event interrupt for CM7	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		
QUADSPI global interrupt	unused		
HSEM1 global interrupt	unused		
ADC3 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

3.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
SPI2 global interrupt	false	true	true
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	false	true	true
DMA2 stream0 global interrupt	false	true	true
Ethernet global interrupt	false	true	true
DMA2 stream6 global interrupt	false	true	true
DMA2 stream7 global interrupt	false	true	true

3.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0

Interrupt Table	Enable	Preenmption Priority	SubPriority
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line[15:10] interrupts	true	0	2
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
CM7 send event interrupt for CM4	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		
HSEM2 global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

3.5.4. NVIC2 Code generation

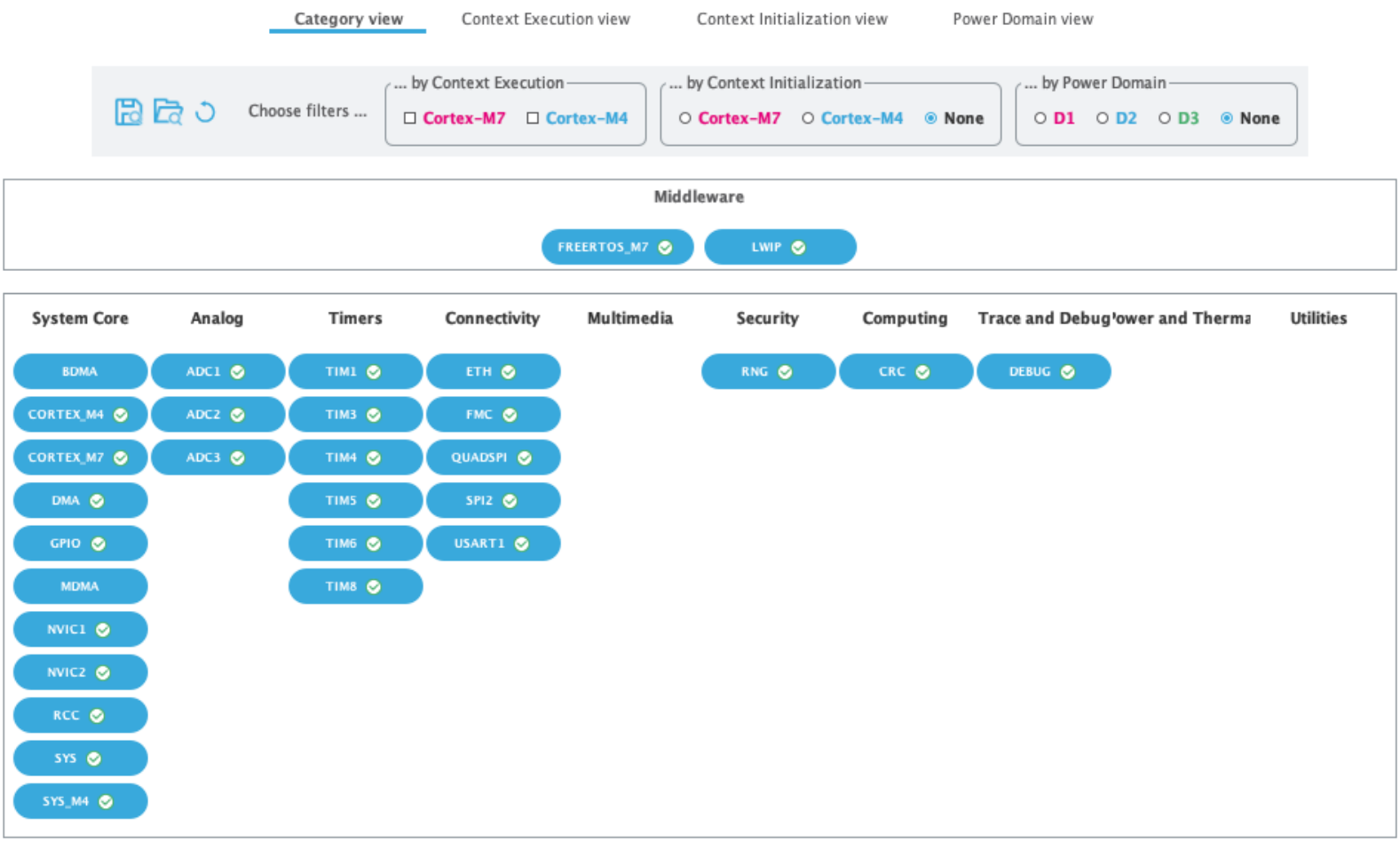
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line[15:10] interrupts	false	true	true

*** User modified value**

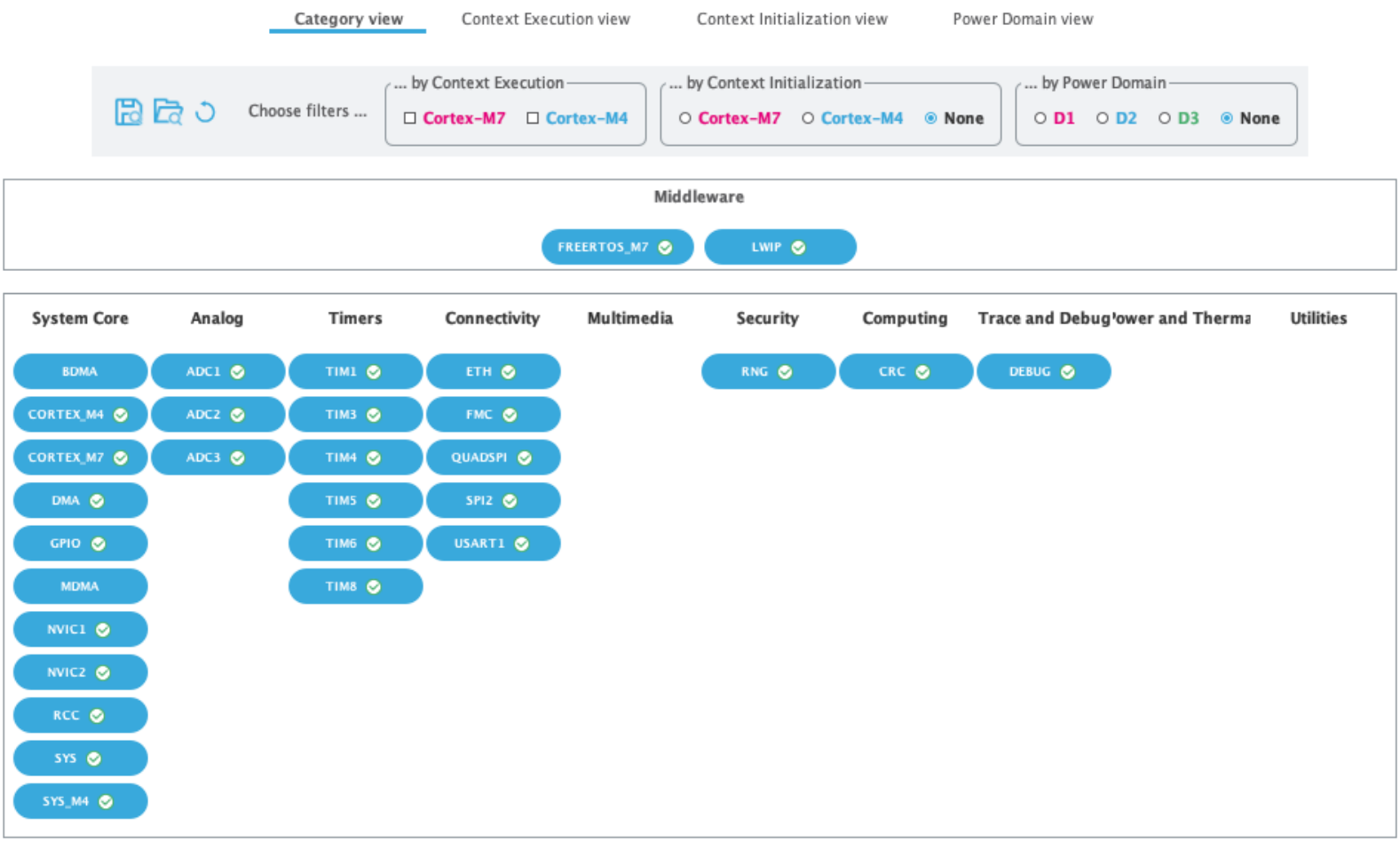
4. System Views

4.1. Category view

4.1.1. Current



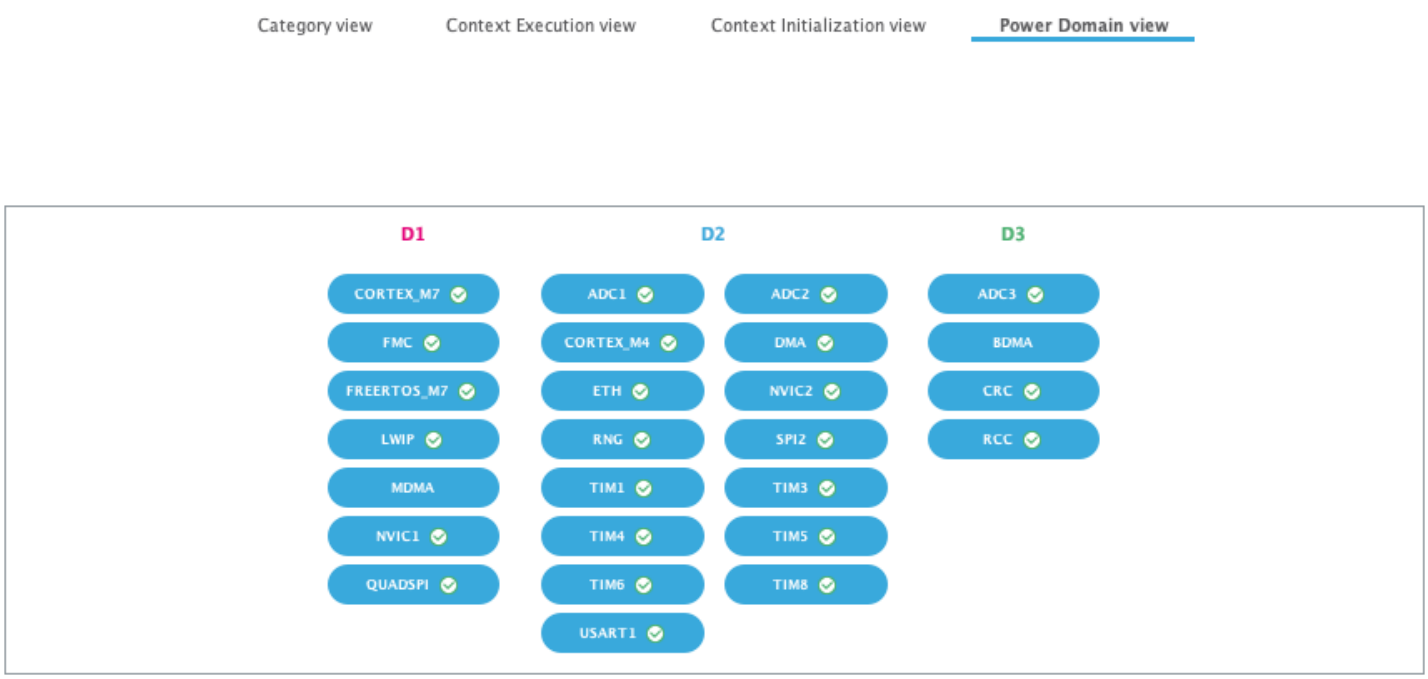
4.1.2. Without filters



4.2. Context Execution view

4.3. Context Initialization view

4.4. Power Domain view



5. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7vl.pdf
Brochures	https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2639-soldering-

	recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an2867-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4013-stm32-crossseries-timer-overview-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4229-how-to-implement-a-vocoder-solution-using-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4277-using-stm32-device-pwm-shutdown-features-for-motor-control-and-digital-power-conversion-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4861-lcdtft-display-controller-ltdc-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4908-stm32-usart-automatic-baud-rate-detection-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4990-getting-started-with-sigmadelta-digital-interface-on-applicable-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4996-hardware-jpeg-codec-peripheral-in-stm32f7677xxx-and-stm32h743534555475750a3b3b0xx-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5020-digital-camera-interface-dcmi-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5036-thermal-management-guidelines-for-stm32-applications-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an5073-receiving-spdif-audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf
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Application Notes	https://www.st.com/resource/en/application_note/an5286-stm32h7x5x7-dualcore-microcontroller-debugging-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5337-stm32h7-series-lifetime-estimates-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5354-getting-started-with-the-stm32h7-series-mcu-16bit-adc-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5405-fdcan-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5543-enhanced-methods-to-handle-spi-communication-on-stm32-devices-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5557-stm32h745755-and-stm32h747757-lines-dualcore-architecture-stmicroelectronics.pdf
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Application Notes	https://www.st.com/resource/en/application_note/an5293-migration-guide-

	from-stm32f7-series-to-stmh74x75x-stm32h72x73x-and-stmh7a37bx-devices-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5156-introduction-to-stm32-microcontrollers-security-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4838-introduction-to-memory-protection-unit-management-on-stm32-mcus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5348-introduction-to-fdcan-peripherals-for-stm32-product-classes-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4230-random-number-generation-validation-using-nist-statistical-test-suite-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5225-introduction-to-usb-typec-power-delivery-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an5342--how-to-use-error-correction-code-ecc-management-for-internal-memories-protection-on-stm32-mcus-stmicroelectronics.pdf
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Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an1602_semihosting_in_truestudio-how-to-do-semihosting-in-truestudio-stmicroelectronics.pdf

Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an1801_stm32cubeprogrammer_in_truestudio-installing-stm32cubeprogrammer-in-truestudio-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/atollic_editing_keyboard_shortcuts-atollic-editing-keyboard-shortcuts-stmicroelectronics.pdf
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Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4323-getting-started-with-stemwin-library-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4435-guidelines-for-obtaining-ulcsaiec-607301603351-class-b-certification-in-any-stm32-application-stmicroelectronics.pdf
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Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4759-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4841-digital-signal-processing-for-stm32-microcontrollers-using-cmsis-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4891-stm32h72x-

for related Tools & Software	stm32h73x-and-singlecore-stm32h74x75x-system-architecture-and-performance-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5001-stm32cube-expansion-package-for-stm32h7-series-mdma-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5014-stm32h7x3-smart-power-management-expansion-package-for-stm32cube-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5054-secure-programming-using-stm32cubeprogrammer-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5056-integration-guide-for-the-xcubesbsfu-stm32cube-expansion-package-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5360-getting-started-with-projects-based-on-the-stm32mp1-series-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5361-getting-started-with-projects-based-on-dualcore-stm32h7-microcontrollers-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5394-getting-started-with-projects-based-on-the-stm32l5-series-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5418-how-to-build-a-simple-usbpd-sink-application-with-stm32cubemx-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5426-migrating-graphics-middleware-projects-from-stm32cubemx-540-to-stm32cubemx-550-stmicroelectronics.pdf
Application Notes for related Tools	https://www.st.com/resource/en/application_note/an5534-stm32h735gdk-firmware-upgrade-for-atbased-emw3080-wifi-module-

& Software	stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5564-getting-started-with-projects-based-on-dualcore-stm32wl-microcontrollers-in-stm32cubeide-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4865-lowpower-timer-lptim-applicative-use-cases-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5698-adapting-the-xcubestl-functional-safety-package-for-stm32-iec-61508-compliant-to-other-safety-standards-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5731-stm32cubemx-and-stm32cubeide-threadsafe-solution-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5450-stm32h7a37b3-lines-and-stm32h7b0-value-line-smart-power-management-expansion-package-for-stm32cube-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an4502-stm32-smbuspmbus-expansion-package-for-stm32cube-stmicroelectronics.pdf
Application Notes for related Tools & Software	https://www.st.com/resource/en/application_note/an5952-how-to-use-cmake-in-stm32cubeide-stmicroelectronics.pdf
Design Notes & Tips	https://www.st.com/resource/en/design_tip/dt0117-microphone-array-beamforming-in-the-pcm-and-pdm-domain-stmicroelectronics.pdf
Errata Sheets	https://www.st.com/resource/en/errata_sheet/es0445-stm32h745xig-stm32h755xi-stm32h747xig-stm32h757xi-device-errata-stmicroelectronics.pdf
Datasheet	https://www.st.com/resource/en/datasheet/dm00600954.pdf
Programming Manuals	https://www.st.com/resource/en/programming_manual/pm0214-stm32-cortexm4-mcus-and-mpus-programming-manual-stmicroelectronics.pdf
Programming Manuals	https://www.st.com/resource/en/programming_manual/pm0253-stm32f7-series-and-stm32h7-series-cortexm7-processor-programming-manual-stmicroelectronics.pdf

Reference Manuals	https://www.st.com/resource/en/reference_manual/rm0399-stm32h745755-and-stm32h747757-advanced-armbased-32bit-mcus-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1163-description-of-wlcsp-for-microcontrollers-and-recommendations-for-its-use-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1204-tape-and-reel-shipping-media-for-stm32-microcontrollers-in-bga-packages-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1205-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-fpn-packages-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1206-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-qfp-packages-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1207-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-so-packages-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1208-tape-and-reel-shipping-media-for-stm8-and-stm32-microcontrollers-in-tssop-and-ssop-packages-stmicroelectronics.pdf
Technical Notes & Articles	https://www.st.com/resource/en/technical_note/tn1433-reference-device-marking-schematics-for-stm32-microcontrollers-and-microprocessors-stmicroelectronics.pdf
User Manuals	https://www.st.com/resource/en/user_manual/um2840-stm32h7-dualcore-series-safety-manual-stmicroelectronics.pdf