1. Description

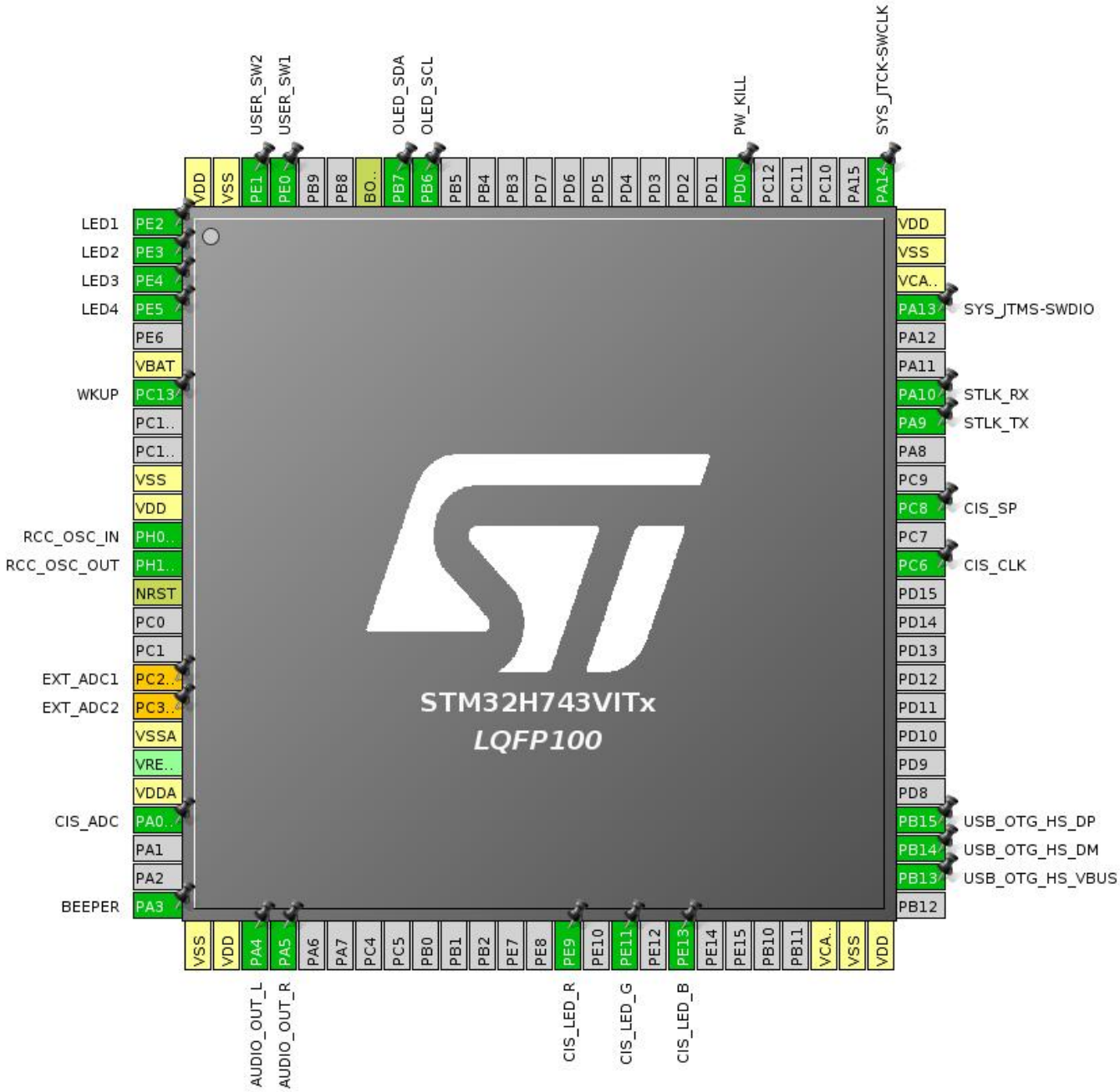
1.1. Project

Project Name	CISYNTH
Board Name	NARA
Generated with:	STM32CubeMX 4.26.0
Date	06/10/2018

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7x3
MCU name	STM32H743VITx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

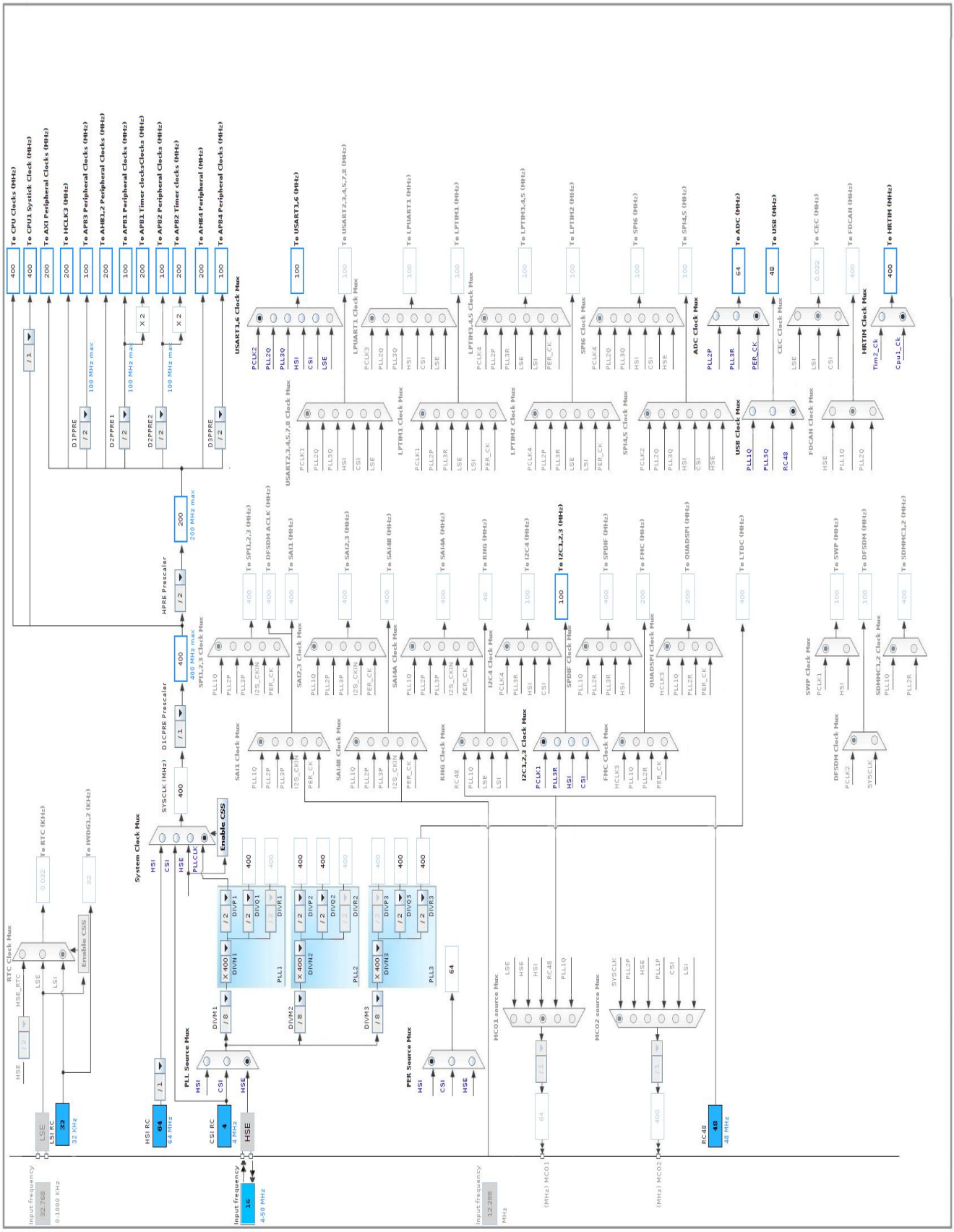
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	LED1
2	PE3 *	I/O	GPIO_Output	LED2
3	PE4 *	I/O	GPIO_Output	LED3
4	PE5 *	I/O	GPIO_Output	LED4
6	VBAT	Power		
7	PC13	I/O	SYS_WKUP2	WKUP
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
17	PC2_C **	I/O	ADC3_INP0	EXT_ADC1
18	PC3_C **	I/O	ADC3_INP1	EXT_ADC2
19	VSSA	Power		
21	VDDA	Power		
22	PA0-WKUP	I/O	ADC1_INP16	CIS_ADC
25	PA3	I/O	TIM5_CH4	BEEPER
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	DAC1_OUT1	AUDIO_OUT_L
29	PA5	I/O	DAC1_OUT2	AUDIO_OUT_R
39	PE9	I/O	TIM1_CH1	CIS_LED_R
41	PE11	I/O	TIM1_CH2	CIS_LED_G
43	PE13	I/O	TIM1_CH3	CIS_LED_B
48	VCAP1	Power		
49	VSS	Power		
50	VDD	Power		
52	PB13	I/O	USB_OTG_HS_VBUS	
53	PB14	I/O	USB_OTG_HS_DM	
54	PB15	I/O	USB_OTG_HS_DP	
63	PC6	I/O	HRTIM_CHA1	CIS_CLK
65	PC8	I/O	HRTIM_CHB1	CIS_SP
68	PA9	I/O	USART1_TX	STLK_TX
69	PA10	I/O	USART1_RX	STLK_RX
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP2	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
81	PD0 *	I/O	GPIO_Input	PW_KILL
92	PB6	I/O	I2C1_SCL	OLED_SCL
93	PB7	I/O	I2C1_SDA	OLED_SDA
94	BOOT0	Boot		
97	PE0 *	I/O	GPIO_Input	USER_SW1
98	PE1 *	I/O	GPIO_Input	USER_SW2
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN16: IN16 Single-ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 2
Resolution	**ADC 14-bit resolution ***
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Boost Mode	Enabled
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	**HRTIM1 Trigger Out 1 event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 16
Sampling Time	**32.5 Cycles ***
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. DAC1

OUT1 mode: Connected to external pin only

OUT2 mode: Connected to external pin only

5.2.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	**Disable ***
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

DAC Out2 Settings:

Output Buffer	**Disable ***
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled
User Trimming	Factory trimming
Sample And Hold	Sampleandhold Disable

5.3. HRTIM

mode: Master Timer Enable

Timer A: TA1 output active

Timer B: TB1 output active

5.3.1. HRTIM Interrupt Configuration:

Sources:

1st Source of interrupt	No interrupt enabled
2nd Source of interrupt	No interrupt enabled
3rd Source of interrupt	No interrupt enabled
4th Source of interrupt	No interrupt enabled
5th Source of interrupt	No interrupt enabled
6th Source of interrupt	No interrupt enabled
7th Source of interrupt	No interrupt enabled
8th Source of interrupt	No interrupt enabled

5.3.2. Synchro Configuration:

Master Timer Synchronization:

Sync Options	HRTIM instance doesn't handle external synchronization signals (SYNCIN, SYNCOUT)

5.3.3. External Event Configuration:

External Event 1:

Event Configuration	Disable

External Event 2:

Event Configuration	Disable

External Event 3:

Event Configuration	Disable

External Event 4:

Event Configuration	Disable

External Event 5:

Event Configuration	Disable

External Event 6:

Event Configuration	Disable

External Event 7:

Event Configuration	Disable

External Event 8:

Event Configuration	Disable

External Event 9:

Event Configuration	Disable

External Event 10:

Event Configuration	Disable

5.3.4. Fault Lines Configuration:

Fault Line 1:

Line Configuration	No Configuration of Fault Line

Fault Line 2:

Line Configuration	No Configuration of Fault Line

Fault Line 3:

Line Configuration	No Configuration of Fault Line

Fault Line 4:

Line Configuration	No Configuration of Fault Line

Fault Line 5:

Line Configuration	No Configuration of Fault Line

5.3.5. ADC Triggers Configuration:

ADC Trigger 1:

ADC Trigger Configuration	**Enable ADC Trigger 1 ***
Update Trigger Source	Master timer
Trigger Sources Selection : Please enter the number of Active Trigger Sources	**1 ***
1st Trigger Source	**ADC Trigger on master compare 1 ***

ADC Trigger 2:

ADC Trigger Configuration	Disable

ADC Trigger 3:

ADC Trigger Configuration	Disable

ADC Trigger 4:

ADC Trigger Configuration	Disable

5.3.6. Burst Mode Configuration:

Burst Mode Enabling:

Burst Mode	Burst mode disabled

5.3.7. Master Timer:

General:

Timer Idx	Master Timer

Time Base Setting:

Prescaler Ratio	HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value = 400MHz)
fHRCK Equivalent Frequency	4.0E8
Period	**1600 ***
Resulting PWM Frequency	250000
Repetition Counter	**0x00 ***
Mode	The timer operates in continuous (free-running) mode

Timing Unit:

Half Mode Enable - The Compare Value of CP Unit 1 is set automatically to half the Timer Period -	Half mode is disabled
Start On Sync	Synchronization input event has no effect on the timer

Reset On Sync	Synchronization input event has no effect on the timer
Dac Synchro	No DAC synchronization event generated
Preload Enable	Preload disabled: the write access is directly done into the active register
Update Gating	Update done independently from the DMA burst transfer completion
Repetition Update	Update on repetition disabled
Burst Mode	Timer counter clock is maintained and the timer operates normally
Interrupt Requests Sources Selection : Please enter the number of Active Interrupt Requests	0
Number of Master Timer Internal DMA Request Sources - you first have to enable the Master Timer DMA Request in the DMA Settings Tab	0

Compare Unit 1:

Compare Unit 1 Configuration	**Enable ***
Compare Value	**800 ***

Compare Unit 2:

Compare Unit 2 Configuration	Disable

Compare Unit 3:

Compare Unit 3 Configuration	Disable

Compare Unit 4:

Compare Unit 4 Configuration	Disable

Burst DMA Controller:

Burst DMA Configuration	Disable

5.3.8. Timer A:

General:

Timer Idx	Timer A
Basic/Advanced Configuration	Advanced (using HAL_Waveform methods)

Time Base Setting:

Prescaler Ratio	HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value = 400MHz)
fHRCK Equivalent Frequency	4.0E8
Period	**200 ***
Resulting PWM Frequency	2000000
Repetition Counter	**0x00 ***
Mode	The timer operates in continuous (free-running) mode

Timing Unit:

Half Mode Enable - The Compare Value of CP Unit 1 is set automatically to half the Timer Period -	Half mode is disabled
Start On Sync	Synchronization input event has no effect on the timer
Reset On Sync	Synchronization input event has no effect on the timer

Dac Synchro	No DAC synchronization event generated
Preload Enable	Preload disabled: the write access is directly done into the active register
Update Gating	Update done independently from the DMA burst transfer completion
Repetition Update	Update on repetition disabled
Burst Mode	Timer counter clock is maintained and the timer operates normally
Push Pull	Push-Pull mode disabled
Number of Faults to enable	0
Fault Lock	Timer fault enabling bits are read/write
Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the number of Triggers to select	0
Reset Update	Update by Timer reset / roll-over disabled
Reset Trigger Sources Selection : Please enter the number of Triggers to select	0
Interrupt Requests Sources Selection : Please enter the number of Active Interrupt Requests	0
Number of Timer A Internal DMA Request Sources - you first have to enable the Timer A DMA Request in the DMA Settings Tab	0

Compare Unit 1:

Compare Unit 1 Configuration	**Enable ***
Compare Value	**100 ***

Compare Unit 2:

Compare Unit 2 Configuration	Disable

Compare Unit 3:

Compare Unit 3 Configuration	Disable

Compare Unit 4:

Compare Unit 4 Configuration	Disable

Burst DMA Controller:

Burst DMA Configuration	Disable

Capture Unit 1:

Capture Unit 1 Configuration	Disable

Capture Unit 2:

Capture Unit 2 Configuration	Disable

External Event 1 Filtering:

Filtering Configuration	Disable

External Event 2 Filtering:

Filtering Configuration	Disable

External Event 3 Filtering:

Filtering Configuration	Disable

External Event 4 Filtering:

Filtering Configuration	Disable

External Event 5 Filtering:

Filtering Configuration	Disable

External Event 6 Filtering:

Filtering Configuration	Disable

External Event 7 Filtering:

Filtering Configuration	Disable

External Event 8 Filtering:

Filtering Configuration	Disable

External Event 9 Filtering:

Filtering Configuration	Disable

External Event 10 Filtering:

Filtering Configuration	Disable

Output 1 Configuration:

Output1 Configuration	TA1
Polarity	Output is active HIGH
Set Source Selection : Please enter the number of Active Set Sources	**1 ***
1st Set Source	**Timer period event forces the output to its active state ***
Reset Source Selection : Please enter the number of Active Reset Sources	**1 ***
1st Reset Source	**Timer period event forces the output to its inactive state ***
Idle Mode	The output is not affected by the burst mode operation
Idle Level	Output at inactive level when in IDLE state
Fault Level	The output is not affected by the fault input
Chopper Mode Enable	Output signal is not altered
Burst Mode Entry Delayed	The programmed Idle state is applied immediately to the Output

Chopper Mode:

Chopper Mode Configuration	Disable

5.3.9. Timer B:

General:

Timer Idx	Timer B
Basic/Advanced Configuration	Advanced (using HAL_Waveform methods)

Time Base Setting:

Prescaler Ratio	HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value = 400MHz)
fHRCK Equivalent Frequency	4.0E8

Period	**200 ***
Resulting PWM Frequency	2000000
Repetition Counter	**0x00 ***
Mode	The timer operates in continuous (free-running) mode

Timing Unit:

Half Mode Enable - The Compare Value of CP Unit 1 is set automatically to half the Timer Period -	Half mode is disabled
Start On Sync	Synchronization input event has no effect on the timer
Reset On Sync	Synchronization input event has no effect on the timer
Dac Synchro	No DAC synchronization event generated
Preload Enable	Preload disabled: the write access is directly done into the active register
Update Gating	Update done independently from the DMA burst transfer completion
Repetition Update	Update on repetition disabled
Burst Mode	Timer counter clock is maintained and the timer operates normally
Push Pull	Push-Pull mode disabled
Number of Faults to enable	0
Fault Lock	Timer fault enabling bits are read/write
Dead Time Insertion	Output 1 and output 2 signals are independent
Delayed Protection Mode	No action
Update Trigger Sources Selection : Please enter the number of Triggers to select	0
Reset Update	Update by Timer reset / roll-over disabled
Reset Trigger Sources Selection : Please enter the number of Triggers to select	0
Interrupt Requests Sources Selection : Please enter the number of Active Interrupt Requests	0
Number of Timer B Internal DMA Request Sources - you first have to enable the Timer B DMA Request in the DMA Settings Tab	0

Compare Unit 1:

Compare Unit 1 Configuration	**Enable ***
Compare Value	**100 ***

Compare Unit 2:

Compare Unit 2 Configuration	Disable

Compare Unit 3:

Compare Unit 3 Configuration	Disable

Compare Unit 4:

Compare Unit 4 Configuration	Disable

Burst DMA Controller:

Burst DMA Configuration	Disable

Capture Unit 1:

Capture Unit 1 Configuration	Disable

Capture Unit 2:

Capture Unit 2 Configuration	Disable

External Event 1 Filtering:

Filtering Configuration	Disable

External Event 2 Filtering:

Filtering Configuration	Disable

External Event 3 Filtering:

Filtering Configuration	Disable

External Event 4 Filtering:

Filtering Configuration	Disable

External Event 5 Filtering:

Filtering Configuration	Disable

External Event 6 Filtering:

Filtering Configuration	Disable

External Event 7 Filtering:

Filtering Configuration	Disable

External Event 8 Filtering:

Filtering Configuration	Disable

External Event 9 Filtering:

Filtering Configuration	Disable

External Event 10 Filtering:

Filtering Configuration	Disable

Output 1 Configuration:

Output1 Configuration	TB1
Polarity	Output is active HIGH
Set Source Selection : Please enter the number of Active Set Sources	**1 ***
1st Set Source	**Timer compare 1 event forces the output to its active state ***
Reset Source Selection : Please enter the number of Active Reset Sources	**1 ***
1st Reset Source	**Timer compare 1 event forces the output to its inactive state ***
Idle Mode	The output is not affected by the burst mode operation
Idle Level	Output at inactive level when in IDLE state
Fault Level	The output is not affected by the fault input
Chopper Mode Enable	Output signal is not altered
Burst Mode Entry Delayed	The programmed Idle state is applied immediately to the Output

Chopper Mode:

Chopper Mode Configuration	Disable

5.4. I2C1

I2C: I2C

5.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	**Disabled ***
Timing	**0x009039BB ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.5.1. Parameter Settings:

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	16

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	**4 WS (5 CPU cycle) ***

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

PLL range Parameters:

PLL1 clock Input range	Between 2 and 4 MHz
PLL1 clock Output range	Wide VCO range
PLL Fractional Part	0

5.6. SYS

Debug: Serial Wire

mode: System Wake-Up 2

Timebase Source: SysTick

5.7. TIM1

Channel1: Output Compare CH1

Channel2: Output Compare CH2

Channel3: Output Compare CH3

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High

BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

Output Compare Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 3:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

5.8. TIM5

Channel4: PWM Generation CH4

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**10000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**100 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	**50 ***
Fast Mode	Disable
CH Polarity	**Low ***

5.9. TIM6

mode: Activated

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0x7FF ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.10. USART1

Mode: Asynchronous

5.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Prescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.11. USB_OTG_HS

Internal FS Phy: Device_Only

Activate_VBUS: Activate-VBUS

5.11.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Physical interface	Internal Phy
Low power	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Enabled
Signal start of frame	Disabled

5.12. USB_DEVICE

Class For HS IP: Communication Device Class (Virtual Port Com)

5.12.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled

USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

5.12.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor HS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	CIS_ADC
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	AUDIO_OUT_L
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	AUDIO_OUT_R
HRTIM	PC6	HRTIM_CHA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	CIS_CLK
	PC8	HRTIM_CHB1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	CIS_SP
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	OLED_SCL
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	**Very High ***	OLED_SDA
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PC13	SYS_WKUP2	n/a	n/a	n/a	WKUP
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	CIS_LED_R
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	CIS_LED_G
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	CIS_LED_B
TIM5	PA3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	BEEPER
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_TX
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_RX
USB_OTG_HS	PB13	USB_OTG_HS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull-down	n/a	EXT_ADC1
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	EXT_ADC2
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down		LED1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					Very High *	
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LED2
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LED3
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	LED4
	PD0	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	PW_KILL
	PE0	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	USER_SW1
	PE1	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	USER_SW2

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low
ADC1	DMA1_Stream2	Peripheral To Memory	**Medium ***

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA1_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. BDMA configuration

nothing configured in DMA service

6.4. MDMA configuration

nothing configured in DMA service

6.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream2 global interrupt	true	0	0
ADC1 and ADC2 global interrupts	true	0	0
USART1 global interrupt	true	0	1
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	0	0
DMA2 stream7 global interrupt	true	0	0
USB On The Go HS global interrupt	true	0	0
HRTIM master timer global interrupt	true	0	0
HRTIM timer A global interrupt	true	0	0
HRTIM timer B global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
TIM5 global interrupt	unused		
USB On The Go HS End Point 1 Out global interrupt	unused		
USB On The Go HS End Point 1 In global interrupt	unused		
FPU global interrupt	unused		
HRTIM fault global interrupt	unused		
HSEM1 global interrupt	unused		
Interrupt for all 6 wake-up pins	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7x3
MCU	STM32H743VITx
Datasheet	030538_Rev1

7.2. Parameter Selection

Temperature	25
Vdd	3.0

8. Software Project

8.1. Project Settings

Name	Value
Project Name	CISYNTH
Project Folder	/mnt/Data/Documents/Pacabot/CISYNTH/Electronique
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_H7 V1.2.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

9. Software Pack Report