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Modified Modulation Signals for GaN-E-HEMTs based HERIC Inverter to Improve Reverse Conduction Performance

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Keywords

«Emerging Topology», «Gallium Nitride (GaN)», «Photovoltaic», «Wide Band Gap Devices», «Reactive Power»

Abstract

This paper presents an application of modified PWM signals to enhance the efficiency of GaN HEMTs based HERIC inverter. Although application of GaN switches might increases the power density and overall efficiency of inverters due to the structure of GaN HEMTs, reverse conduction losses are increased during the second and fourth quadrant operation of the inverter. Hence, control of the inverter requires modifications to tackle additional losses introduced by GaN switches. Conventional PWM signals were designed to suppress the leakage current by keeping the voltage level constant at the switching nodes in all operating modes. However, modified PWM signals not only suppress the leakage current but also reduce the reverse conduction losses in GaN HEMTs. In this paper, proposed theory is validated by simulations based on spice models provided by the manufacturer of switches on LTspice. Simulation results validated the proposed solution and reported almost 50% reduction in reverse conduction losses. Practical prototype based on GaN HEMTs was also designed and tested. This study aids understanding the effect of the reverse losses on the device behavior and overall efficiency of the inverter.

I. Introduction

Performance of power electronics converters govern the overall efficiency of the system [1]. However, converters are usually equipped with bulky transformers for galvanic isolation purposes or to shift the power level. On an average these bulky transformers accounts for 49% of total losses and 58% of total converter weight [2]. In order to improve the conversion efficiency and energy density, transformerless inverters have been introduced. These inverters are more efficient and lighter in weight than conventional transformer isolation-based inverters [3]. However, absence of high frequency or low frequency transformers also increases the problems related to Common Mode (CM) noise as there will be no galvanic isolation between the inverter and the grid [4].

Grid-connected photovoltaic inverters must comply with standards related to electromagnetic compatibility and power quality [5]. In transformerless solar inverters varying voltage at switching nodes can generate leakage current through parasitic capacitance. This leakage current will flow into the grid through the ground. Without appropriate filters conventional H-bridge with four switches does not meet the leakage current requirements imposed by standards with both bipolar and unipolar Pulse Width Modulation (PWM) techniques. In order to comply with standards and improve electromagnetic compatibility of the inverter, it is very important to eliminate or reduce the leakage current under limit

specified by the standards [3]. Leakage current to the ground through parasitic capacitances can be reduced by keeping the constant voltage level at switching nodes for all operation modes. [6]. Following this theory, many transformerless topologies based on H-bridge have been proposed to suppress common mode noise [7].

Various new transformerless topologies have been introduced and few of them have been reviewed in [8]. Highly Efficient and Reliable Inverter Concept (HERIC) with six switches was proposed in 2006 [9], offering superior noise suppression properties. This topology has various applications in grid-connected systems. In such systems solar inverters are also required to supply reactive power and hence inverter will also operate and in second and fourth quadrant [10].

Efficiency of the solar inverters can be further increased by the application of GaN-devices with low drain-source resistance, input capacitance (C_{ISS}) and output capacitance (C_{OSS}) [11], [12] .Normally-off GaN E-HEMT [13] is an excellent choice for applications with high efficiency and high-power density. However, when the inverter supplies reactive power to the grid, current flows in reverse direction i.e. from grid to the inverter. During reverse conduction of current, it flows through the body diodes of the switches [14]. GaN E-HEMT has the intrinsic capability of conducting current in reverse direction [15],[13]. However, it is recommended to apply negative gate-source voltage to turn-off GaN switches because of their low threshold voltage. The voltage drop during reverse conduction across GaN HEMT depends on the gate-source biasing. Hence, it becomes critical to consider their reverse conduction performance before choosing one for application.

In this study, the performance of GaN E-HEMT during reverse conduction has been evaluated for their application in HERIC inverters under loads with different power factors. To reduce the reverse losses, modified PWM signals for HERIC inverter are also presented. A comprehensive analysis is made to study the effect of modified PWM signals on power quality and noise elimination capability of the HERIC inverter. Spice based simulation and a 500W experimental prototype are constructed to perform analysis for reverse conduction of GaN E-HEMT.

This paper is organized as follows. A brief description of the HERIC inverter topology and its working principle are given in Section II. Section III presents the proposed modifications in PWM signals or efficiency optimization during reverse conduction and analysis of the HERIC inverter with modified PWM. In Section IV, experimental platform is presented. Finally, conclusions are given in Section V.

II. HERIC Inverter Topology

HERIC Inverter topology is derived from the simple H-bridge, with two extra switches and two diodes in isolated legs. DC bus of the inverter is disconnected from the AC grid at each zero crossing. Fig. 1 shows the schematic of HERIC inverter.

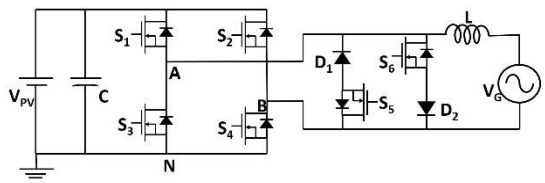


Fig 1: HERIC Inverter

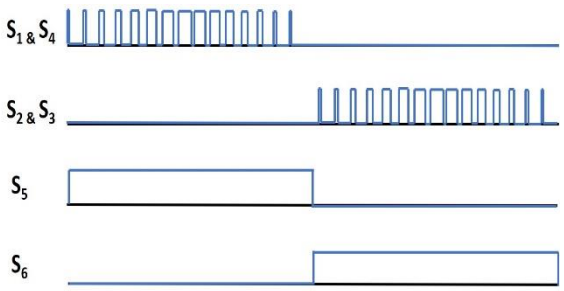


Fig 2: PWM Signals for HERIC Inverter

Fig. 2 represents the PWM signals for the HERIC inverter. Operating modes of HERIC inverter are presented in Fig 3. In Fig.3 (a) S_1 and S_4 are conducting to generate a positive voltage at the output. Switch S_5 is kept switched on for the entire positive half cycle. However, it will only conduct through D_1 when both S_1 and S_4 are switched off. In Fig.3 (b) S_5 is conducting through diode D_1 to realize zero voltage state during the positive half cycle. As shown in Fig.3(c) during the negative half cycle, S_2 and S_3 are switched at the carrier frequency to generate negative voltage at the output and S_6 short-circuits the load to produce zero voltage during the negative half cycle in Fig. 3 (d).

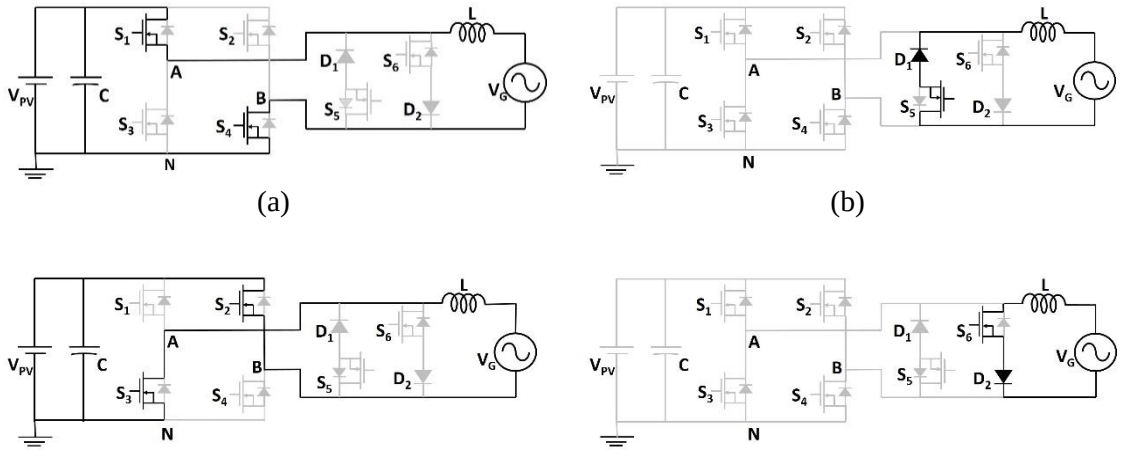


Fig 3: Conduction cycles of the HERIC inverter

However, at switching nodes A and B in Fig. (4), high frequency switching voltages across the parasitic capacitances C_1 and C_2 generate leakage current that flows through the ground. Common mode voltage can be defined as [16].

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \qquad (1)$$

Where V_{AN} and V_{BN} are the voltages at switching nodes as shown in Fig. 4. Common mode voltage in all four conducting states, as shown in Table 1, remains constant and eliminates the leakage current in the HERIC inverter. This explains the excellent leakage current elimination capability of the HERIC inverter. However, presence of inductive load, introduces irregularities in the current waveform. Fig.5 demonstrates the output current waveform of the HERIC inverter with RL load.

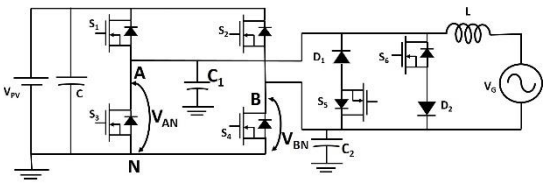


Fig 4: Parasitic capacitance across switching nodes

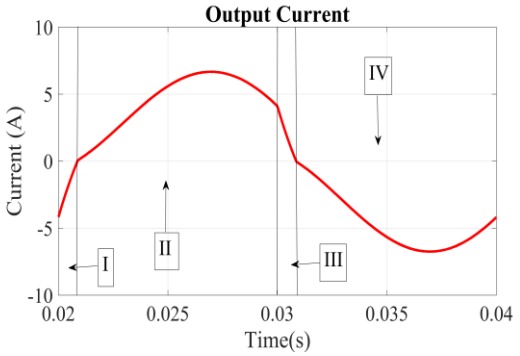
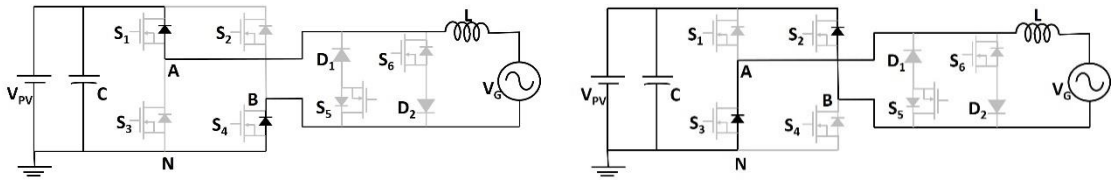


Fig 5: Current waveform for HERIC Inverter

Table I: Voltage at Switching Nodes

STATE		V_{AN}	V_{BN}	V_{CM}
Fig. 3 (a)	V_P^+	V_{PV}	0	$V_{PV}/2$
Fig. 3 (b)	V_P^0	$V_{PV}/2$	$V_{PV}/2$	$V_{PV}/2$
Fig. 3 (c)	V_N^-	0	V_{PV}	$V_{PV}/2$
Fig. 3 (d)	V_N^0	$V_{PV}/2$	$V_{PV}/2$	$V_{PV}/2$

During section I and section III of Fig. 5 grid current will flow through the body diodes of the switches to dump the energy into input capacitor. Conduction states during these intervals are presented in Fig.6(a) and Fig.6(b) respectively.



(a) (b)

Fig 6: Reverse conduction in the HERIC Inverter

III. Efficiency optimization during Reverse Conduction

Conventionally power losses across the switching device are estimated by using the Eq.(1). [17]

$$P_{DEVICES} = V_D I_{AVG} + V_O (Q_{rr} + I_{L,MIN} t_{rr}) f_{SW} + R_{DS,(ON)} I_{T,\mathrm{Re}\,f}^{\ 2} + C_{ISS} V_{CG}^{\ 2} f_{SW} + V_O I_i (t_r + t_f) + \frac{1}{2} C_{OSS} V_O^{\ 2} f_{SW} \quad (2)$$

In Eq. (2), first two terms that are incorporating the losses during reverse conduction of the switches. Where, Q_{rr} is reverse recovery charge stored in P-N junction and t_{rr} is the reverse recovery time of the body diode. Detailed parameters of GaN E-HEMTs chosen for this study are given in Table II. As both reverse recovery charge and reverse recovery time is 0 for GaN E-HEMTs, switching losses during reverse conduction should be zero. In Eq. (1) conduction losses of body diode of the switch are estimated by the first term i.e. $V_D I_{AVG,}$ where V_D is the forward drop of the body diode. However, unlike in Si Mosfets forward drop of body diode in GaN E-HEMTs is dependent on the Gate-Source V_{GS} voltage. Hence, we can't estimate the reverse conduction losses for GaN E-HEMTs by using the Eq. (1).

Table II: Parameter of switching devices

Technology	C_{ISS} (pF)	C_{OSS} (pF)	t_r (ns)	t_f (ns)	$R_{DS,ON}$ (mΩ)	Q_{rr} (nC)	t_{rr} (ns)
E-HEMT	160	28	5.20	2.40	290	0	0
	195	49	4.90	5.20	175	0	0

Table III: Simulation Parameters

Parameter	Value
DC Bus Voltage	400 V
Switching frequency (f_{sw})	200 kHz
Grid Voltage	230 V_{RMS}
Output Current	2.5 A

As shown in Fig. 6, during reverse conduction current flows through the body diodes of the switches. Duration of reverse conduction depends on the power factor of the load. To estimate the reverse losses, simulations for HERIC inverter based on spice models of 650 V GaN E-HEMT and gate driver from Texas Instruments have been performed. Parameters of simulations are given in Table III. For this study voltage level of 400 V has been chosen for DC bus to maintain the inverter output voltage at grid level of 230 $V_{RMS.}$ To keep balance between the switching efficiency and power density switching frequency of 200 kHz has been selected. As GaN E-HEMTs have lower gate threshold voltage (V_{TH} = 1.3V), during switching off, negative biasing of -2V has been applied across gate-source terminals to avoid false switching.

Fig.7 shows the normalized reverse conduction losses with respect to the total losses (reverse conduction + forward conduction + switching losses) for different values of displacement angle between grid voltage and output current of the inverter. At higher values of displacement angle, majority of the

losses across GaN E-HEMTs in the application of HERIC inverter originates during the reverse conduction.

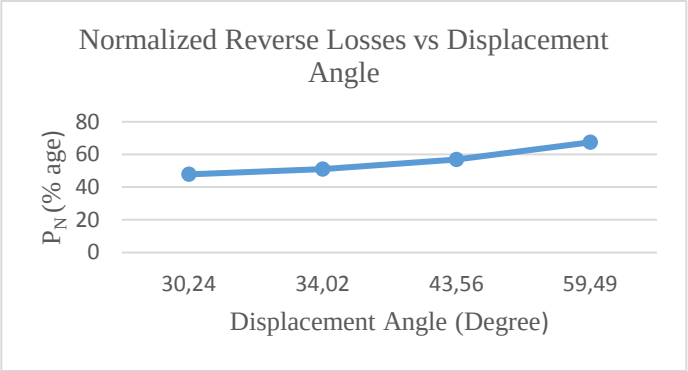


Fig 7: Losses vs. Displacement Angle

One way to reduce the reverse conduction losses is to remove negative biasing during switching off the GaN E-HEMTs. However, this will also increase chances of false switching and hence can lead to an accident. Another way of improving the efficiency and reducing the reverse losses is by modifying the PWM signals only during the sections I and III of Fig. 5, i.e. only when the switches are conducting in reverse direction.

In order to reduce the reverse conduction losses, two modified PWM schemes namely Modified PWM Signals (a) and Modified PWM signals (b) have been introduced in this paper.

Modified PWM Signals – (a)

As described in previous section that forward voltage drop in body diode of the GaN E-HEMT is dependent on the voltage across its gate-source terminals. Hence, by switching on the GaN E-HEMT while they are conducting in reverse direction, forward drop across body diode can be reduced.

As duration of reverse conduction in HERIC inverter depends on the displacement angle of the load, there is a need of an intelligent feedback system to find the duration of Section I and III i.e. duration of reverse conduction during positive and negative half cycle. Fig .8 demonstrates the feedback loop comprising of zero crossing detector circuit (ZCD) and a DSP, required to generate modified PWM signals.

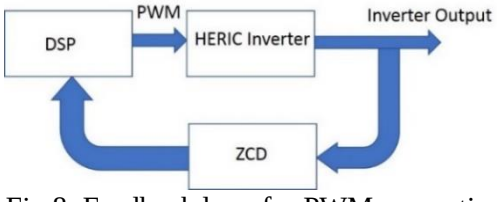


Fig 8: Feedback loop for PWM generation

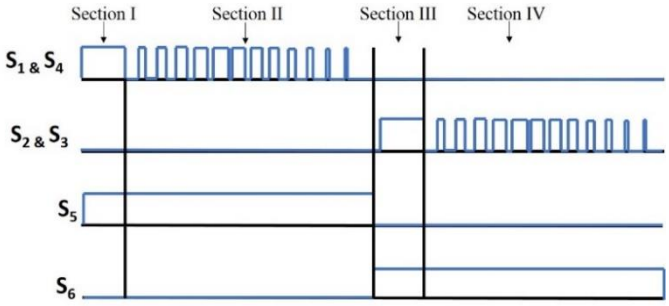


Fig 9: Modified PWM Signals-(a)

Sections (I-IV) in Fig. 9 corresponds to conduction states that are explained in Fig. 3. Spice based simulations with parameters defined in Table. III are performed with modified PWM signals to estimate the normalized reverse conduction losses for different displacement angles. Results of the simulations are displayed in Fig 10.

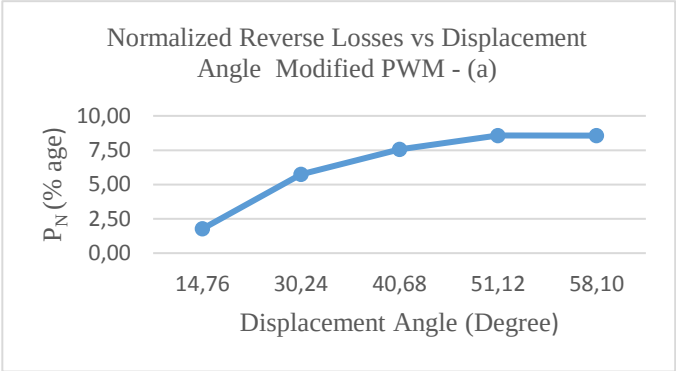


Fig 10: Losses Vs Displacement Angle- Modified PWM (a)

These results exhibit reductions in reverse losses by the factor of almost 50% with application of the modified PWM signals in the HERIC inverter. For the modified PWM signals, common mode voltage at switching nodes will also remain constant, hence it will not affect the capability of HERIC topology to eliminate the leakage current.

Modified PWM Signals – (b)

Though PWM signals described in previous section reduce the reverse conduction losses, but the power quality remains same as in with conventional PWM signals. [18], [19] proposed modified PWM signals to improve the power quality of the HERIC inverter. After slight modification these PWM signals can also be employed to reduce the reverse conduction losses across GaN HEMTs. In PWM signals shown in Fig.9, switches S_5 and S_6 are switched at fundamental frequency i.e. 50Hz. However, to control the free-wheeling current during Section I & III, PWM signals are further modified.

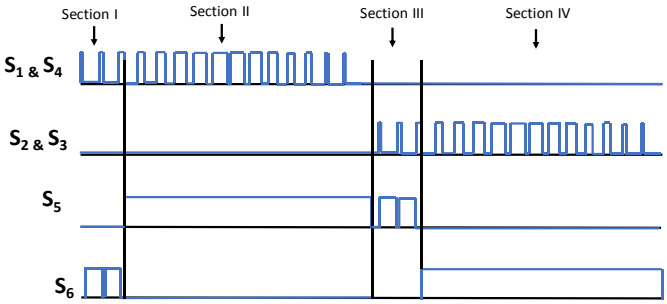


Fig 11: Modified PWM Signals (b)

Fig.11 represents the modified PWM signals that are employed to improve the power quality and efficiency of the HERIC inverter. Here, switches S_6 & S_5 are switched at carrier frequency during section I & III respectively. During section I, there will be freewheeling current flowing back through the switches S_1 and S_4. In order to provide an alternative path to that circulating current, S_6 is switched at switching frequency and complimentary to S_1 & S_4. In order to avoid short circuiting of input DC source, it is crucial to keep S_6 switched off when switches S_1 and S_4 are switched on.. When S_6 is switched on, negative freewheeling current will flow through S_6 and diode D_2 as shown in Fig. 3 (d). However, when S_6 is switched off and S_1 & S_4 are switched on, as shown in Fig 6 (a), body diodes of S_1 & S_4 will conduct.

During section III, freewheeling current flows through the body diodes of switches S_2 and S_3. Hence, following the same principle as described, S_5 is switched at switching frequency and complimentary to switches S_2 and S_3 during this section. When S_5 is switched on S_5 and D_1 will conduct as in Fig. 3(b). Otherwise body diodes of S_2 & S_3 will be conducting and it is shown in Fig. 6(b). Results of spice simulations for HERIC inverter with modified PWM with same parameters as in Table. II are presented in Fig. 12.

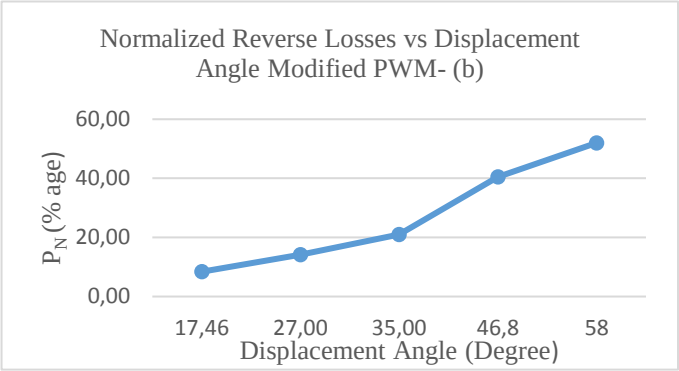


Fig 12: Losses Vs Displacement Angle- Modified PWM (b)

Results from Fig.12 show that the reverse conduction losses have been reduced as compared losses with conventional PWM. However, losses are higher than with modified PWM (a). Reason for increase in losses is due to increase in switching losses during section I and III. With modified PWM (b) signals freewheeling current is being shared between HERIC switch S_5 and switches S_2, S_3 during section III and between S_6 and S_1, S_4 during section I. As described above during section I, when S_6 is switched off, current starts flowing through the body diodes of S_1 and S_4. As S_6 will take some finite time to completely switch off, hence during turn off time of S_6, input DC source is short circuited which results in higher switching losses. Similarly, this process repeats during section III as well. As duration of section I and III depends on the displacement angle, hence for higher inductive loads, larger duration

of these sections will result in higher switching losses. This aspect of modified PWM (b) signals will be studied more in detail in future publications.

IV. Experimental Setup

A double layer PCB has been designed for prototyping, with signal tracks on top layer and ground plains on bottom layer to improve the electro-magnetic compatibility. GaN E HEMT has been chosen as a switching device. Table IV shows the detailed parameters of the practical prototype.

Fig. 13 shows the practical prototype of HERIC inverter with digital signal processor (DSP).DSP from Texas Instrument TMS320F28335 has been used to generate PWM signals while core-less current sensor CQ3200 has been used to realize ZCD. Inverter was operated at 100 VDC with R-L passive load. Output voltage and current of the inverter without ant capacitive filter is shown in Fig.14.

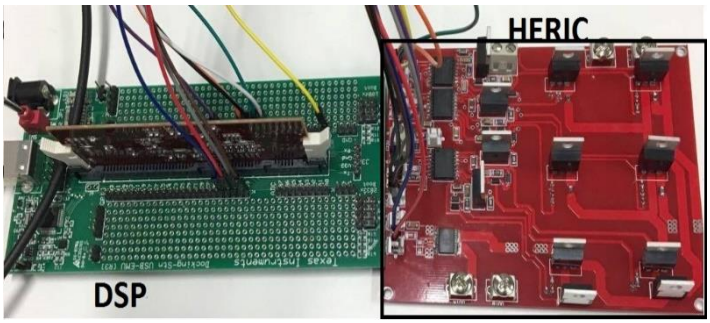


Fig 13: Practical Prototype

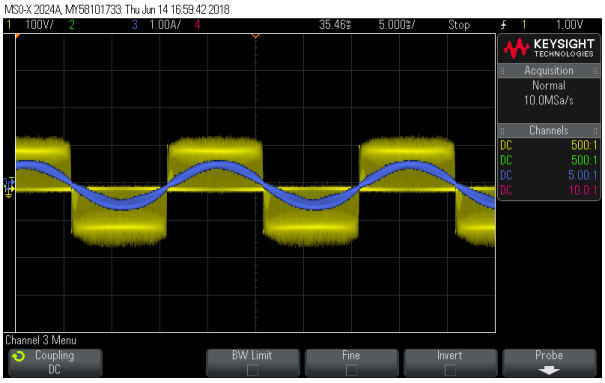


Fig 14: HERIC output voltage and output current

Variable inductive load was connected to the inverter to obtain losses across the switch for different values of displacement angle. Normalized reverse conduction losses for conventional PWM signals at different displacement angles are shown in Fig. 15.

Table IV: Parameters for prototype

Circuit Parameters		
V_{DC}	DC Input Voltage	100 V
P_R	Rated Power	500 W
f_{SW}	Switching Frequency	100 kHz
f_g	Grid Frequency	50 Hz
Switching Device	GSS´66504B	

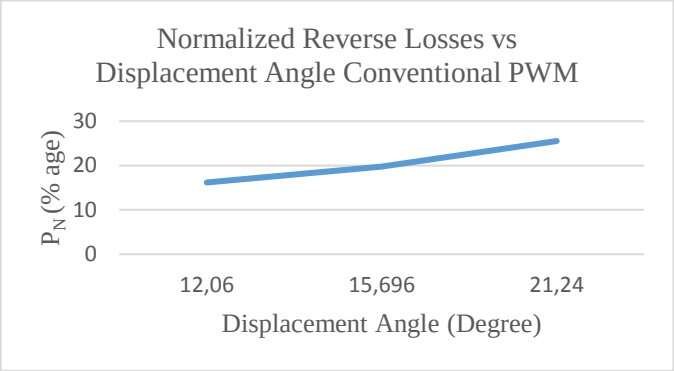


Fig 15: Losses Vs Displacement Angle (Practical Results)

V. Conclusion

In this paper, modified pulse width modulations (Fig.9 & Fig. 11) are introduced in HERIC inverter for efficiency optimization during injection of reactive power. The first proposed modulation shown in Fig. 9 successfully reduced the reverse conduction losses by a factor of almost 50% without effecting the power quality and noise elimination capability of the HERIC inverter. However, in second proposed modulation method (Fig.11), during the reverse conduction period switching losses are increased across S_5 and S_6. Despite higher switching losses, overall reverse conduction losses are reduced by 20% by the application of second proposed method in comparison to the conventional modulation signals. Second modified modulation signals also improve the power quality without effecting the noise elimination capability [18], [19]. This paper also provides a basis for the future studies to develop an empirical formula to estimate the reverse conduction losses as a function of grid displacement angle in transformerless solar inverters during injection of reactive power. That estimation will aid engineers during design of inverters.

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