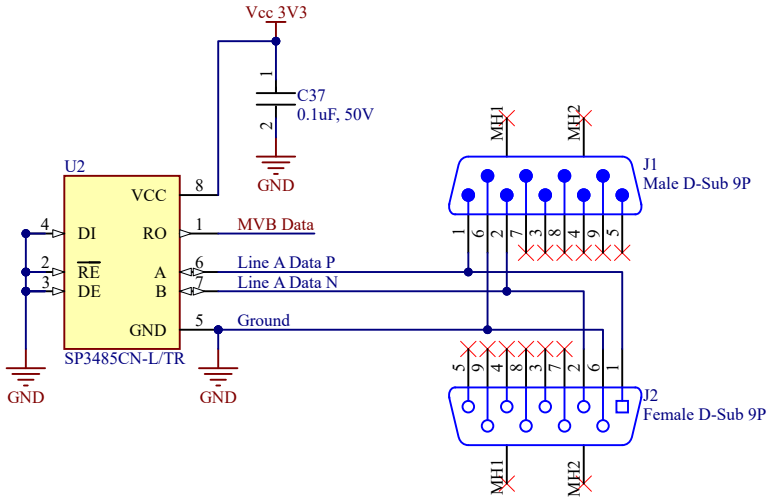
MVB to RS485



FPGA Banks

U1H

BANK 1A

IO, ADC1IN2, (DIFFIO_RX_L1p, DIFFOUT_L1p)
IO, ADC1IN1, (DIFFIO_RX_L1n, DIFFOUT_L1n)
IO, ADC1IN4, (DIFFIO_RX_L3p, DIFFOUT_L3p)
IO, ADC1IN3, (DIFFIO_RX_L3n, DIFFOUT_L3n)
IO, ADC1IN6, (DIFFIO_RX_L5p, DIFFOUT_L5p)
IO, ADC1IN5, (DIFFIO_RX_L5n, DIFFOUT_L5n)
IO, ADC1IN8, (DIFFIO_RX_L7p, DIFFOUT_L7p)
IO, ADC1IN7, (DIFFIO_RX_L7n, DIFFOUT_L7n)

10M08SAE144C8GES

U1I

BANK 1B

IO, TCK, (DIFFIO_RX_L11p, DIFFOUT_L11p) — TCK
IO, TMS, (DIFFIO_RX_L11n, DIFFOUT_L11n) — TMS
IO, TDO, (DIFFIO_RX_L12p, DIFFOUT_L12p) — TDO
IO, TDI, (DIFFIO_RX_L12n, DIFFOUT_L12n) — TDI
IO, (DIFFIO_RX_L14p, DIFFOUT_L14p)
IO, (DIFFIO_RX_L14n, DIFFOUT_L14n)
IO, (DIFFIO_RX_L16p, DIFFOUT_L16p)
IO, (DIFFIO_RX_L16n, DIFFOUT_L16n)
IO, JTAGEN — JTAGEN
IO, VREFB1N0

10M08SAE144C8GES

U1A

BANK 2

IO, CLK0p, (DIFFIO_RX_L18p, DIFFOUT_L18p) — OSC OUT
IO, CLK0n, (DIFFIO_RX_L18n, DIFFOUT_L18n)
IO, CLK1p, (DIFFIO_RX_L20p, DIFFOUT_L20p)
IO, CLK1n, (DIFFIO_RX_L20n, DIFFOUT_L20n)
IO, PLL_L_CLKOUTp, (DIFFIO_RX_L27p, DIFFOUT_L27p)
IO, PLL_L_CLKOUTn, (DIFFIO_RX_L27n, DIFFOUT_L27n)
IO, VREFB2N0

10M08SAE144C8GES

U1G

BANK 8

IO
IO, (DIFFIO_RX_T16p, DIFFOUT_T16p)
IO, DEV_CLRn, (DIFFIO_RX_T16n, DIFFOUT_T16n) — RESET N
IO, (DIFFIO_RX_T19p, DIFFOUT_T19p)
IO, (DIFFIO_RX_T19n, DIFFOUT_T19n)
IO, (DIFFIO_RX_T20p, DIFFOUT_T20p)
IO, (DIFFIO_RX_T20n, DIFFOUT_T20n)
IO, (DIFFIO_RX_T22p, DIFFOUT_T22p)
IO, CRC_ERROR, (DIFFIO_RX_T22n, DIFFOUT_T22n)
IO, nSTATUS, (DIFFIO_RX_T24p, DIFFOUT_T24p)
IO, CONF_DONE, (DIFFIO_RX_T24n, DIFFOUT_T24n)
IO, (DIFFIO_RX_T26p, DIFFOUT_T26p)
IO, (DIFFIO_RX_T26n, DIFFOUT_T26n)
IO, CONFIG_SEL — BOOT SEL
IO, DEV_OE
IO, VREFB8N0
nCONFIG — NCONFIG

3V3 FPGA
R5 1k
R6 1k

10M08SAE144C8GES

U1B

BANK 3

IO
IO, (DIFFIO_TX_RX_B1p, DIFFOUT_B1p)
IO, (DIFFIO_TX_RX_B1n, DIFFOUT_B1n)
IO, (DIFFIO_TX_RX_B3p, DIFFOUT_B3p)
IO, (DIFFIO_TX_RX_B3n, DIFFOUT_B3n)
IO, (DIFFIO_TX_RX_B5p, DIFFOUT_B5p)
IO, (DIFFIO_TX_RX_B5n, DIFFOUT_B5n)
IO, (DIFFIO_TX_RX_B7p, DIFFOUT_B7p)
IO, (DIFFIO_TX_RX_B7n, DIFFOUT_B7n)
IO, (DIFFIO_TX_RX_B9p, DIFFOUT_B9p)
IO, (DIFFIO_TX_RX_B9n, DIFFOUT_B9n)
IO, (DIFFIO_TX_RX_B12p, DIFFOUT_B12p)
IO, (DIFFIO_TX_RX_B12n, DIFFOUT_B12n)
IO, (DIFFIO_TX_RX_B14p, DIFFOUT_B14p)
IO, (DIFFIO_TX_RX_B14n, DIFFOUT_B14n)
IO, (DIFFIO_TX_RX_B16p, DIFFOUT_B16p)
IO, (DIFFIO_TX_RX_B16n, DIFFOUT_B16n)
IO, VREFB3N0

MISO
HS FPGA
INTR FPGA
MVB Data
MVB Active
RES1
RES2
RES3
RES4
FPGA RES5
FPGA RES6
FPGA RES7

R2 0 CS
R3 0 MOSI
R4 0 SCLK

10M08SAE144C8GES

Unused

U1C

BANK 4

IO
IO
IO, (DIFFIO_TX_RX_B23p, DIFFOUT_B23p)
IO, (DIFFIO_TX_RX_B23n, DIFFOUT_B23n)
IO, (DIFFIO_TX_RX_B27p, DIFFOUT_B27p)
IO, (DIFFIO_TX_RX_B27n, DIFFOUT_B27n)
IO, VREFB4N0

10M08SAE144C8GES

U1D

BANK 5

IO
IO, (DIFFIO_RX_R1p, DIFFOUT_R1p)
IO, (DIFFIO_RX_R1n, DIFFOUT_R1n)
IO, (DIFFIO_RX_R2p, DIFFOUT_R2p)
IO, (DIFFIO_RX_R2n, DIFFOUT_R2n)
IO, (DIFFIO_RX_R7p, DIFFOUT_R7p)
IO, (DIFFIO_RX_R7n, DIFFOUT_R7n)
IO, (DIFFIO_RX_R10p, DIFFOUT_R10p)
IO, (DIFFIO_RX_R10n, DIFFOUT_R10n)
IO, (DIFFIO_RX_R11p, DIFFOUT_R11p)
IO, (DIFFIO_RX_R11n, DIFFOUT_R11n)
IO, VREFB5N0

10M08SAE144C8GES

U1E

BANK 6

IO, CLK2p, (DIFFIO_RX_R14p, DIFFOUT_R14p)
IO, CLK2n, (DIFFIO_RX_R14n, DIFFOUT_R14n)
IO, CLK3p, (DIFFIO_RX_R16p, DIFFOUT_R16p)
IO, CLK3n, (DIFFIO_RX_R16n, DIFFOUT_R16n)
IO, (DIFFIO_RX_R18p, DIFFOUT_R18p)
IO, (DIFFIO_RX_R18n, DIFFOUT_R18n)
IO, DPCLK3, (DIFFIO_RX_R26p, DIFFOUT_R26p)
IO, DPCLK2, (DIFFIO_RX_R26n, DIFFOUT_R26n)
IO, (DIFFIO_RX_R27p, DIFFOUT_R27p)
IO, (DIFFIO_RX_R27n, DIFFOUT_R27n)
IO, (DIFFIO_RX_R28p, DIFFOUT_R28p)
IO, (DIFFIO_RX_R28n, DIFFOUT_R28n)
IO, (DIFFIO_RX_R33p, DIFFOUT_R33p)
IO, (DIFFIO_RX_R33n, DIFFOUT_R33n)
IO, VREFB6N0

10M08SAE144C8GES

U1F

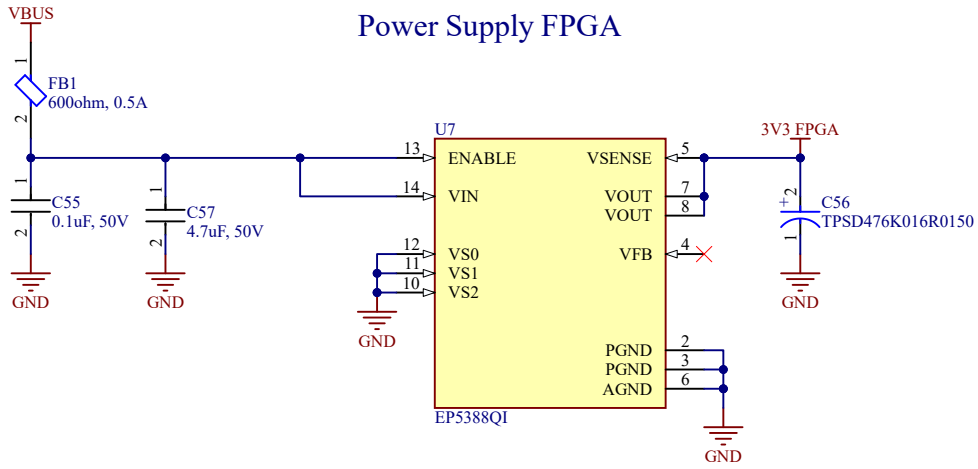
BANK 7

IO
IO
IO, (DIFFIO_RX_T1p, DIFFOUT_T1p)
IO, (DIFFIO_RX_T1n, DIFFOUT_T1n)
IO, (DIFFIO_RX_T10p, DIFFOUT_T10p)
IO, (DIFFIO_RX_T10n, DIFFOUT_T10n)
IO, VREFB7N0

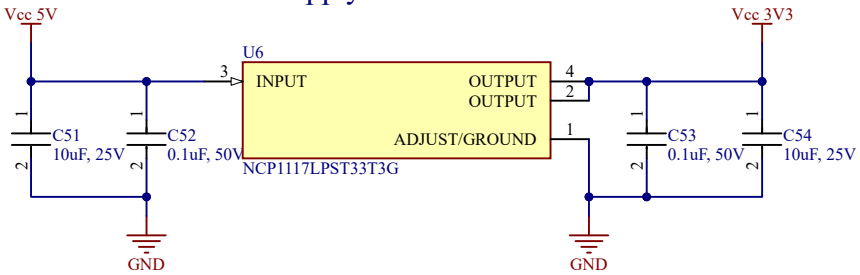
10M08SAE144C8GES

Title	MVB-Sniffer: RS485 & FPGA Banks	
Size: A4	Number	Revision: 1.1
Date: 12.16.2024		Sheet 1 of 5
File: E:\00_PA\..\RS485_FPGA_Banks.SchDoc		Drawn By:

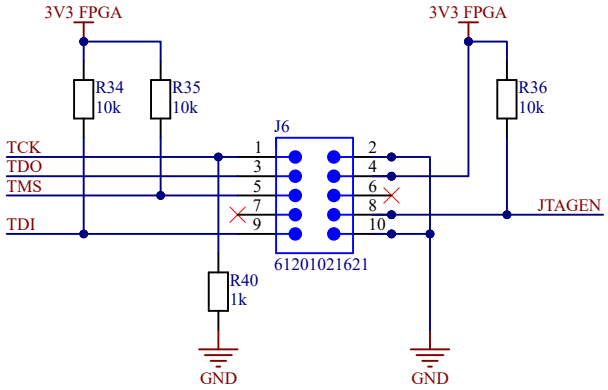
Power Supply FPGA



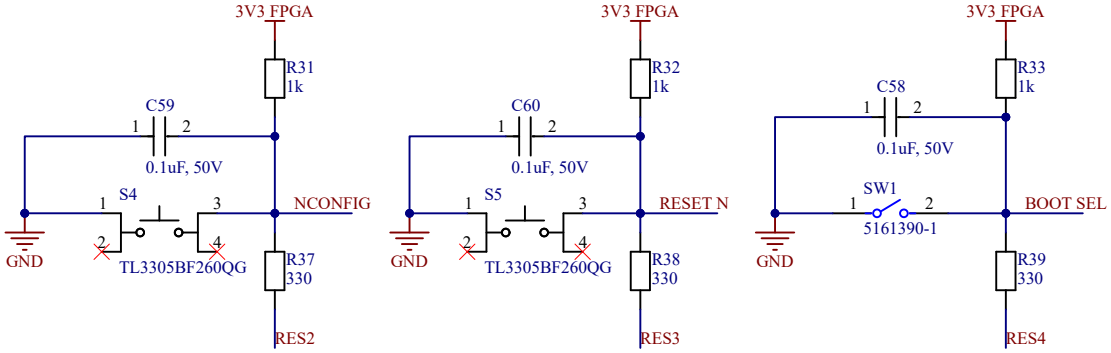
Power Supply ESP32 & RS485



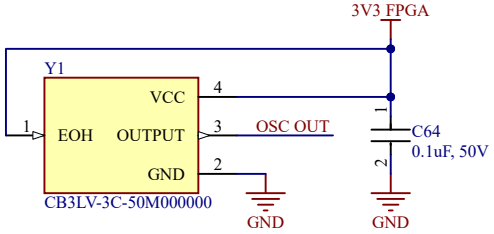
JTAG FPGA



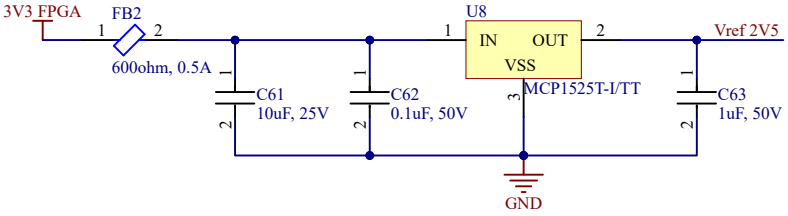
FPGA Buttons



Oscillator

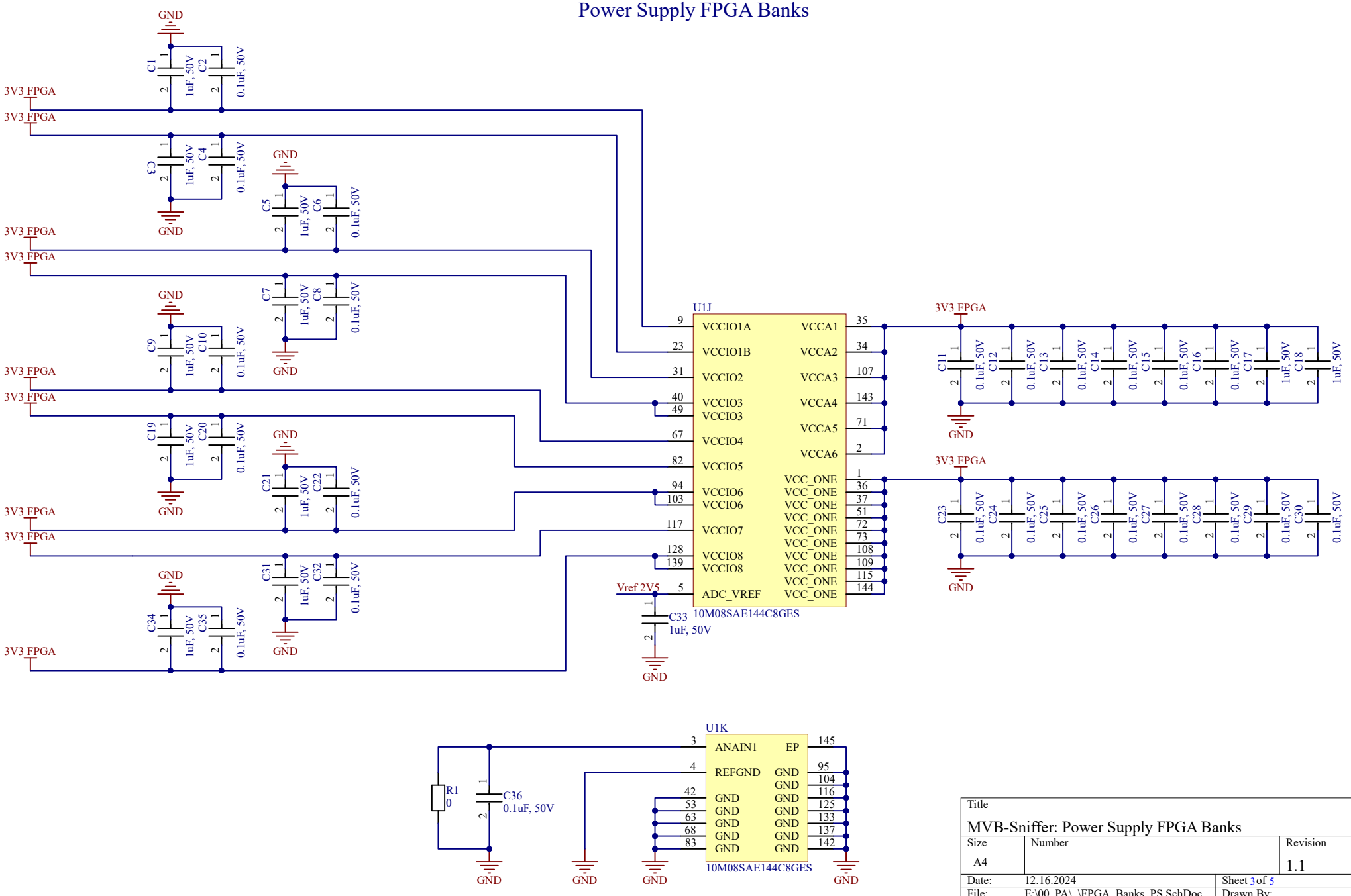


FPGA Vref 2V5



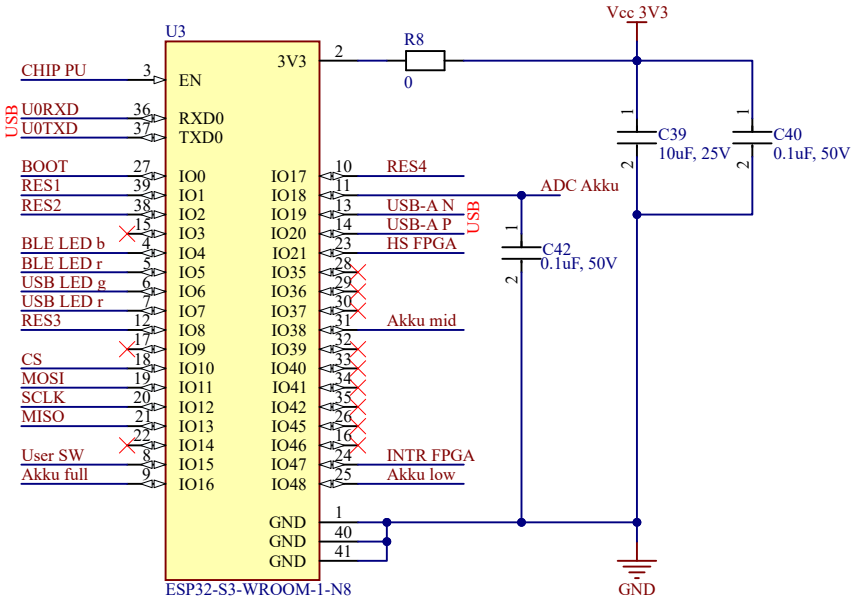
Title: MVB-Sniffer: Power Supply, FPGA Peripherals		
Size: A4	Number:	Revision: 1.1
Date: 12.16.2024		Sheet 2 of 5
File: E:\00_PA\..\PS_FPGA_Peripherals.SchDoc		Drawn By:

Power Supply FPGA Banks

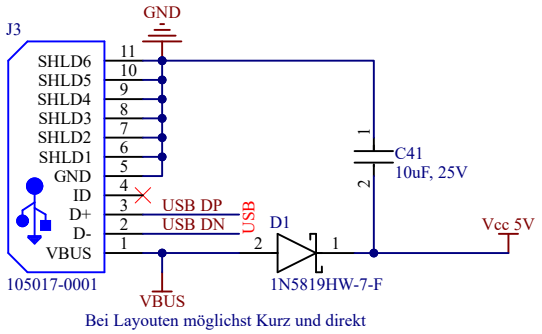


Title	MVB-Sniffer: Power Supply FPGA Banks		
Size	Number		Revision
A4			1.1
Date:	12.16.2024	Sheet 3 of 5	
File:	E:\00_PA\..\FPGA_Banks_PS.SchDoc	Drawn By:	

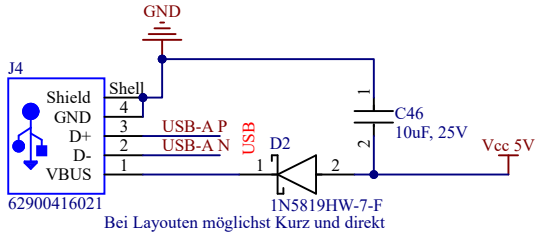
ESP32-S3-WROOM-1



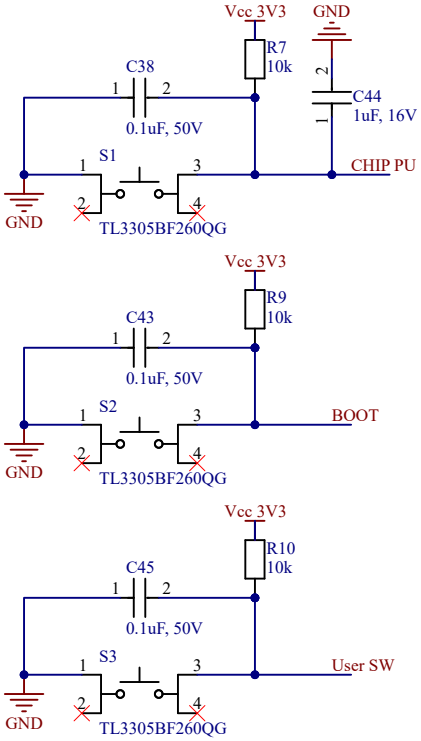
Micro USB UART



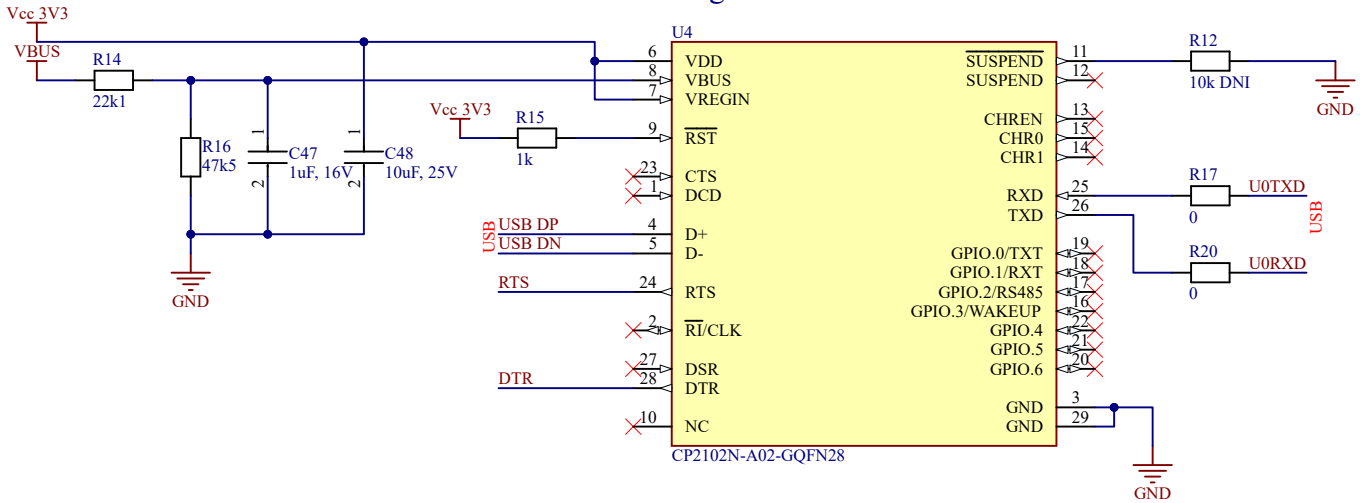
USB A Memory to ESP32



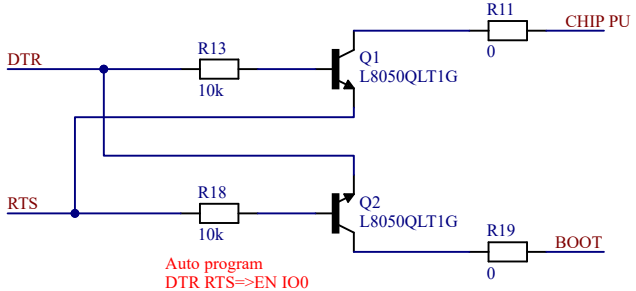
ESP32 Buttons



USB-Serial-Bridge ESP32



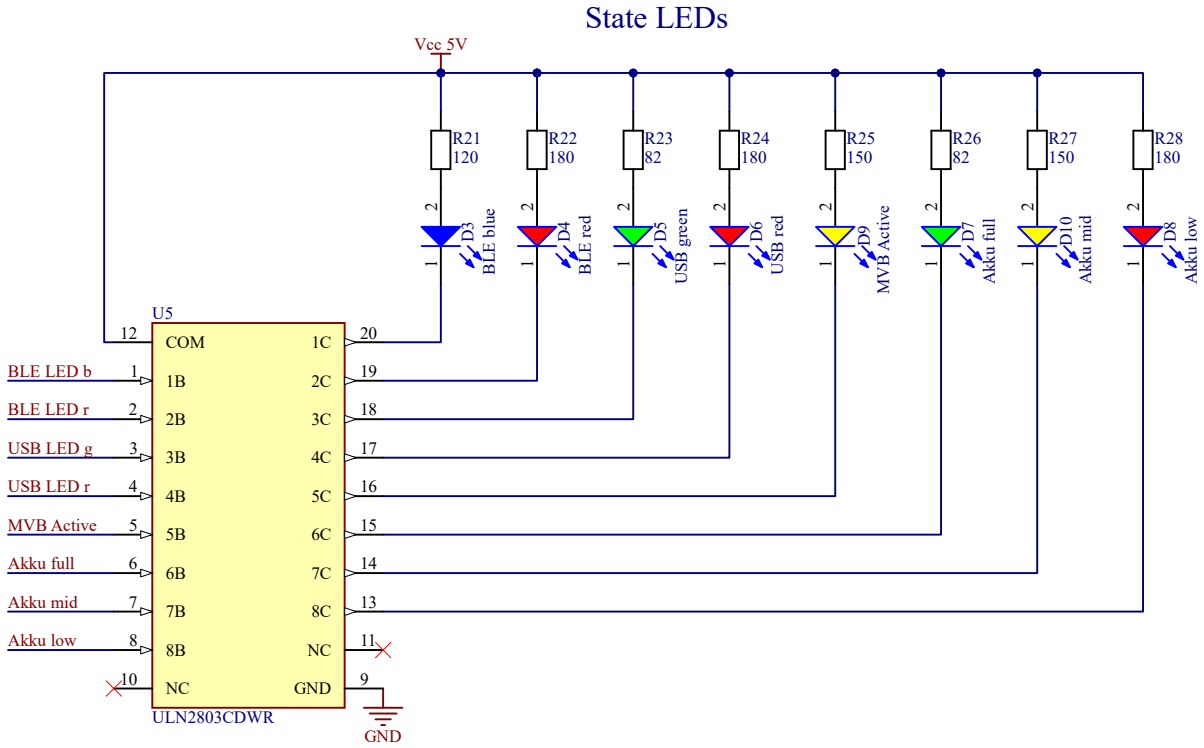
Serial Signals Handling

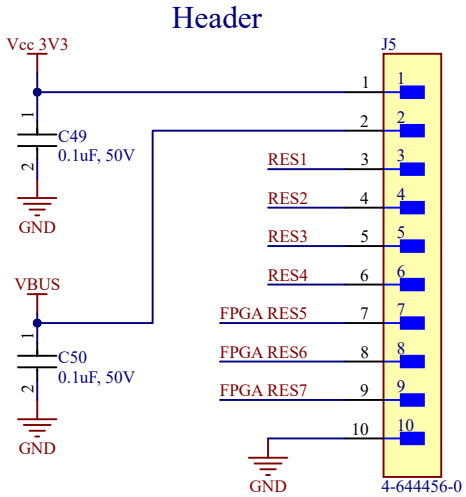


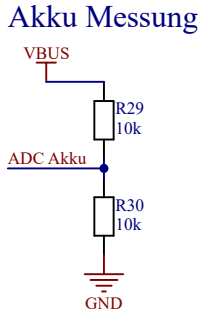
Auto program

DTR	RTS	=>EN	IO0	
1	1	1	1	Run
0	0	1	1	-
1	0	0	1	Reset
0	1	1	0	Programm

Title	MVB-Sniffer: ESP32, USB Interfaces, ESP Peripherals	
Size: A4	Number:	Revision: 1.1
Date: 12.16.2024		Sheet 4 of 5
File: E:\00_PA\..\ESP32_S3.SchDoc		Drawn By:







Title: MVB-Sniffer: Indicators		
Size: A4	Number:	Revision: 1.1
Date: 12.16.2024		Sheet 5 of 5
File: E:\00_PA\..\Indicators.SchDoc		Drawn By: