#### Tribhuvan University

#### **Institute of Science and Technology**

2066

Bachelor Level/ First Year/ Second Semester/ Science Computer Science and Information Technology (CSc. 151) (Digital Logic) Full Marks: 60 Pass Marks: 24 Time: 3 hours.

Candidates are required to give their answers in their own words as for as practicable. The figures in the margin indicate full marks.

## **Long Answer Questions:**

## Attempt any TWO questions.

(2x10=20)

- 1. Design the 4 bit Synchronous up/down counter with timing diagram, logic diagram and truth table.
- 2. Design a Full subtractor with truth table and logic gates.
- 3. Design a decimal adder with logic diagram and truth table.

## **Short Answer Questions:**

# Attempt any EIGHT questions.

(8x5=40)

- 4. Differentiate between Analog and Digital system.
- 5. Convert the following octal numbers to hevadecimal.
  - a) 1760.46
  - b) 6055.263
- 6. Which gates can be used as Inverters in addition to the NOT gate and how?
- 7. Draw a logic gates that implements the following
  - a)  $A = (Y_1 \oplus Y_1)(Y_3 \odot Y_4) + (Y_5 \oplus Y_6 \oplus Y_7)$
  - b)  $A = (X_1 \odot X_2) + (X_3 \odot X_4) + (X_4 \odot X_5) \oplus (X_6 \odot X_7)$
- 8. State and prove De-Morgan's theorem 1<sup>st</sup> and 2<sup>nd</sup> with logic gates and truth table.
- 9. Reduce the following expressions using K map

a. 
$$\bar{A} + B(A + \bar{B} + D)(\bar{B} + C)(B + C + D)$$

- 10. Differentiate between a MUX and DEMUX.
- 11. Explain the operation of Decoder.
- 12. What are the various types of shift registers?
- 13. What do you mean by synchronous counter?