

Tribhuvan University  
Institute of Science and Technology  
2072  


Bachelor Level / First Year/ Second Semester/ Science  
Computer Science and Information Technology (CSc 151)  
(Digital Logic)

Full Marks: 60  
Pass Marks: 24  
Time: 3 hours.

*Candidates are required to give their answers in their own words as far as practicable.  
The figures in the margin indicate full marks.*

**Long Answer Questions:**

Attempt any two questions.

(2x10=20)

- 1 Design and Implement with logic diagram, truth table and timing diagram of synchronous 3 bit up/down counter using J-K Flip Flops.
2. Design a Magnitude comparator using logic gates and truth table.
3. Design a Master-slave S-R flip-flop with logic diagram and truth table.

**Short Answer Questions:**

Attempt any eight questions.

(8x5=40)

4. What do you mean by the Gray code? What are its applications?

5. Convert the following:

a)  $(A\ 08E.FA)_{16} = (?)_{10}$

b)  $AE9.B0E)_{16} = (?)_2$

6 State and prove commutative laws, associative laws and distributive laws using logic gates and truth table.

7. Show that both NAND gate and NOR gate are universal gates.

8. Prove that

a)  $\overline{ABC}(\overline{A + B + C}) = ABC$

b)  $A + \overline{BC}(A + \overline{BC}) = A$

9. Reduce the following expressions using K-map.

a)  $(A + B)(A + \overline{B} + C)(A + \overline{C})$

b)  $A + B(A + \overline{B} + D)(B + \overline{C})(B + C + D)$

10. How does a J – K Flip Flop differ from an S-R Flip Flop in its basic operation? Explain.

11. Differentiate between a counter and a shift register.

12. Design a 4 input Multiplexer using logic diagram and truth table.

13. Explain the serial –In, Parallel out shift register.