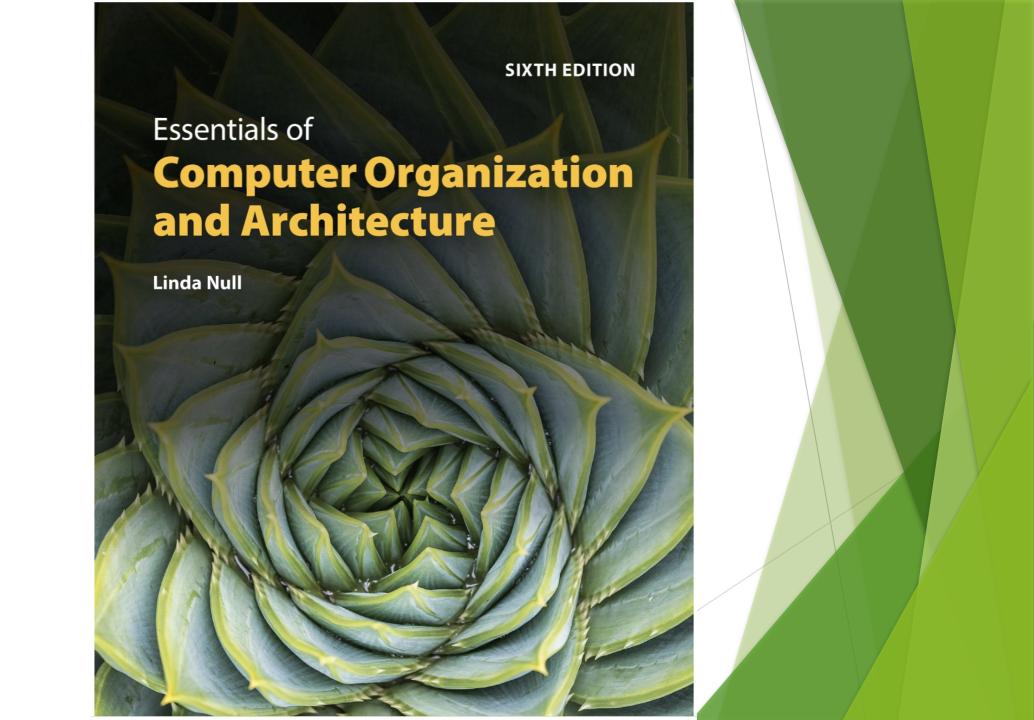
COSC 2425 - COMPUTER ORGANIZATION



CHAPTER 1 Introduction

- 1.1 Overview
- 1.2 Computer Systems
 - 1.2.1 The Main Components of a Computer
 - 1.2.2 System Components
 - 1.2.3 Classification of Computing Devices
- 1.3 An Example System: Wading Through the Jargon
- 1.4 Standards Organizations
- 1.5 Historical Development
 - 1.5.1 Generation Zero: Mechanical Calculating Machines (1642–1945)
 - 1.5.2 The First Generation: Vacuum Tube Computers (1945–1953)
 - 1.5.3 The Second Generation: Transistorized Computers (1954–1965)
 - 1.5.4 The Third Generation: Integrated Circuit Computers (1965-1980)
 - 1.5.5 The Fourth Generation: VLSI Computers (1980-????)
 - 1.5.6 Moore's Law
- 1.6 The Computer Level Hierarchy
- 1.7 Cloud Computing: Computing as a Service
- 1.8 The Fragility of the Internet
- 1.9 The Von Neumann Model
- 1.10 Non-Von Neumann Models
- 1.11 Parallel Processors and Parallel Computing

CHAPTER 2	Data	Representation in Computer Systems	
	2.1	Introduction	
	2.2	Positional Numbering Systems	
	2.3	Converting Between Bases	
		2.3.1 Converting Unsigned Whole Numbers	
		2.3.2 Converting Fractions	
		2.3.3 Converting Between Power-of-Two Radices	
	2.4	Signed Integer Representation	
		2.4.1 Signed Magnitude	
		2.4.2 Complement Systems	
		2.4.3 Excess-M Representation for Signed Numbers	
		2.4.4 Unsigned Versus Signed Numbers	
		2.4.5 Computers, Arithmetic, and Booth's Algorithm	
		2.4.6 Carry Versus Overflow	
		2.4.7 Binary Multiplication and Division Using Shifting	
	2.5	Floating-Point Representation	
		2.5.1 A Simple Model	
		2.5.2 Floating-Point Arithmetic	
		2.5.3 Floating-Point Errors	
		2.5.4 The IEEE-754 Floating-Point Standard	
		2.5.5 Range, Precision, and Accuracy	
		2.5.6 Additional Problems with Floating-Point Numbers	3
	2.6	Character Codes	
		2.6.1 Binary-Coded Decimal	
		2.6.2 EBCDIC	
		2.6.3 ASCII	
		2.6.4 Unicode	
	2.7	Error Detection and Correction	
		2.7.1 Cyclic Redundancy Check	
		2.7.2 Hamming Codes	
		2.7.3 Reed-Solomon	

CHAPTER 3	Boo	olean Algebra and Digital Logic	
		Introduction	
	3.2	Boolean Algebra	
		3.2.1 Boolean Expressions	
		3.2.2 Boolean Identities	
		3.2.3 Simplification of Boolean Expressions	
		3.2.4 Complements	
		3.2.5 Representing Boolean Functions	
	3.3		
		3.3.1 Symbols for Logic Gates	
		3.3.2 Universal Gates	
		3.3.3 Multiple Input Gates	
	3.4	Karnaugh Maps	
		3.4.1 Introduction	
		3.4.2 Description of Kmaps and Terminology	
		3.4.3 Kmap Simplification for Two Variables	
		3.4.4 Kmap Simplification for Three Variables	
		3.4.5 Kmap Simplification for Four Variables	
		3.4.6 Don't Care Conditions	
		3.4.7 Summary	
	3.5	Digital Components	
		3.5.1 Digital Circuits and Their Relationship to Boolean Algebra	
		3.5.2 Integrated Circuits	
		3.5.3 Putting It All Together: From Problem Description to Circuit	
	3.6	Combinational Circuits	
		3.6.1 Basic Concepts	
		3.6.2 Examples of Typical Combinational Circuits	
	3.7	Sequential Circuits	
		3.7.1 Basic Concepts	
		3.7.2 Clocks	
		3.7.3 Flip-Flops	
		3.7.4 Finite-State Machines	
		3.7.5 Examples of Sequential Circuits	

CHAPTER 4 MARIE: An Introduction to a Simple Computer Introduction CPU Basics and Organization 4.2.1 The Registers 4.2.2 The ALU 4.2.3 The Control Unit The Bus 4.4 Clocks The Input/Output Subsystem Memory Organization and Addressing 4.6 4.7 Interrupts MARIE 4.8.1 The Architecture 4.8.2 Registers and Buses 4.8.3 Instruction Set Architecture 4.8.4 Register Transfer Notation Instruction Processing 4.9.1 The Fetch-Decode-Execute Cycle 4.9.2 Interrupts and the Instruction Cycle 4.9.3 MARIE's I/O 4.10 A Simple Program 4.11 A Discussion on Assemblers 4.11.1 What Do Assemblers Do? 4.11.2 Why Use Assembly Language? 4.12 Extending Our Instruction Set 4.13 A Discussion on Decoding: Hardwired Versus Microprogrammed Control 4.13.1 Machine Control 4.13.2 Hardwired Control 4.13.3 Microprogrammed Control 4.14 Real-World Examples of Computer Architectures 4.14.1 Intel Architectures

CHAPTER 5 A Closer Look at Instruction Set Architectures

- 5.1 Introduction
- 5.2 Instruction Formats
 - 5.2.1 Design Decisions for Instruction Sets
 - 5.2.2 Little Versus Big Endian
 - 5.2.3 Internal Storage in the CPU: Stacks Versus Registers
 - 5.2.4 Number of Operands and Instruction Length
 - 5.2.5 Expanding Opcodes
- 5.3 Instruction Types
 - 5.3.1 Data Movement
 - 5.3.2 Arithmetic Operations
 - 5.3.3 Boolean Logic Instructions
 - 5.3.4 Bit Manipulation Instructions
 - 5.3.5 Input/Output Instructions
 - 5.3.6 Instructions for Transfer of Control
 - 5.3.7 Special-Purpose Instructions
 - 5.3.8 Instruction Set Orthogonality
- 5.4 Addressing
 - 5.4.1 Data Types
 - 5.4.2 Address Modes
- 5.5 Instruction Pipelining
- 5.6 Real-World Examples of ISAs
 - 5.6.1 Intel
 - 5.6.2 MIPS
 - 5.6.3 Java Virtual Machine
 - 5.6.4 ARM

CHAPTER 6 Memory

- 6.1 Introduction
- 6.2 Types of Memory
- 6.3 The Memory Hierarchy
 - 6.3.1 Locality of Reference
- 6.4 Cache Memory
 - 6.4.1 Cache Mapping Schemes
 - 6.4.2 Replacement Policies
 - 6.4.3 Effective Access Time and Hit Ratio
 - 6.4.4 When Does Caching Break Down?
 - 6.4.5 Cache Write Policies
 - 6.4.6 Instruction and Data Caches
 - 6.4.7 Levels of Cache

6.5 Virtual Memory

- 6.5.1 Paging
- 6.5.2 Effective Access Time Using Paging
- 6.5.3 Putting It All Together: Using Cache, TLBs, and Paging
- 6.5.4 Advantages and Disadvantages of Paging and Virtual Memory
- 6.5.5 Segmentation
- 6.5.6 Paging Combined with Segmentation
- 6.6 Real -World Examples of Memory Management

CHAPTER 7 Input/Output Systems 7.1 Introduction I/O and Performance 7.3 Amdahl's Law 7.4 I/O Architectures 7.4.1 I/O Control Methods 7.4.2 Character I/O Versus Block I/O 7.4.3 I/O Bus Operation 7.4.4 I/O Buses and Interfaces 7.5 Data Transmission Modes 7.5.1 Parallel Data Transmission 7.5.2 Serial Data Transmission 7.6 Disk Technology 7.6.1 Rigid Disk Drives 7.6.2 Solid State Drives Optical Disks 7.7.1 CD-ROM 7.7.2 DVD 7.7.3 Blue-Violet Laser Discs 7.7.4 Optical Disk Recording Methods 7.8 Magnetic Tape 7.8.1 LTO: Linear Tape Open 7.9 RAID 7.9.1 RAID Level 0 7.9.2 RAID Level 1 7.9.3 RAID Level 2 7.9.4 RAID Level 3 7.9.5 RAID Level 4 7.9.6 RAID Level 5 7.9.7 RAID Level 6 7.9.8 RAID DP 7.9.9 Hybrid RAID Systems

BEST WISHES